FPGA Verification Engineer

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**Professional Summary**

* Motivated FPGA **Verification** Engineer with 5 years of experience in functional verification of RTL and software models at Western Digital and NVIDIA.
* Strong expertise in **SystemVerilog** and UVM methodology, developing **testbenches**, **coverage** models, assertions, and debugging pre-silicon simulations.
* Proven ability to collaborate closely with design and **architecture** teams to root-cause and resolve complex issues.
* Hands-on with scripting (Python, Tcl), test plan development, and simulation using Cadence and Vivado tools
* B.Sc. in Electronic Engineering.

**Work Experience**

2023 - 2025 **Software Verification Engineer**, **Nvidia**

* Verified C-based software modules such as NVLink, Subnet Manager, and Network Simulator.
* Detected and reported critical software **bugs** early in the development cycle, preventing customer-side issues.
* Developed Python-based **automation** **scripts** to streamline testing and validation workflows.
* Collaborated with other teams to ensure feature compliance, robustness, and performance optimization.
* Applied in-depth knowledge of the InfiniBand protocol to validate communication layers and ensure system stability.

2019 - 2023 **FPGA Verification Engineer**, **Western Digital**

* Created full UVM environments for module and system-level verification in storage controller SoCs.
* Authored SystemVerilog assertions, scoreboards, monitors, and coverage models for compliance testing.
* Led simulation debug and regression management, ensuring early bug discovery and resolution.
* Partnered with architecture and RTL teams to review specs, define **test plans**, and track bug fixes.
* Used scripting (Python, Tcl) to enhance test automation and regression infrastructure.

**Education**

2025  **FPGA Design Student**, **Logtel**

* Developed **VHDL** designs with synthesis constraints to understand test coverage and failure points.
* Simulated data-driven testbenches using TextIO and validated results through waveform and log analysis.
* Gained experience in integrating and verifying IP cores such as BRAM, FIFO, DSPs, and clocking logic.

2015 - 2020 **B.Sc. in Electrical and Electronics Engineering,** Braude Academic College

* Grade: 85; Psychometric Entrance Test - Grade: 727.

**Technical Skills**

Xilinx Vivado, Cadence Simulator | VHDL, SystemVerilog, UVM | Python | VGA, I2C, InfiniBand, UFS | Git, Linux, Jira, Redmine | Visual Studio Code, GVIM, Sublime.

**Military Service**

2011 - 2014 Combat Soldier, Golani Brigade.

**Languages**

**English** - Fluent, **Hebrew** - Native.