Circuit Design Contest-2020

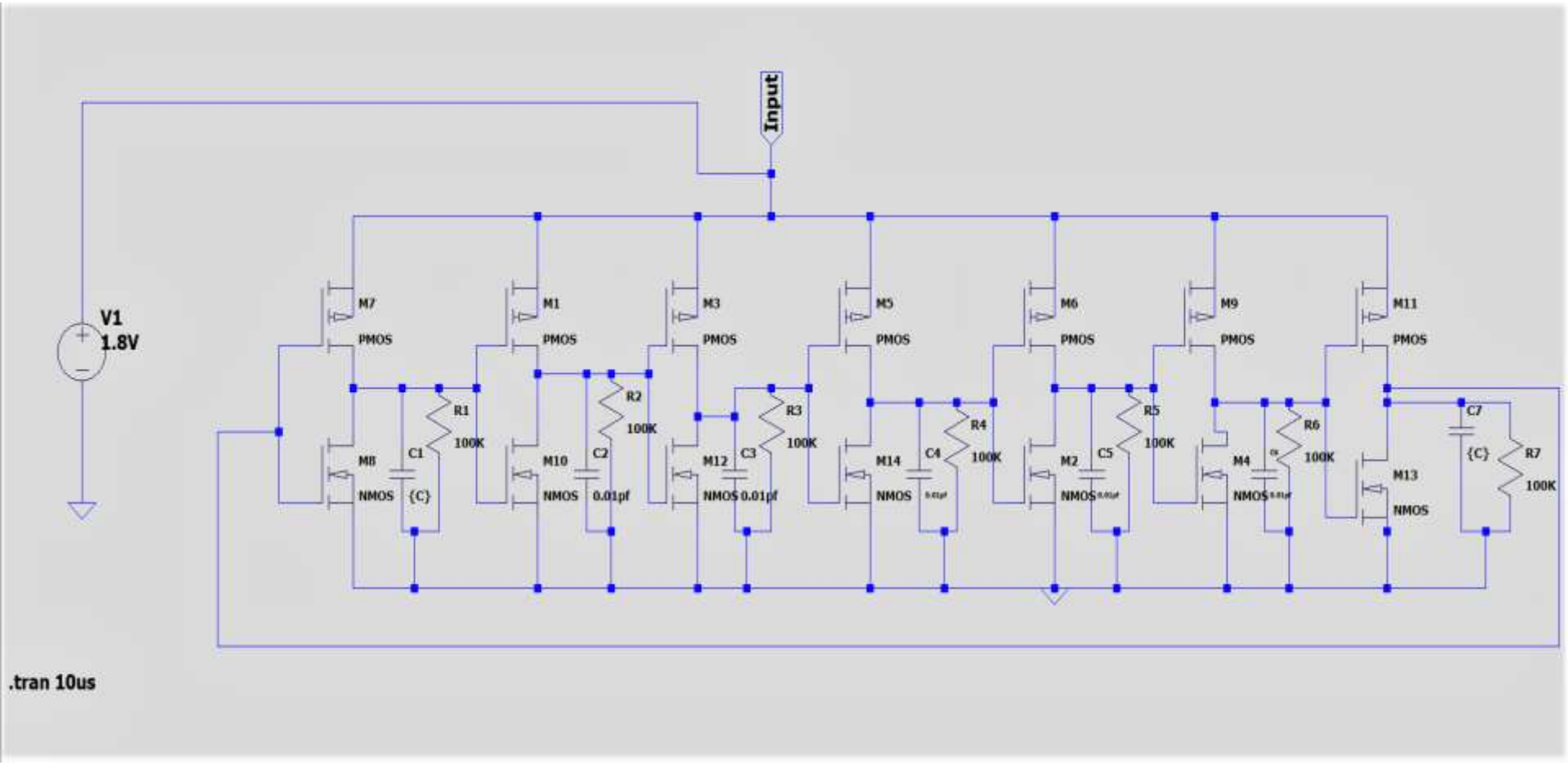
Organized by IEEE SSCS Kolkata Chapter

Name of the Participant 1: SHIRSHENDU CHATTERJEE

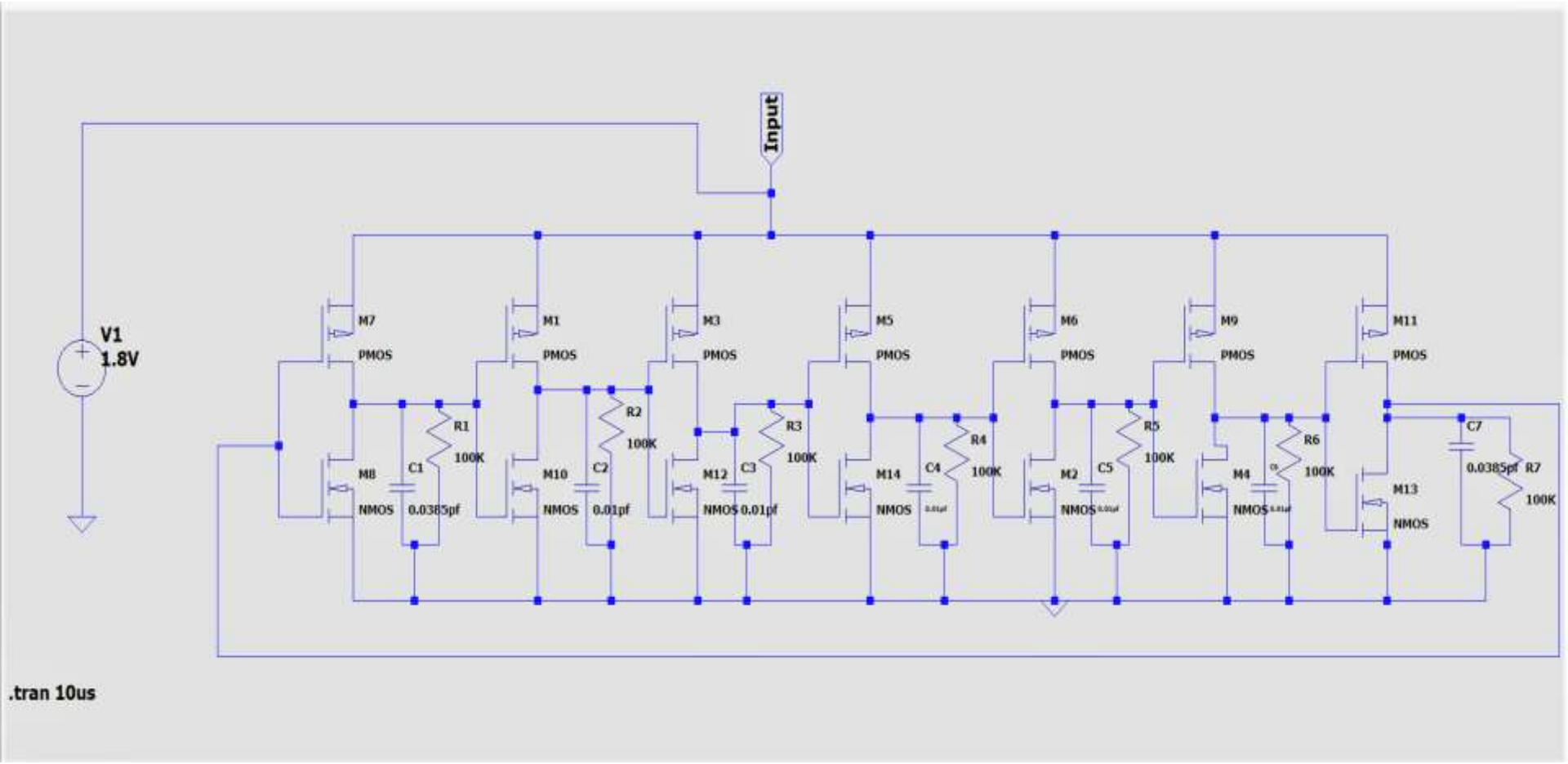
Name of the Participant 2: ANKITA MODAK

College: UNIVERSITY OF CALCUTTA(Institute of Radiophysics and Electronics)

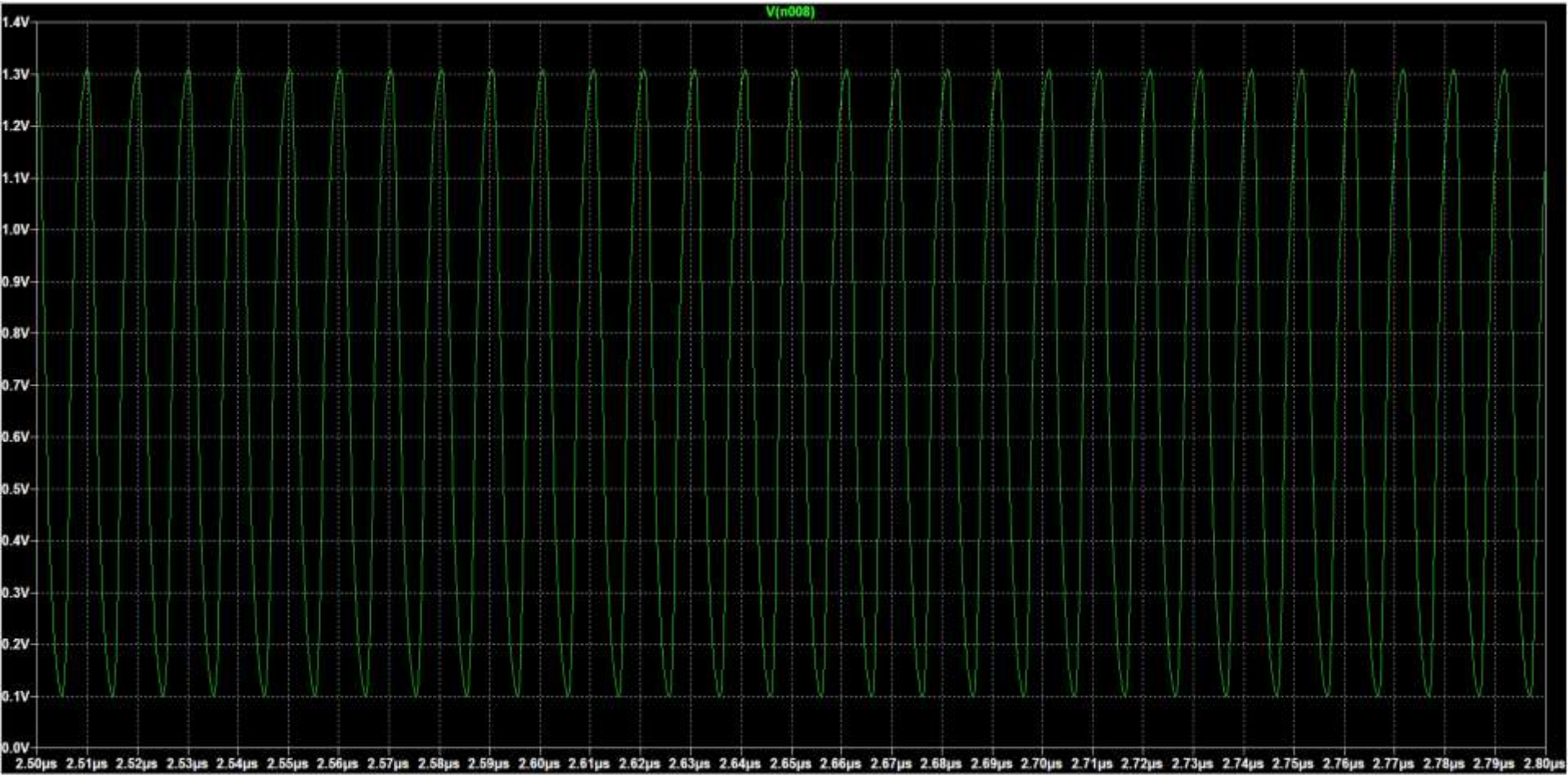
CIRCUIT DIAGRAM(GENERAL)



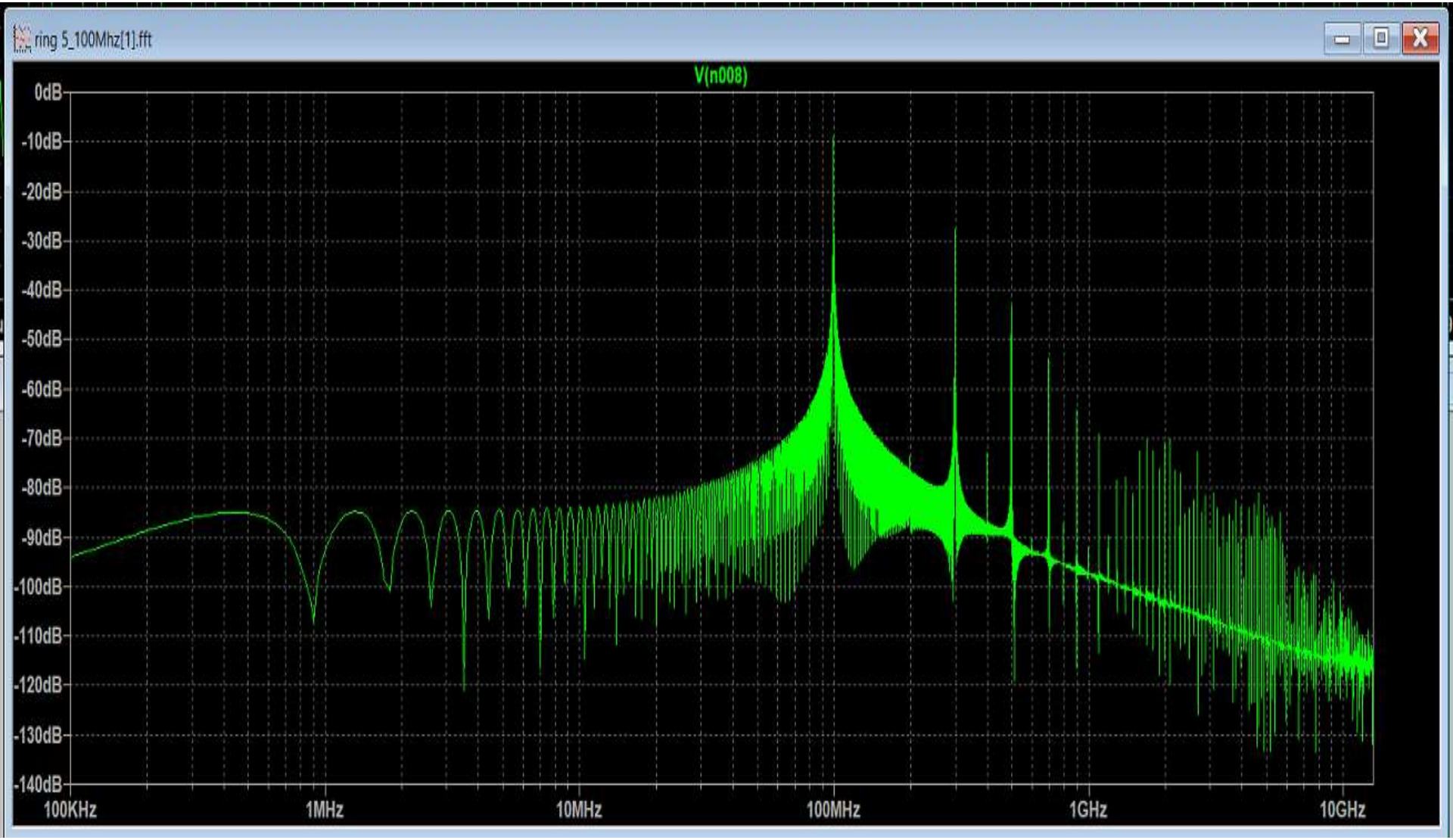
CIRCUIT DIAGRAM FOR 100MHz



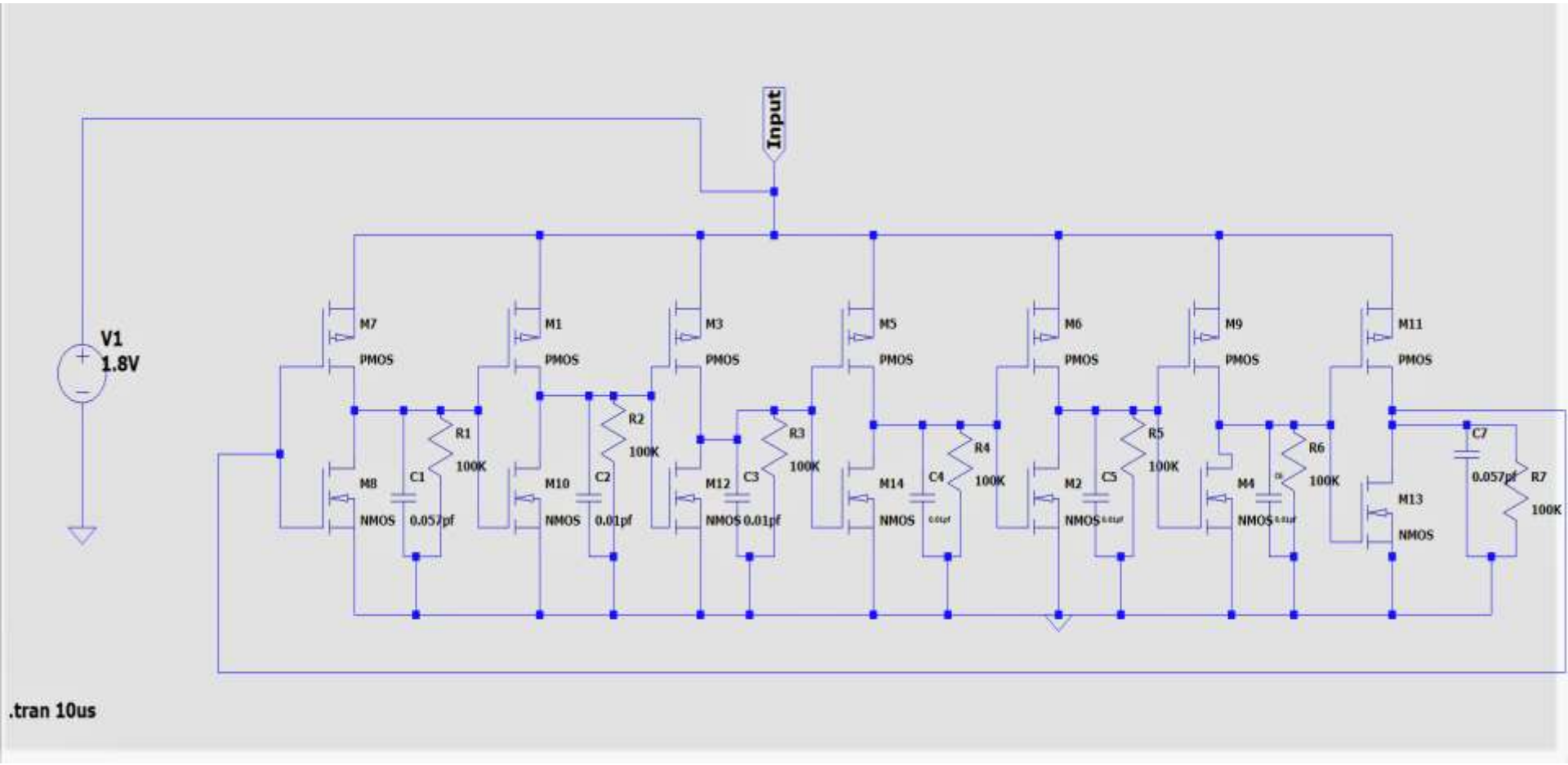
Voltage vs. Time Plot for 100MHz



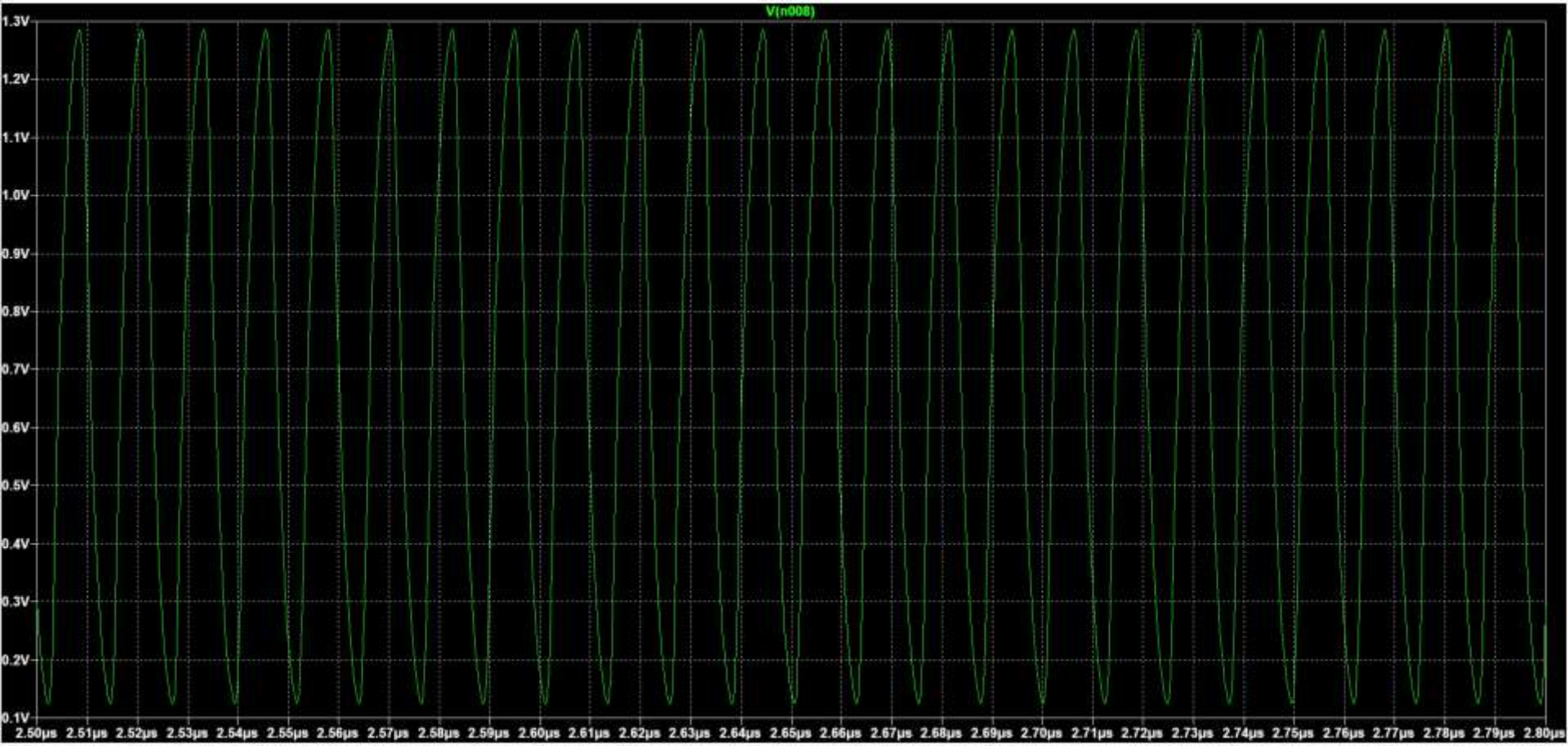
FFT Plot of 100MHz



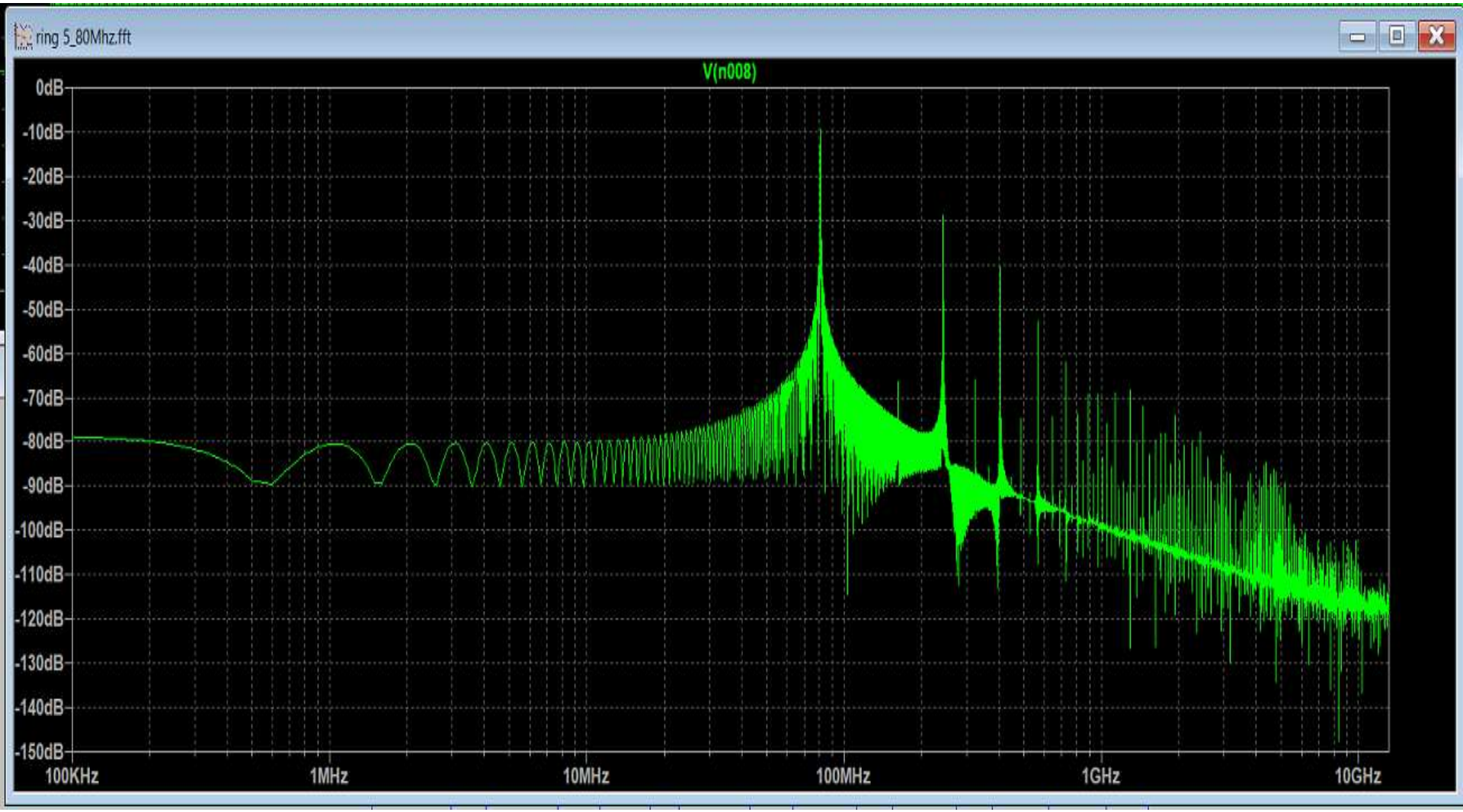
CIRCUIT DIAGRAM FOR 80MHz



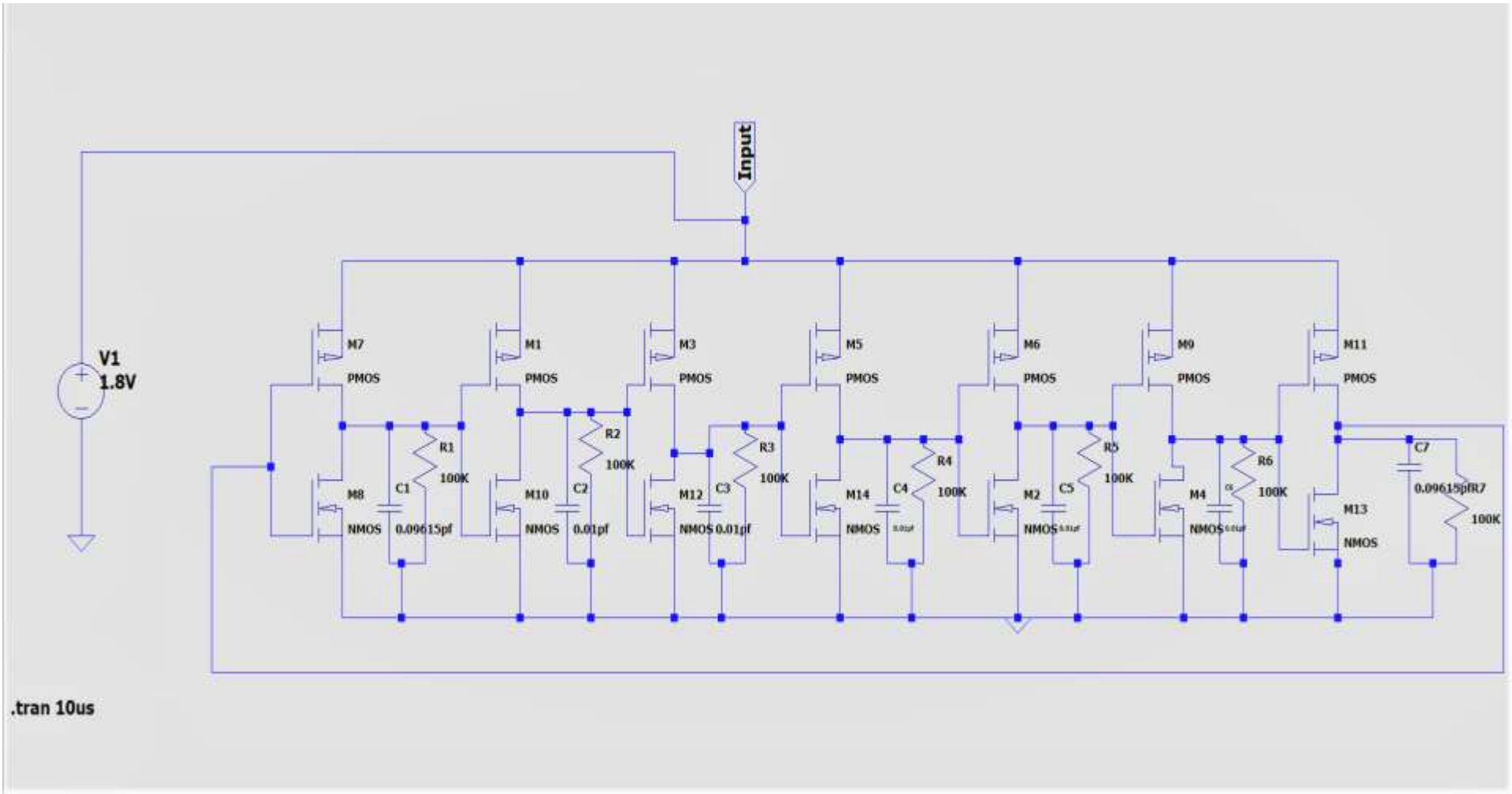
Voltage vs. Time Plot for 80MHz



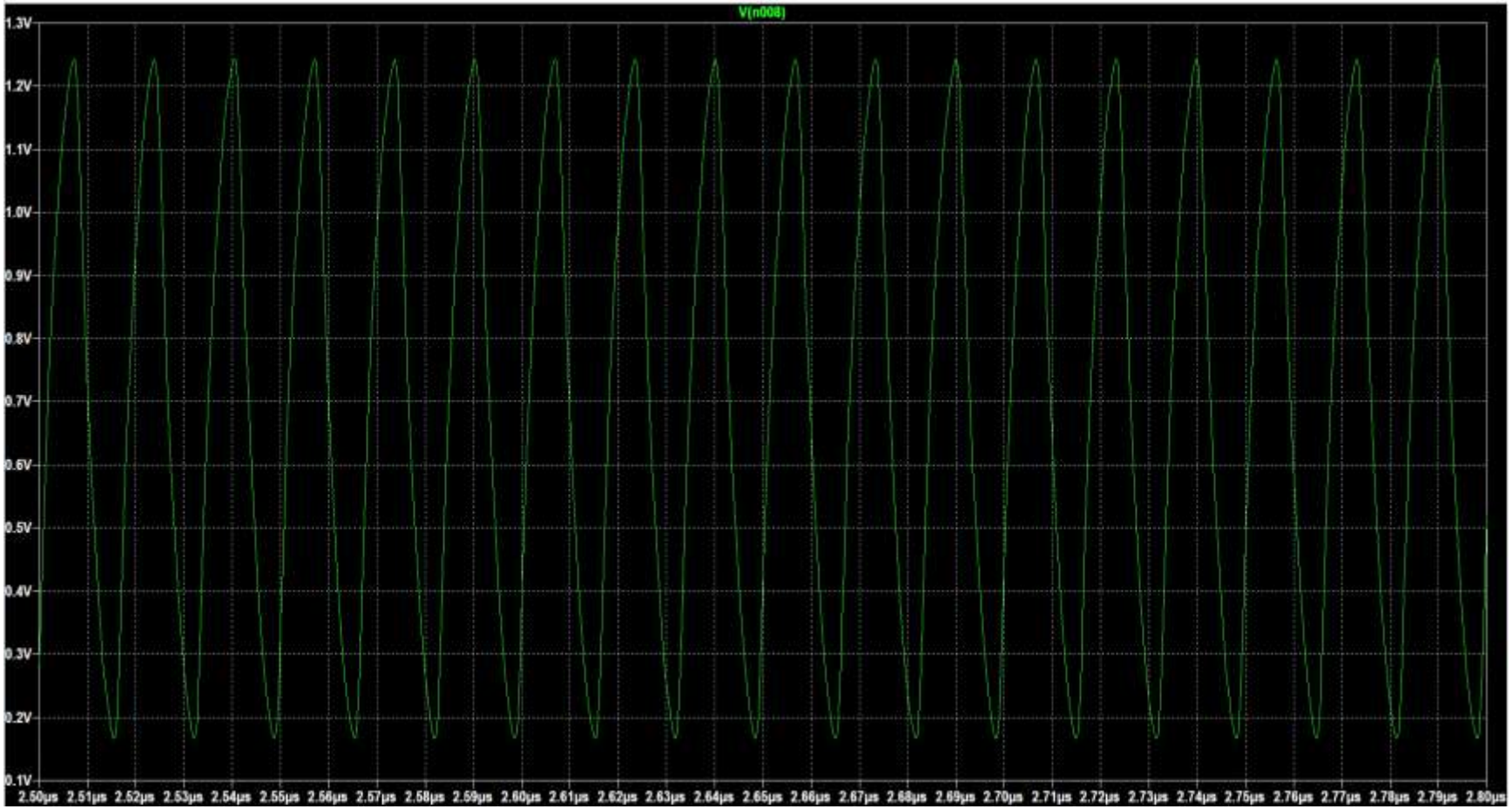
FFT Plot for 80MHz



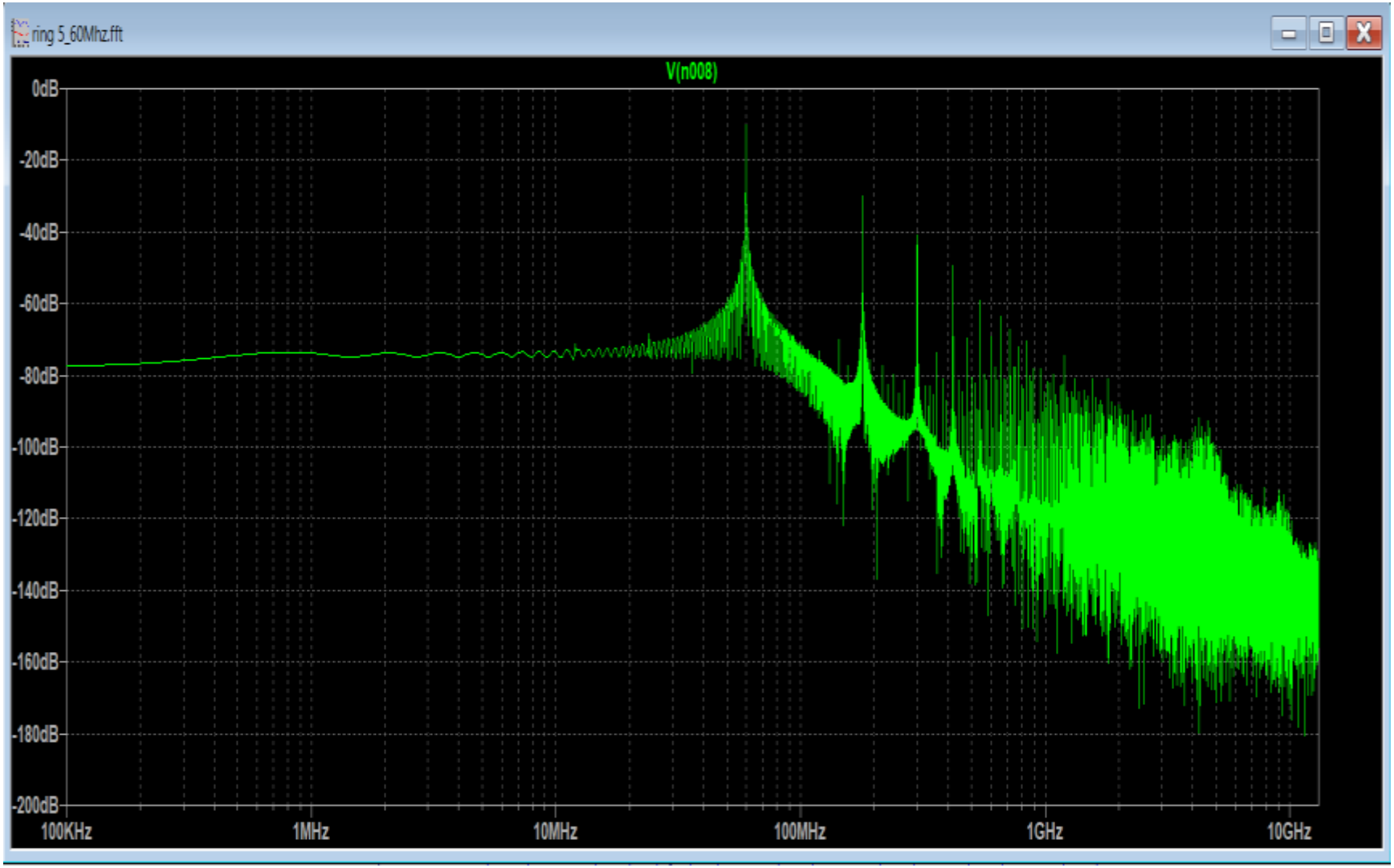
CIRCUIT DIAGRAM OF 60MHz



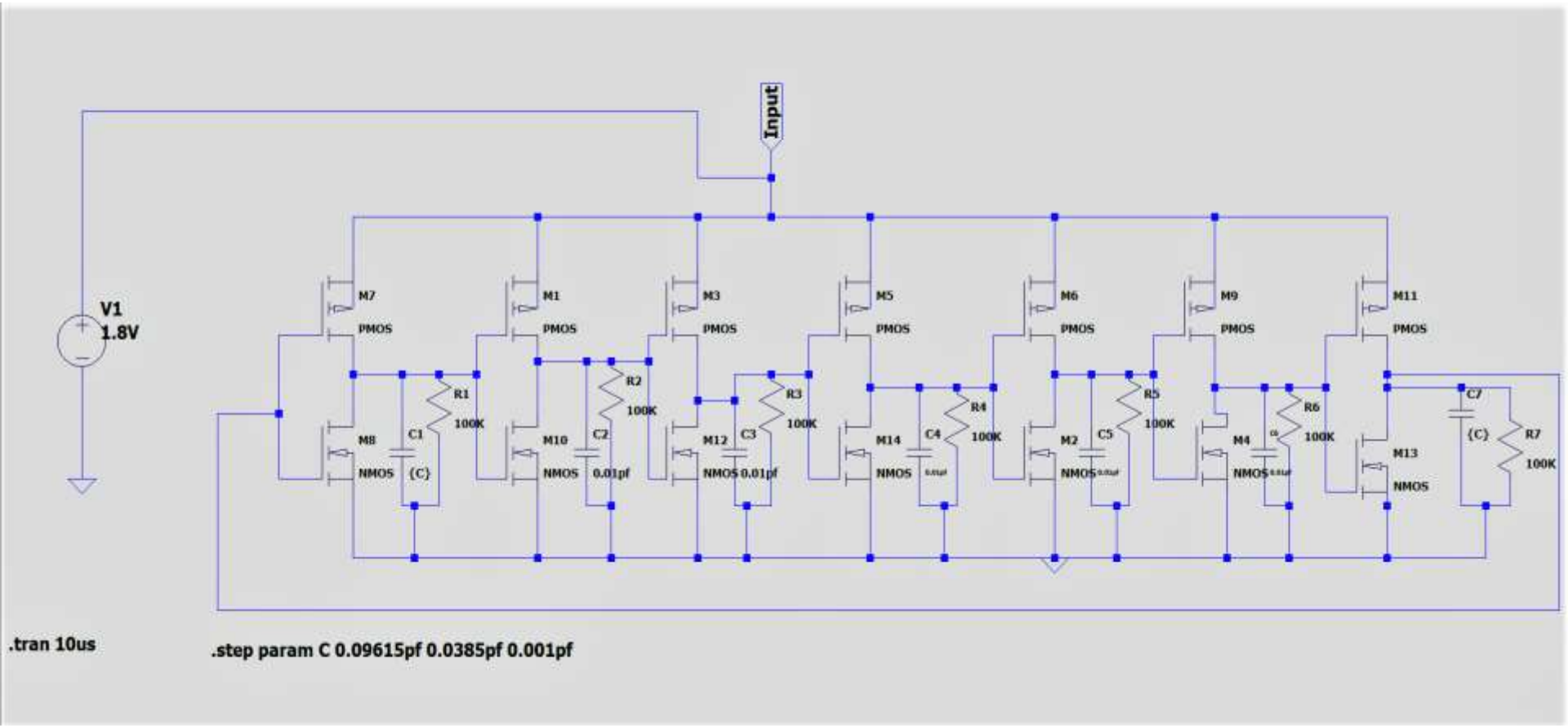
Voltage vs. Time Plot for 60 MHz



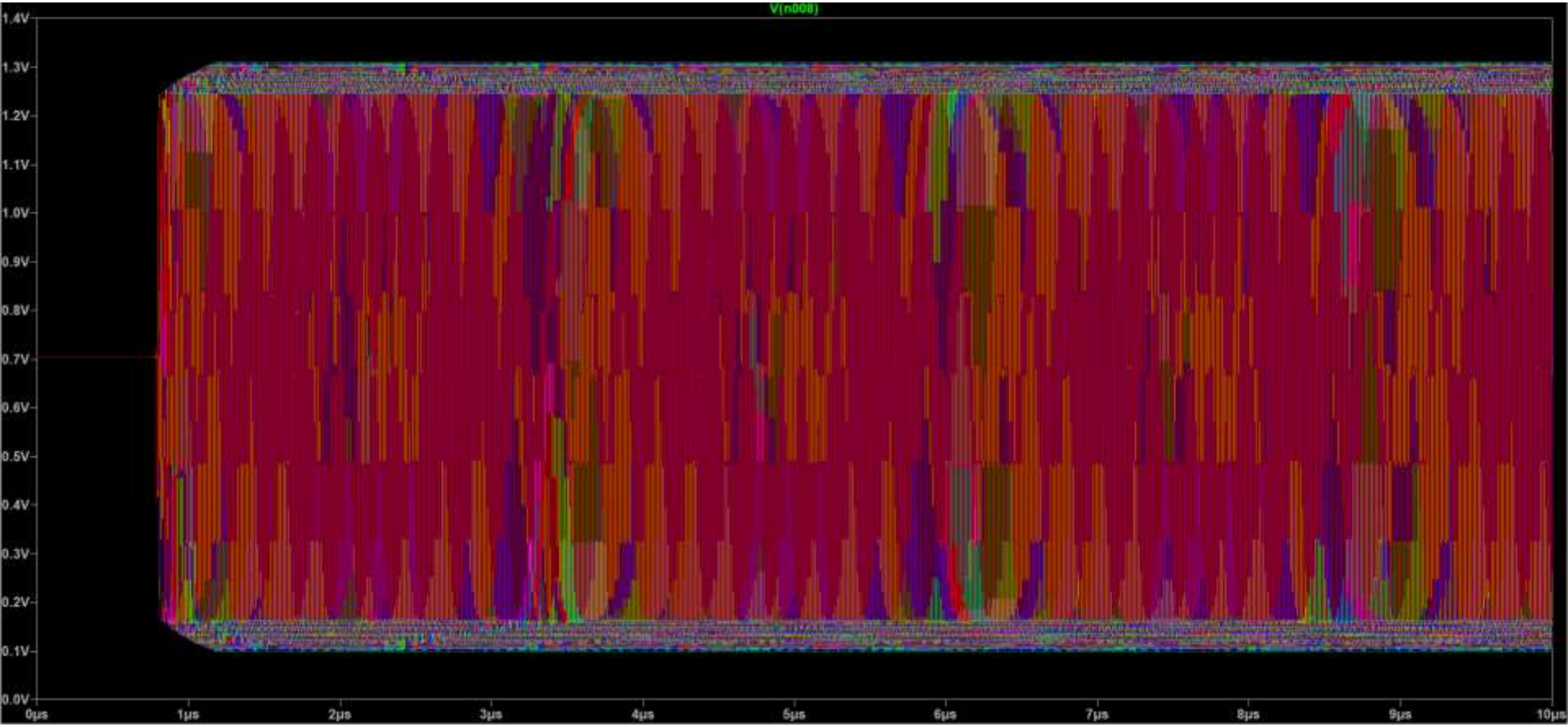
FFT Plot for 60 MHz



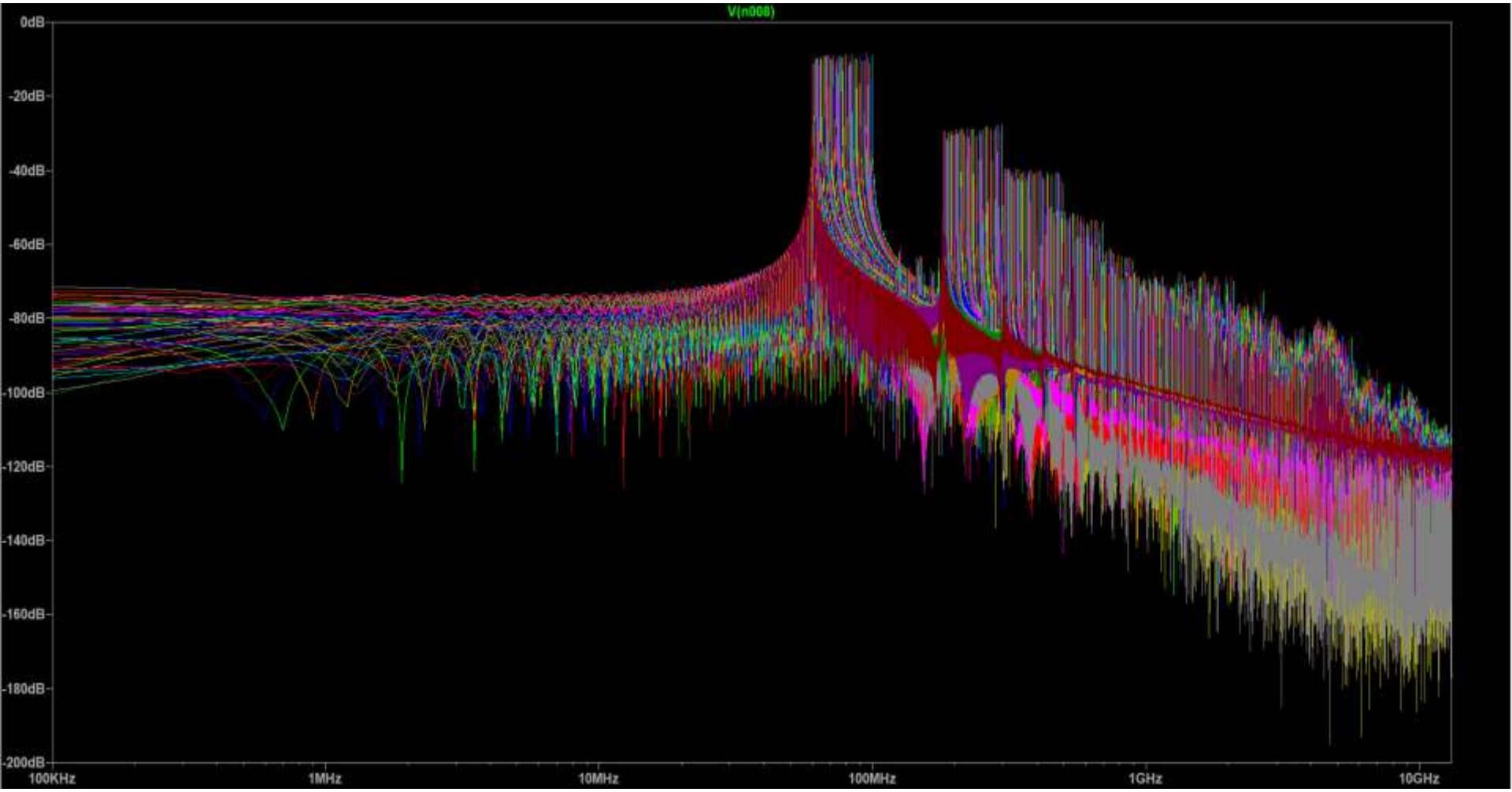
CIRCUIT DIAGRAM FOR 60 MHz-100 MHz



60MHz to 100MHz scan using Variable Capacitance

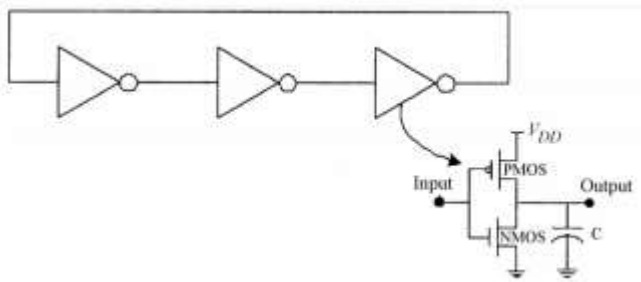


FFT Plot of frequency ranging from 60MHz-100MHz



Working Principle

The switching between ON and OFF the transistor performs in the saturation, linear and cut-off mode.



The input of the inverter switches from low to high is considered PMOS is in cut-off region and the capacitor C discharges through NMOS.

The discharge current is given by- $I_{DN} = -C\frac{dv_{out}}{dt}$

The NMOS transistor changes from the saturation to linear mode of operation during high to low transition.

The output propagation high to low delay time is defined as fall time of the output voltage and is expressed by-

$$\tau_{dhl} = \int_{V_{DD}}^{V_{DD}/2} \frac{dv_{out}}{I_{DN}}.$$

When the input of the inverter switches from high to low, the NMOS transistor goes into cut-off region and the capacitor charges through PMOS transistor and the current is given by- $I_{DP} = C\frac{dv_{out}}{dt}$

The PMOS transistor changes the mode of operation during output from low to high transition. It changes from saturation to the linear region when v_{out} reaches threshold($-v_{TP}$)

The output propagation low to high delay time is given by- $\tau_{dlh} = C\int_{0}^{-v_{TP}} \frac{dv_{out}}{I_{DPS}} + C\int_{-v_{TP}}^{V_{DD}/2} \frac{dv_{out}}{I_{DPL}}$

Working Principle

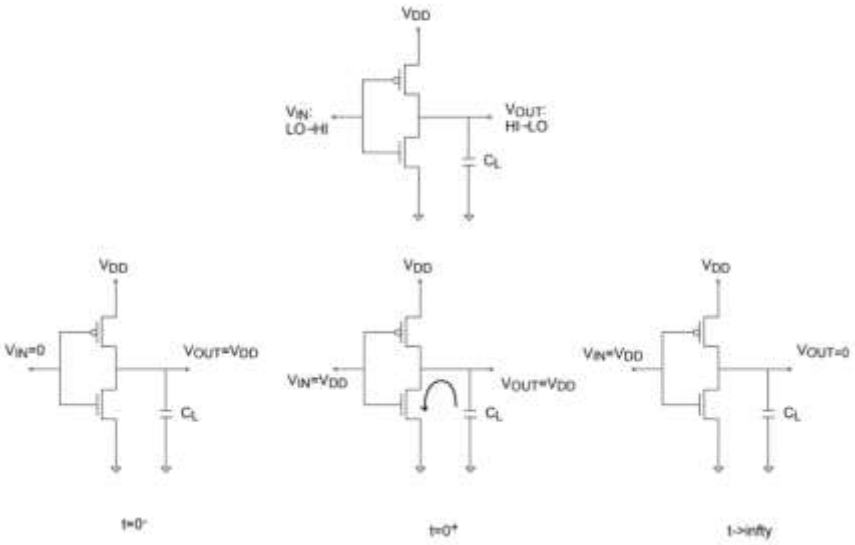
It was thus seen the total delay in the decay and rise for the m stage oscillator is given by- $m(\tau_{dhl}+\tau_{dlh})$

Thus the frequency of oscillation is given by-

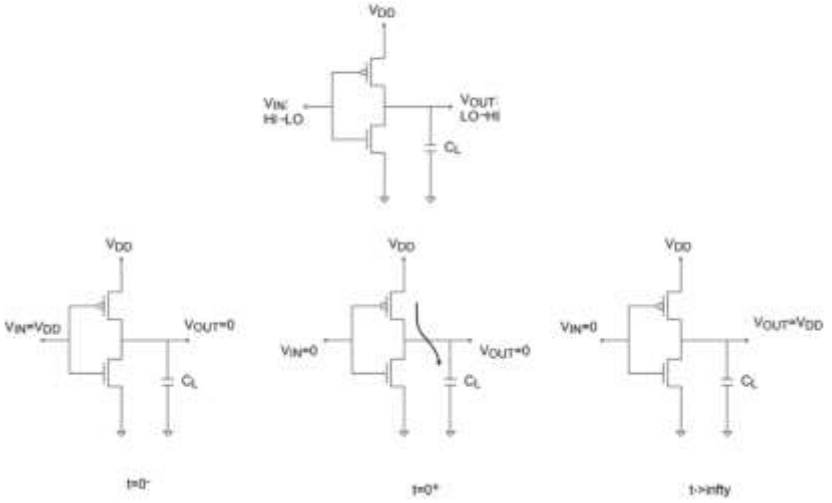
$$f_o = \frac{1}{m(\tau_{dhl} + \tau_{dlh})}$$

From the above concepts the oscillator has been designed and the value of the resistance and capacitance was well found out to tune the circuit to the given frequency needed.

Propagation delay high-to-low



Propagation delay low-to-high



Working Principle

- The circuit is designed on the principle of changing propagation delay by continuous changing of capacitance value in the range of 0.0915pf to 0.0385pf with the help of common variable capacitor with fixed resistor 100K at initial stage and final stage i.e. at stage 1 and stage 7.

- Remaining stages are unchanged, having fixed capacitance value and resistance.

- The circuit has been designed by choosing center frequency at 80 MHz and having two side band of 20 MHz covering 60 to 100 MHz

- Here the major issue is Propagation delay high to low or low to high depend on instantaneous value of variable capacitance.

- Any frequency can be selected by changing value of variable capacitance {C} of tune circuit at stage 1 and 7.

Result Summary

Parameter(unit)	Minimum value	Typical Value	Maximum Value
Supply Voltage	-	1.8V	-
Supply Current	-55.75µA	-56.42µA	-57.94µA
Resistance	-	100K	-
Capacitance(Fixed)	-	0.01pf	-
Capacitance(Variable)	0.0385pf	-	0.09615pf