Design of Low Power CMOS based VHF Ring Oscillator with RC network

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***Abstract*—A ring oscillator circuit consists of an odd number of inverter stages, where the output of each stage of the ring oscillator is given to the input of next stage and output of final stage is then fed to its input. No such external input is given to the circuit, just only a reset pulse is provided at once which drives the circuit. In this paper, a 7-stage ring oscillator is designed with a low power CMOS device with desirable propagation delay to cover the bandwidth of 60-100MHz and with a target frequency of 80MHz. A cost effective tunable circuit using only RC network with single variable capacitors at the first and the last stage which effectively tunes the circuit at the required working frequency with high performance. To meet the entire bandwidth, optimization of 7-stages odd number inverter and using close loop feedback was used to maintain the adequate accuracy for start, stop and centre frequency in the frequency spectrum.**

***Index Terms*—Ring Oscillator, LT-Spice, CMOS, Frequency, Bandwidth**

I. Introduction

With the proliferation of electronics system in various state of the art technologies, it is imperative to maintain frequency management in Analog and digital circuit with highly reliable oscillator. The demand of low power design has become an essential requirement to produce a reliable, cost effective system. We know that oscillatory behavior is ubiquitous in all physical systems, especially in analog/digital signal processing (DSP) and optical communication system [14]–[16]. It has also wide range of usability data communication, modulation in radio frequency and light wave communication systems where the noise free oscillation has a major impact and degradation of performance of a system. However all physical oscillators are corrupted by undesired perturbation/noise. To mitigate the unwanted noise the selection of device like NMOS and PMOS has been restricted to nanometer scale in LTspice and voltage range 1.8V maximum to optimise the design to trade-off low power consumption and performance. This paper shows the concept of design compliance in the bandwidth range- 60MHz to 100 MHz with simple low power MOSFET and simple RC network which leads the designer to establish single chip micro ring oscillator. The linearity of this oscillator is totally independent on control voltage. Any selection of frequency component will be accomplished by one tuneable capacitor in the circuit. The major advantage to use this circuit that only one variable capacitor having range 0.09615 pf to 0.001pf is covering the bandwidth and to maintain the low propagation delay.

II. Ring Oscillator

In the ring oscillator the basic element which is used is the inverter cell. The oscillator comprises an inverter cells in cascaded combination delay stages in a close loop manner. The cell consists of complementary pairs of PMOS and NMOS. The ring oscillator produces some very useful features which are listed as follows-
(1) It can be easily designed with the state-of-art integrated circuit technology. (2) Oscillation can be achieved with low voltage. (3) It can be tuneable at any frequency defined bandwidth.(4) It can produce multiple phase out putbased on its structural characteristic and applicable in communication system.
Inverting operation means when input is low output gets high and vice-versa. CMOS inverter is the combination of PMOS and NMOS, where PMOS is called as pull-up network and NMOS is called as pull-down network. When input is low, nmos is OFF, pmos gets ON, pulling the transistor high and when input becomes high, nmos gets ON, driving the network down and output becomes low. An odd number of inverters form a closed loop with positive feedback forming a ring oscillator circuit.

The generation of oscillation frequency depends on the propagation delay τ_d per stage and in line with the number of stages. The gain stages are connected in a loop that output from the last stage is given to the input of first stage. This circuit provides a self-sustained oscillation(To maintain the sustained oscillation the circuit should conform with the Barkhausen criteria) when it in state of unit voltage gain and phase shift of 2π. The dc inversion provides π phase shift and the remaining π phase shift divide equally among the stages in entire oscillation circuit, so delay of each stage provides a phase delay of $\frac{\pi}{m}$ and therefore, the oscillating signal must go through each of the m delay stages once to provide the first π phase. The oscillation frequency of this CMOS ring oscillator circuit is calculated using the following equation.

$$f_{osc} = \frac{1}{2m\tau_d} \tag{1}$$

Assuming that the inverters are identical and m is the odd number of inverters in the ring oscillator. Since the ring oscillator is self-starting, it is often added to a test portion of the wafer to indicate the speed of a particular process run.

When identical inverters are used the capacitance on the inverter's input/output will be the sum of the inverter's input capacitance with the inverter's output capacitance.

III. CMOS INVERTER:

For a general single stage ring oscillator, the oscillators consists of a PMOS and an NMOS connected through gate to acquire the single input with additional delay element at its output. When high input is given at its input NMOS becomes ON and PMOS becomes OFF. Since the source of NMOS transistor is connected to ground so that it gives the low output at its drain therefore the output of inverter is inverted and becomes low. Similarly when an inverter input is low, output becomes high as PMOS is at high voltage. [6], [7]

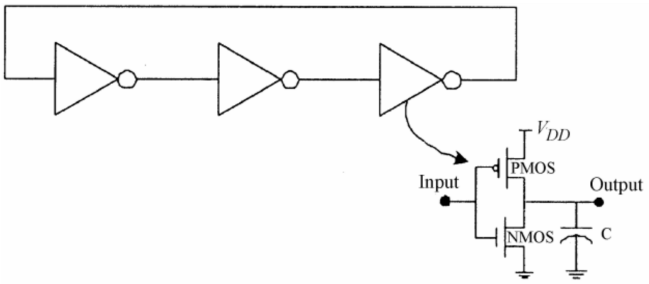

Fig. 1. Structure of single ended inverter based ring oscillator.

A. Working Principle

The inverter works through switching its operation between on and off with MOSFET performing in saturation, linear and cut-off mode. The input of the inverter switches from low ($v_{in} = 0$) to high($v_{in} = V_D D$). In that time the PMOS is in cut-off region and the capacitor C_L discharges through NMOS transistor as shown in Fig 2. Thus, the associated discharge current is given by:

$$I_{DN} = -C_L \frac{dv_{out}}{dt} \tag{2}$$

The output propagation for high to low delay time(τ_{dhl}) is defined as the fall time of the output voltage from V_{DD} to $V_{DD}/2$.

$$\tau_{dhl} = -C_L \int_{V_{DD}}^{V_{DD}-v_{TN}} \frac{dv_{out}}{I_{DNS}} - C_L \int_{V_{DD}-v_{TN}}^{V_{DD}/2} \frac{dv_{out}}{I_{DNL}} \tag{3}$$

Here, I_{DN} is the drain current of the n-channel MOS transistor. The transistor changes from the saturation to the linear mode of operation during the high to low transition at $v_{out} = V_{DD} - v_{TN}$ and $v_{in} = V_{DD}$ during the transition, with v_{TN} as the threshold voltage of the NMOS transistor.

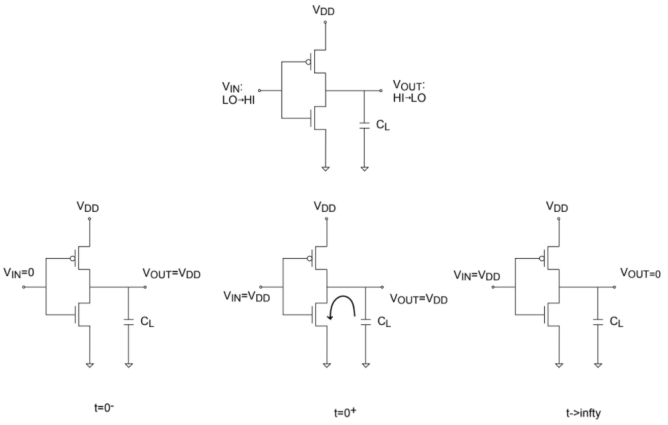

Fig. 2. Propagation delay from high to low.

Now, considering the output from low to high propagation delay time(τ_{dlh}), defined as the time delay to reach the output voltage at 50% of its maximum value V_{DD}. When the input of an inverter switches from high to low, the NMOS transistor goes into cutoff region. In that moment load capacitor C_L charges through PMOS transistor and the charging current is given by:

$$I_{DP} = C_L \frac{dv_{out}}{dt} \tag{4}$$

The PMOS transistor changes the mode of operation during the output from low to high transition. It changes from saturation to linear mode when v_{out} reaches $-v_{TP}$ while $v_m = 0$ during this entire transition. Thus the propagation delay can be expressed as:

$$\tau_{dlh} = C_L \int_0^{-v_{TP}} \frac{dv_{out}}{I_{DPS}} + C_L \int_{-v_{TP}}^{V_{DD/2}} \frac{dv_{out}}{I_{DPL}} \tag{5}$$

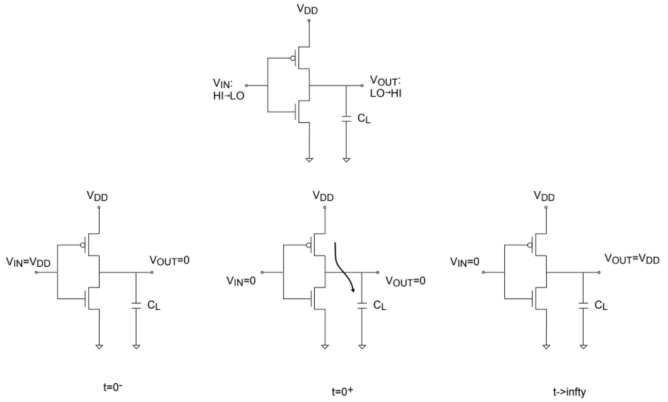

Fig. 3. Propagation delay from low to high.

As shown the total time delay in the decay and rise for a m stage oscillator is given by m($\tau_{dhl} + \tau_{dlh}$) and the oscillation frequency is given by:

$$f_o = \frac{1}{m(\tau_{dhl} + \tau_{dlh})} \tag{6}$$

With the advent of CMOS technology it becomes necessary to integrate more function within given silicon area thus reducing the fabrication cost, increasing the operating speed, and dissipating less power. As the density and operating speed of CMOS chips increase power dissipation has become a critical concern in the design of VLSI circuits, especially in mobile and portable ASIC system. In conventional CMOS circuits, the approach is to low-power design, including the reduction of supply voltage node capacitance and switching activity. [1]

B. Power Dissipation in CMOS Circuits

With dissipation of power , the temperature of the chip rises which affects the device both when the device is off as well as when the device is on. Thus, the low power design methodology is dedicated to reduce power dissipation. Two main sources of power dissipation is found:

Static Power Dissipation(P_s) - This power dissipation occurs when the device is in standby mode.Since, there is no DC current path exits from to GND, the resultant quiescent (steady-state) current, and hence power(P_s), is zero. However, there is some small static dissipation due to reverse bias leakage between diffusion regions and the substrate, that includes.

- **Sub-threshold Current**: Sub-threshold current that arises from the inversion charges that exists at the gate voltages below the threshold voltage.
- **Tunneling Current**: There is a finite probability for carrier being passed through the gate oxide. This results in tunneling current thorough the gate oxide.
- **Reverse-biased Diode Leakage**: Reverse bias current in the parasitic diodes.
- **Contention Current in Ratioed Circuits**: Ratioed circuits burn power in fight between ON transistors.

The static power dissipation is the product of the device leakage current and the supply voltage, which is given by:

$$P_s = i_{leakage} * V_{DD} \tag{7}$$

Where, $P_s$is the static power dissipation, $i_{leakage}$ is the leakage current and $V_{DD}$is the power supply voltage.

Dynamic Power Dissipation It occurs due to charging and discharging of load capacitances (mostly gate and wire capacitance, but also drain and source capacitances). In one complete cycle, current flows from to the load capacitance to charge it and then flows from the charged load to ground during discharge.

$$P_D = \alpha C_L V_{DD}^2 f_{clk} \tag{8}$$

Where $P_D$is the dynamic power dissipation, C_L is the load capacitance, V_{DD} is the power supply voltage and $f_{clk}$is the clock frequency and is activity factor. A clock has $\alpha = 1.0$ because it rises and fall every cycle, but most data have a maximum activity factor $\alpha = 0.5$ because they transition only once every cycle.

Short Circuit Power Dissipation

It occurs during signal transitions when both the NMOS and PMOS transistors are ON for a short period of time and there is a direct path between Vdd and GND, which results in a "short-circuit" current pulse from to GND. Typically this increases power dissipation by about 10%. Thus the total power dissipationis given by, $P_{total} = P_s + P_D + P_{SC}$. To cope up with the limitations of power dissipation we scale down the dimensions of the transistor since the power delivered is proportional to the square of supply voltage . [4]

IV. Design of the Ring Oscillator

The ring oscillator was designed and simulated through LT-Spice. We used a 7-stage inverter Ring oscillator which had the target frequency of 80 MHz. The design was such that the circuit could work at a very low power and which was tunable through a simple RC network with two variable capacitors at the first and the last stages of the circuit. A voltage of 1.8V is input to the drain of the CMOS inverter.

A. Frequency control Capacitor

The circuit is designed on the principle of changing propagation delay by continuous changing of capacitance value in the range of 0.09615pf to 0.0385pf with the help of one common variable capacitor with fixed resistor 100K at initial stage and final stage i.e. at stage 1 and stage 7.Remaining stages are unchanged,having fixed capacitance value of 0.01pf and resistance. The circuit has been designed by choosing centre frequency at 80MHz and having two sideband of 20MHz covering 60 to 100MHz. Here, the major issue is Propagation delay high to low or low to high depend on instantaneous value of variable capacitance and changing when common capacitance using in final stage and 1st stage of inverter in this RO circuit. This unique conception is concise the number of stages and covering entire bandwidth 60MHZ to 100MHz having centre frequency 80MHz.Any frequency can be selected by changing value of variable capacitance C of tune circuit at stage1 and 7. The design of the circuit is shown in Fig 4.

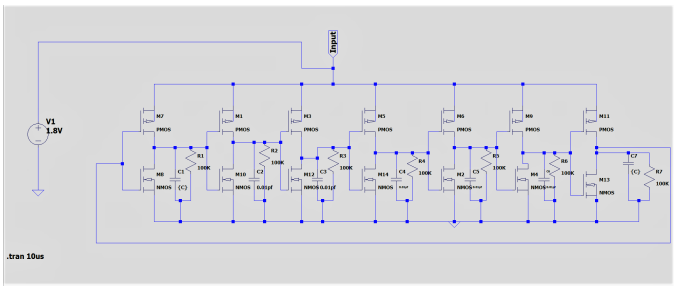

Fig. 4. 7-Stage Ring Oscillator.

Here in Table 1,we include the particular values of the capacitances at which the circuit will work at a frequency of 60,80 and 100 MHz.

TABLE I
VALUE OF CAPACITANCES AT DIFFERENT FREQUENCY

Frequency	Capacitance
60 MHz	0.09615pF
80MHz	0.057pF
100MHz	0.0385pF

V. SIMULATION AND RESULTS

The oscillator circuit designed ran successfully in LT-Spice. We have used the 45nm technology for the design of the circuit. Waveform and the FFT plots were obtained for different frequencies.

A. For 60MHz oscillation circuit

Here the value of the variable capacitance was tuned to 0.09615pF at the first and the last stage with other stages being constant.
The waveform and the FFT plot is shown below in Fig. 5 and Fig. 6 respectively.

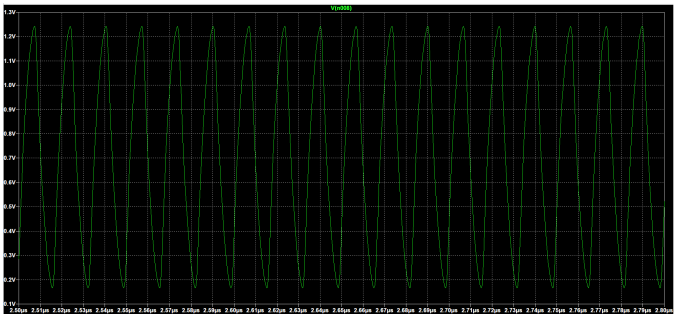

Fig. 5. Waveform of the Ring oscillator at 60 MHz

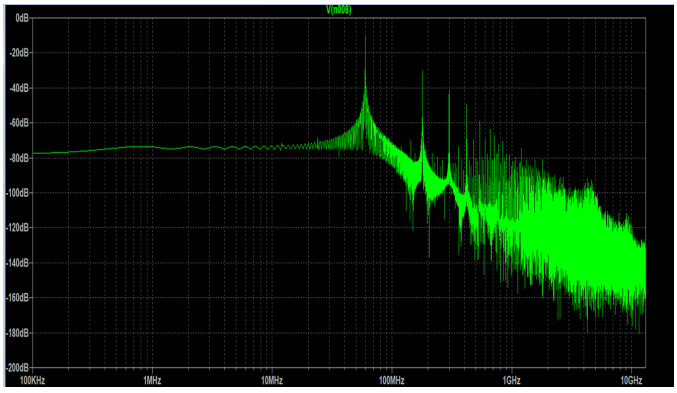

Fig. 6. FFT plot of the Ring Oscillator at 60 MHz.

B. For 80MHz oscillation circuit

Here the value of the variable capacitance was tuned to 0.057pF at the first and the last stage with other stages being constant.
The waveform and the FFT plot is shown below in Fig. 7 and Fig. 8 respectively.

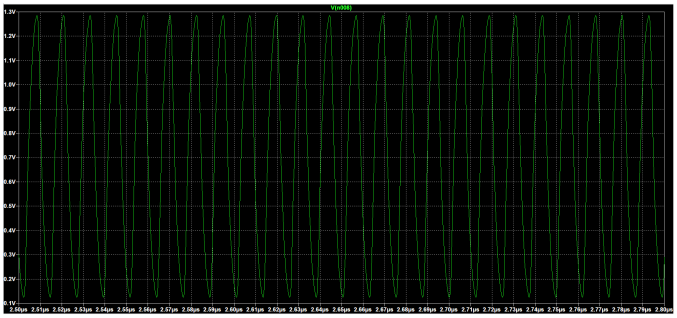

Fig. 7. FFT plot of the Ring Oscillator at 80 MHz.

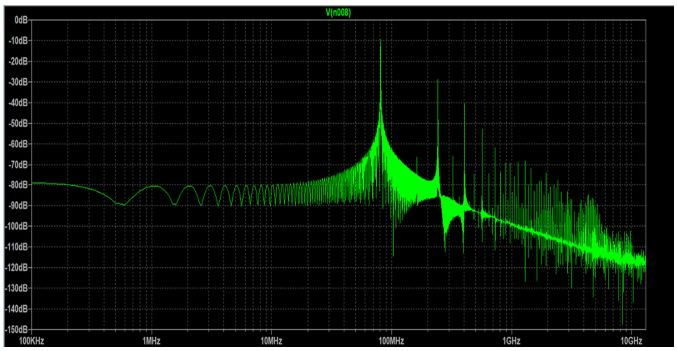

Fig. 8. FFT plot of the Ring Oscillator at 80 MHz.

C. For 100MHz oscillation circuit

Here the value of the variable capacitance was tuned to 0.0385pF at the first and the last stage with other stages being constant.
The waveform and the FFT plot is shown below in Fig. 9 and Fig. 10 respectively.

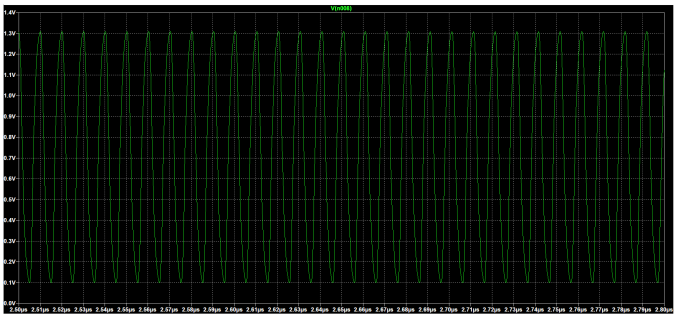

Fig. 9. FFT plot of the Ring Oscillator at 100 MHz.

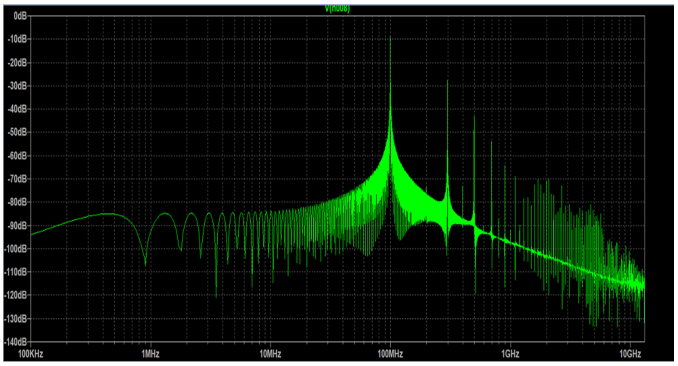

Fig. 10. FFT plot of the Ring Oscillator at 100 MHz.

D. For any frequency(60-100MHz) oscillation circuit

The whole bandwidth of the circuit has been shown with the capactiors being tunable at the minimum and maximum range. It can be seen such a subtle change in frequency can alter the time delay thus altering the frequency. The waveform and the FFT plot is shown below in Fig. 11 and Fig. 12 respectively.

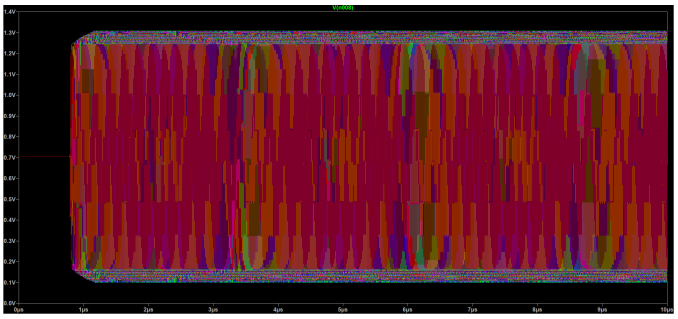

Fig. 11. FFT plot of the Ring Oscillator

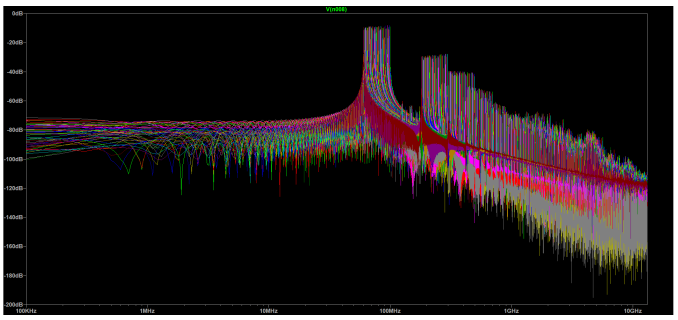

Fig. 12. FFT plot of the Ring Oscillator

VI. Conclusion

The 7-stage ring oscillators have been successfully designed and simulated using LT-Spice tool. In this paper it have shown how the optimization of a capacitor is being taken a major role to establish the desire bandwidth with the power comparison results are tabulated and shown the reduction in power dissipation. The use of the RC Network serves as a huge advantage as a large bandwidth can be achieved with changing the value of the capacitor and the resistor. This knowledge will be highly helpful for the future works to be done on Ring Oscillator.

TABLE II
Observation Table

Parameter(unit)	Minimum Value	Typical Value	Maximum Value
Supply Voltage	-	1.8V	-
Supply Current	55.75μA	56.42μA	57.94μA
Resistance	-	100K	-
Capacitance(Fixed)	-	0.01pF	-
Capacitance(Variable)	0.0385pf	0.057pF	0.09615pf

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