Comparative Analysis of Different Power Efficient SRAM Architectures

University at Buffalo, The State University of New York

Sagnik Ghosh

Shishir Suvarna

INTRODUCTION TO VLSI ELECTRONICS

CSE - 593

GUIDED BY

Dr. Ramalingam Sridhar (Professor, Computer Science and Engineering)

Miss Sheena Ratnam Priya (Teaching Assistant)

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INTRODUCTION:

Today, there is a great need for efficient memory structures which can provide good performance while consuming less power. SRAM stands for Static Random Access Memory. It is static in the sense that its value doesn't need to be refreshed.

It holds its value as long as supply voltage is given. SRAM is popular in the industry because of its reliability, performance, low idle power consumption.

Apart from the standard 6T SRAM cell, other modified architectures have been developed to achieve low power consumption and analyses have been performed.

WHAT IS SRAM?

SRAM stands for Static Random Access Memory. It is a subtype of the more general Access Memory (RAM). One of the main characteristics of SRAM is that it can hold its contents as long as power is being supplied. In other words, data bits are retained as long as supply voltage is active.

SRAM has some important advantages over Dynamic Random Access Memory (DRAM). It is much faster than DRAM as it provides access to data at higher speeds. Unlike DRAM, it is a static memory and can hold its state without needing to be refreshed. DRAM on the other hand, might need to be refreshed hundreds of times per second. Other practical advantages include reliable performance and low idle power consumption making it an efficient form of memory.

However, SRAM is also significantly more expensive than DRAM. Hence, it is more useful for applications like CPU caches while DRAM is more useful as main memory.

There are two types of SRAM – synchronous and asynchronous. Synchronous RAM is the faster of the two, as it is able to synch with the microprocessor or CPU's clock speed.

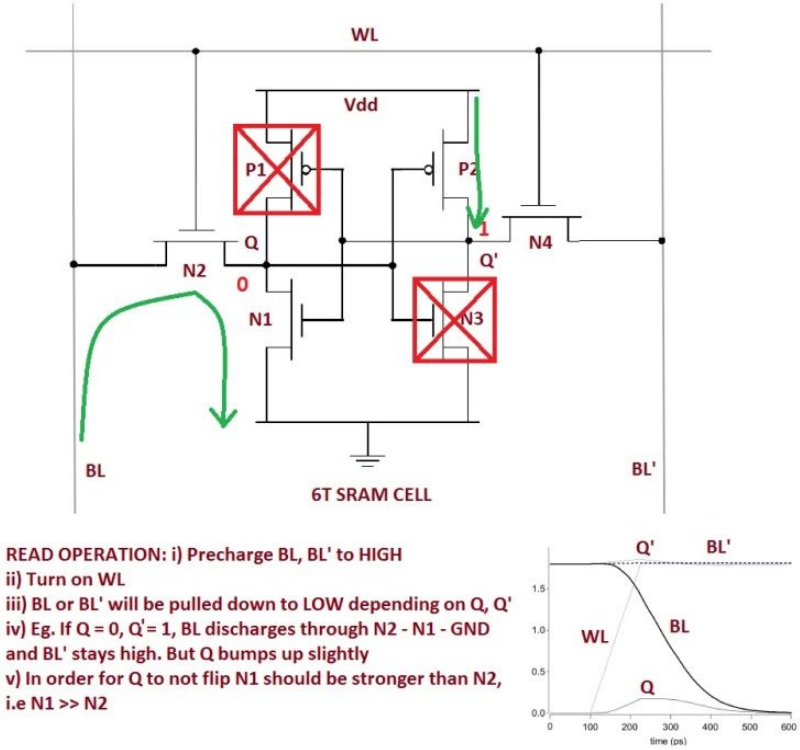
SRAM cell is a volatile memory and the data is lost when the power is cut off. But unlike DRAM, it doesn't have leakage and holds its value in a stable value when active. Hence, it doesn't need to be refreshed.

6T SRAM CELL:

Depending on the number of transistors in the cell, SRAM cell may be 6T, 7T or 8T. A 6T SRAM cell consists of six MOSFET transistors. Four of these transistors are used to constitute two inverters which are cross coupled with each other. The other two transistors are used as access transistors. It uses bi-stable flip flop circuits and holds two stable states, 0 and 1.

The access transistors are activated when the Word-Line is high.

READ OPERATION:

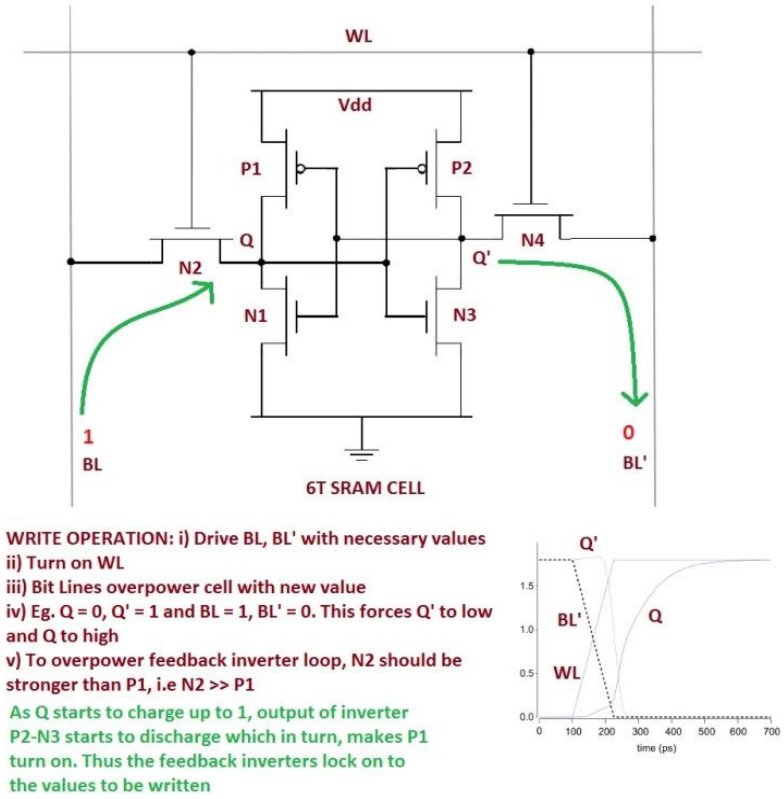


The Read operation is one of the two main operations of the SRAM cell. Both the read and write operations are facilitated by the activations of the two bitlines.(Bitline and Bitline'). This occurs when the Word-Line is active.

Depending upon the values of Q and Q', BL and BL' can be pulled down provided they have been pre-charged to high. If Q=0 and Q'=1, then BL discharges through the path N2 then N1 and then ground. BL' stays high.

The value of Q will not flip provided that access transistor N1 is stronger than N2. This change in voltage is read by the Sense Amplifier which reads the decrease in voltage BL' and shows a high output for Q. This is a Read operation for the cell.

WRITE OPERATION:



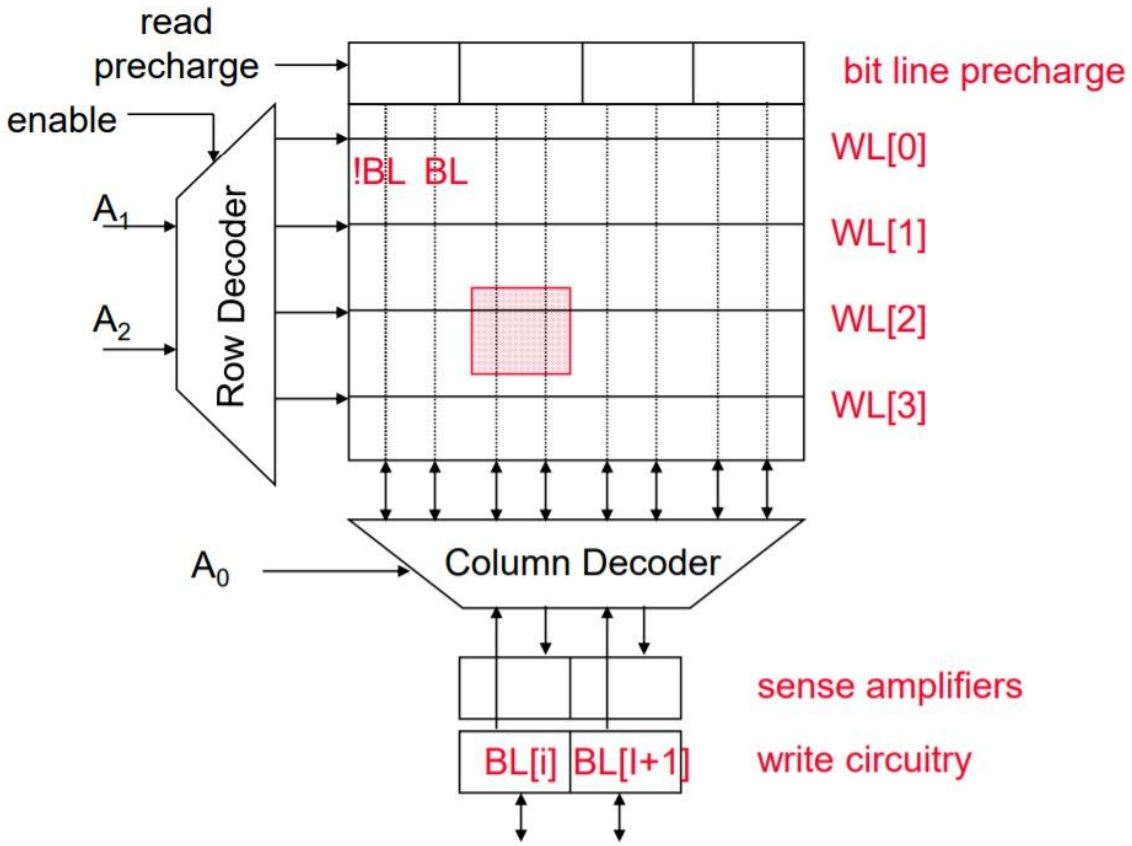
In the write operation bit and bit' are input lines. Consider the memory bits consists of Q=0 and Q'=1. Initially word line is high and hence write operation can be performed.

As we have control on the bit lines, initially make the BLB connected to ground so that we can have the voltage difference between Q' and BLB.

To write 1 into the SRAM cell, M1 must be stronger than M2, this can be achieved by changing the aspect ratio of the transistors. Hence Q will be 1. Initially Q=0 after the operation Q=1, hence we write successfully into the memory.

SRAM ARCHITECTURE:

SRAM array consists of SRAM cell, write driver circuit, precharge circuit, sense amplifier and row/column decoder. A SRAM cell is capable of storing one bit of binary information. SRAM array consists of horizontal rows and vertical columns. In array architecture, there are 2N rows that are called as word lines and 2M columns that are called as bitlines. The total number of memory cells in the array is 2(N+M). For this implementation, we have a write driver circuit and sense amplifier dedicated for one column.



ADDRESS DECODER:

In digital electronics, an address decoder is a binary decoder that has two or more inputs for address bits and one or more outputs for device selection signals.When the address for a particular device appears on the address inputs, the decoder asserts the selection output for that device. A dedicated, single-output address decoder may be incorporated into each device on an address bus, or a single address decoder may serve multiple devices.

A single address decoder with n address input bits can serve up to 2n devices. The name “Decoder” means to translate or decode coded information from one format into another, so a binary decoder transforms “n” binary input signals into an equivalent code using 2n outputs.

Binary Decoders are another type of digital logic device that has inputs of 2-bit, 3-bit or 4-bit codes depending upon the number of data input lines, so a decoder that has a set of two or more bits will be defined as having an n-bit code, and therefore it will be possible to represent 2n possible values. Thus, a decoder generally decodes a binary value into a non-binary one by setting exactly one of its n outputs to logic “1”.

If a binary decoder receives n inputs (usually grouped as a single Binary or Boolean number) it activates one and only one of its 2n outputs based on that input with all other outputs deactivated.

Generally a decoders output code normally has more bits than its input code and practical “binary decoder” circuits include, 2-to-4, 3-to-8 and 4-to-16 line configurations.

For the purpose of this project we use two 2-to-4 line address decoders, namely, **a row decoder** and a column **decoder.** These two address decoders are employed to decode the given address and alter the actual row or column. Row and column decoder is employed to pick out a specific WL and that of an SRAM array. Figure shows the diagram of decoder that have two inputs (A and B) and four outputs.

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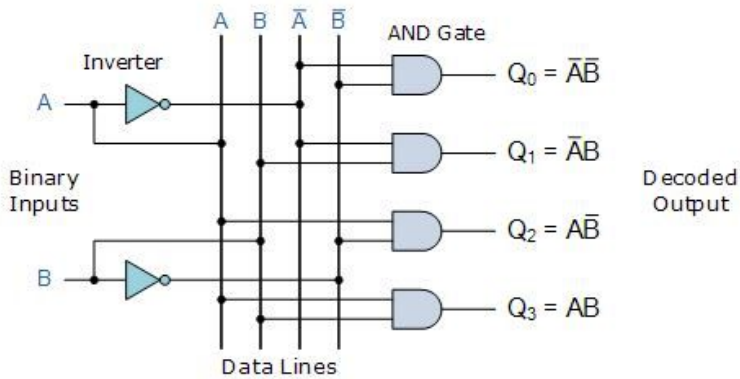
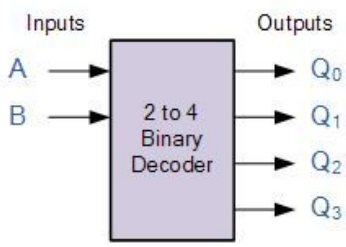
A 2-to-4 Binary Decoders



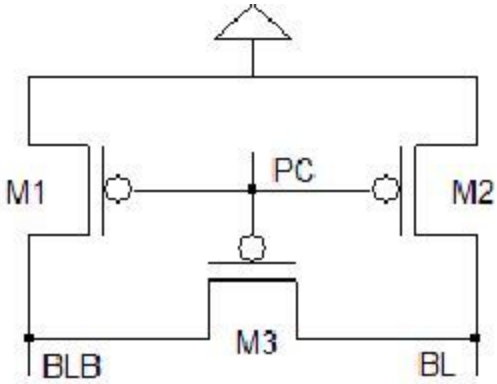


Truth Table

A	B	Q_0	Q_1	Q_2	Q_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

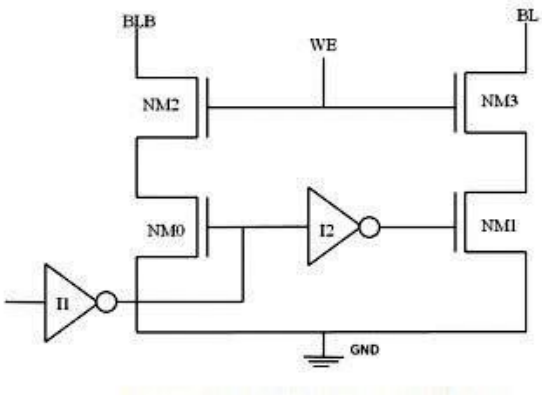
PRECHARGE CIRCUIT:

The pre-charge circuit is the main component that is implemented in SRAM array. following figure represents the circuit diagram of pre-charge circuit. Pre-charge circuit consists of three PMOS transistors. Two upper transistors are used for pre-charging and the lower one is used for equalization. The main role of pre-charge circuit is to charge both the bit lines up to VDD before a read and write operations. Each column incorporates a single pre-charge circuit within the array.



WRITE DRIVER CIRCUIT:

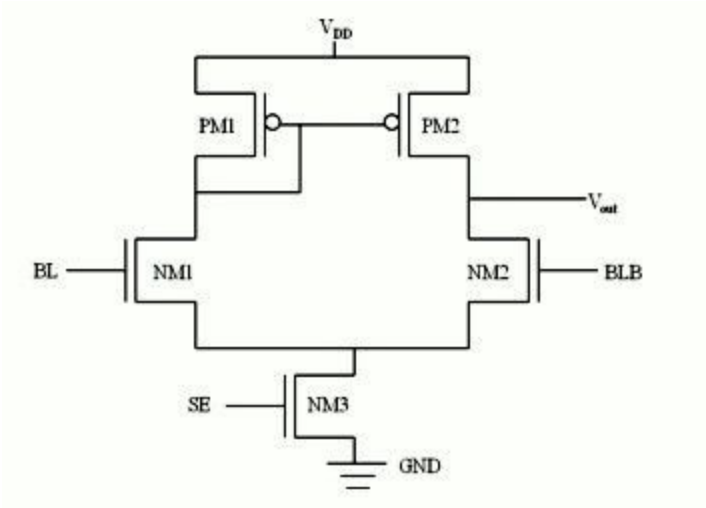
The main role of write driver circuit is to complete discharge one of the bitlines from the precharge level. Write driver is enabled by a Write Enable (WE) signal. Only one write driver circuit is required for each column in the array. Write driver circuit shows in the following figure. It consists of two inverters (I1 and I2) and four NMOS (NM0, NM1, NM2 and NM3) transistors. Channel length of NMOS transistor is 5µm and channel width is 200nm is considered.



SENSE AMPLIFIER:

Sense electronic equipment is an important element of SRAM. Figure below shows the circuit diagram of Differential Sense electronic equipment. It's conjointly referred to as voltage mode sense electronic equipment.

Sense amplifiers detects the voltage difference between the bit-lines and show which data value stored in the memory cell. The circuit consists of cross coupled inverters that converts the bit-line voltage difference at their input to full swing output. BL and BLB inputs are coupled to the column bit-lines of the cell.



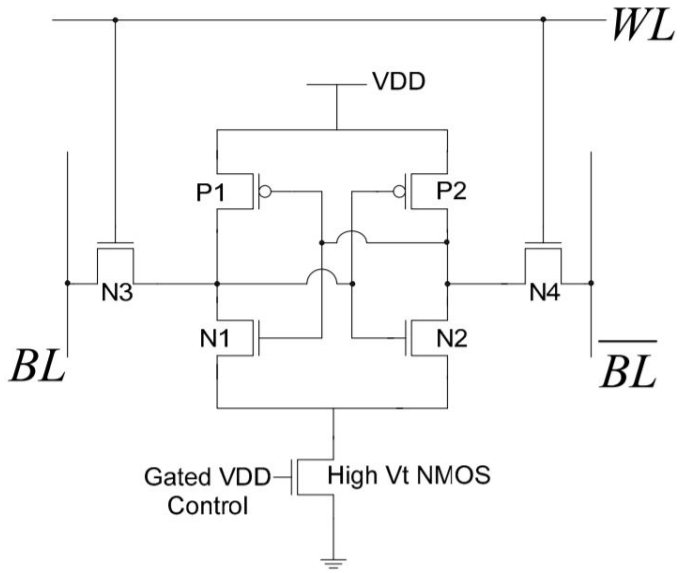
To read a bit from a particular memory cell, the word line along the cell's row is turned on, activating all the cells in the row. The stored value (Logic 0 or 1) from the cell then comes to the Bit-lines associated with it. The sense amplifier at the end of the two complementary bit-lines amplify the small voltages to a normal logic level. The bit from the desired cell is then latched from the cell's sense amplifier into a buffer, and put on the output bus.

GATED VDD SRAM CELL:

In this version of the SRAM Cell, a voltage control mechanism is used. This can disable the supply voltage (VDD) when the SRAM cell is not in use thereby reducing leakage current. This in turn reduces the leakage power dissipation by a great amount. In order to implement this mechanism, we

introduced a High Threshold Voltage transistor in the ground path (can also be introduced in the supply (VDD)) of the SRAM cell.

Transistors with High threshold voltages can greatly reduce static power leakage in the circuit, but they switch slower. On the other hand, transistors with low threshold voltages switch faster but at the expense of higher static power leakage.



The other transistors are kept as Low Threshold Voltage transistors. The 'Gated VDD Control' signal is used to turn on or turn off the SRAM cell. Thus, the term 'Gated' is used to describe this technique.

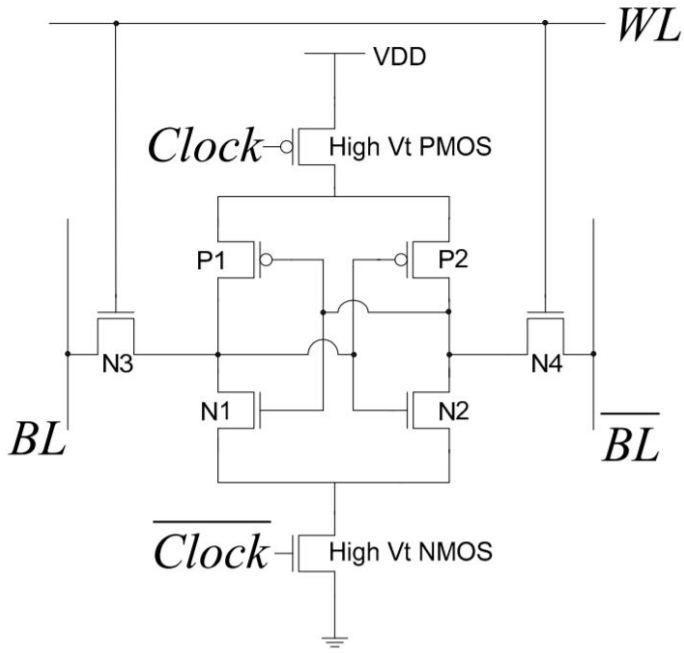
The low Vt transistors (which switch faster than High Vt transistors) are used in the main cell for quicker operation. advantage of this technique is the maintenance of system performance even when supply voltage and threshold voltages of the transistors are reduced.

Low Vt transistors are used as they switch faster than High Vt transistors. This makes the SRAM cell operate fast. This configuration results in optimum power consumption and delay.

MTCMOS SRAM CELL:

MTCMOS stands for "Multi-Threshold CMOS". The MTCMOS SRAM cell utilizes multiple threshold voltages for different transistors in the circuit in order to increase power efficiency of the circuit.

One efficient way to introduce multiple voltages is to introduce sleep transistors in the circuit. Sleep transistors are high threshold voltage transistors which can be controlled by clock signals clk and clkbar. When clk and clkbar are low and high respectively, the sleep transistors are activated and are said to be in "active mode". Conversely, in sleep mode, the transistors can be turned off.



By creating sleep transistors, we create virtual power rails in the circuit. What this means, is that instead of connecting the SRAM cell to the power rails (Vdd and ground), we connect it to a virtual Vdd and Virtual Ground. These in turn supply the logic for the circuit.

For the main circuit, we have used low threshold voltage transistors which allow it to perform efficiently, while constructing the sleep transistors to have a high threshold voltage for the purpose of power optimization. Hence the circuit as a whole is able to achieve a balance between performance and efficiency. MTCMOS implementation is the most efficient among all three designs in terms of power consumption. This is because we are controlling both Vdd and Gnd as opposed to Gated Vdd where we control just the Gnd.

SLEEP TRANSISTORS

As discussed earlier, sleep transistors need to have high threshold voltage. In order to achieve this, we need to vary the threshold Voltage Vt for it. However, Cadence doesn't allow us to change this value directly. We referred to the CMOS textbook by Sung-Mo Kang and understood the threshold voltage equation. We understood that we could vary the threshold voltage by varying the Source to body substrate bias (Vsb). In order to accomplish this in cadence, we had to introduce a Vdc component in our circuit and connect it with the sleep transistors.

Thus, the most general expression of the threshold voltage V_T can be found as follows:

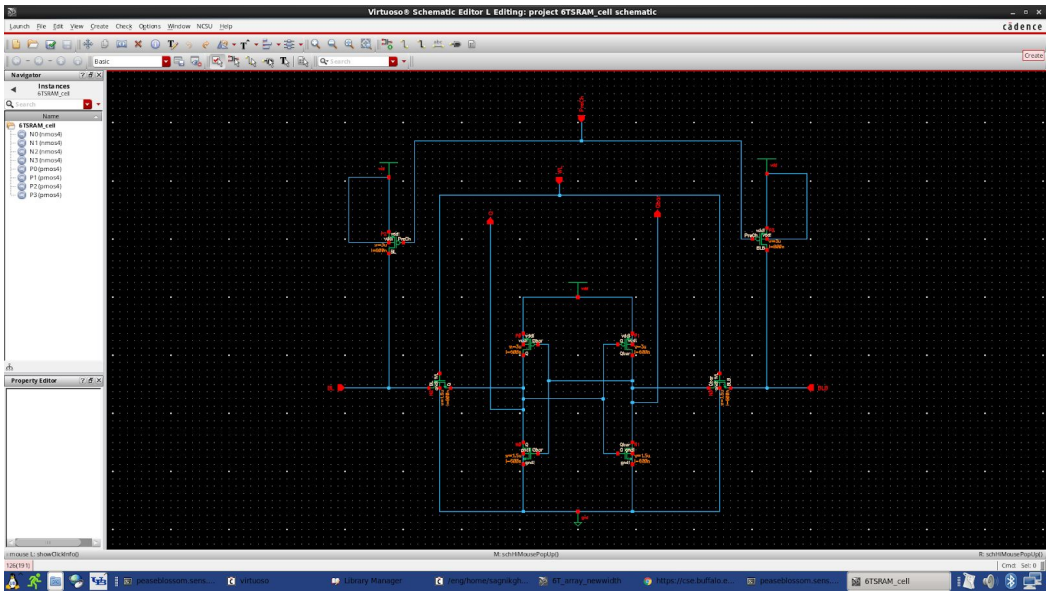
$$V_T = V_{T0} + \gamma \cdot \left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|} \right) \qquad (3.23)$$

Introduction of sleep transistors in circuits can cause data loss in an SRAM cell. As mentioned before, the sleep transistors act as virtual power rails and are responsible for data retention in the cell. When the cell is in sleep mode, the virtual Vdd is prone to discharge . Hence, the cell can be kept in sleep mode only for a fixed period of time before which the data is lost due to discharge.

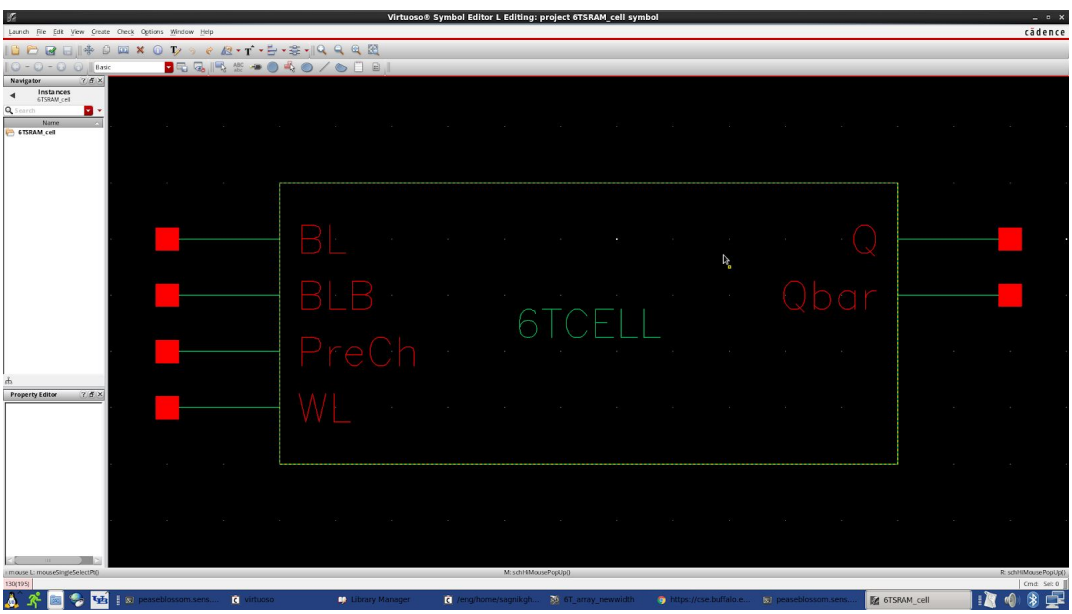
To overcome this issue, we must activate the sleep transistors before the time period expires. Upon doing so, the actual VDD and ground is restored to the network, thereby preventing data loss in the cell. Therefore the frequency of the Clock pulse that controls the sleep transistors is very important. Alternatively, a smart power management unit can be designed which provides the Clock signal to the sleep transistors as and when required.

SCREENSHOTS AND OUTPUTS

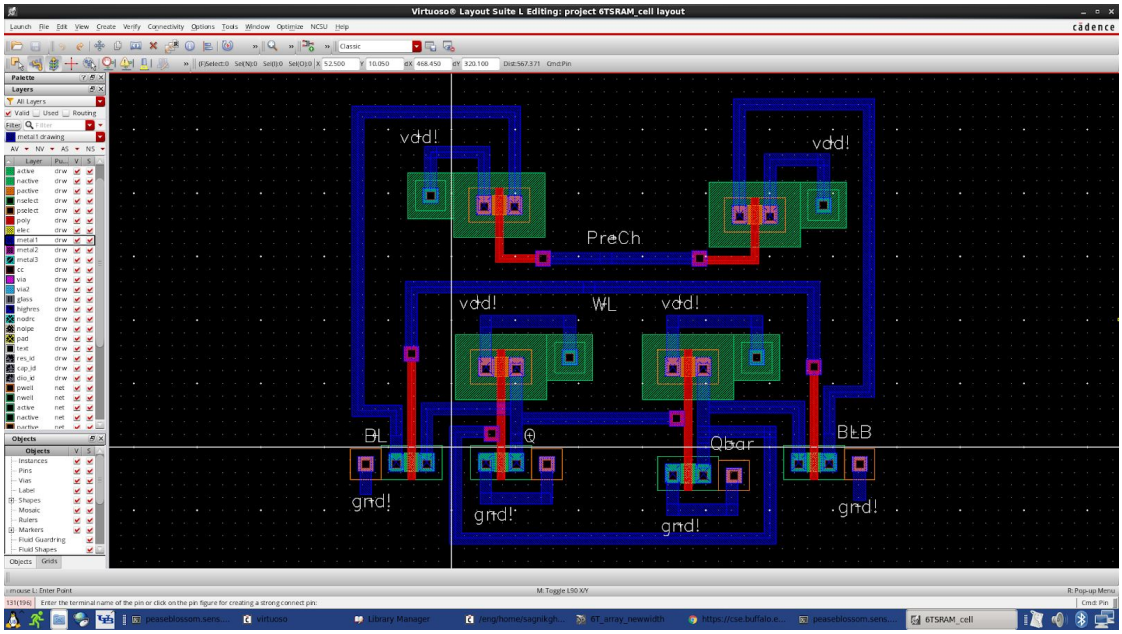
- **6T CELL**



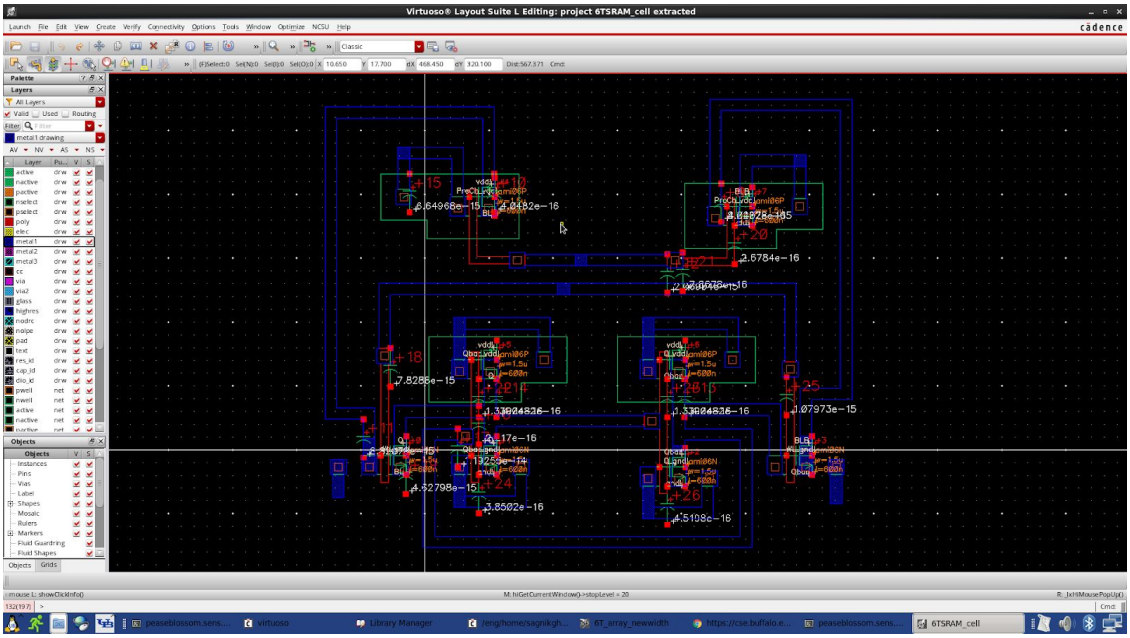
Schematic Diagram



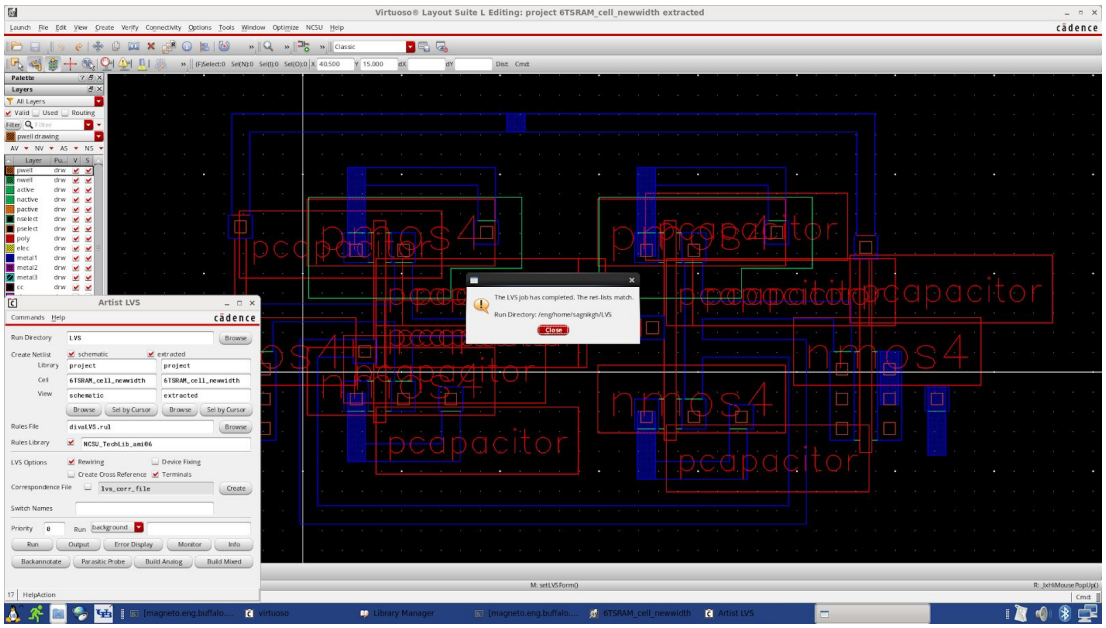
Symbol



Layout View



Extracted View

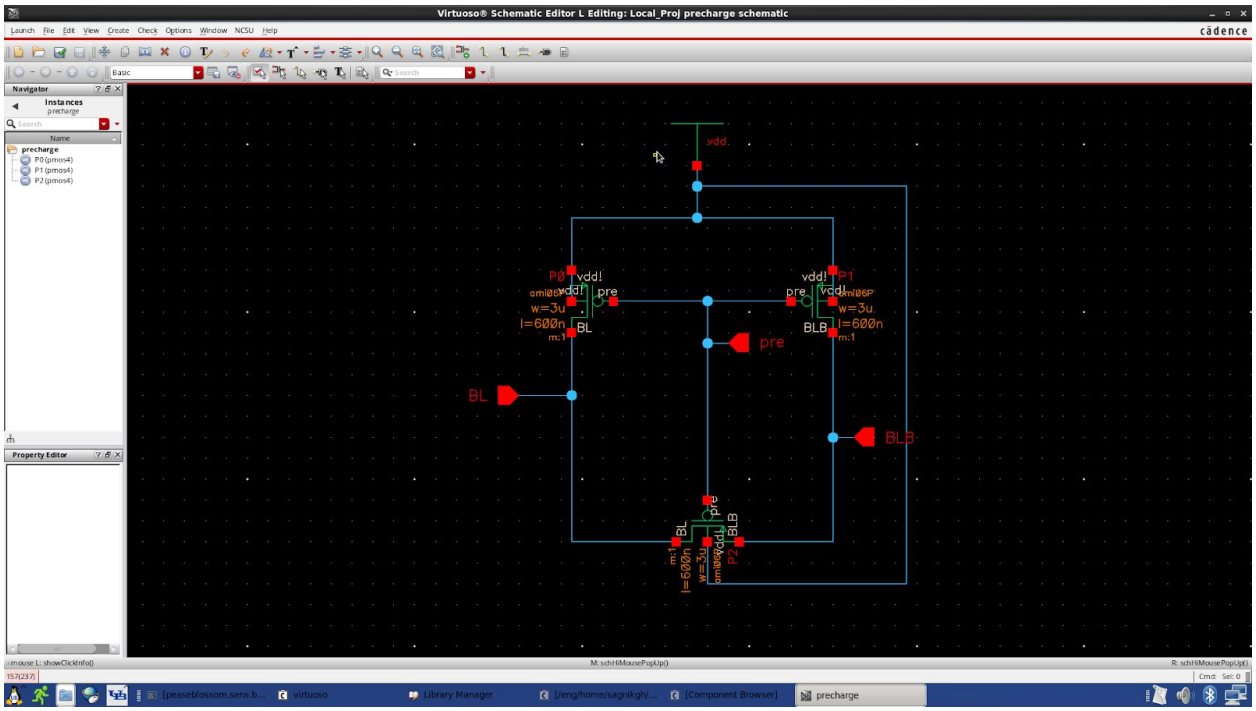


LVS match

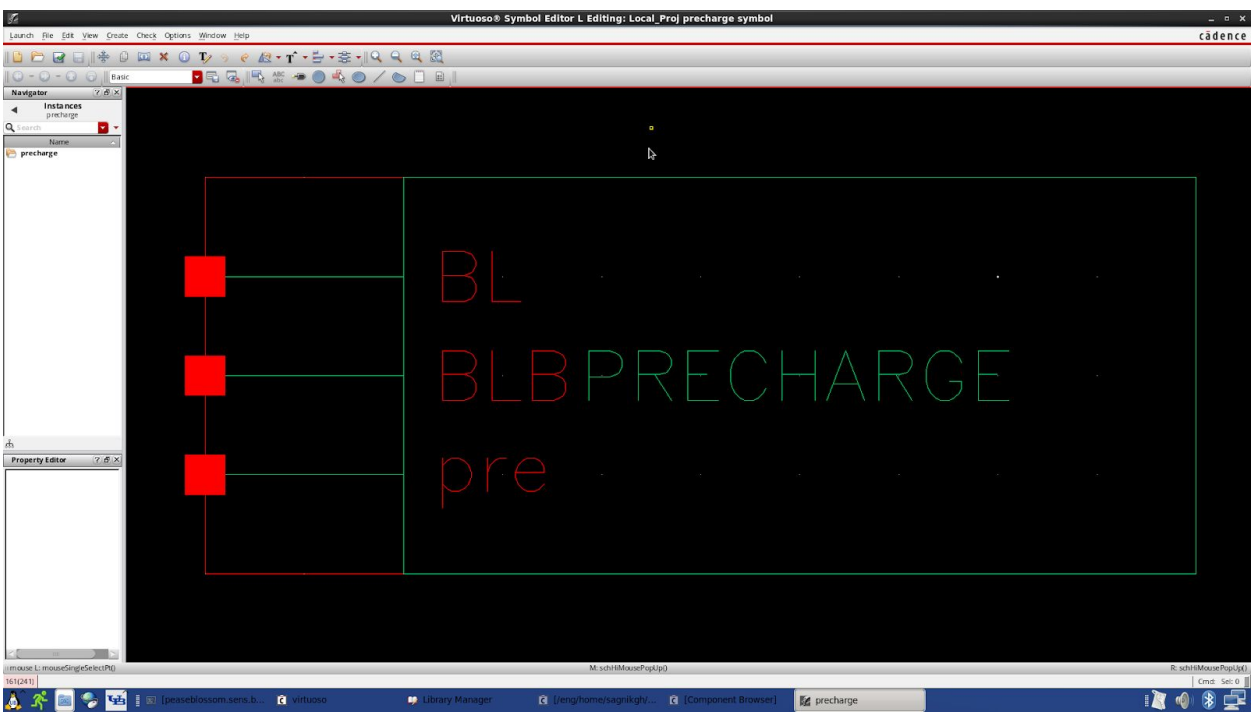
Simulation (Read and Write Operation)

Both values in BL and BLB are varying according to the given pattern parameters. The above simulation result shows how the Q and Q' is following BL and BLB respectively. Both Q and Q are both are starting from their threshold voltage and after one clock cycle its following the exact voltage pattern of BL and BLB. This signifies that the write operation is being performed. This is continuing as long as the Wordline is high, as soon as the word lines turning off, the cell is shifting to the hold state and it is retaining the final value.

- ## PRECHARGE CIRCUIT



Schematic Diagram



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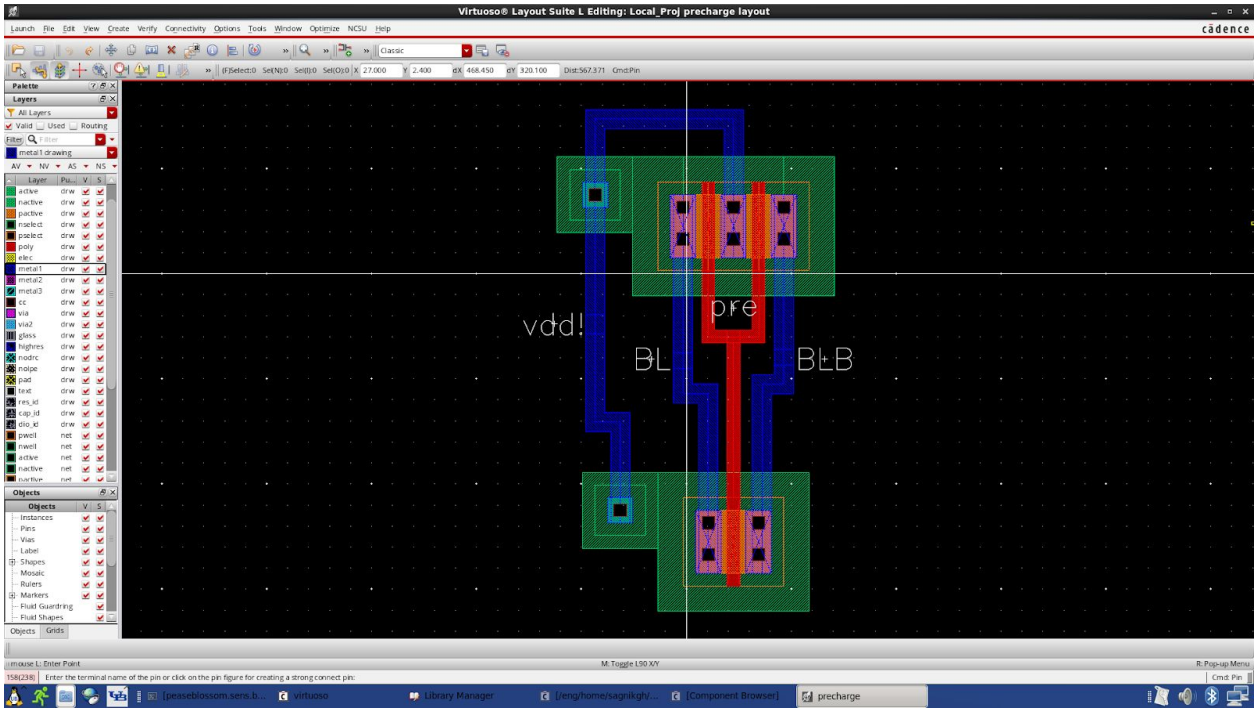

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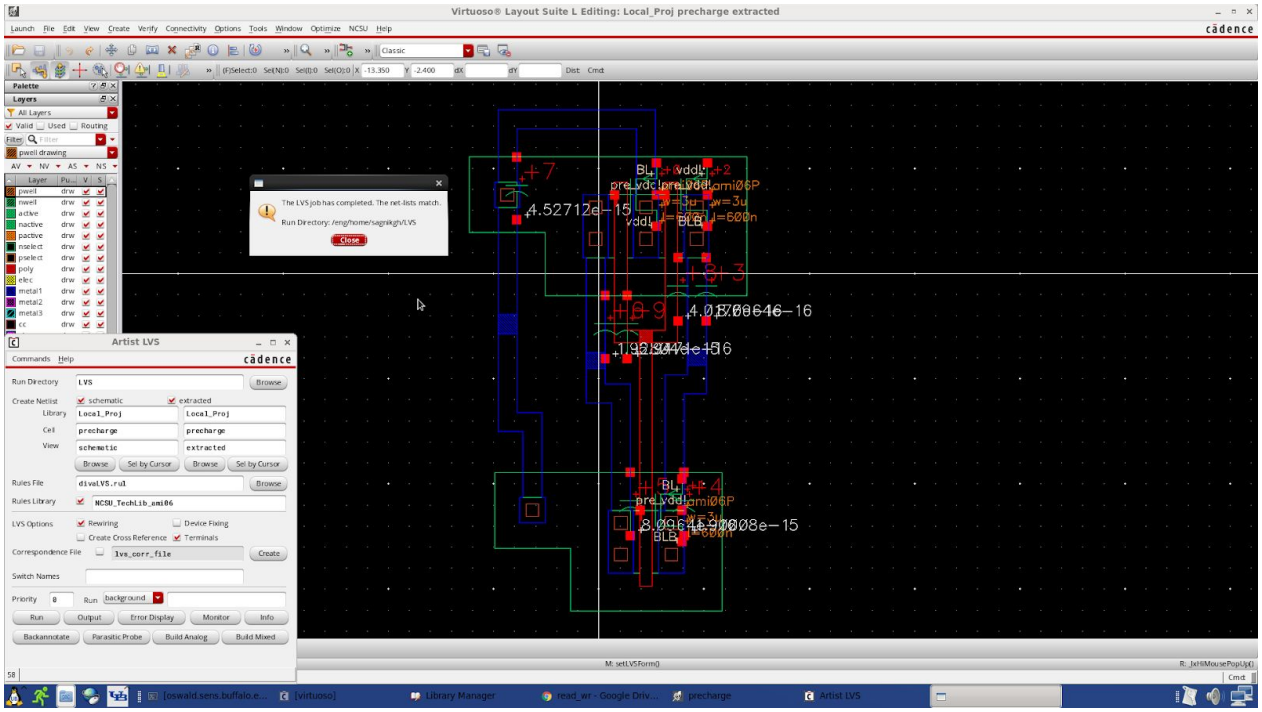
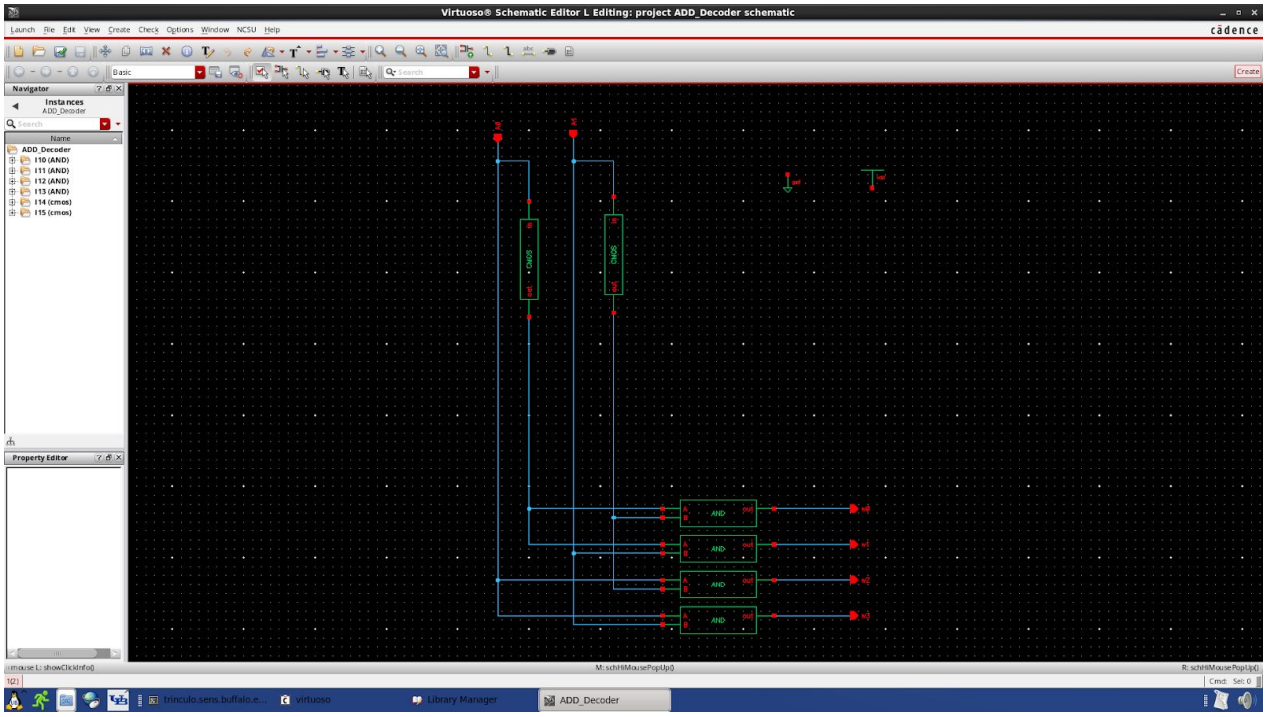
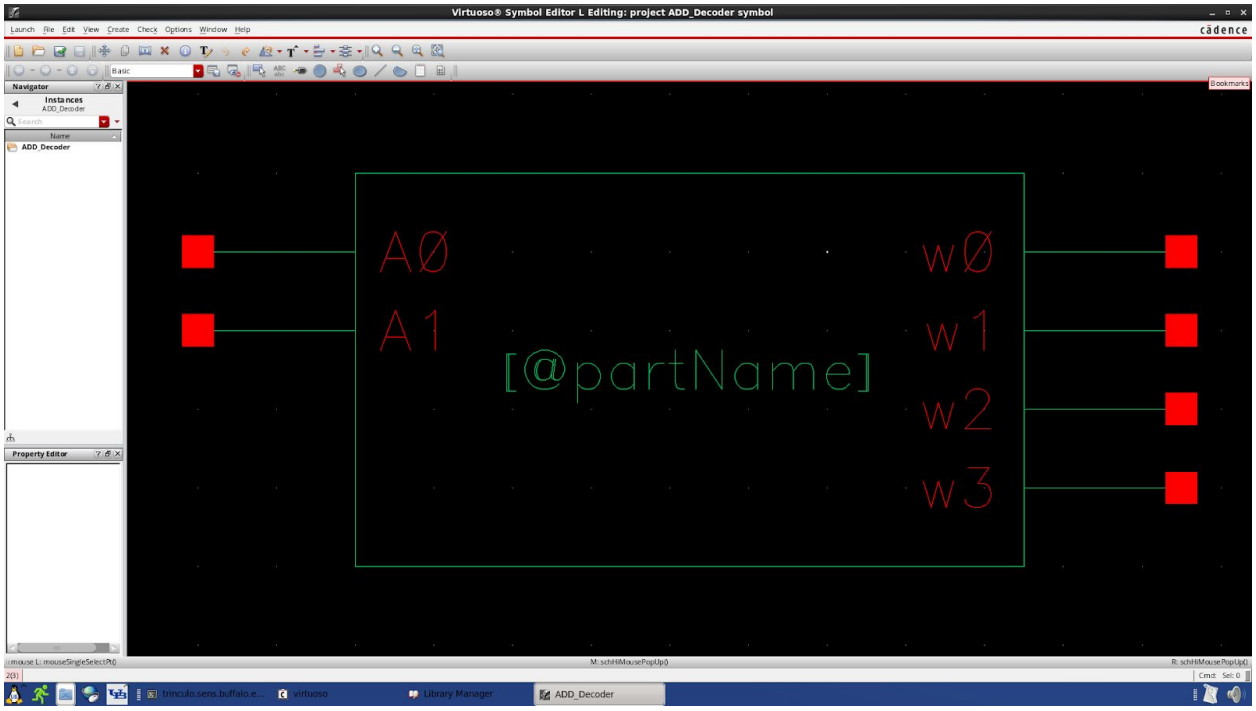


Extracted View

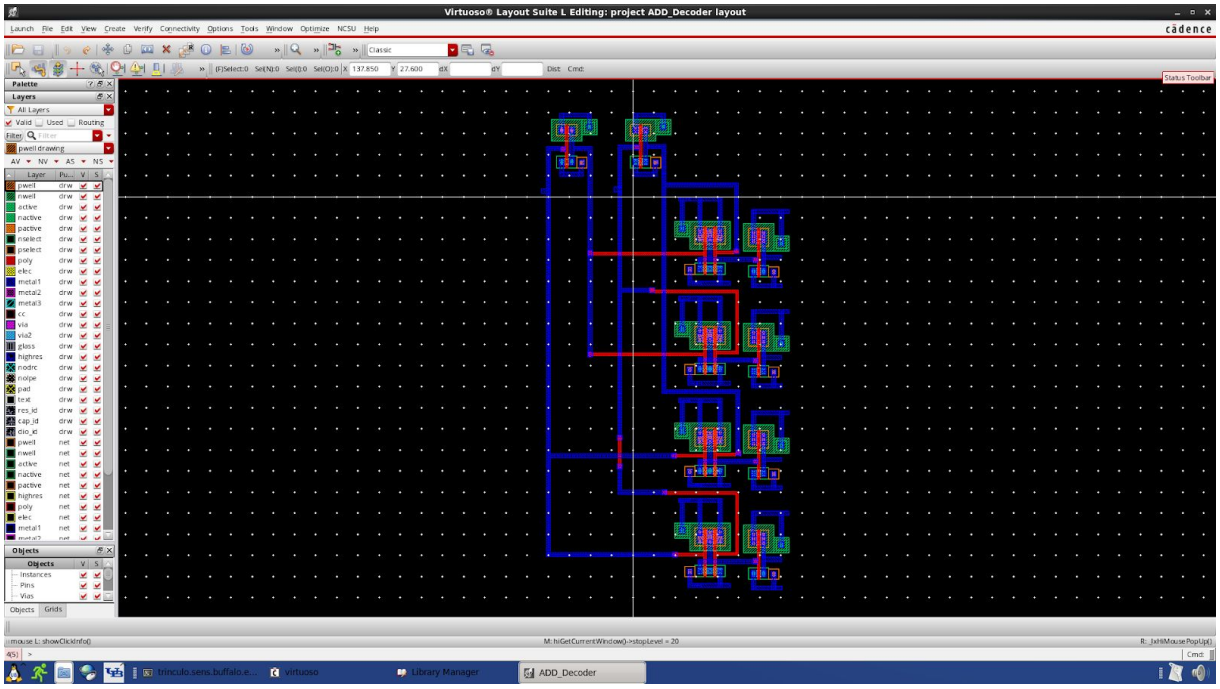
- ## ADDRESS DECODER



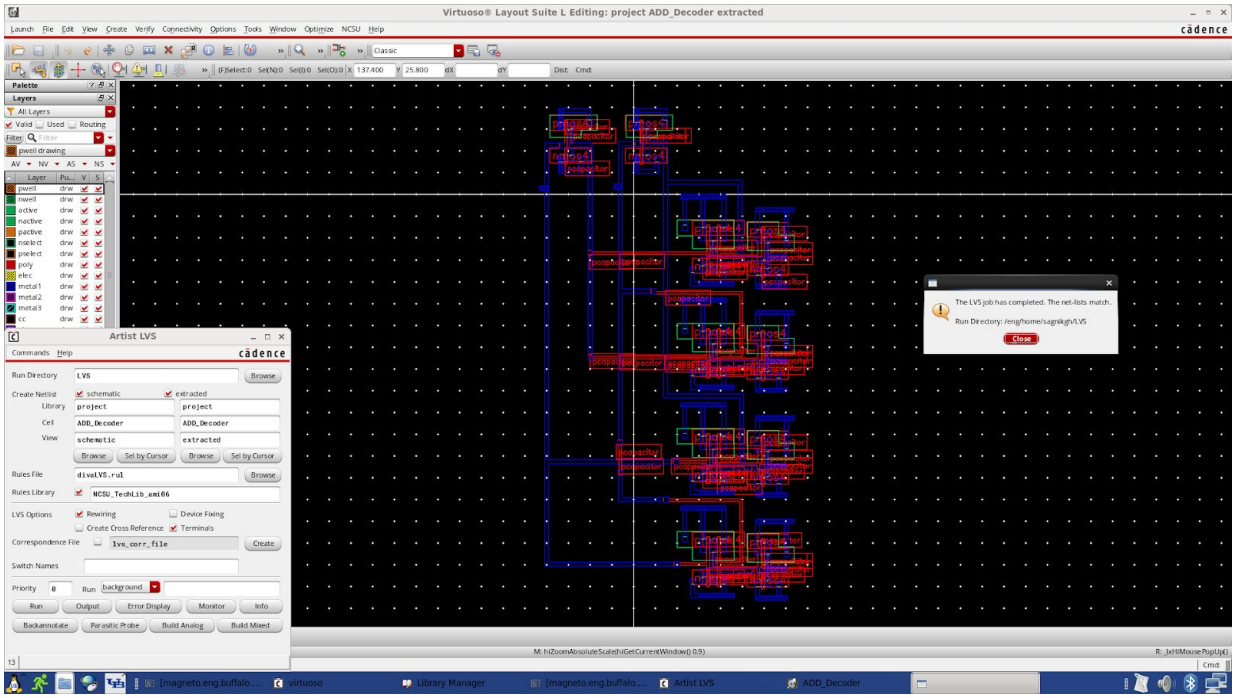
Schematic Diagram



Symbol

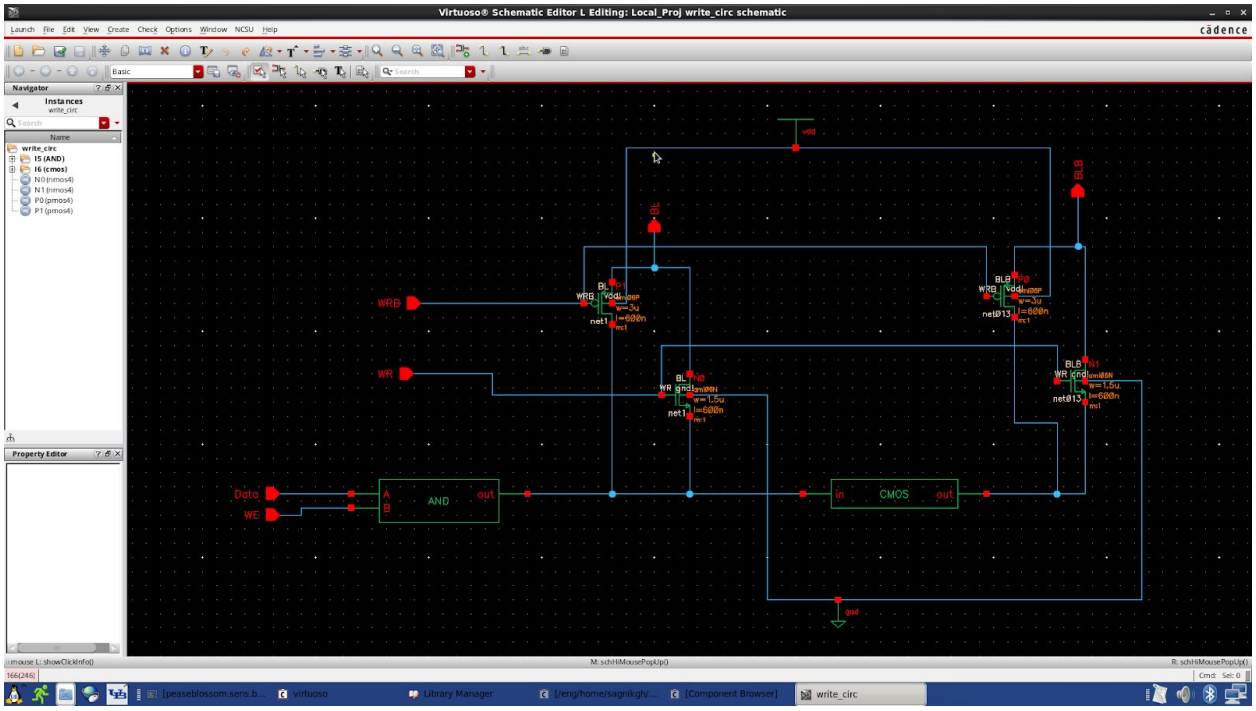


Layout View

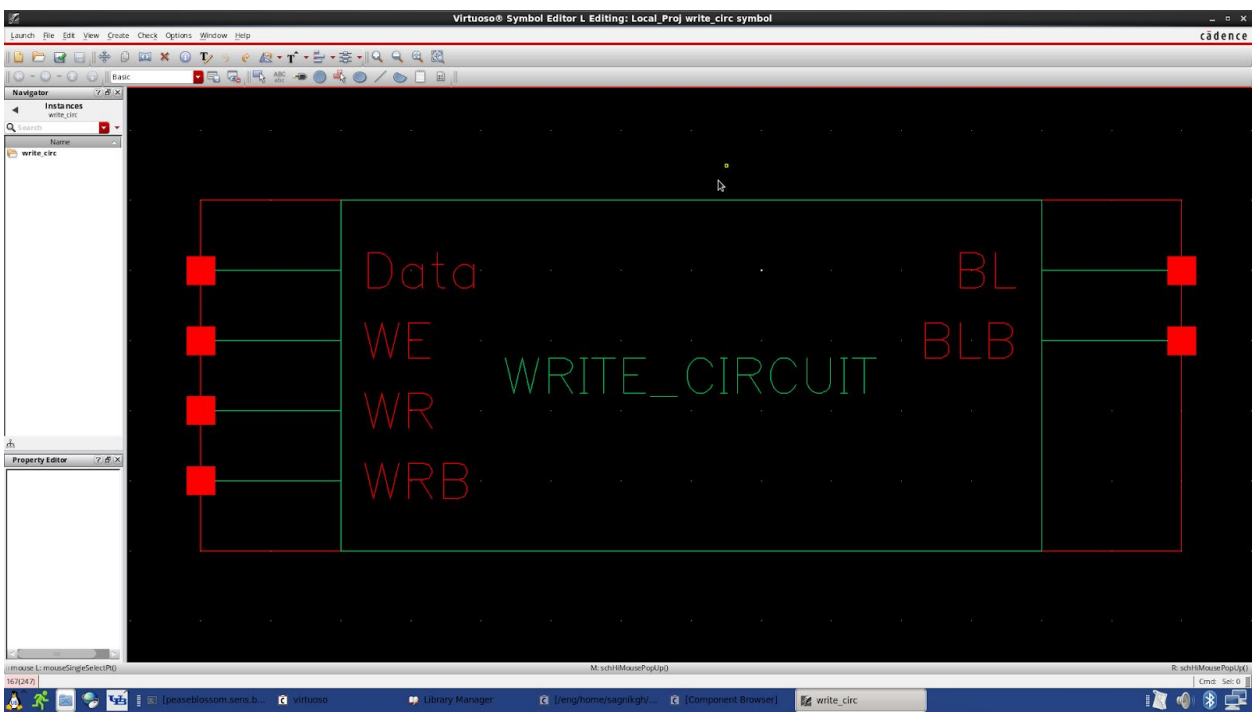


Extracted View

- ## WRITE DRIVER CIRCUIT



Schematic Diagram



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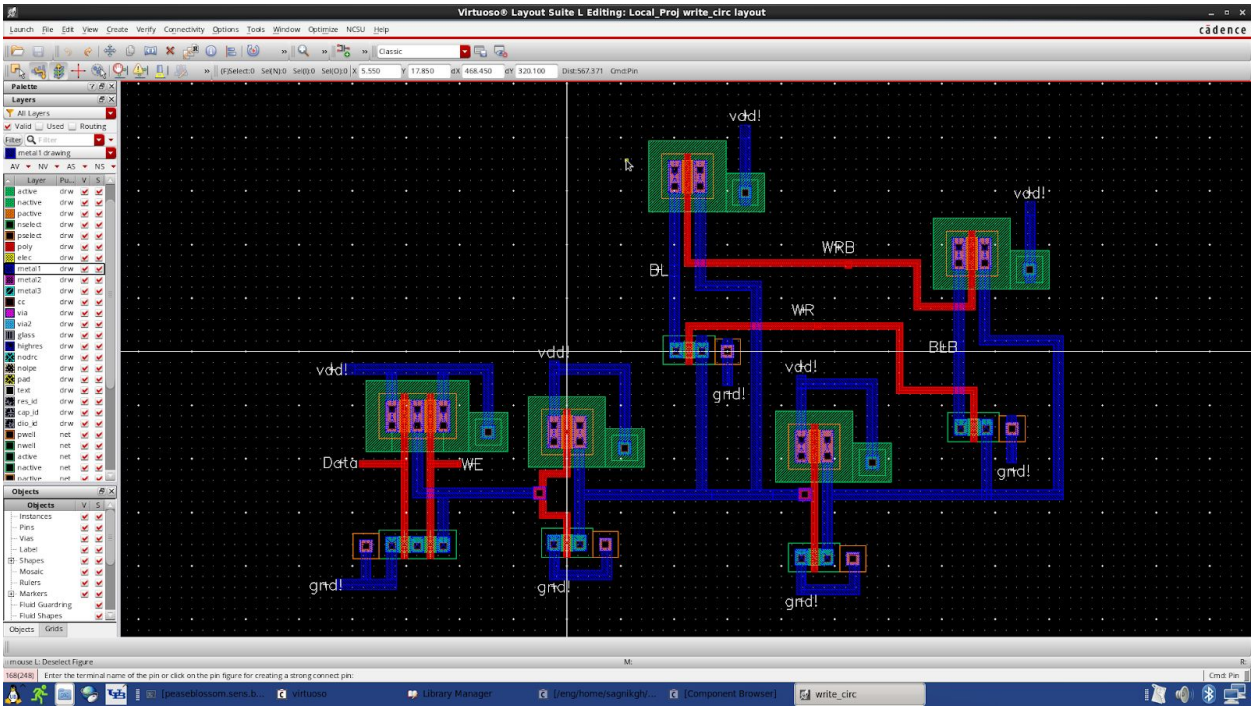

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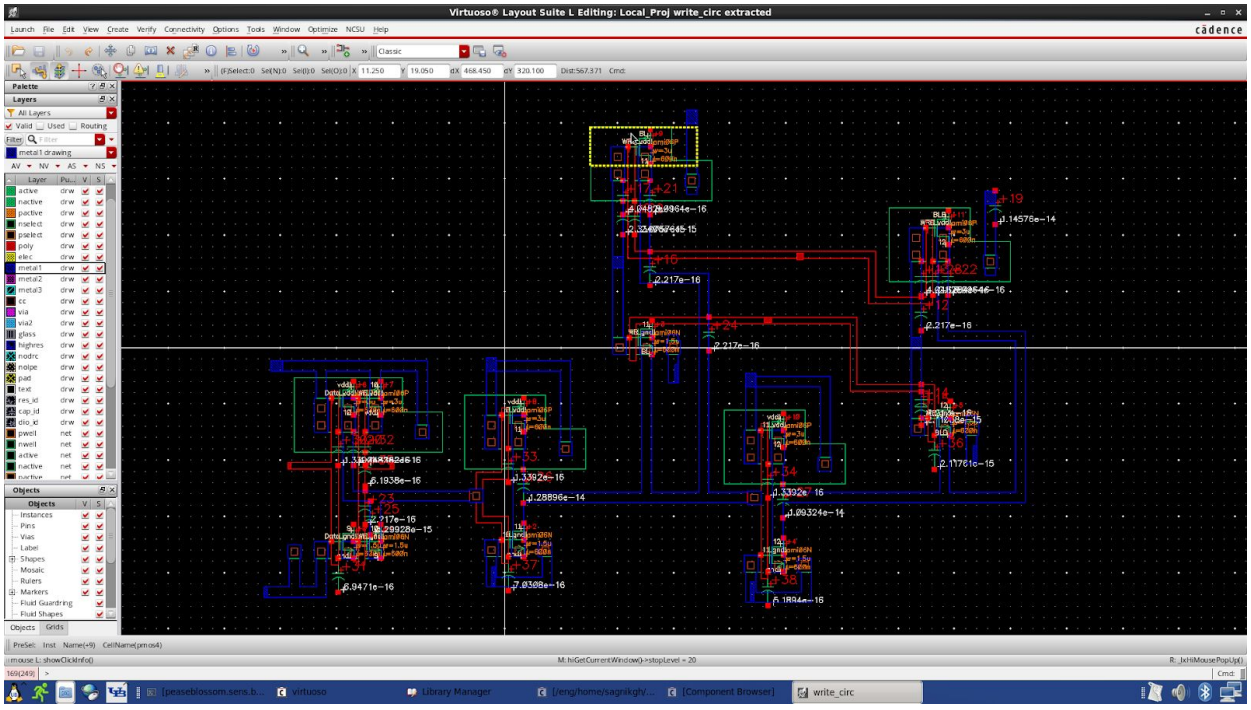
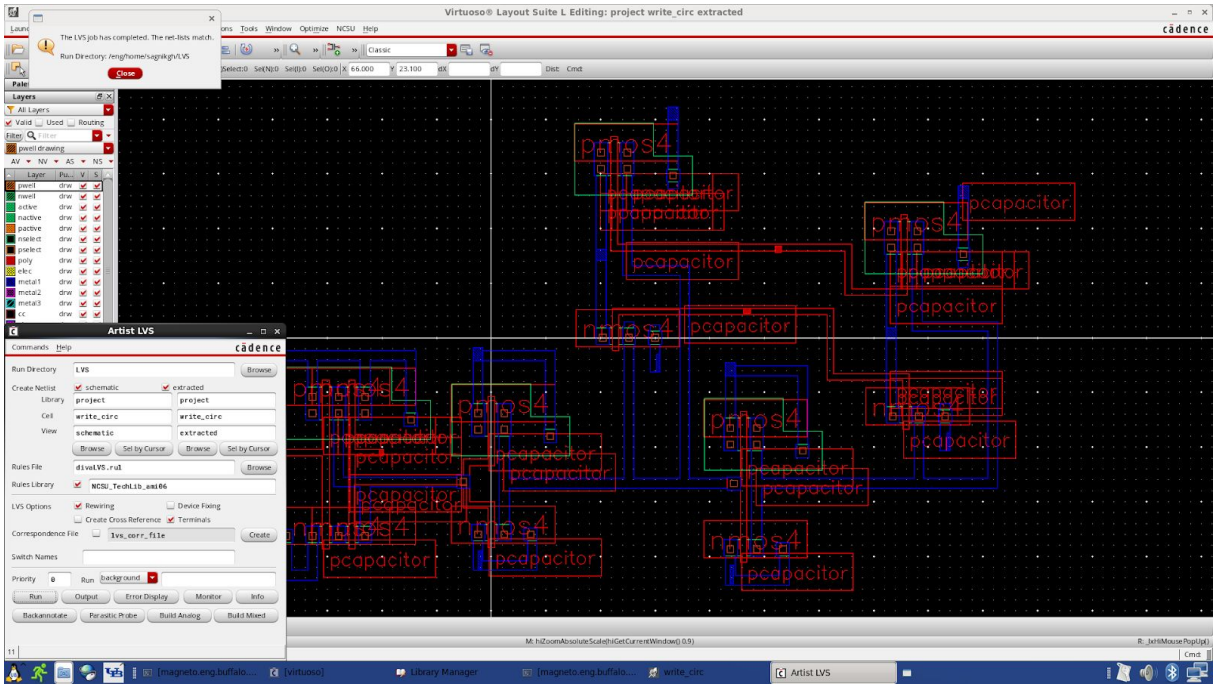
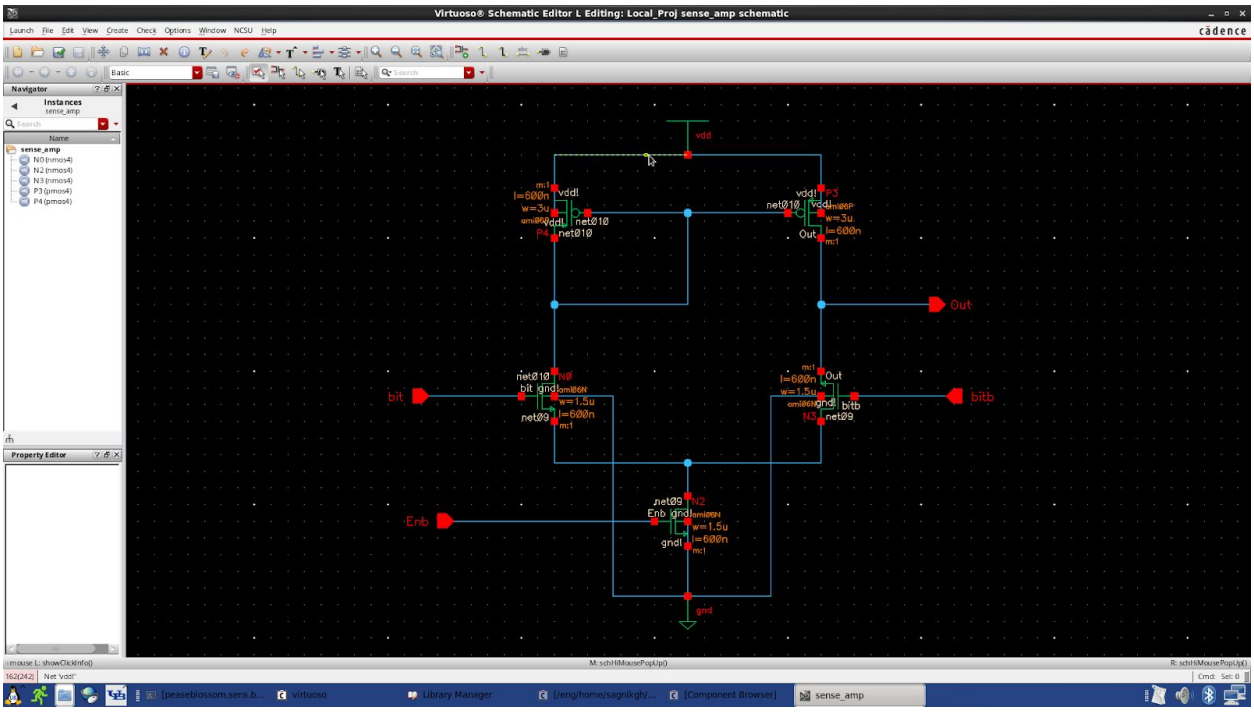


Extracted View

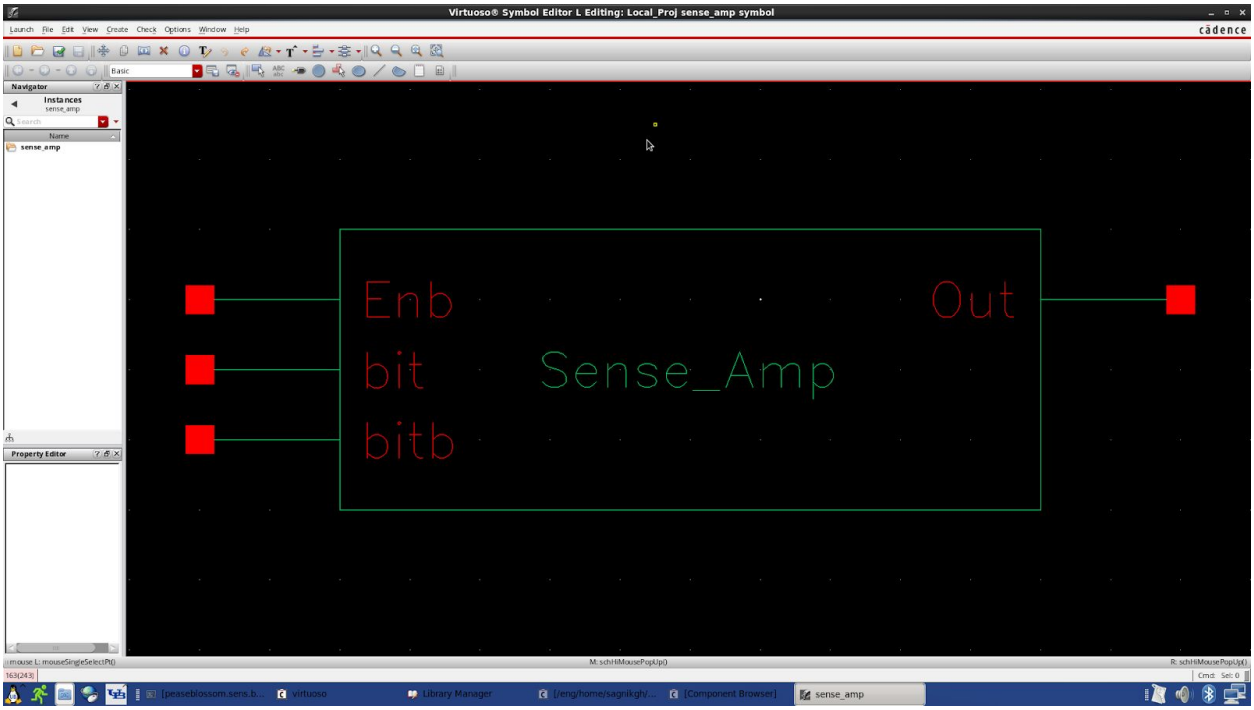


LVS Match

- ## SENSE AMPLIFIER



Schematic Diagram



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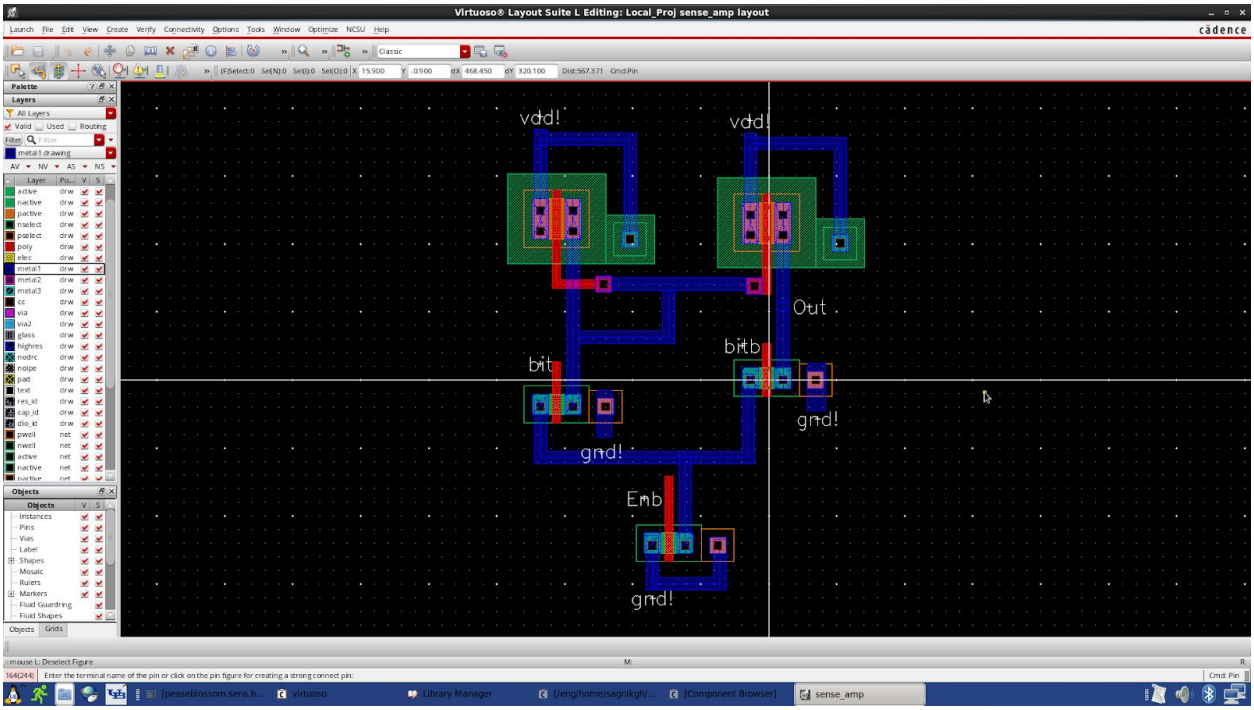
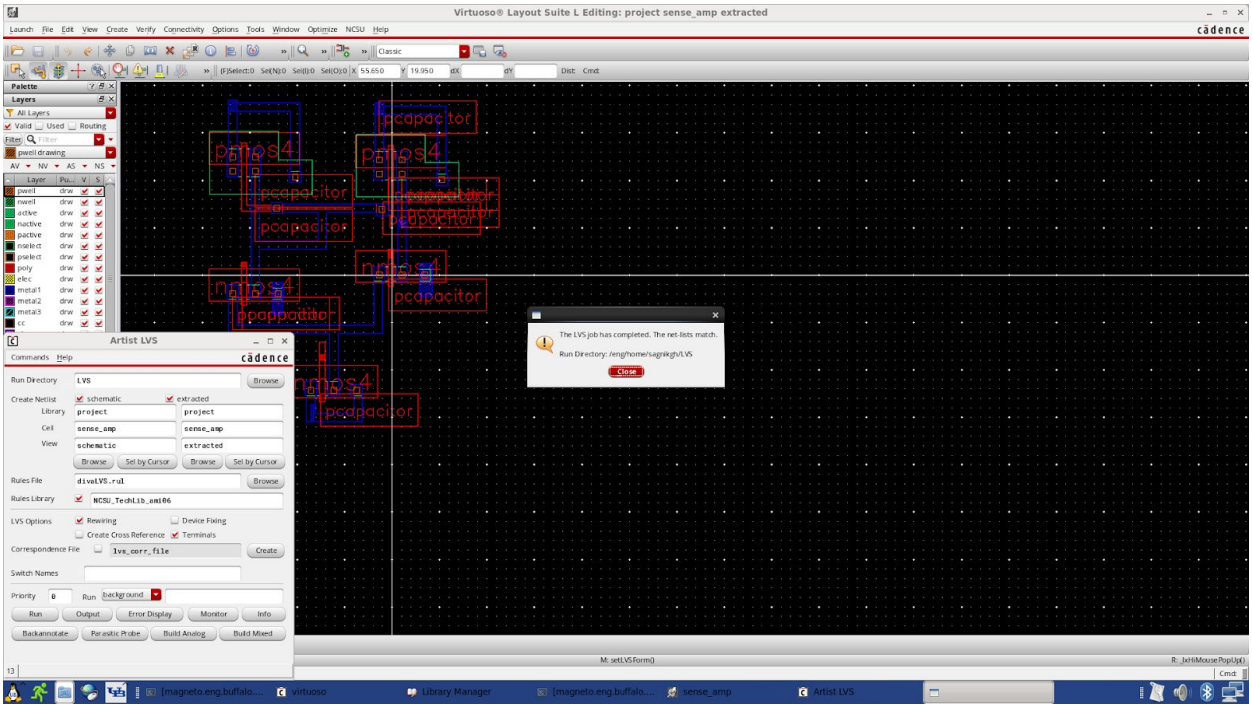
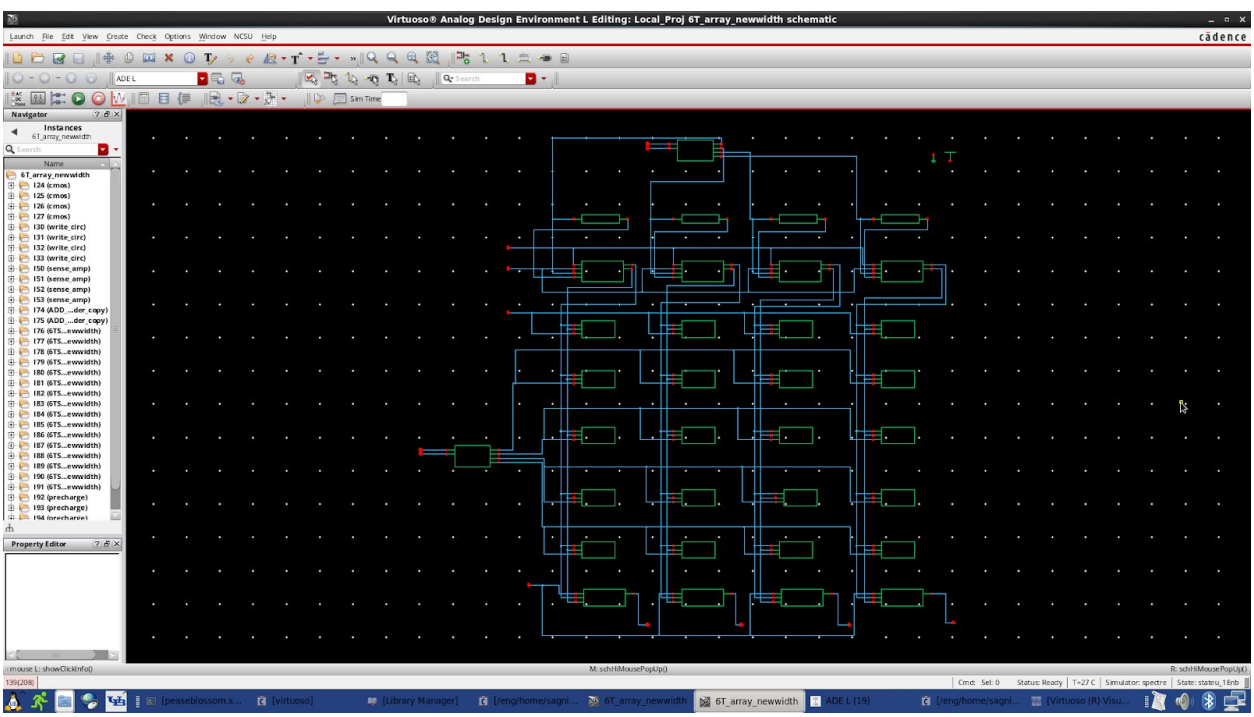


Layout View

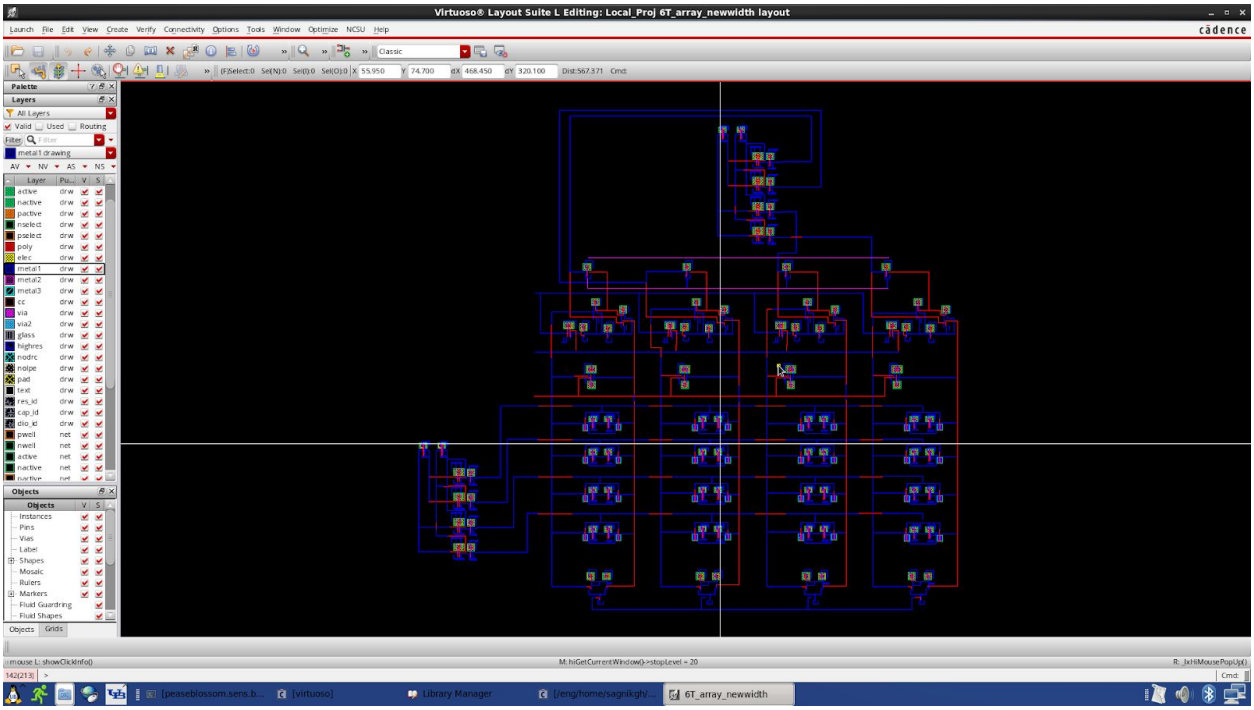


Extracted View

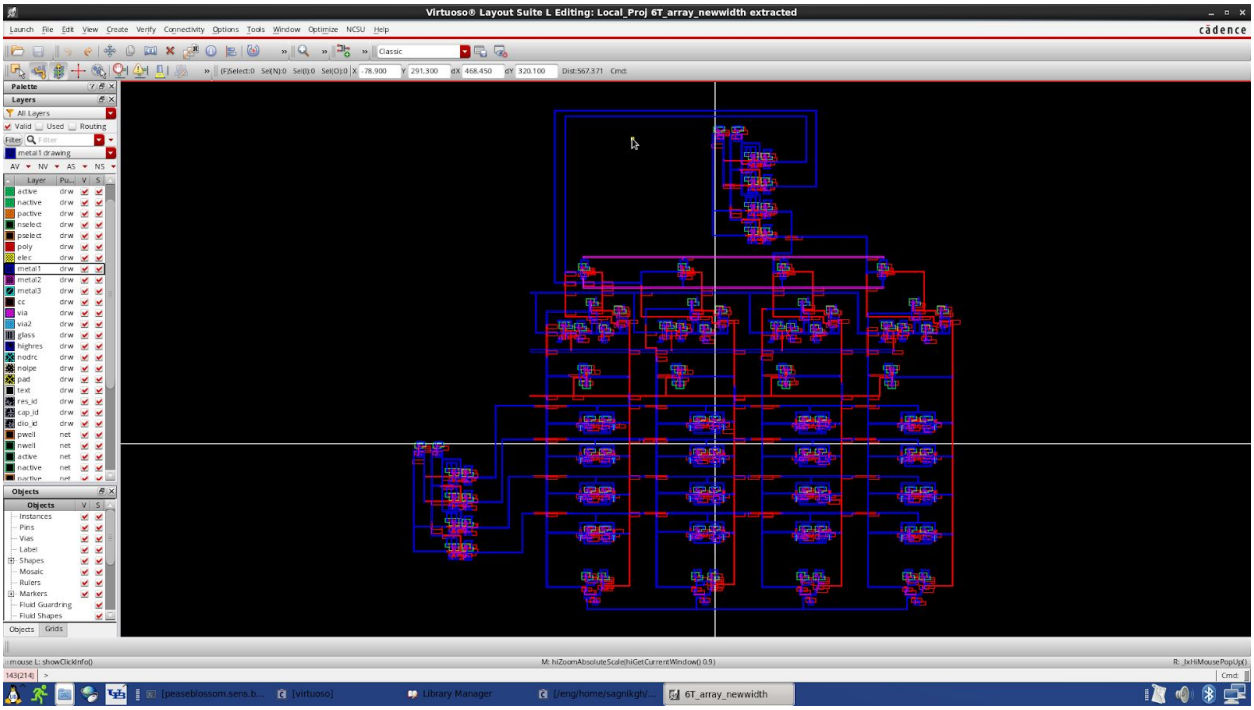
- ## 4X4 MEMORY ARRAY USING 6T SRAM CELL



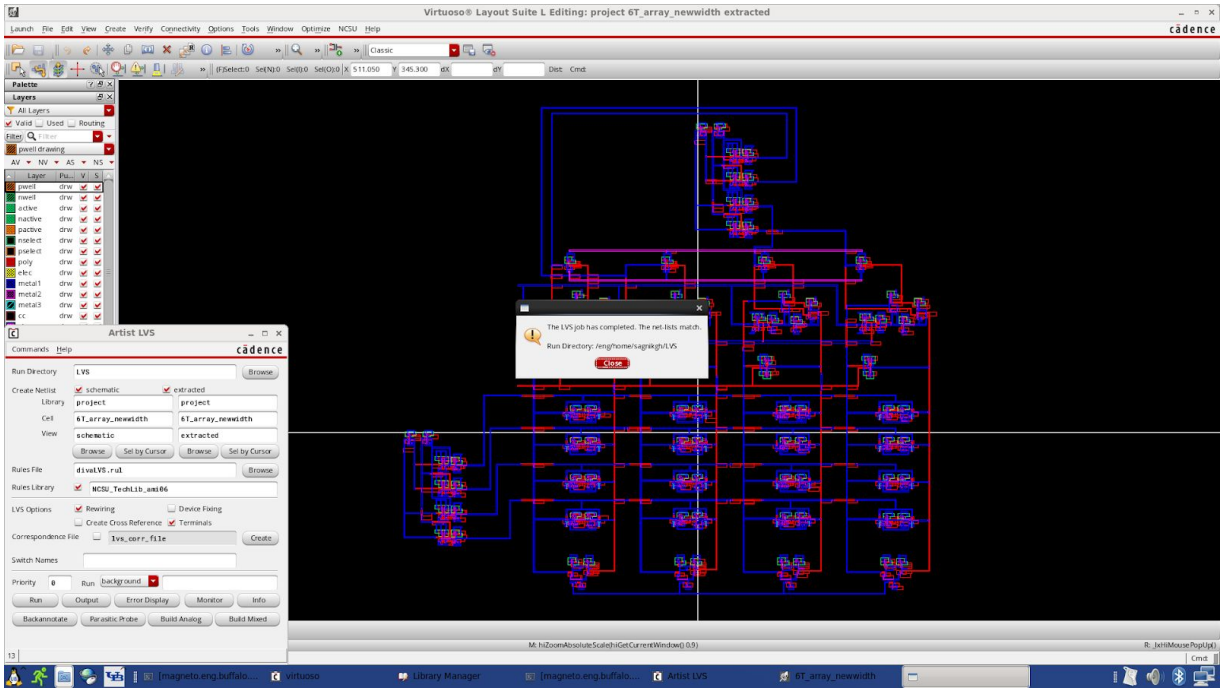
Schematic Diagram



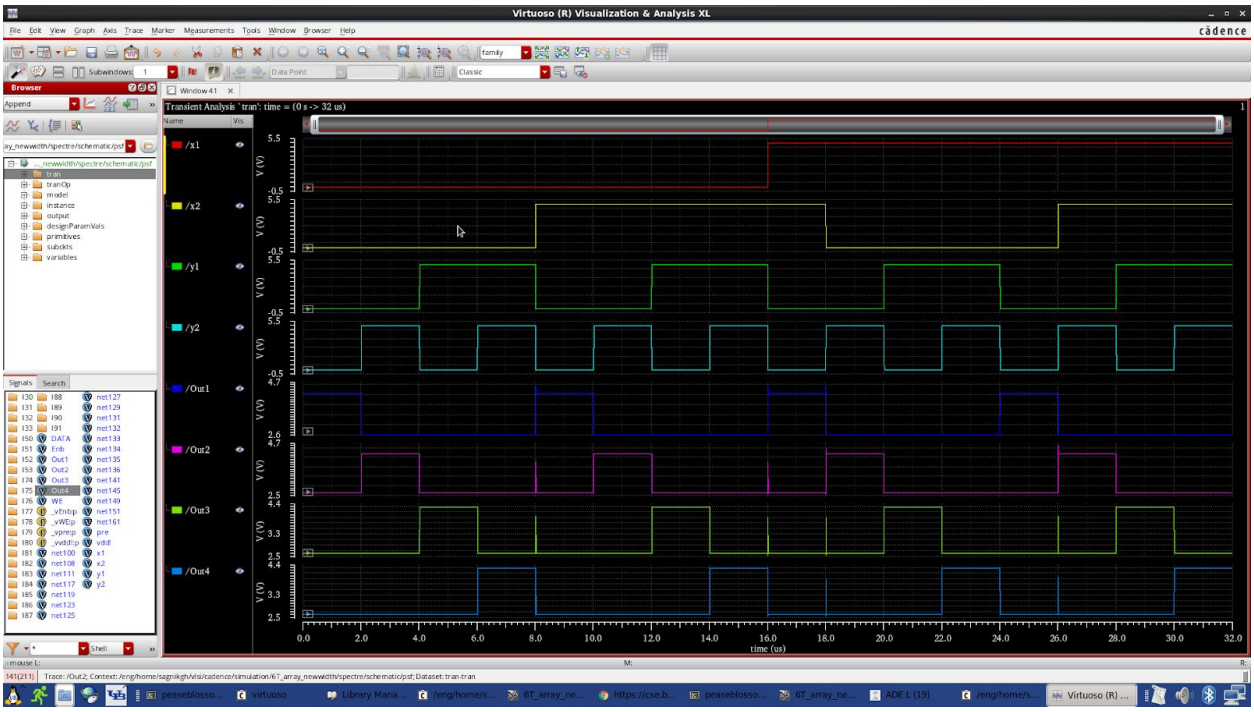
Layout View



Extracted View

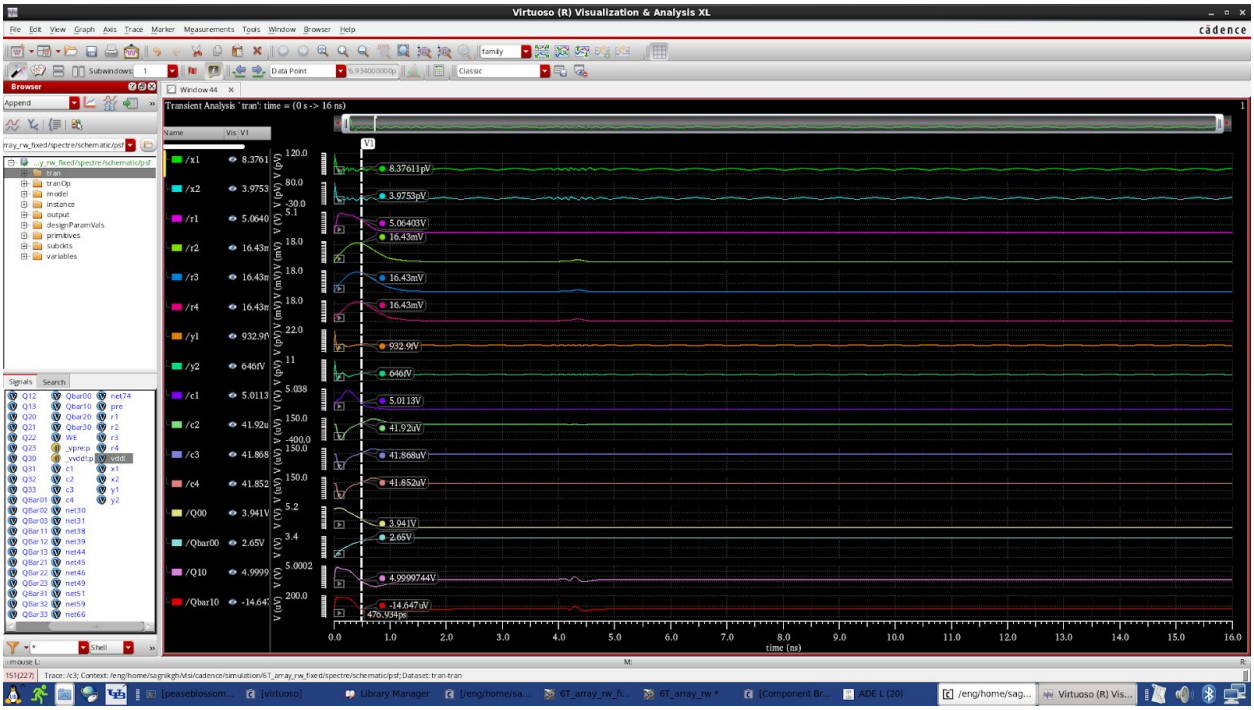


LVS Match

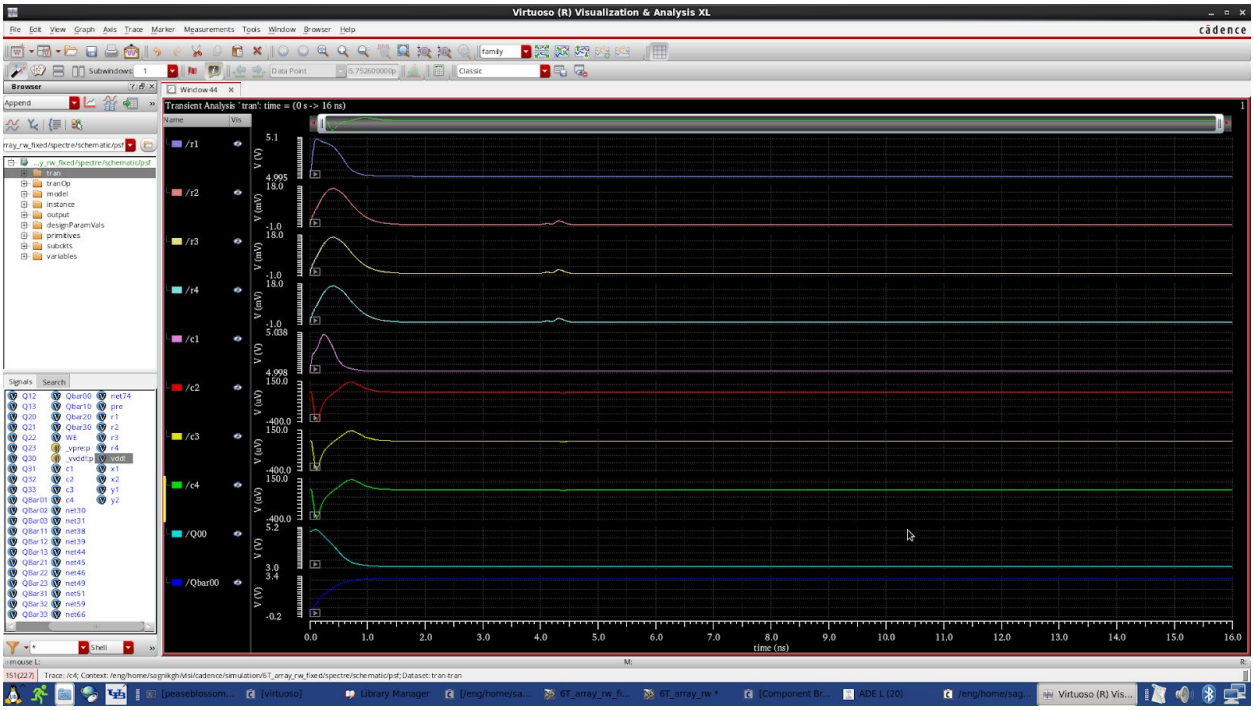


Simulation

The above simulation explains the working of the SRAM array and the address decoders. When both x1 x2 are low first row and first column is selected and so on. When x1= 0 and x2 = 1, second column is selected and so on. Similarly when y1 = y2 = 0 first column is selected and so on.



Simulation (Write Circuit)



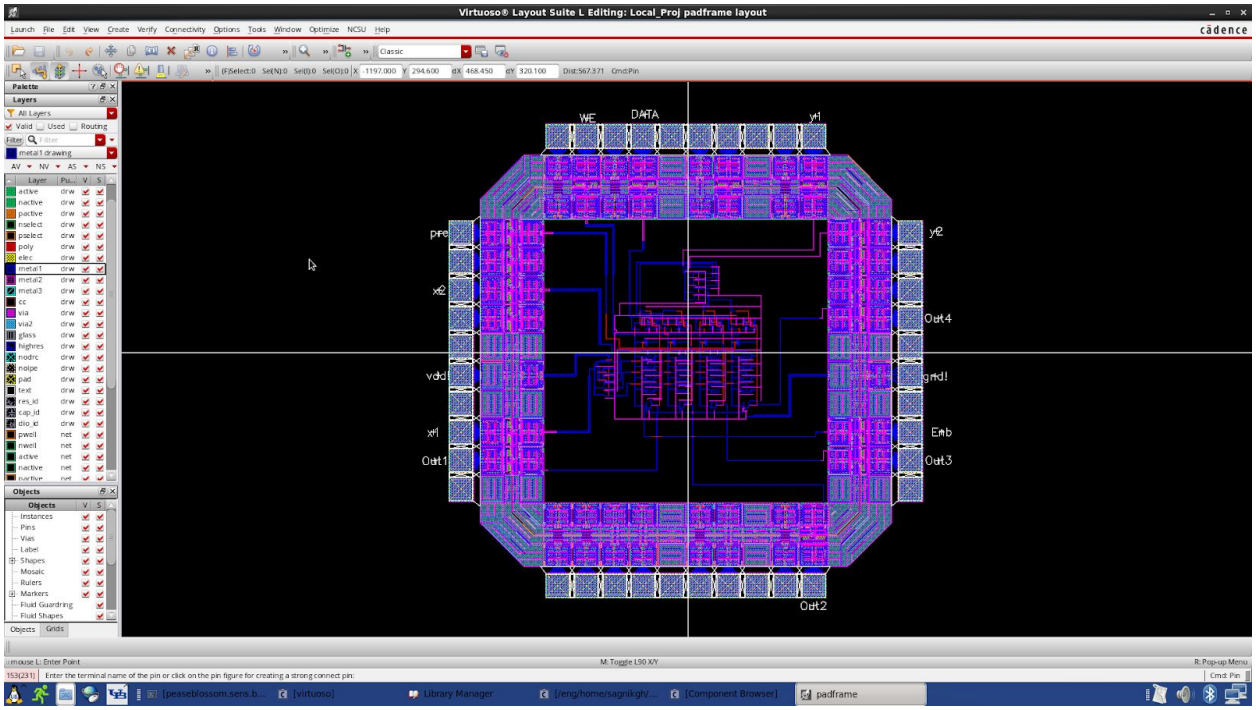
Simulation (Write Operation - Cell Row 1 Column 1)

Above simulation explains the write operation of the SRAM array, when all inputs of the address decoders are low (x1=x2=y1=y2=0) then the top left cell is activated and as it is visible, write operation is happening in that particular cell only .

Simulation (Write Operation - Cell 00 Vs. Cell 10)

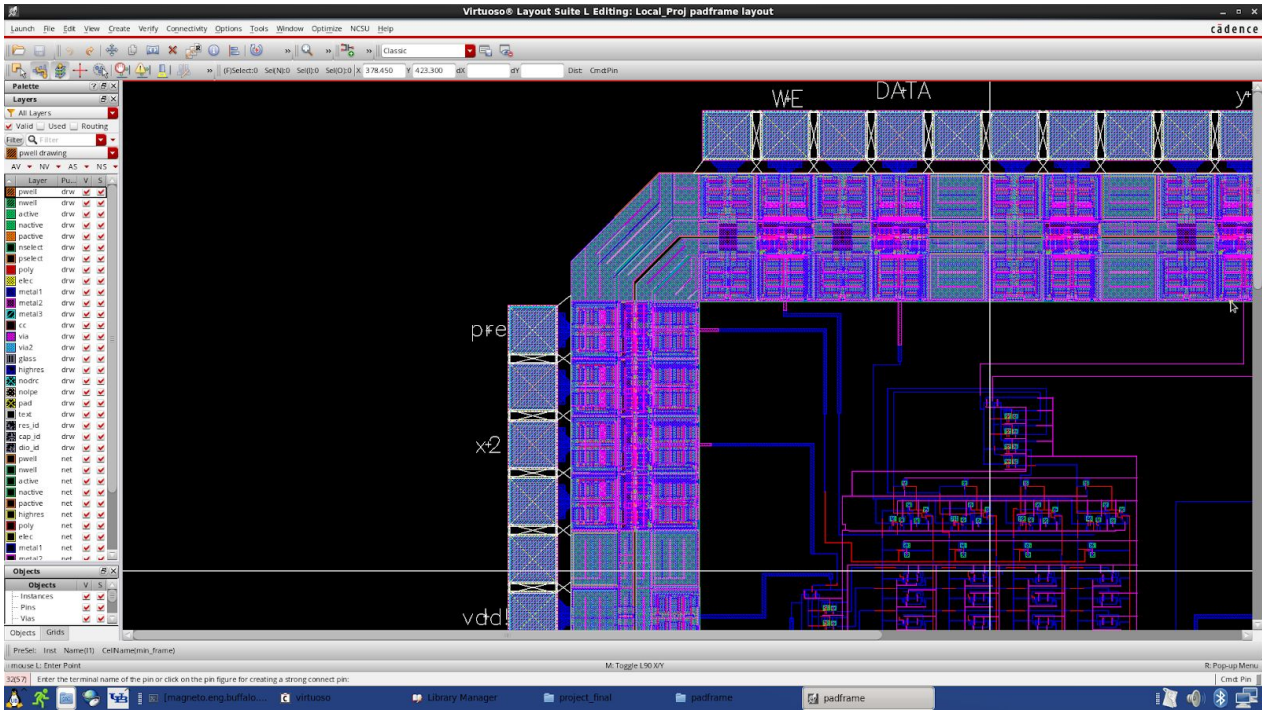
This is the comparison of two cells of the same column. This diagrams describes that while writing to a particular cell, other cells are unaffected.

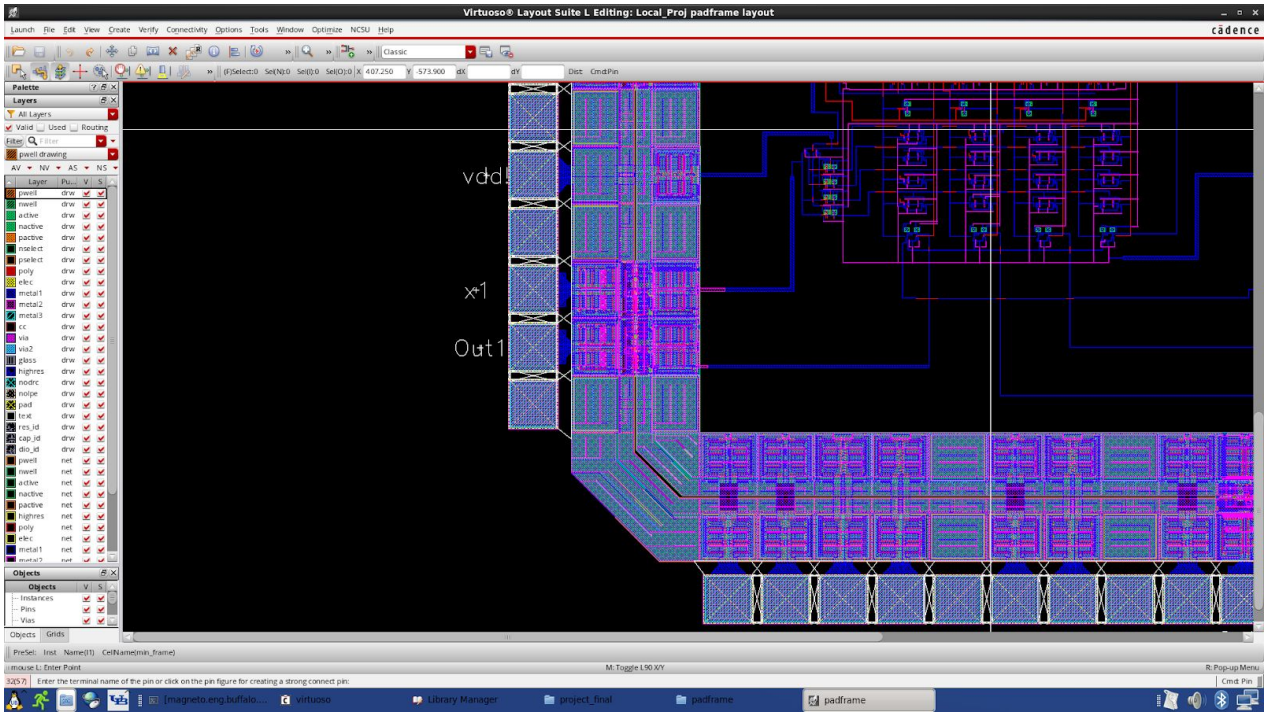
- ## 4X4 MEMORY ARRAY FITTED IN PADFRAME

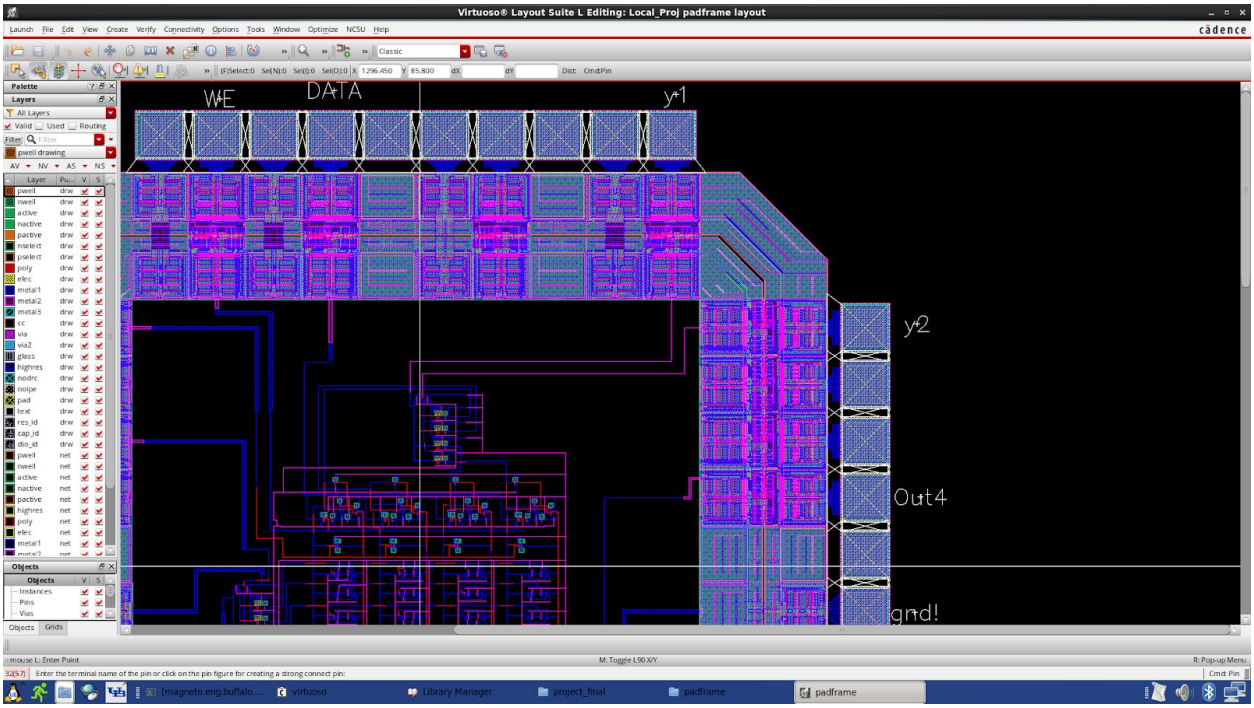


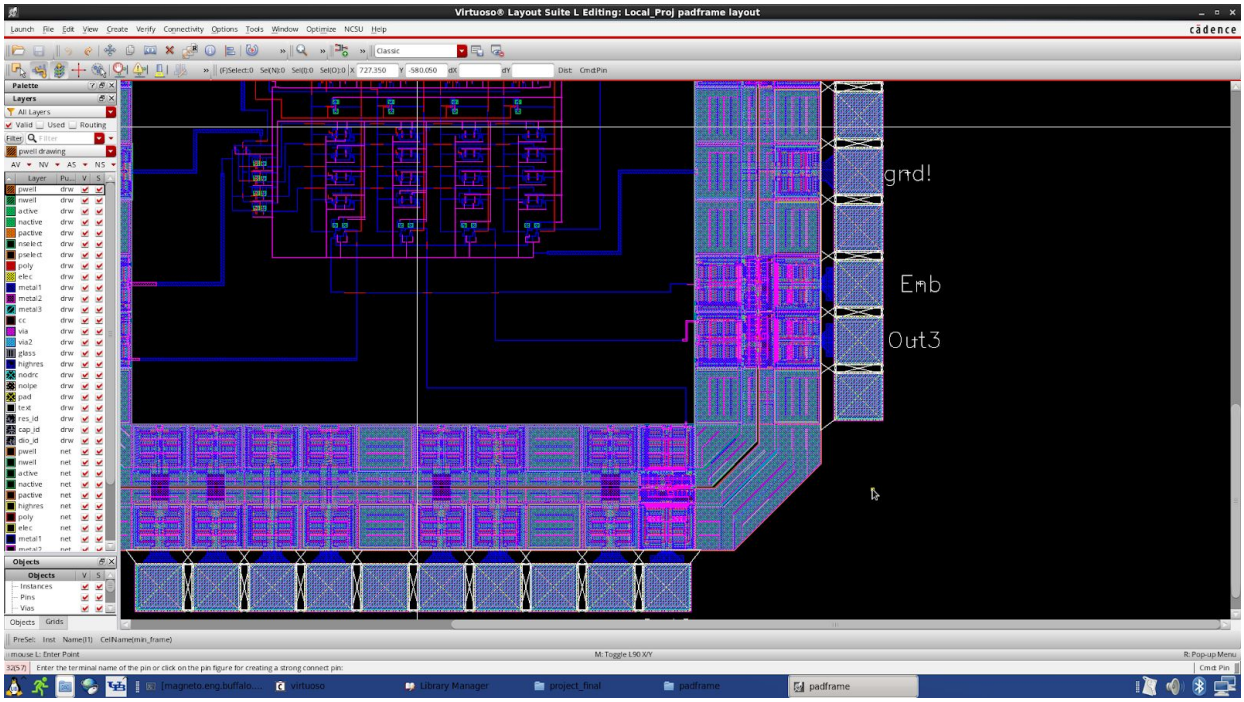
Layout View

- **PIN PLACEMENT:**






Virtuoso® Layout Suite L Editing: Local_Proj padframe layout
WE
DATA
y1
y2
Out4
gnd!


Virtuoso® Layout Suite L Editing: Local_Proj padframe layout
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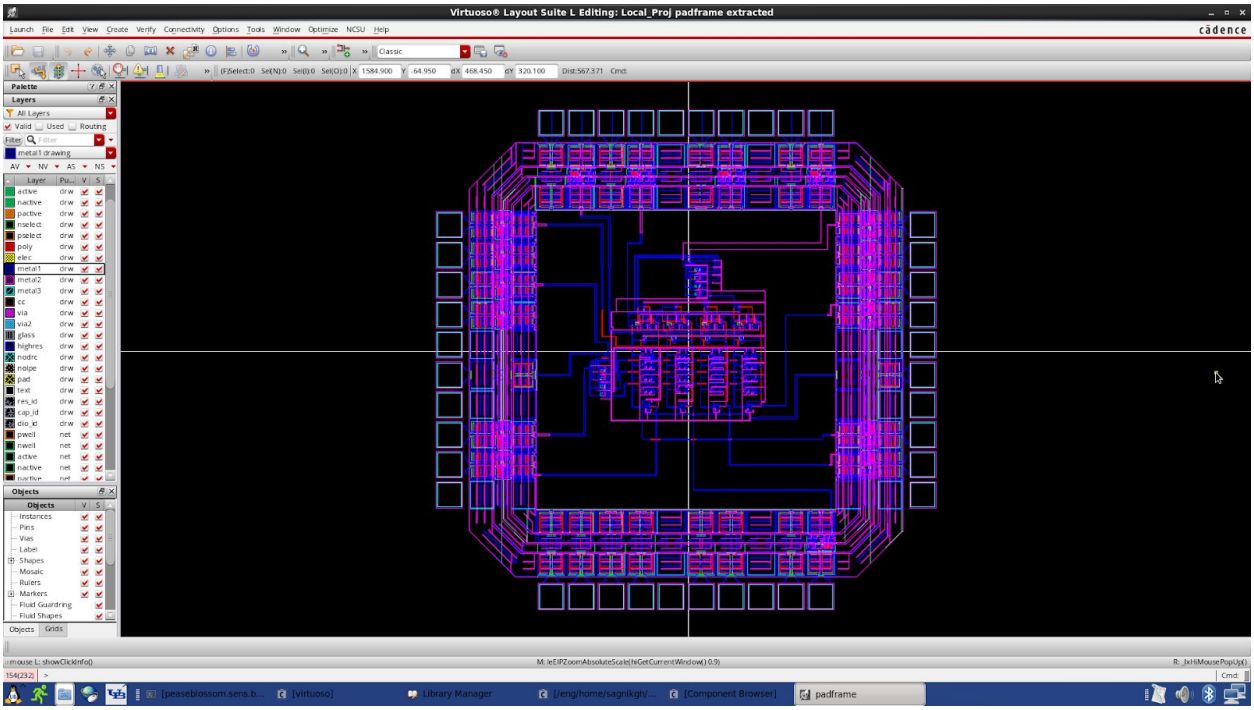
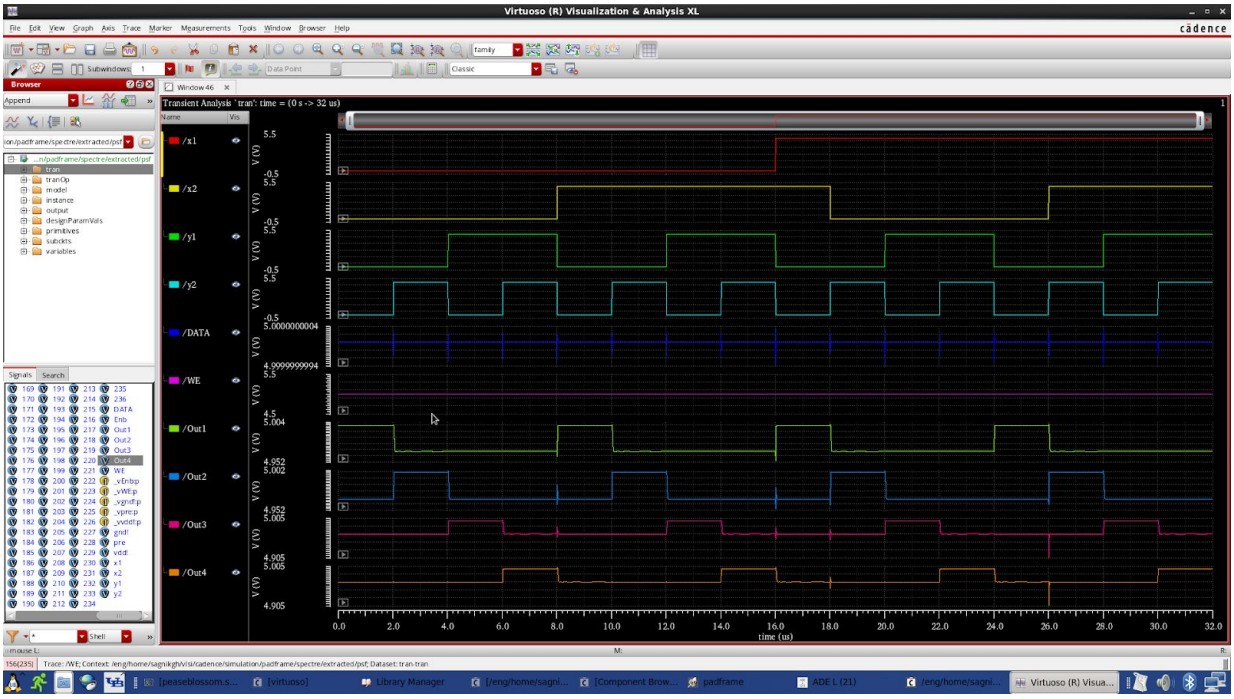


Extracted View

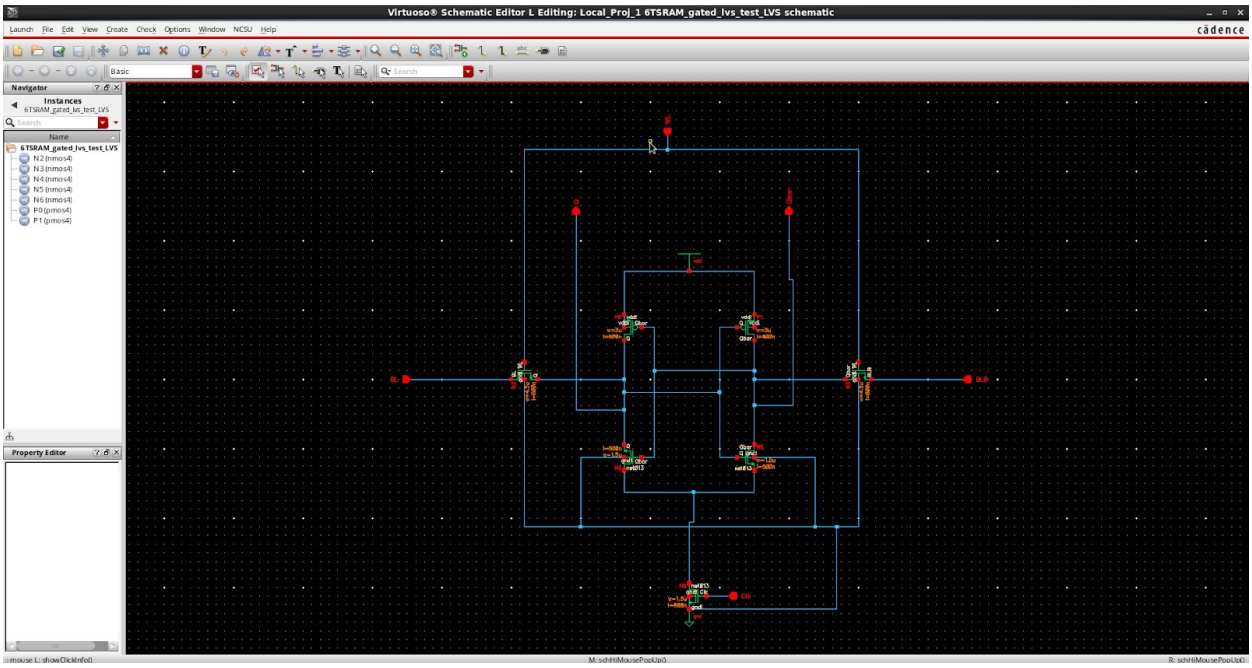


Simulation

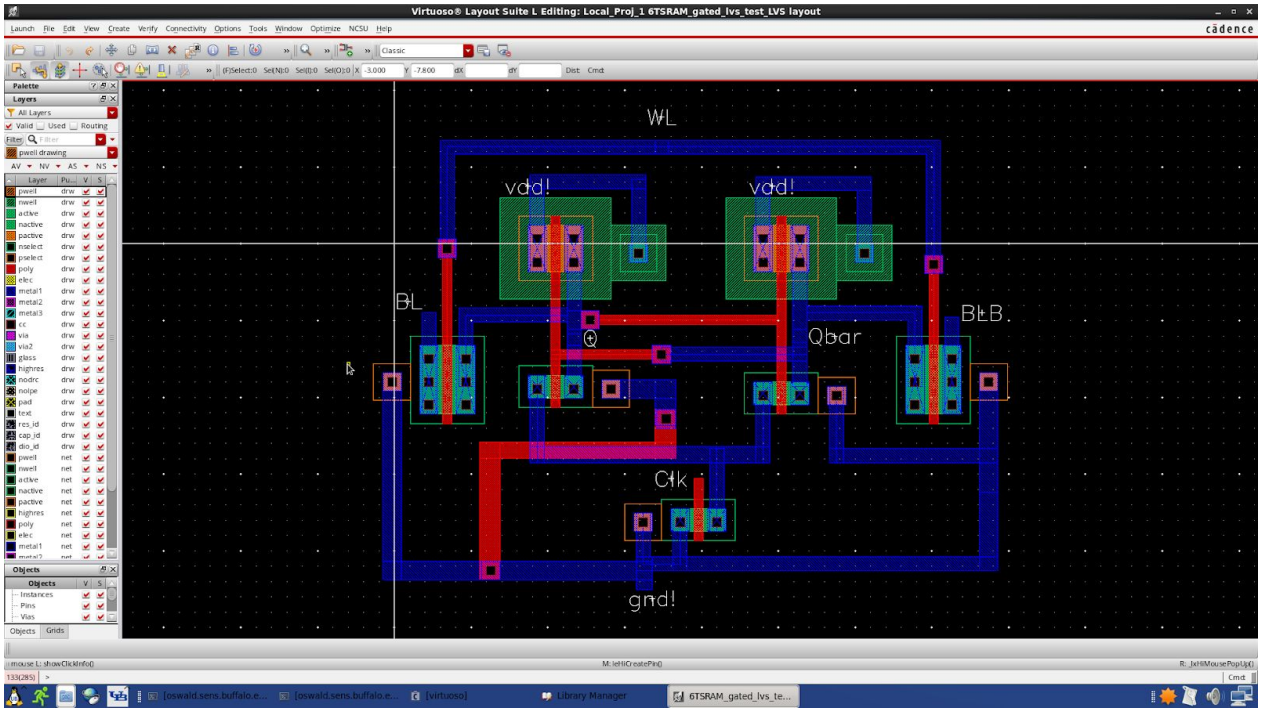
Above is the simulation of the 6T SRAM array circuit fitted in the pad frame, as it is visible, the waveform is similar to the simulation waveform of the circuit without the padframe.When both x1 x2 are low first row and first column is selected and so on. When x1= 0 and x2 = 1, second column is selected and so on. Similarly when y1 = y2 = 0 first column is selected and so on.

MODIFIED SRAM CELLS (PROJECT EXTENSION)

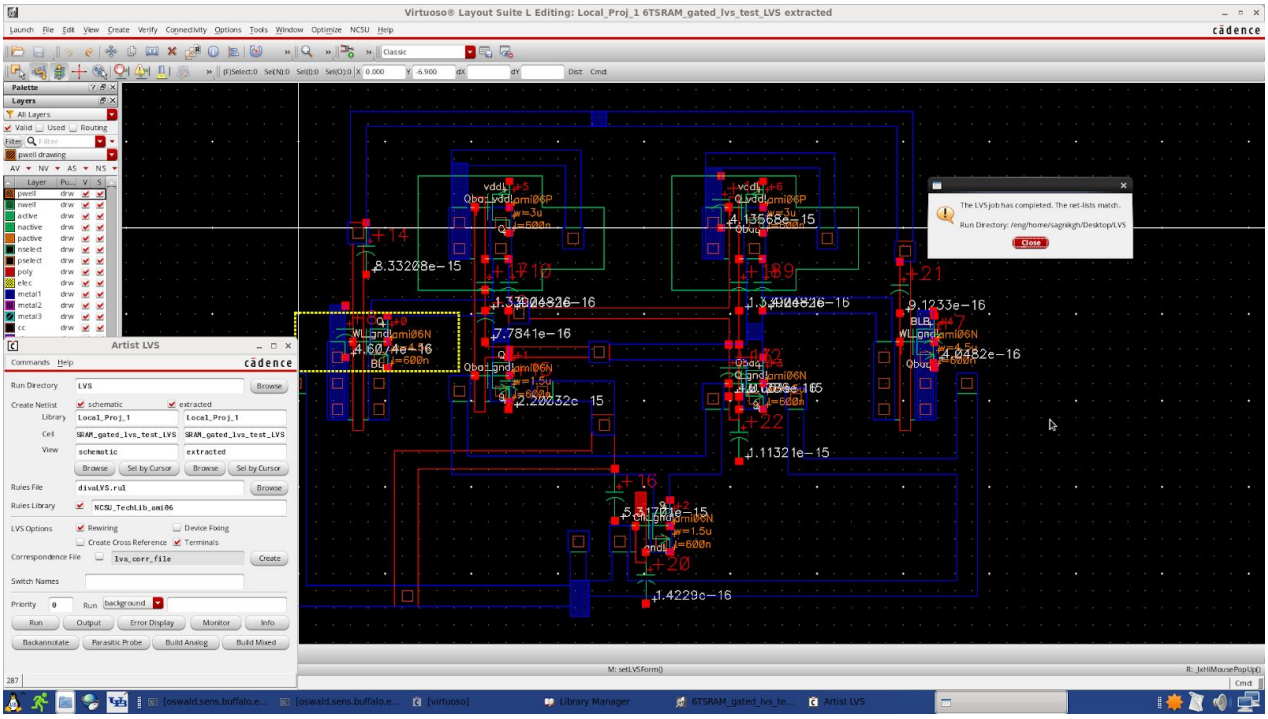
- **GATED VDD SRAM CELL**



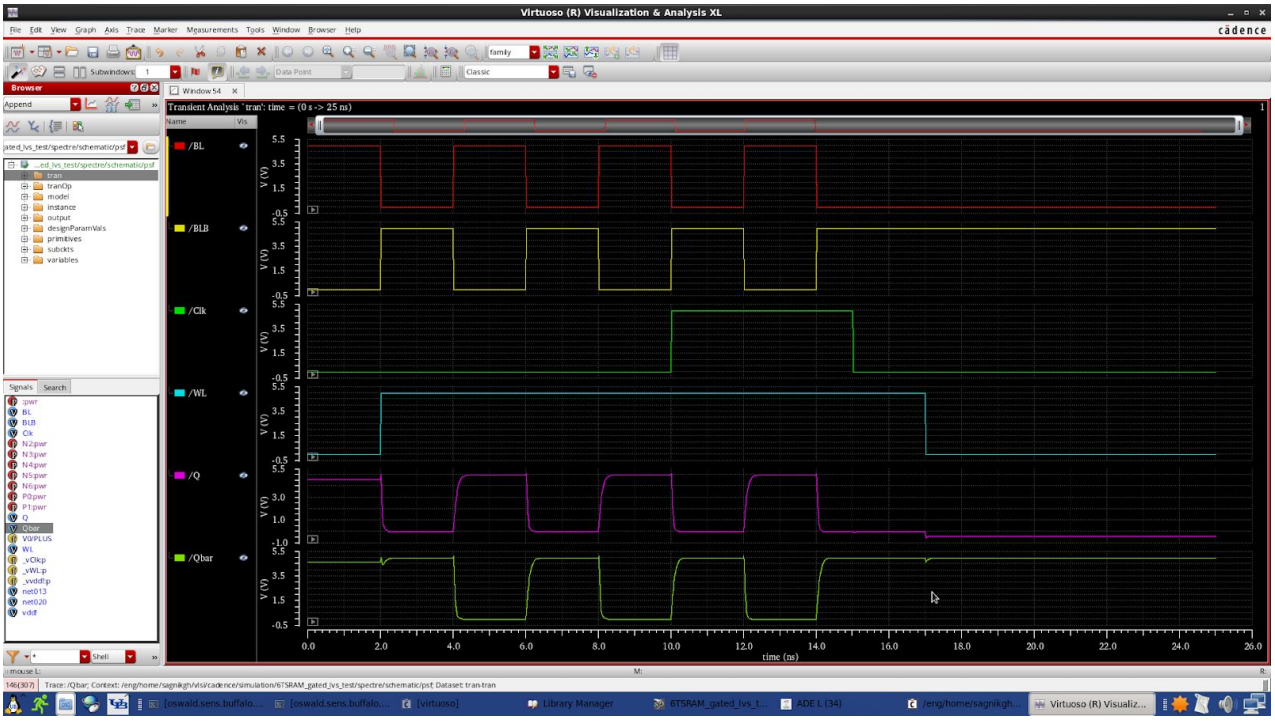
Simulation



Layout

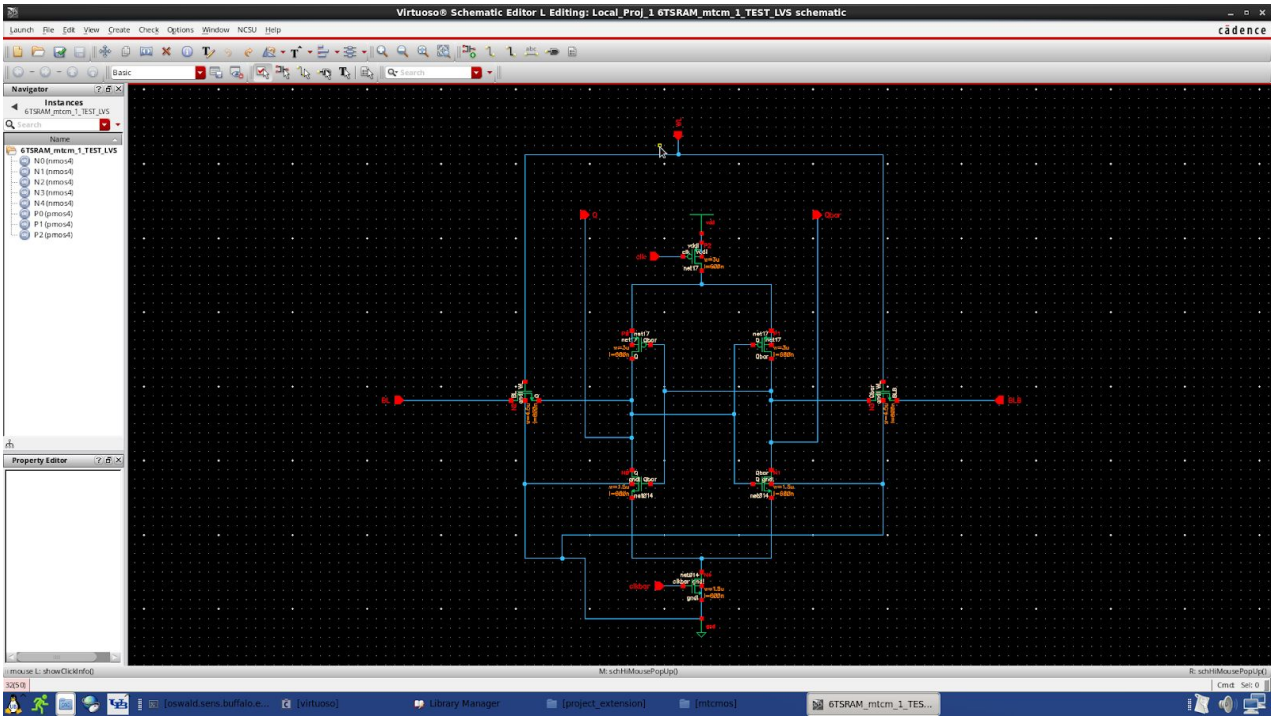


Extracted

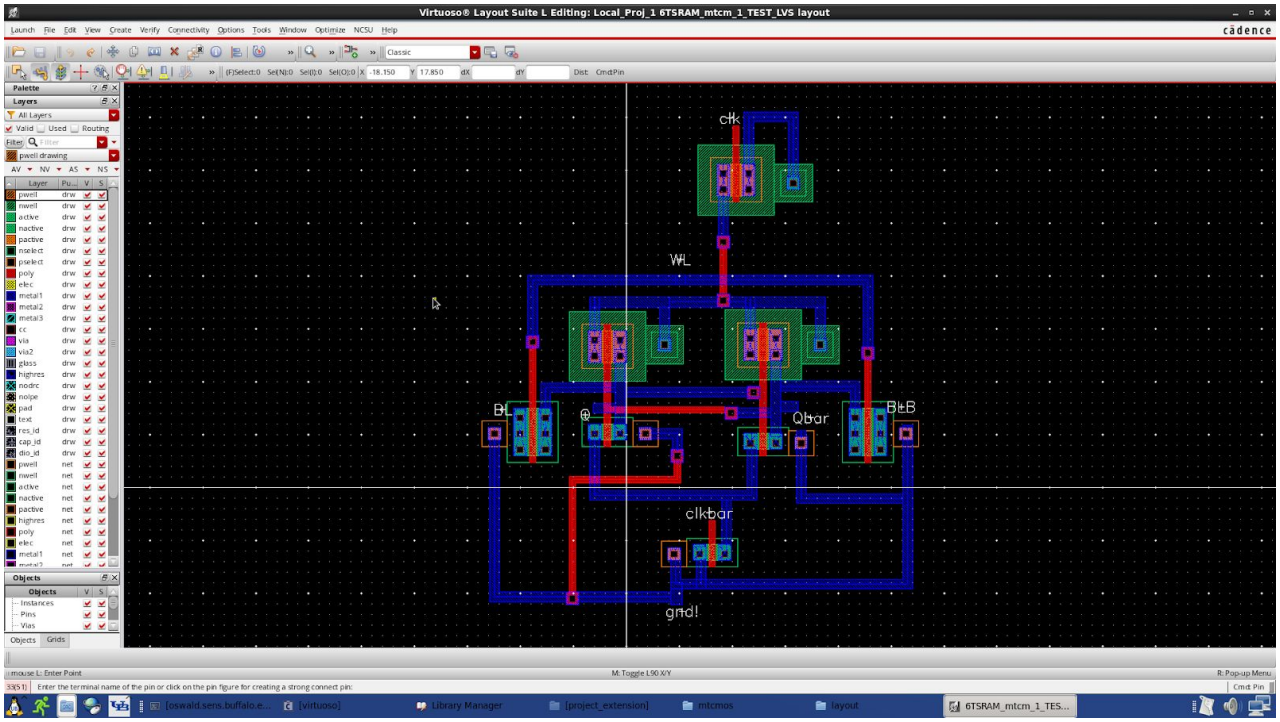


Simulation (Read and Write Operation)

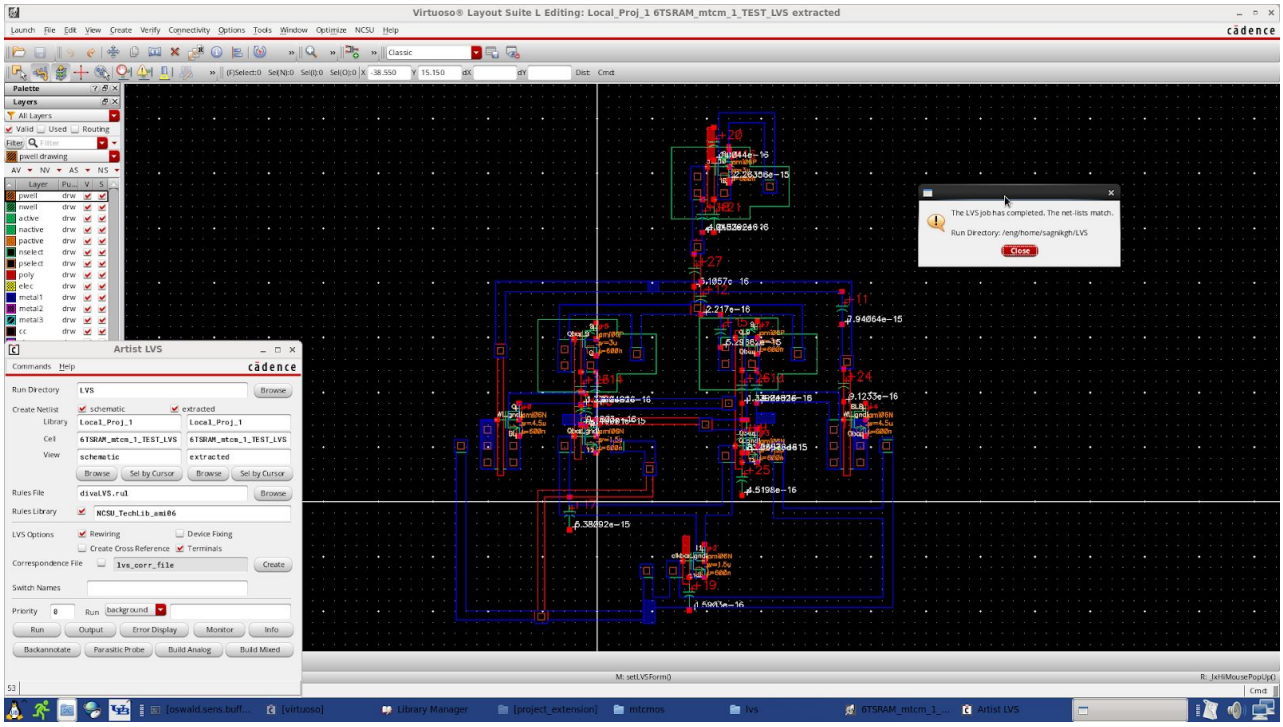
- **MTCMOS**



Schematic



Layout

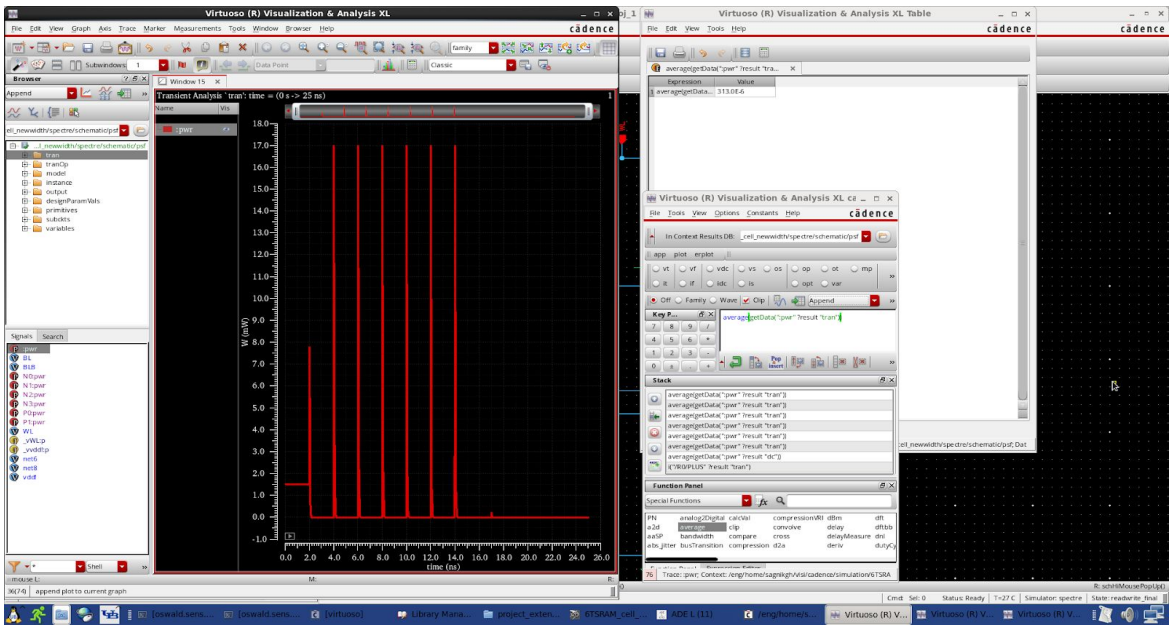


Extracted

Simulation (Read and Write Operation)

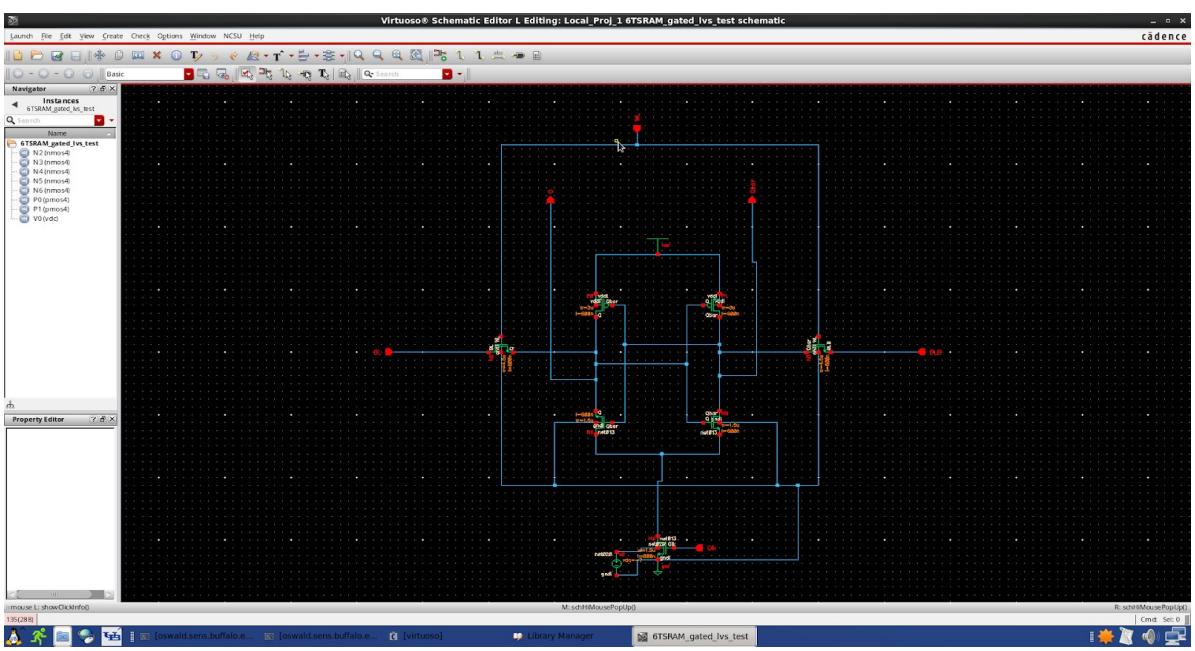
POWER ANALYSIS

- **6T CELL**

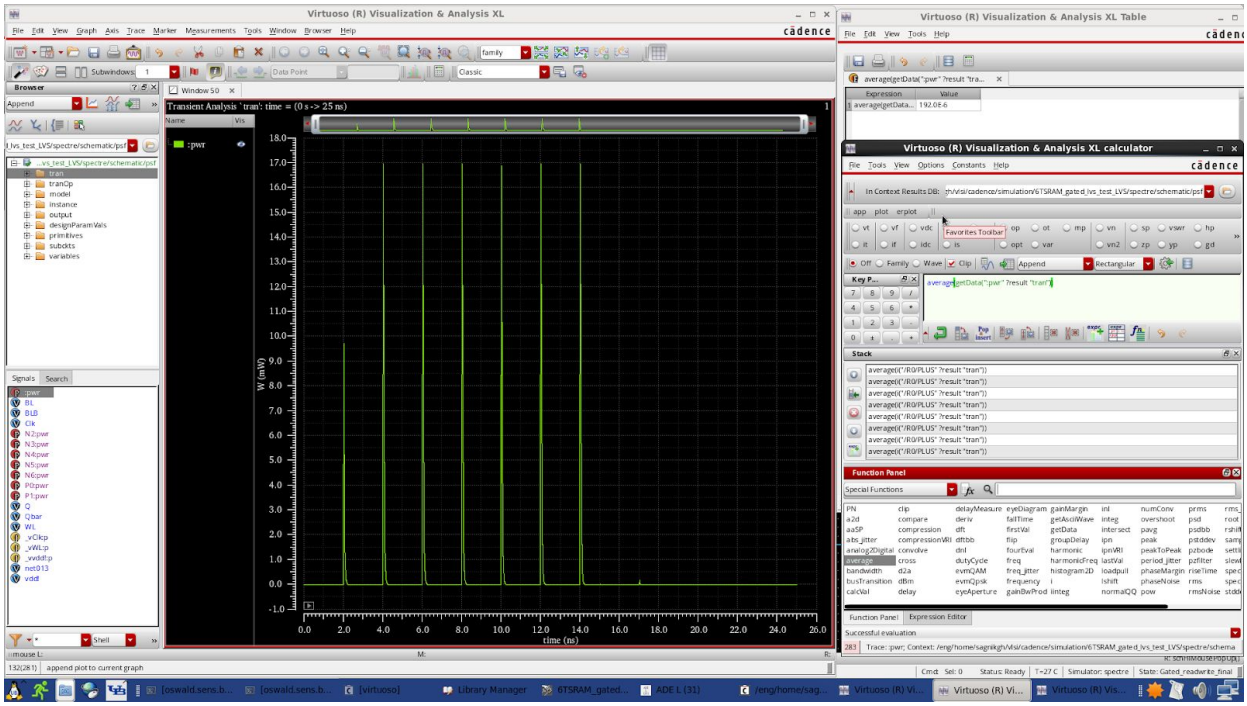


Result for power analysis

- **GATED VDD SRAM CELL**

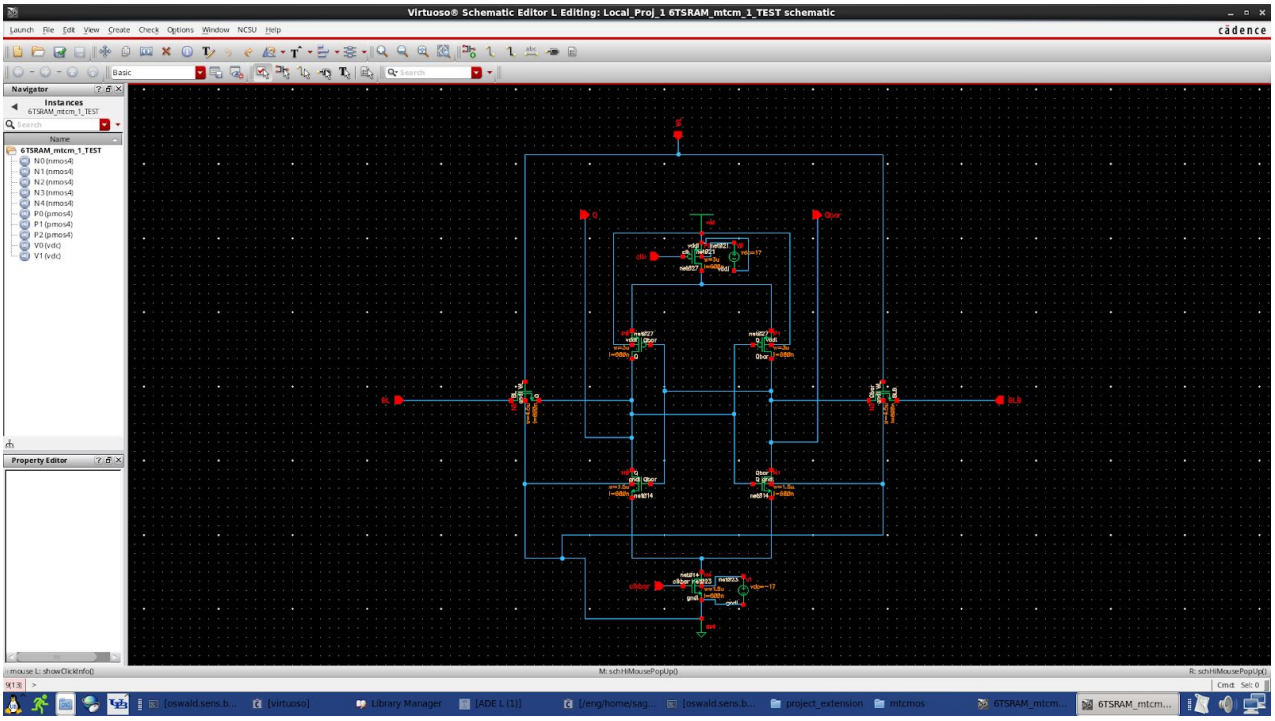


Schematic Diagram used for Power analysis

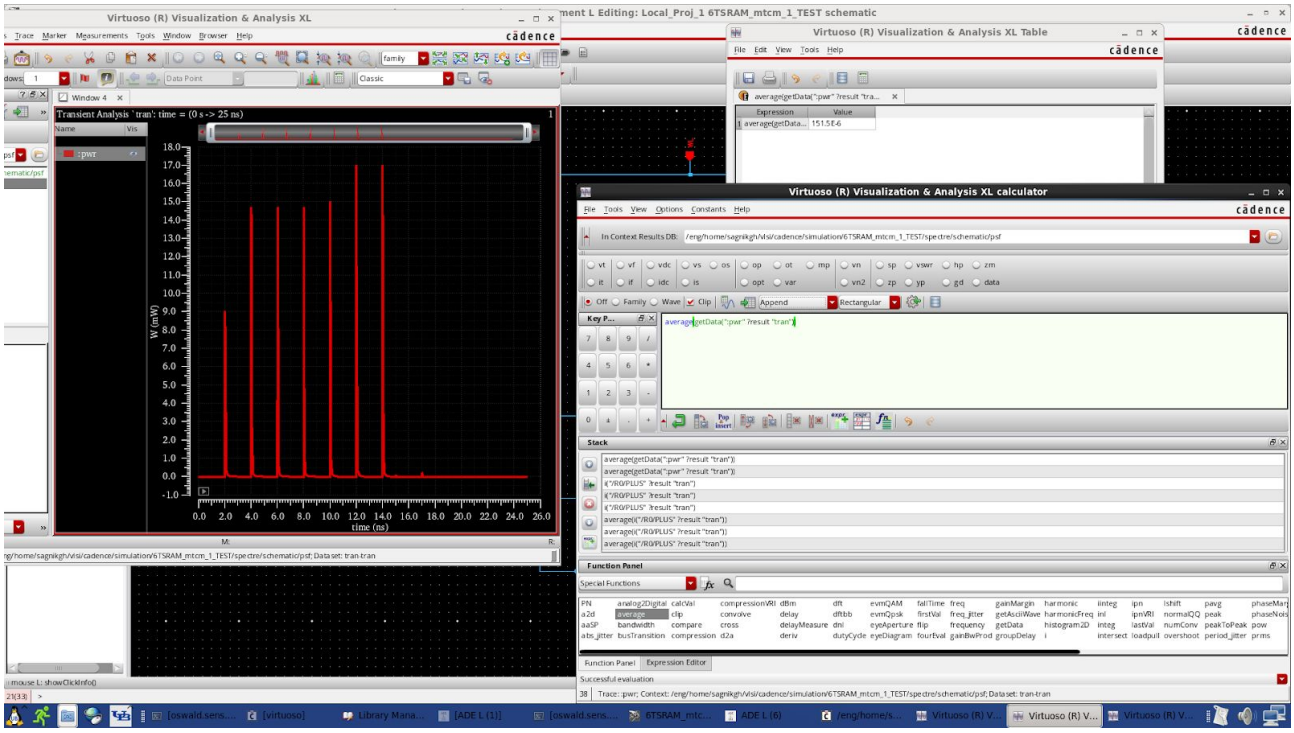


Power analysis results

- **MT-COMS**



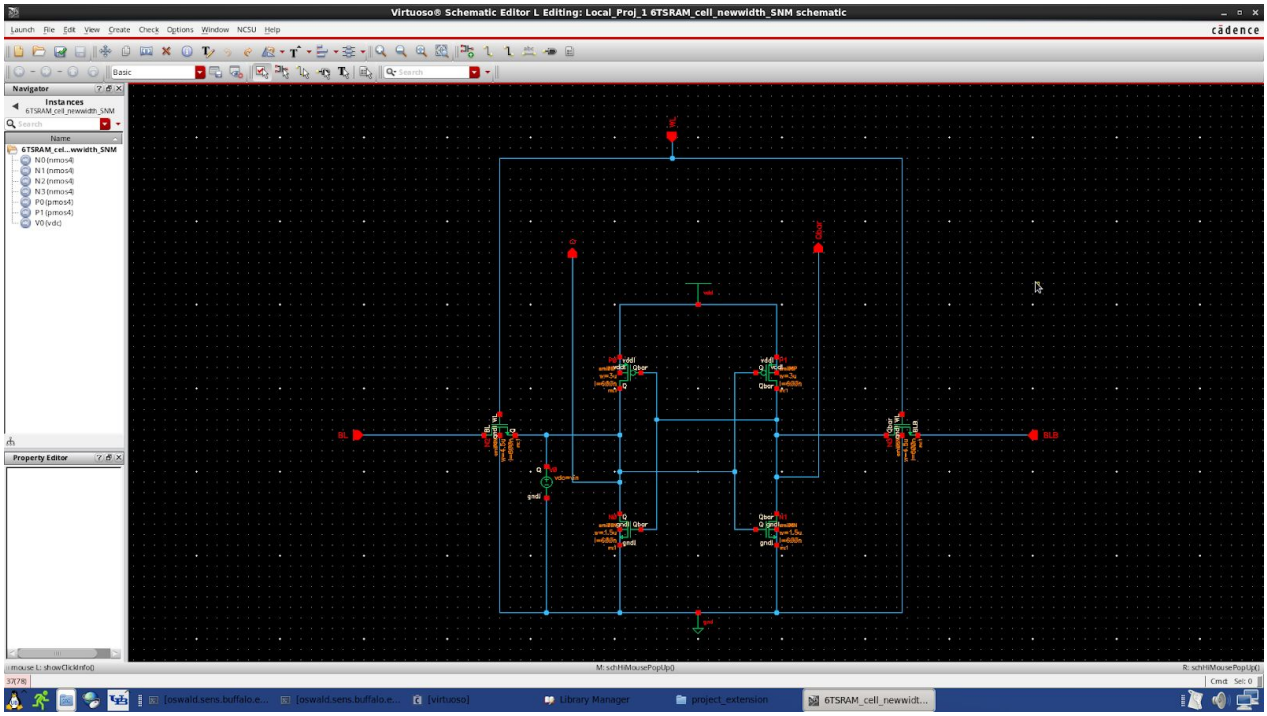
Schematic Diagram used for Power analysis



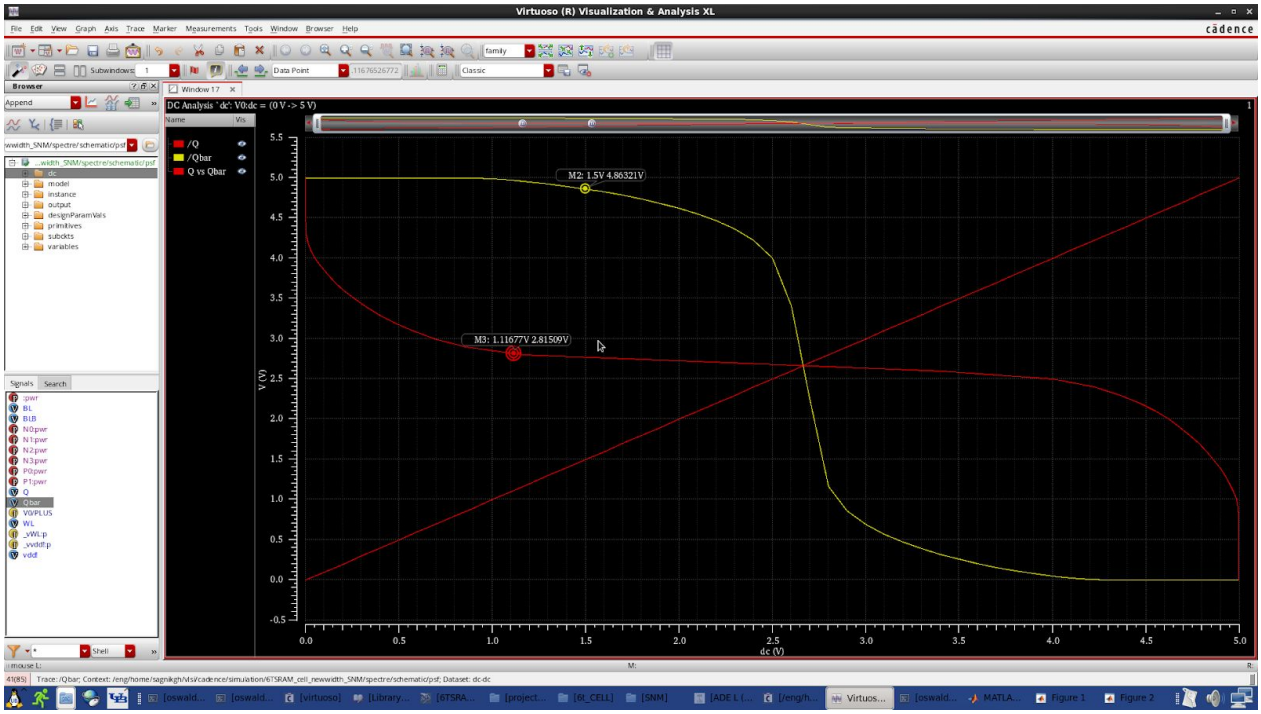
Power analysis results

STATIC NOISE MARGIN ANALYSIS

- 6T CELL

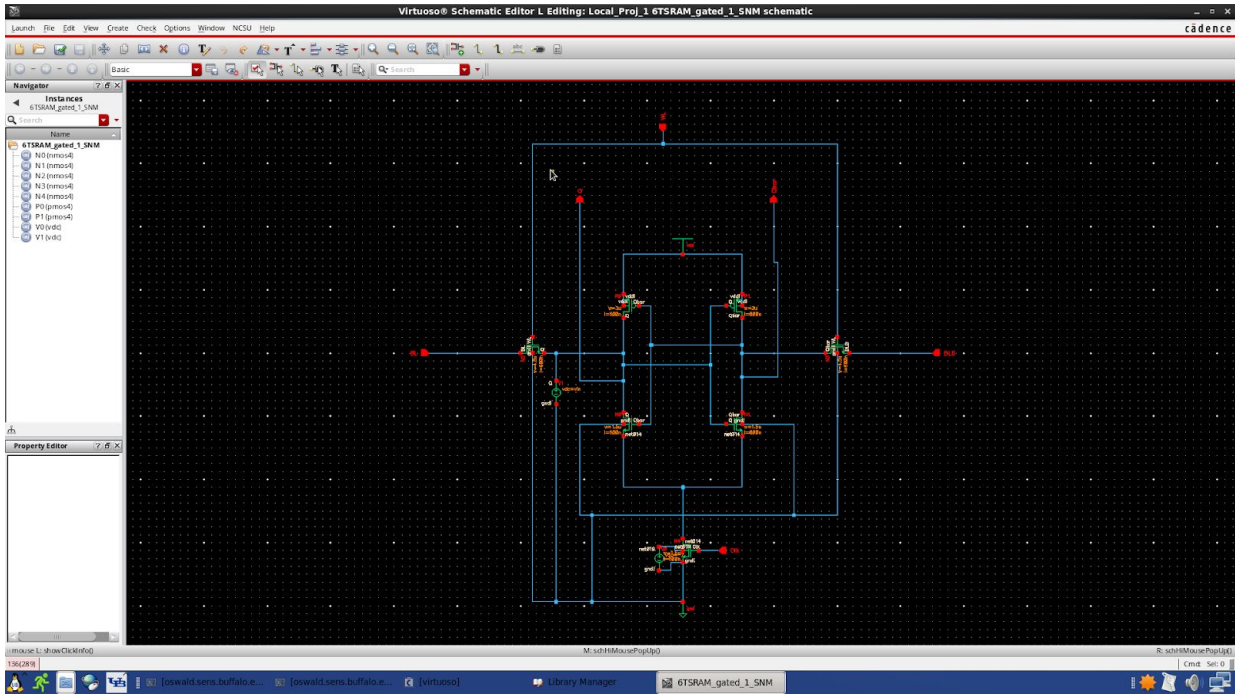


Schematic Diagram used for SNM analysis

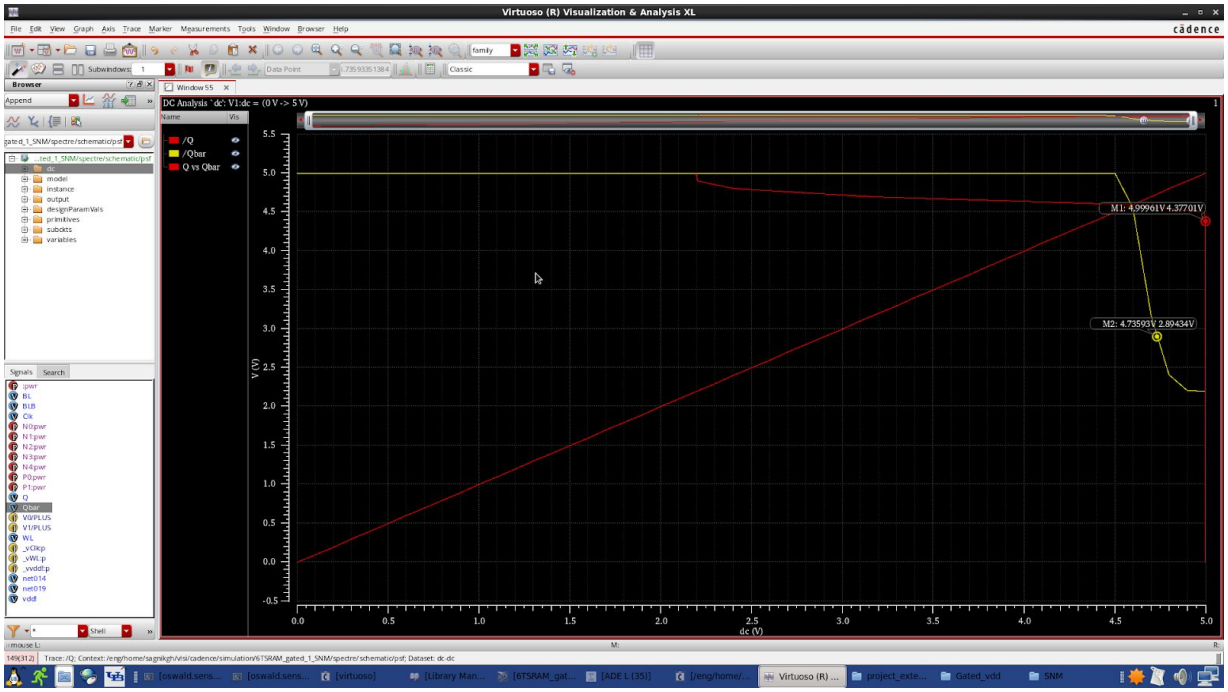


SNM analysis

- ## GATED VDD SRAM CELL

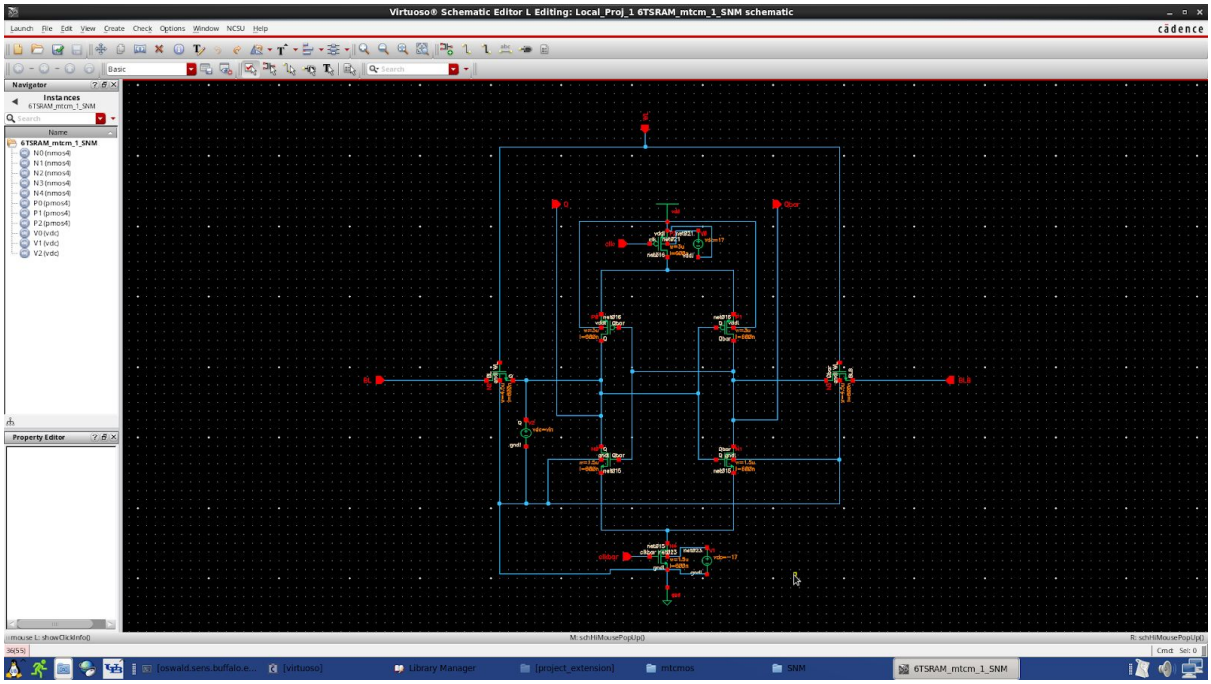


Schematic Diagram used for SNM analysis



SNM analysis

- **MTCMOS**

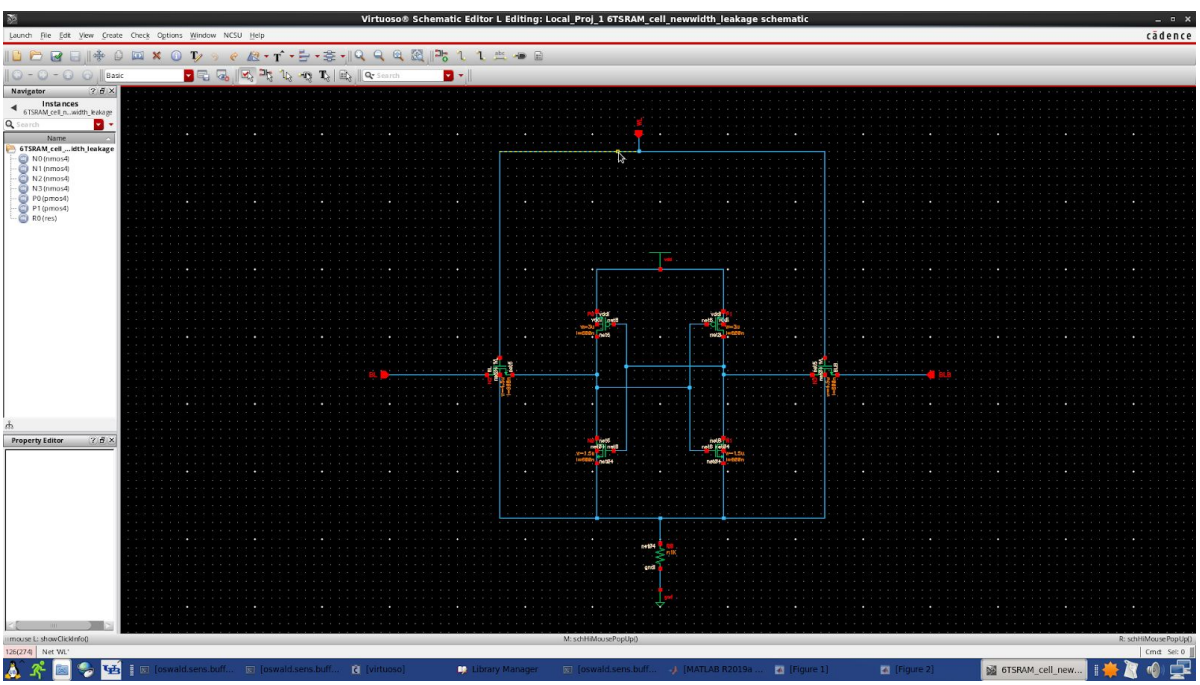


Schematic Diagram used for SNM analysis

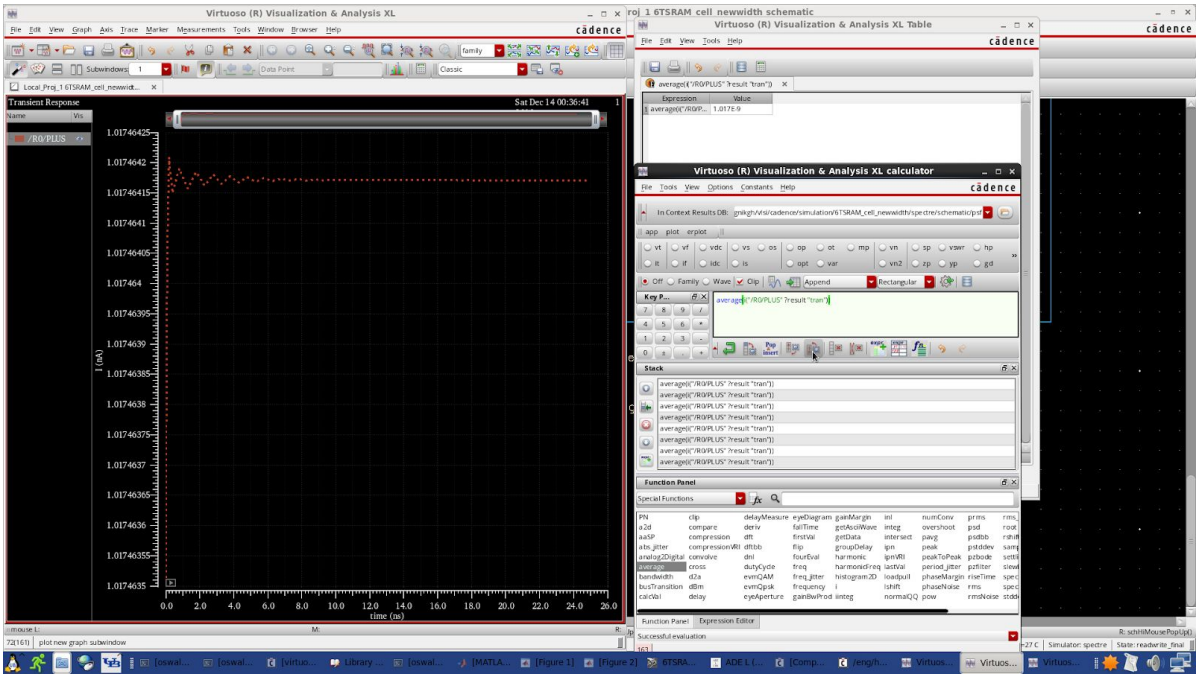
SNM analysis

LEAKAGE CURRENT ANALYSIS

- **6T CELL**

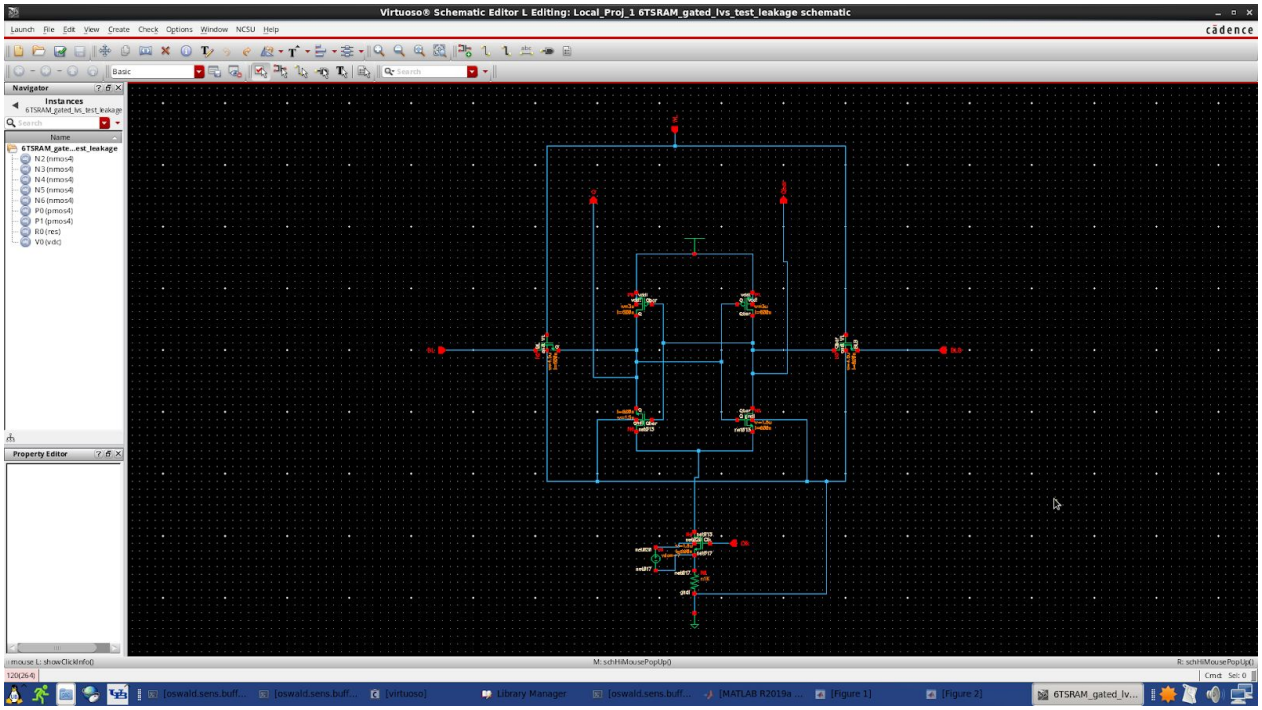


Schematic Diagram used for Leakage power analysis

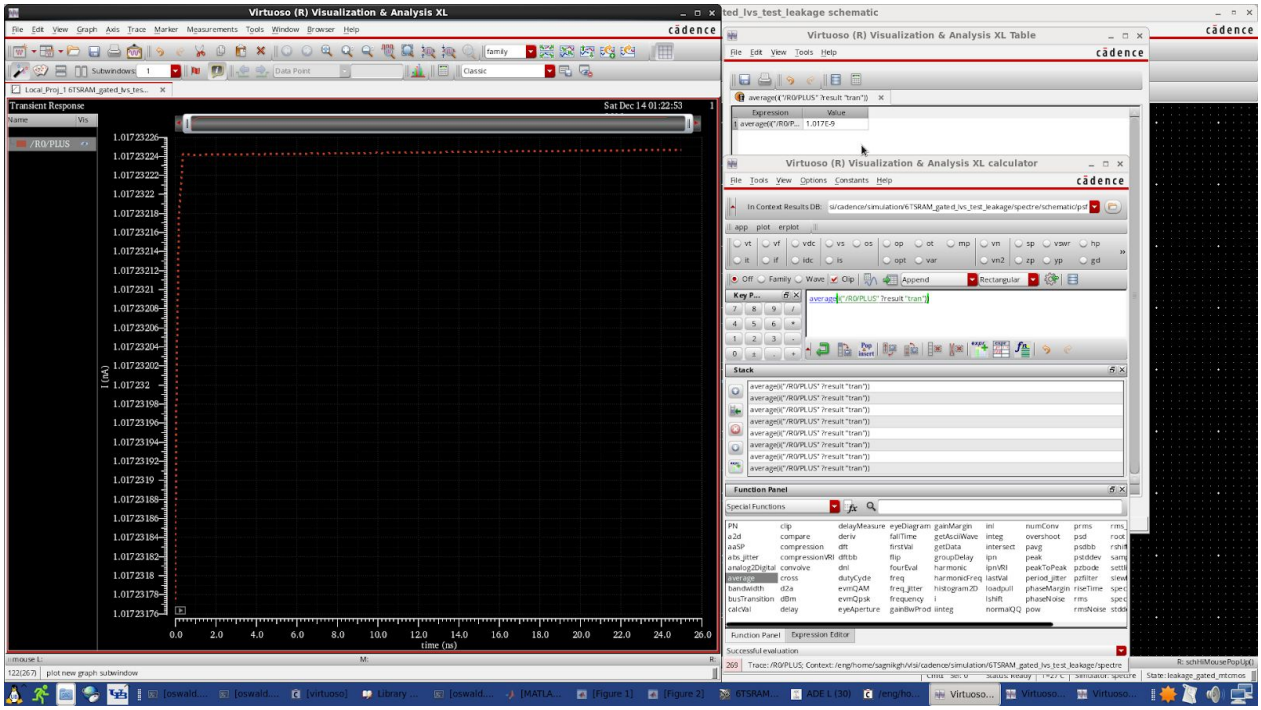


Leakage current analysis results

- ## GATED VDD SRAM CELL

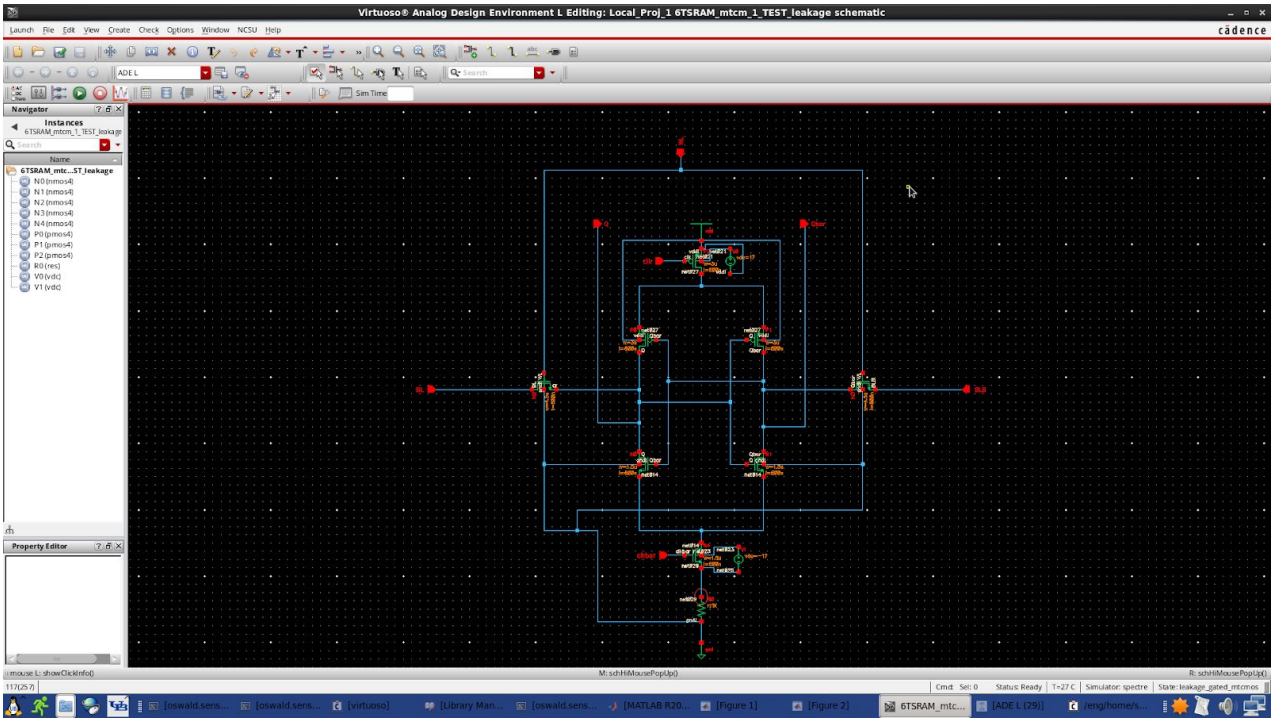


Schematic Diagram used for Leakage power analysis

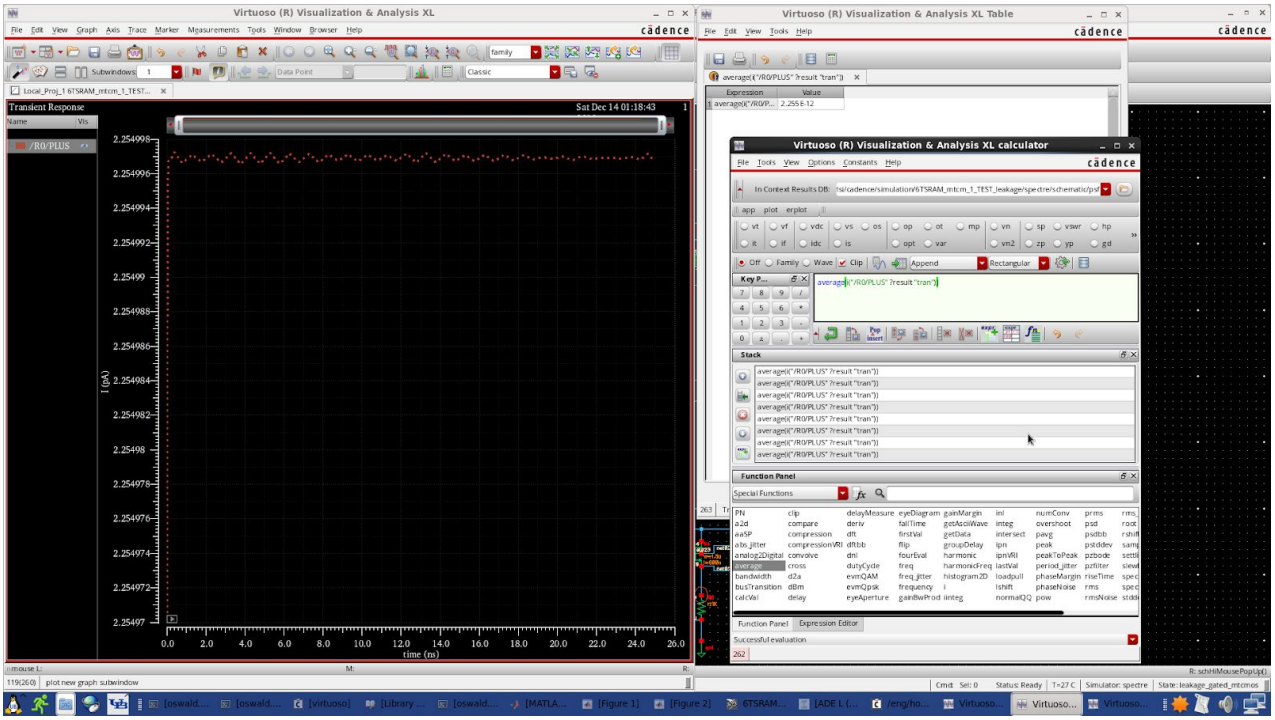


Leakage current analysis results

- **MT-CMOS**



Schematic Diagram used for Leakage power analysis

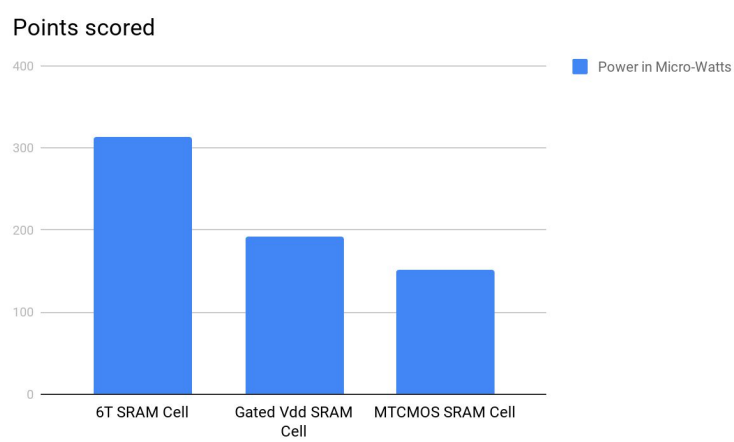


Leakage current analysis results

OBSERVATIONS AND INFERENCES

- ### POWER ANALYSIS

In this analysis, we simulated and plotted the power consumption of the circuits and calculated the average power consumption by using the Visualization and Analysis tool in Cadence. On comparing the results, we observed that the average power consumed by the original 6T cell is the highest. This is because it has no mechanism to manage its power supply which causes significant static leakage power dissipation. In the case of Gated Vdd SRAM Cell, we introduced a control mechanism attached to a high threshold voltage transistor which can control the supply voltage Vdd. In the MTCMOS technique, we introduce sleep transistors before both the Vdd and Gnd terminals. These are high threshold voltage transistors which act as full fledged virtual power rails and hence control both Vdd and Gnd. Since we are controlling Vdd too,the leakage power dissipation in circuit reduces right after Vdd. This ensures very good performance in the circuit. Hence, the expected outputs align with the research and expected results.



- ## STATIC NOISE MARGIN ANALYSIS

Static Noise Margin (SNM) is one of the most important parameters for memory design. It affects both read and write margin and is related to the threshold voltages of the NMOS and PMOS devices of the SRAM. SNM is a measure of how tolerant an SRAM cell is to noise before it starts to incur data loss. SNM must be improved to improve the performance of the circuit. The voltage transfer characteristics have been plotted in the form of a two-lobed curve known as a butterfly curve.

- ## LEAKAGE CURRENT ANALYSIS

(*We have performed this analysis as an additional experiment apart from the proposed components in an effort to learn more about SRAM circuits*)

A leakage current is an electric current in an unwanted conductive path under normal operating conditions. A small leakage current flows through the transistors, even when the circuit is turned off. We have attempted to measure and compare the leakage currents for different SRAM Cells by adding a resistor in the circuit, before the ground terminal. Ideally a circuit has very low leakage current.

We observed that MTCMOS SRAM cell has the least leakage current and there is no significant difference between the leakage current of Gated Vdd SRAM Cell and MTCMOS SRAM Cell.

6T SRAM Cell	Gated Vdd SRAM Cell	MTCMOS SRAM Cell
1.017 nA	1.017 nA	2.225 pA

FUTURE SCOPE:

- Apart from these techniques, other methods to increase the performance and reduce power consumption can be developed.
- These are sleep transistor technique, Forced stack technique and sleepy stack technique.
- Sleepy stack technique can produce better results by introducing four additional transistors and adjusting their W/L ratio.

CONCLUSION

The complete 4x4 array which includes peripheral components such as memory bit cell, write driver circuit, pre-charge circuit, Sense amplifier are designed and integrated. The functioning of various components within the array and how they are enabled was understood.

Various analyses on the different versions of the SRAM Cells were performed. It was observed that introducing mechanisms such as sleep transistors and adjusting their threshold voltages leads to greater power efficiency. Hence, MTCMOS version of SRAM cell in general is the most power efficient among the three.

Introducing such control mechanisms also increases the area of the circuit. Thus, we can conclude that a balance between compactness and performance is essential. In conclusion, the addition of techniques discussed are useful in making the circuit better in terms of power efficiency in comparison to a regular SRAM cell.

REFERENCES

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