Lab 3: Ripple Carry Adder and 1 Bit Full Adder

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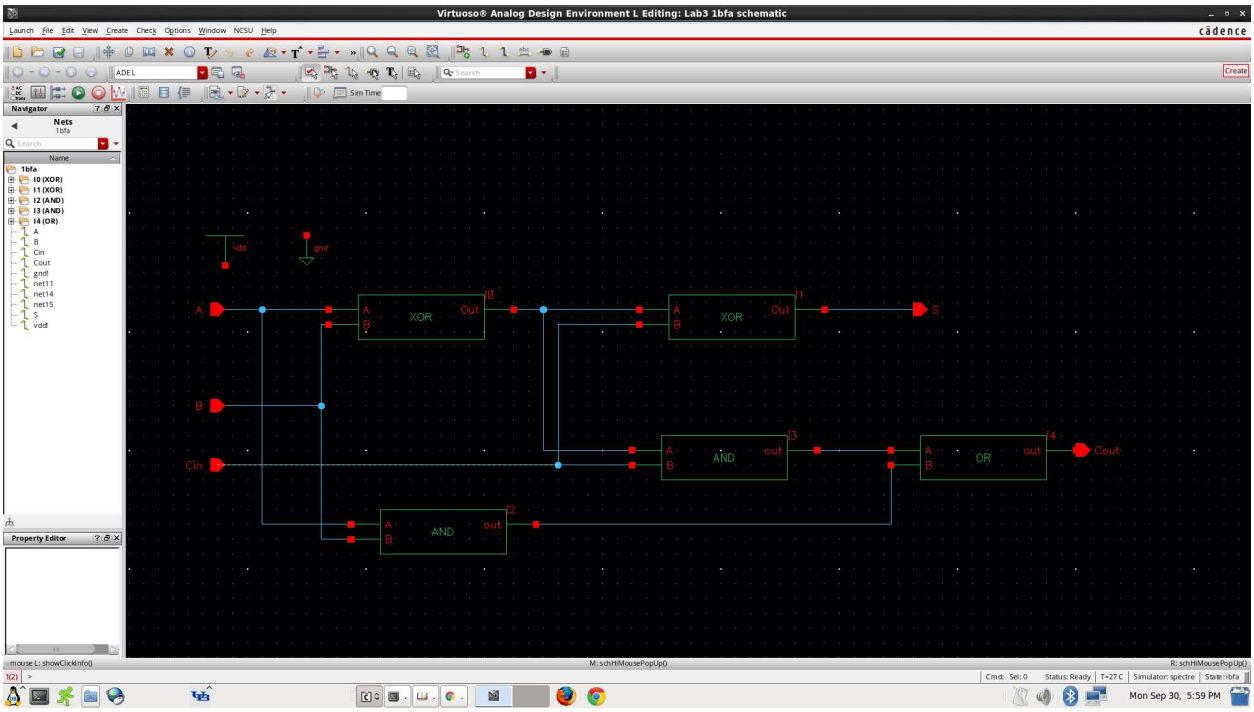
Objective:

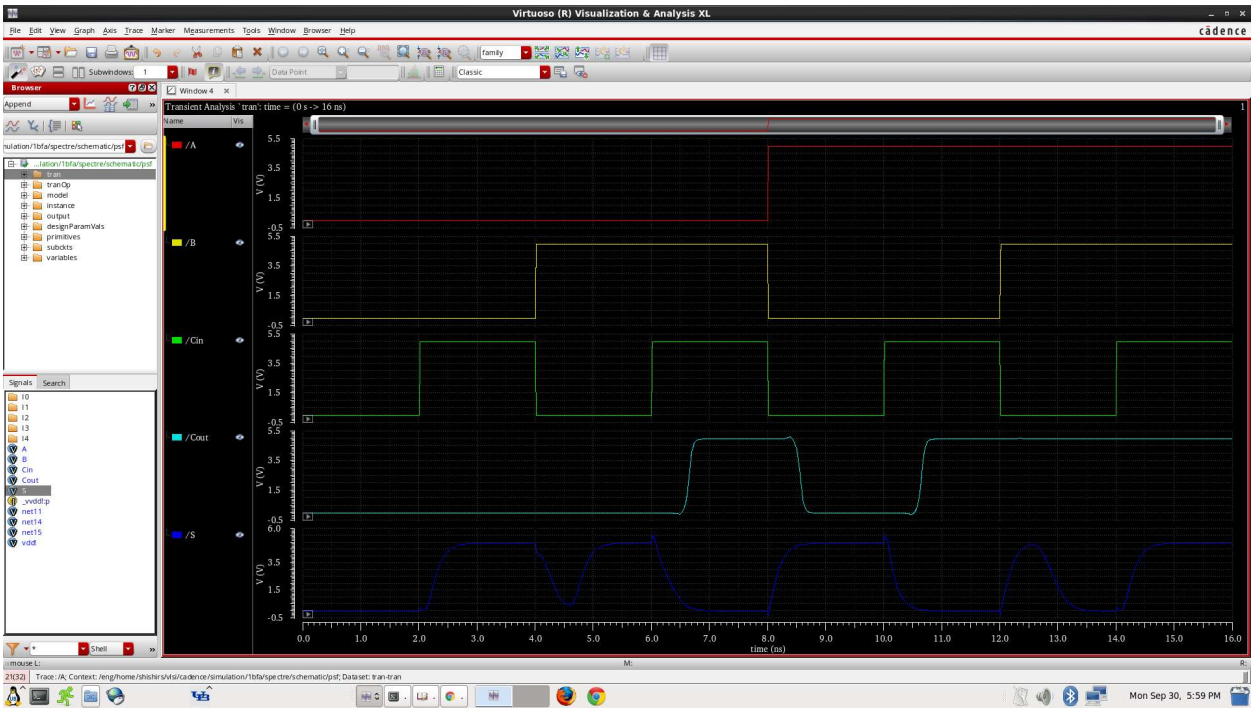
- To understand the working and design of 1 Bit Full Adder and Ripple Carry Adder
- To implement their schematic and layout versions using Cadence
- Prepare a report to summarize the results of the lab activity

1 Bit Full Adder:

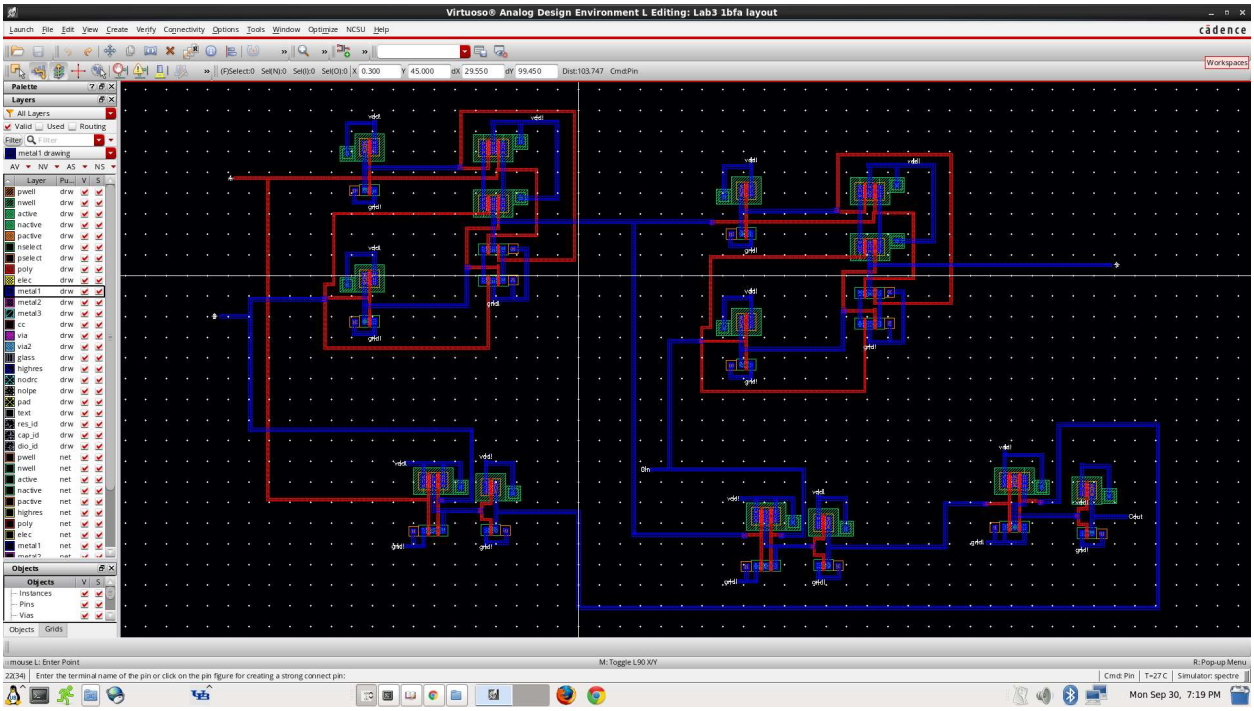
Schematic View:



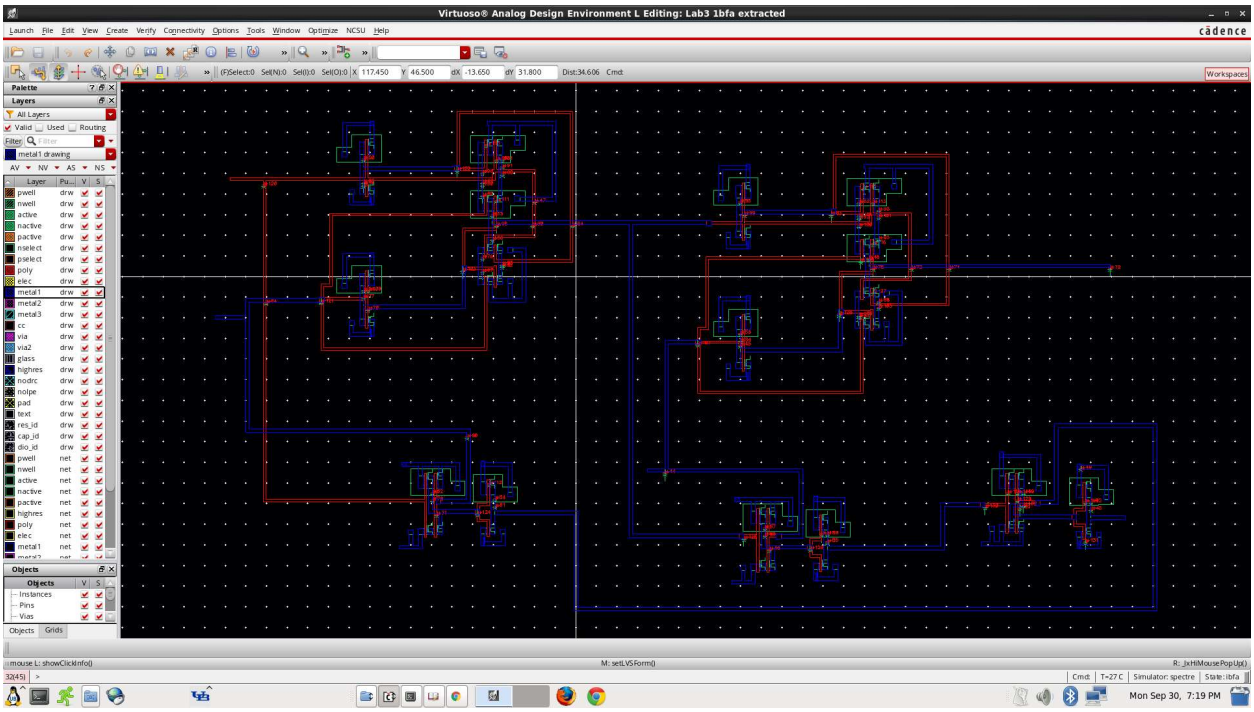
Schematic View Simulation:



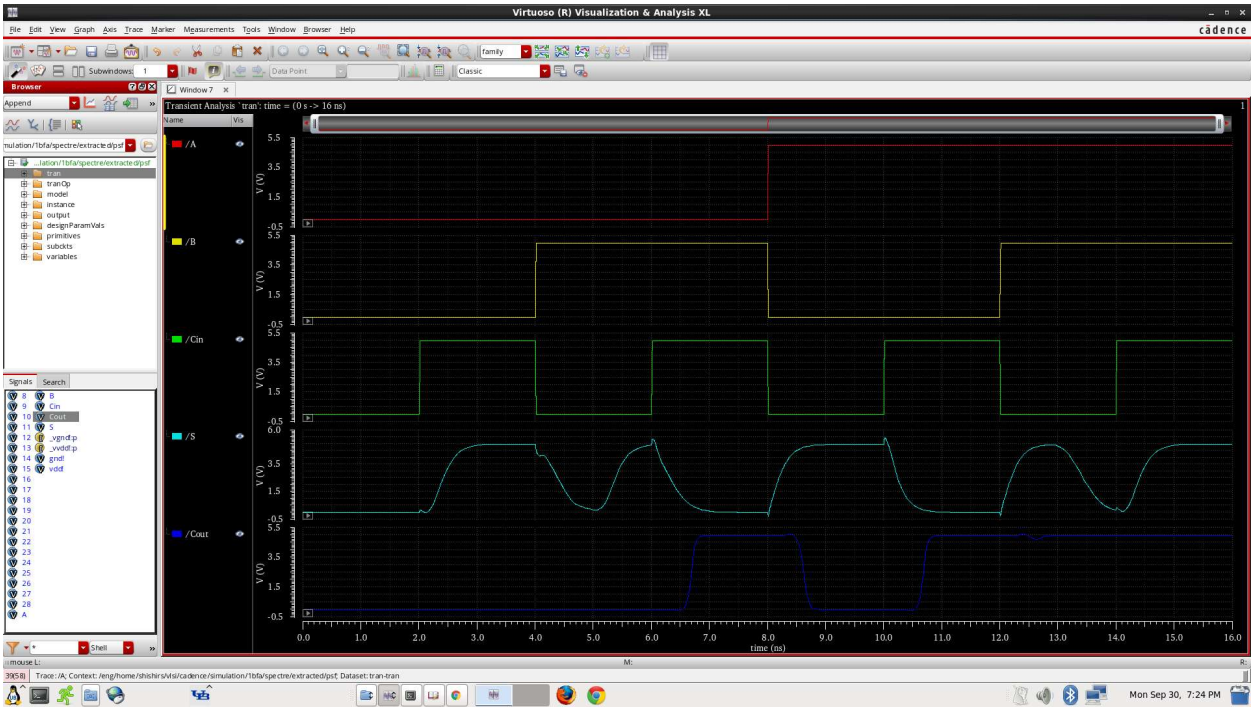
Layout View:



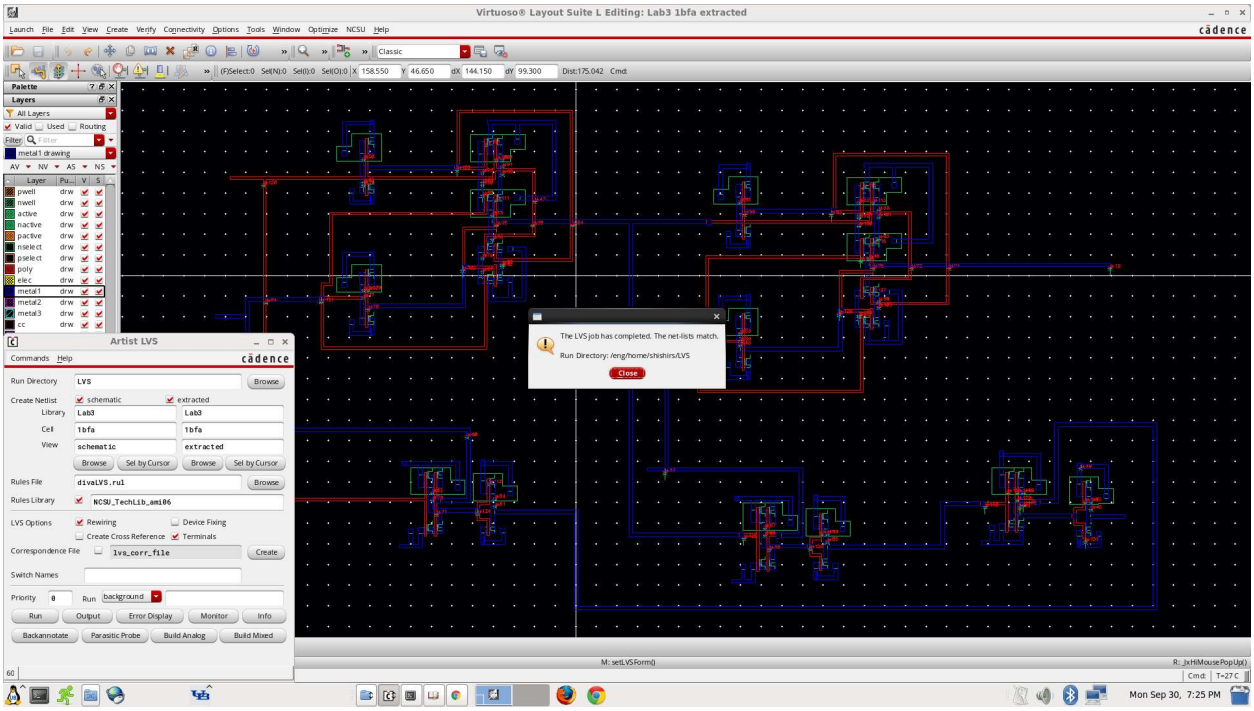
Extracted View:



Extracted View Simulation:



LVS Match between Schematic and Extracted Views:

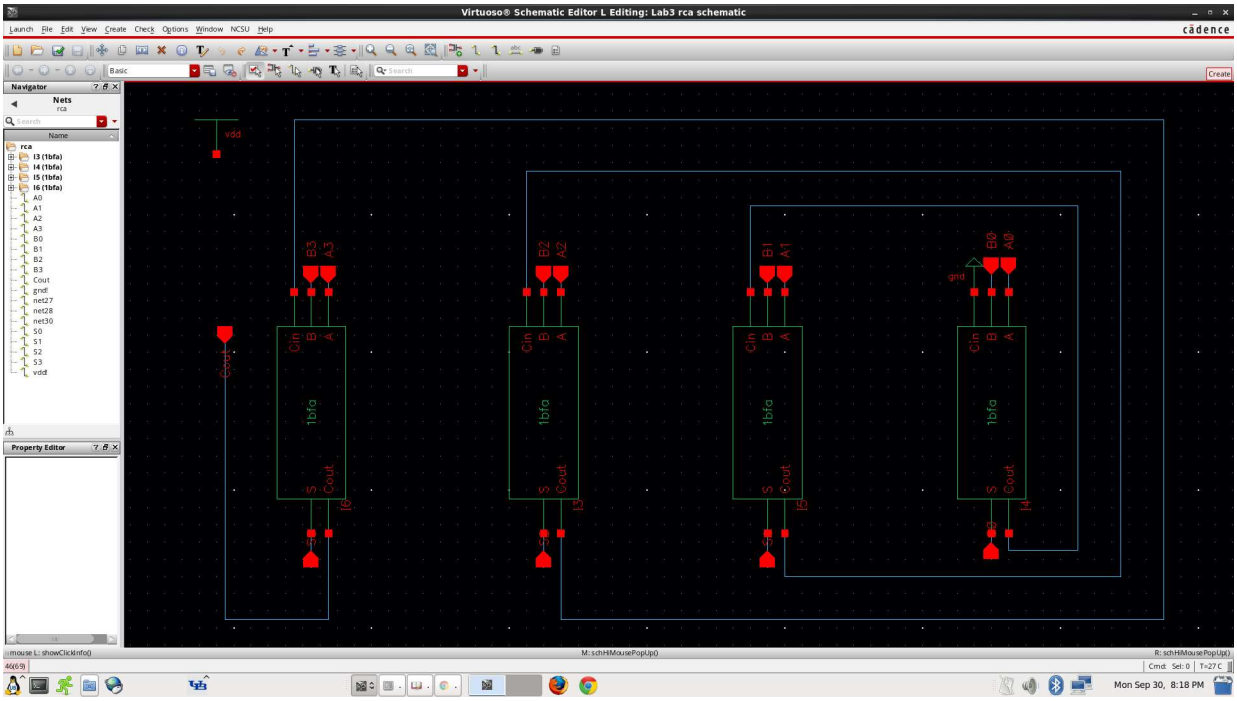


Truth Table:

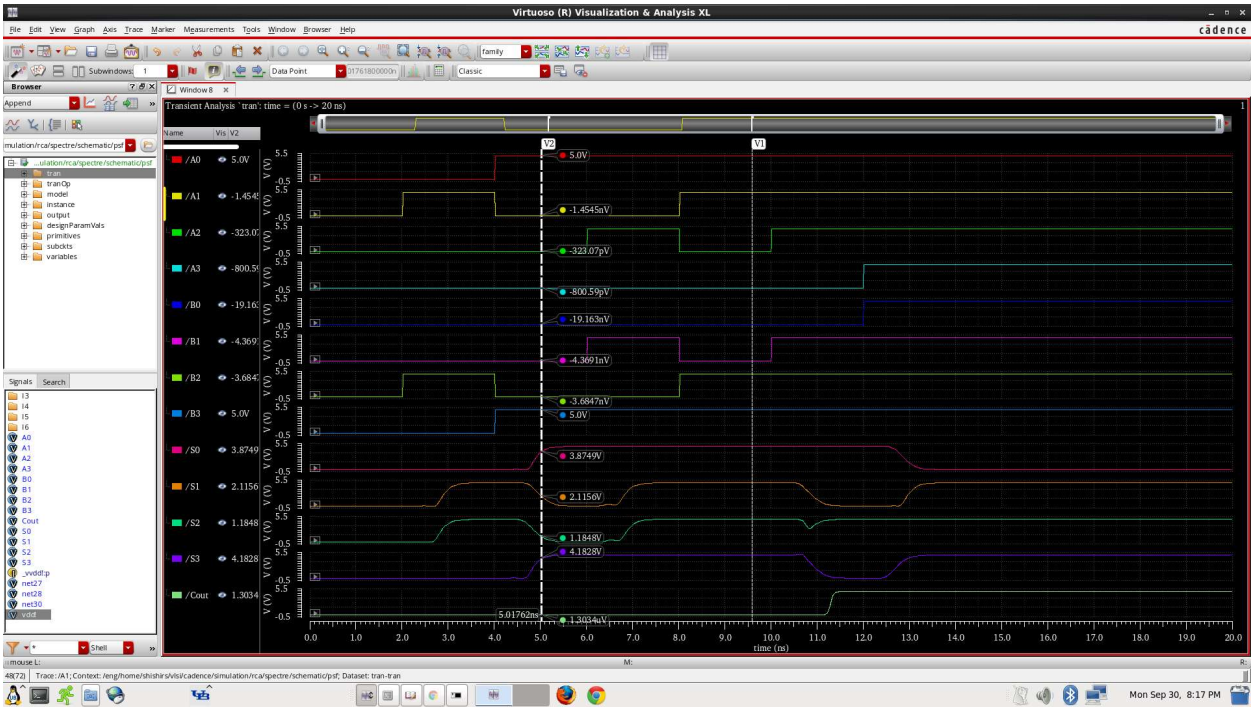
Inputs			Outputs	
A	***B***	C_{in}	C_{out}	***Sum***
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Ripple Carry Adder:

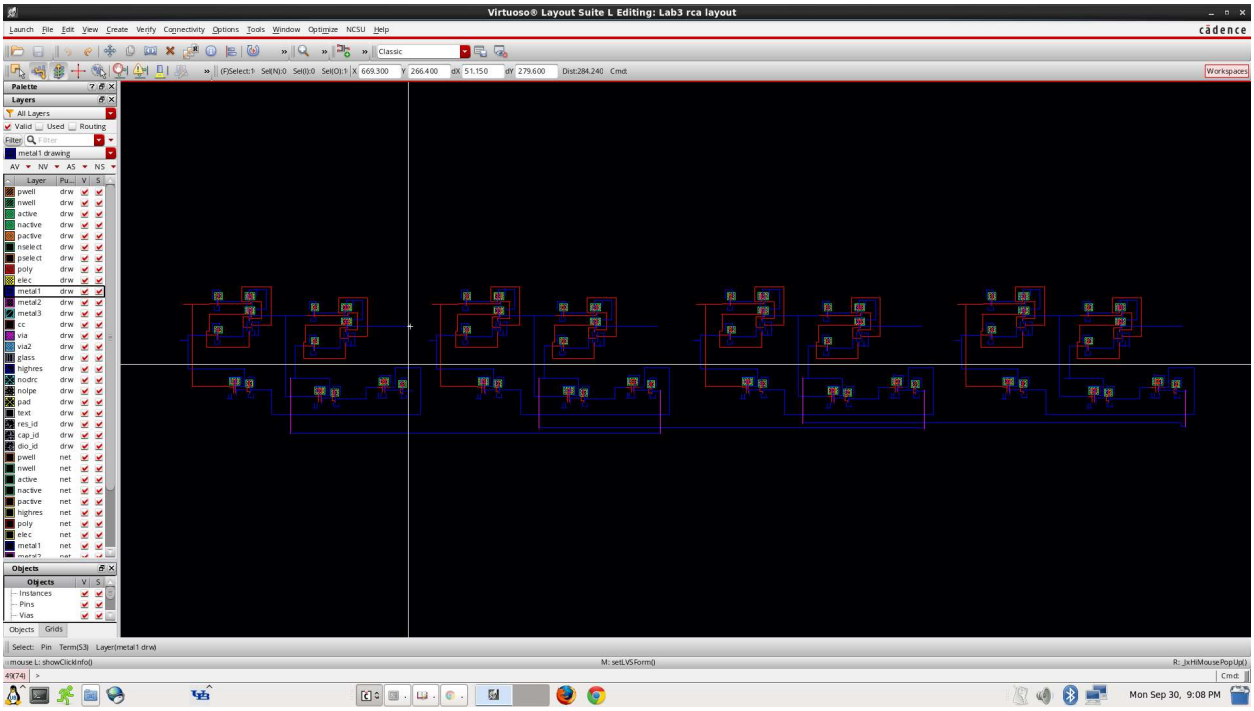
Schematic View:



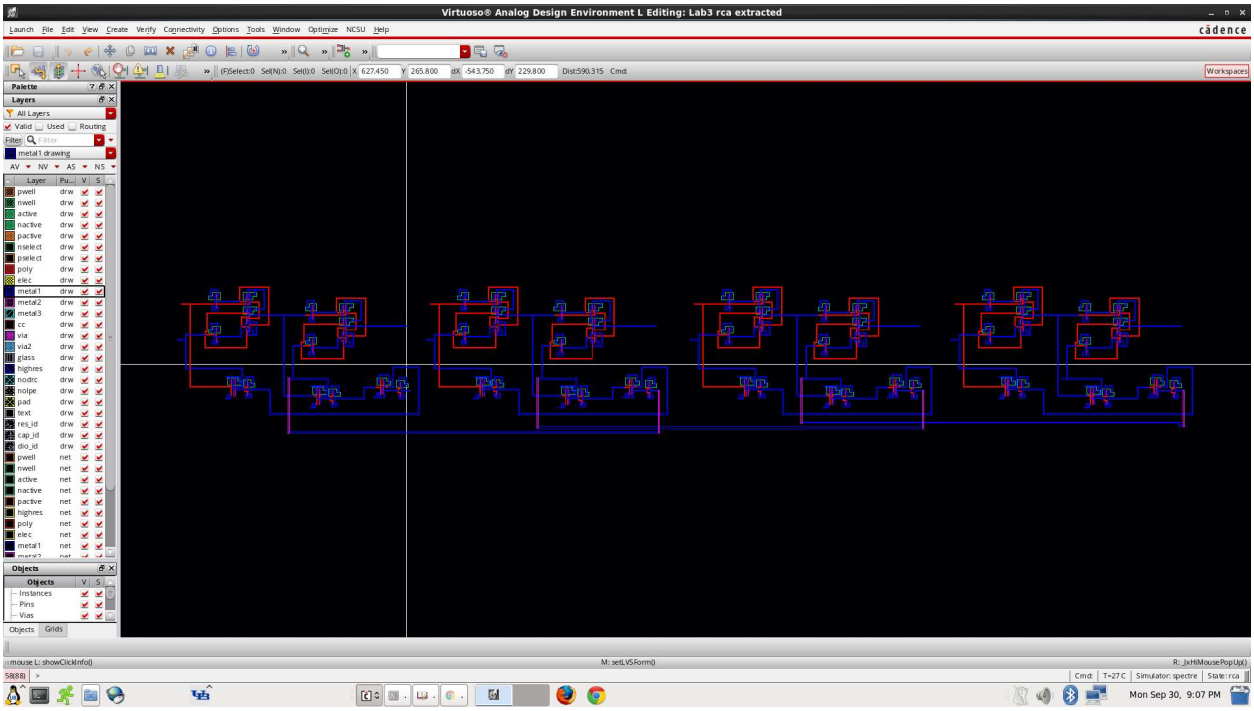
Schematic View Simulation:



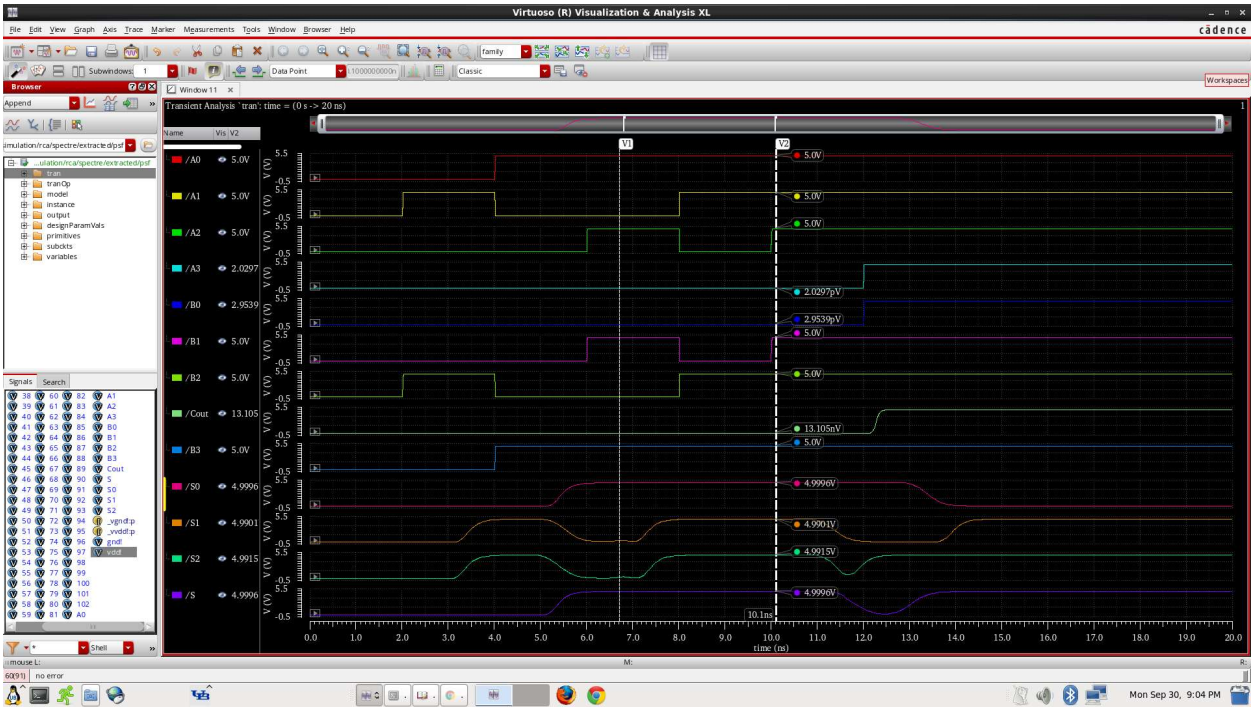
Layout View:



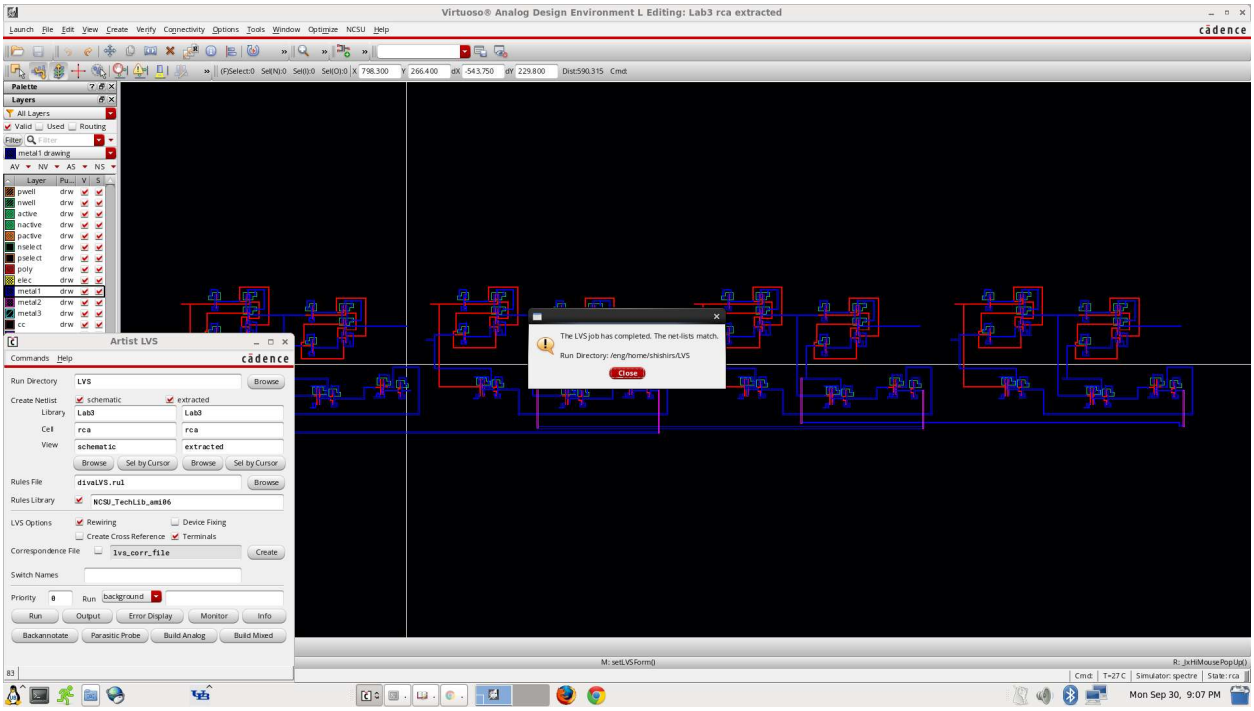
Extracted View:



Extracted View Simulation:



LVS Match between Schematic and Extracted Views:



Truth Table:

A1	A2	A3	A4	B4	B3	B2	B1	S4	S3	S2	S1	carry
0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	1	0	0	1	0	0	0	0
1	0	0	0	1	0	0	0	0	0	0	0	1
1	0	1	0	1	0	1	0	0	1	0	0	1
1	1	0	0	1	1	0	0	1	0	0	0	1
1	1	1	0	1	1	1	0	1	1	0	0	1
1	1	1	1	1	1	1	1	1	1	1	0	1

Working of circuit:

- An adder is a digital circuit that performs addition of numbers that is widely used in computer processors
- 1 Bit Full Adder takes in three numbers A, B and a Carry (Cin) and outputs two binary numbers, a Sum and a Carry Value
- It is constructed using a combination of various logic gates including XOR, AND and OR gates
- A Full adder is usually a cascade of adders
- A Ripple Carry Adder on the other hand is a combination of 1 Bit Full Adders in sequence
- Each Full Adder gets an input of Cin from the Cout of the previous Adder
- It is known as a “Ripple Carry Adder” as Carry from each Adder ripples forward to next adder
- Cin of first Adder is connected to Ground while the Cout of the last Adder represents the final Carry value

Inference and Conclusion:

- The working of 1 Bit Full Adder circuits was learnt using circuit design techniques
- The working of Ripple Carry Adder circuits was learnt using circuit design techniques
- We learnt how to combine Full Adders to assemble a Ripple Carry Adder
- The schematic and Layout versions of the gates were implemented in the form of circuits in Cadence
- The correctness of the circuit design was verified using simulation tools and output was recorded

- LVS (Layout vs Schematic) check was performed to check if both versions of a gate matched