# Lab 2: Implementation of D Flip Flop

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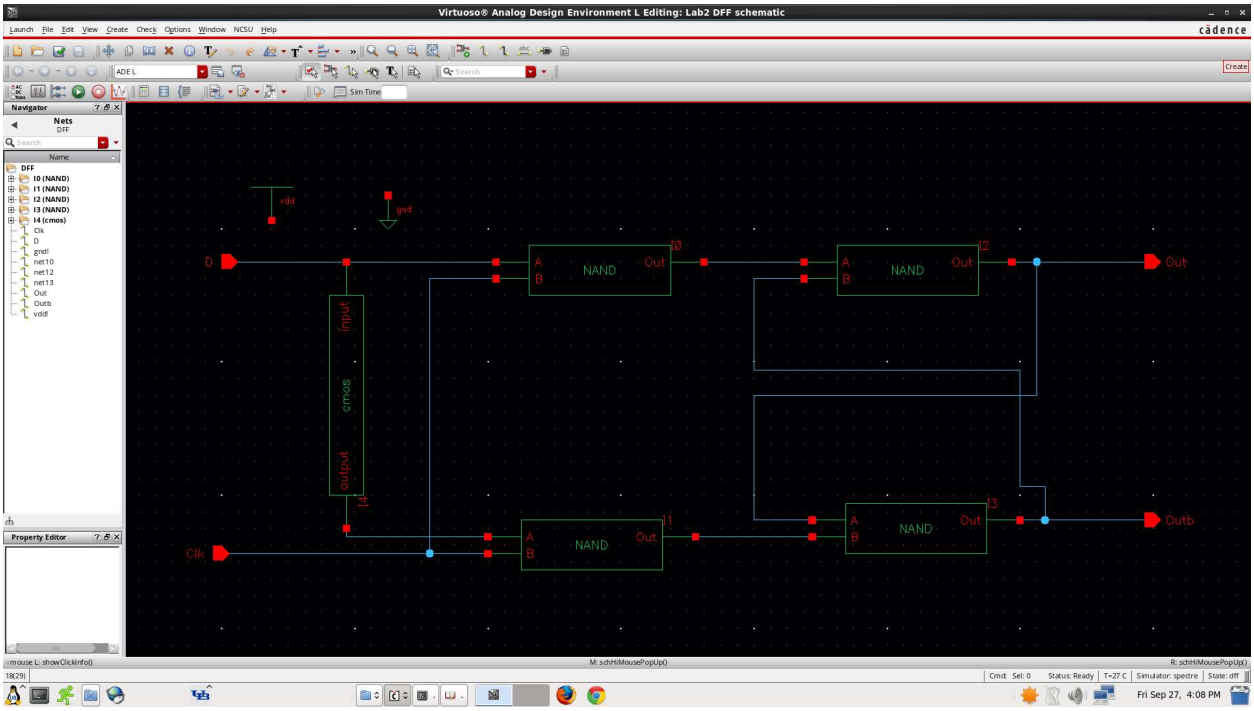
## Objective:

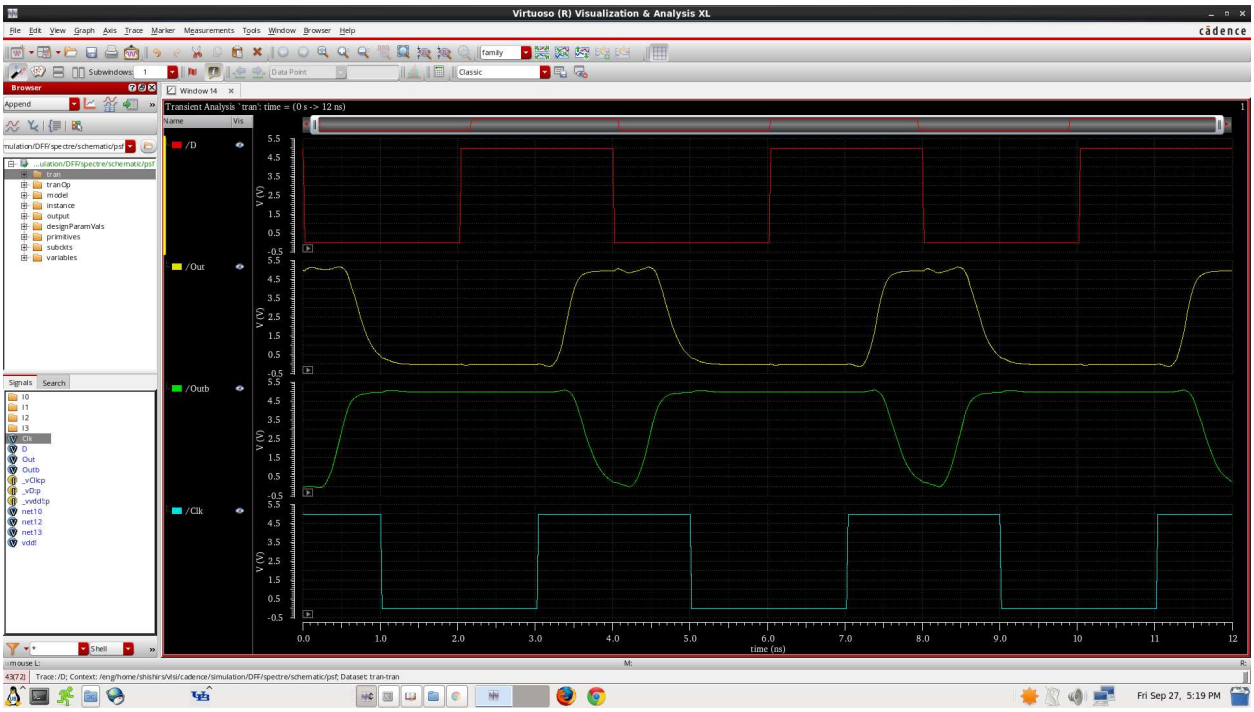
- To understand the working and design of Delay Flip Flop
- To implement their schematic and layout versions using Cadence
- Prepare a report to summarize the results of the lab activity

## D Flip Flop using CMOS:

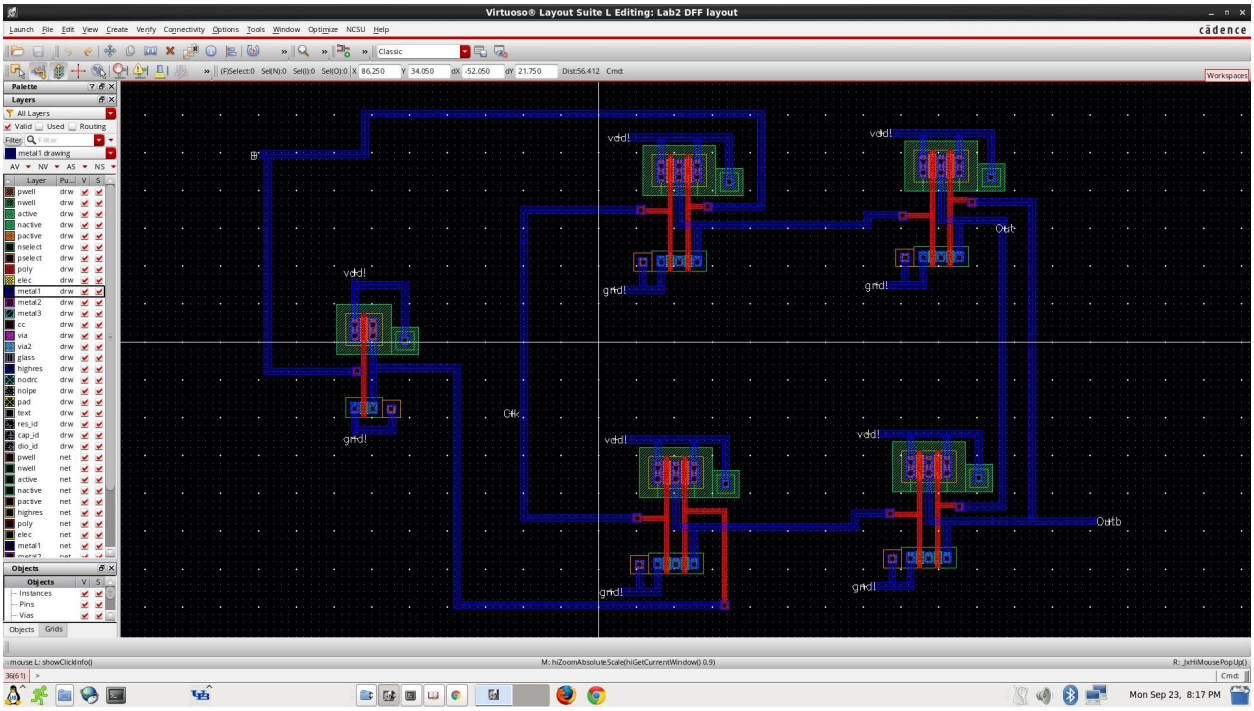
### Schematic View:



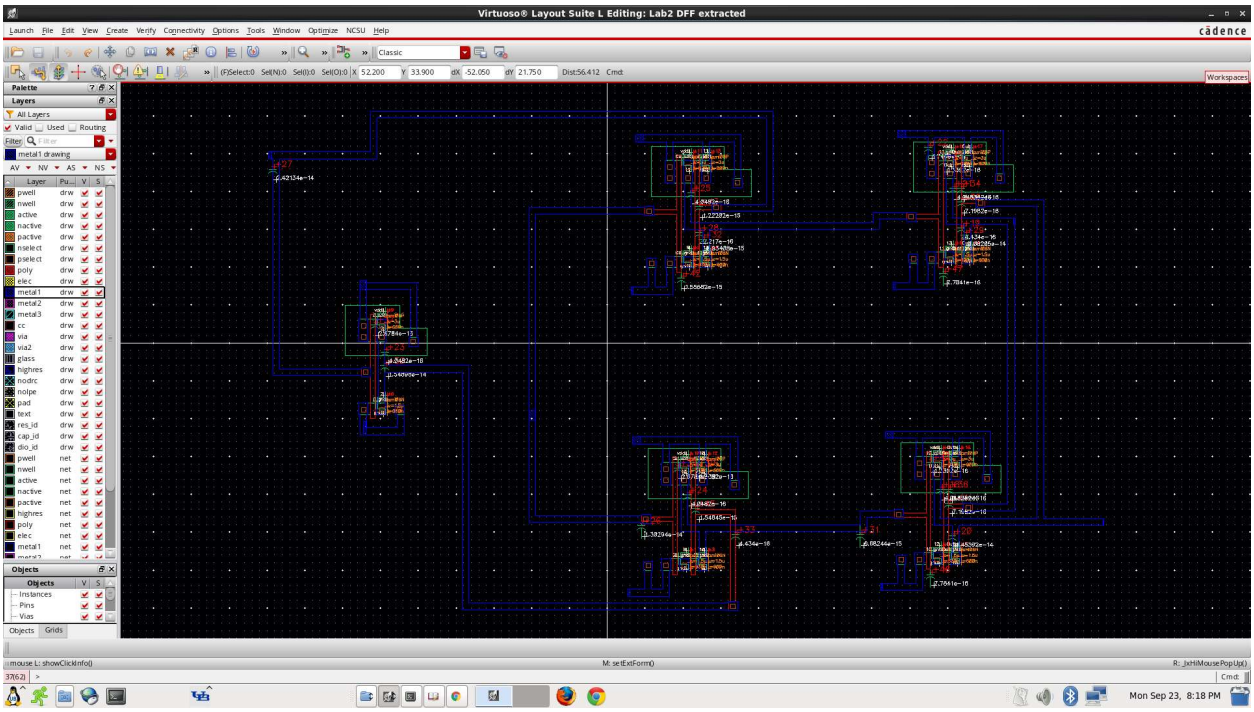
## Schematic View Simulation:



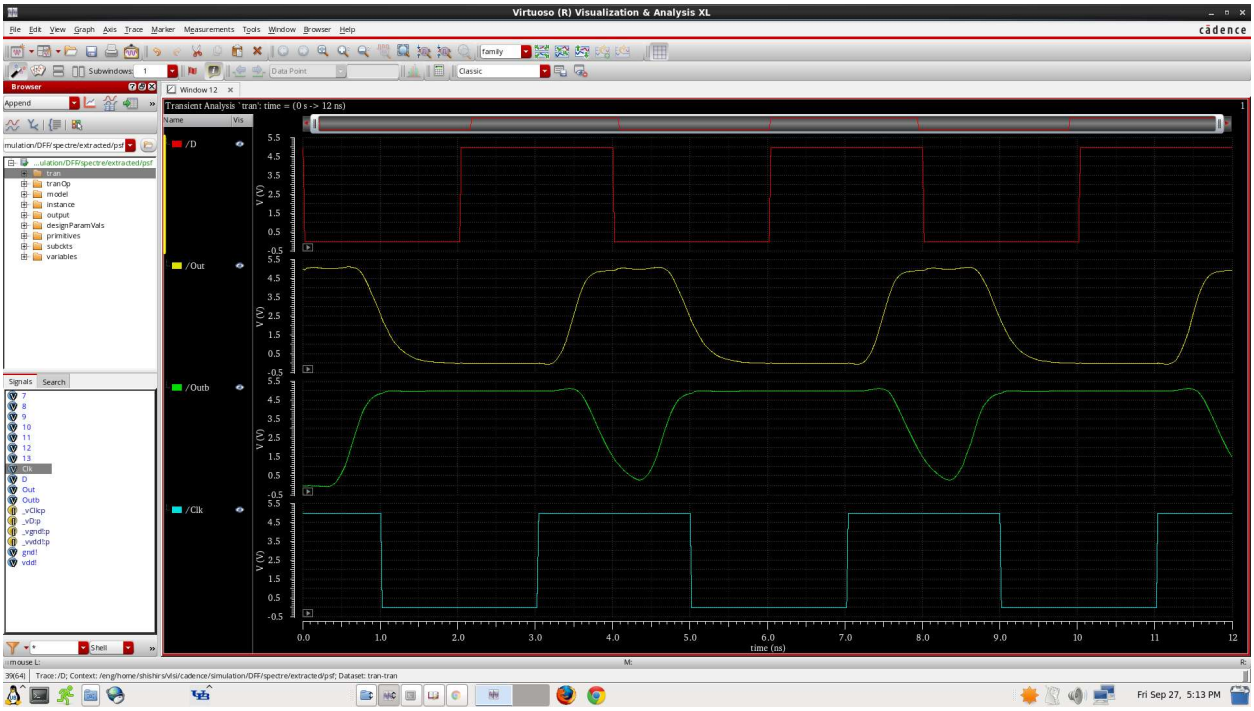

## Layout View:



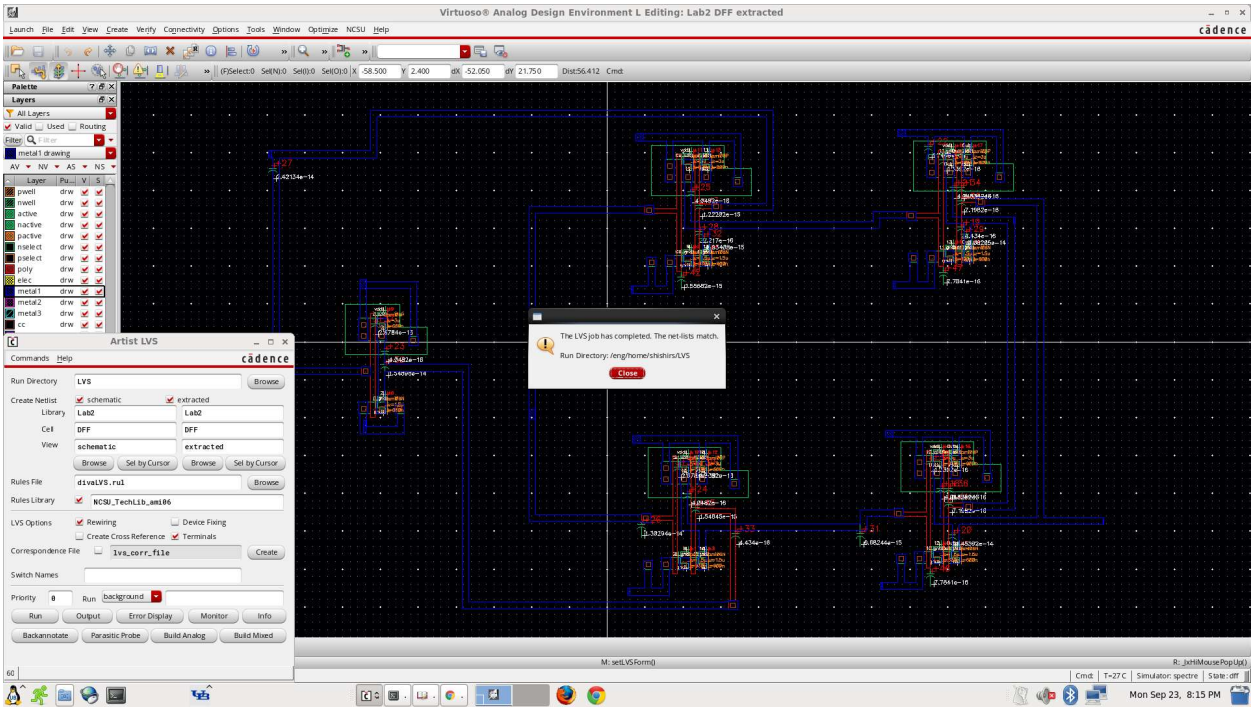
## Extracted View:




## Extracted View Simulation:



## LVS Match between Schematic and Extracted Views:

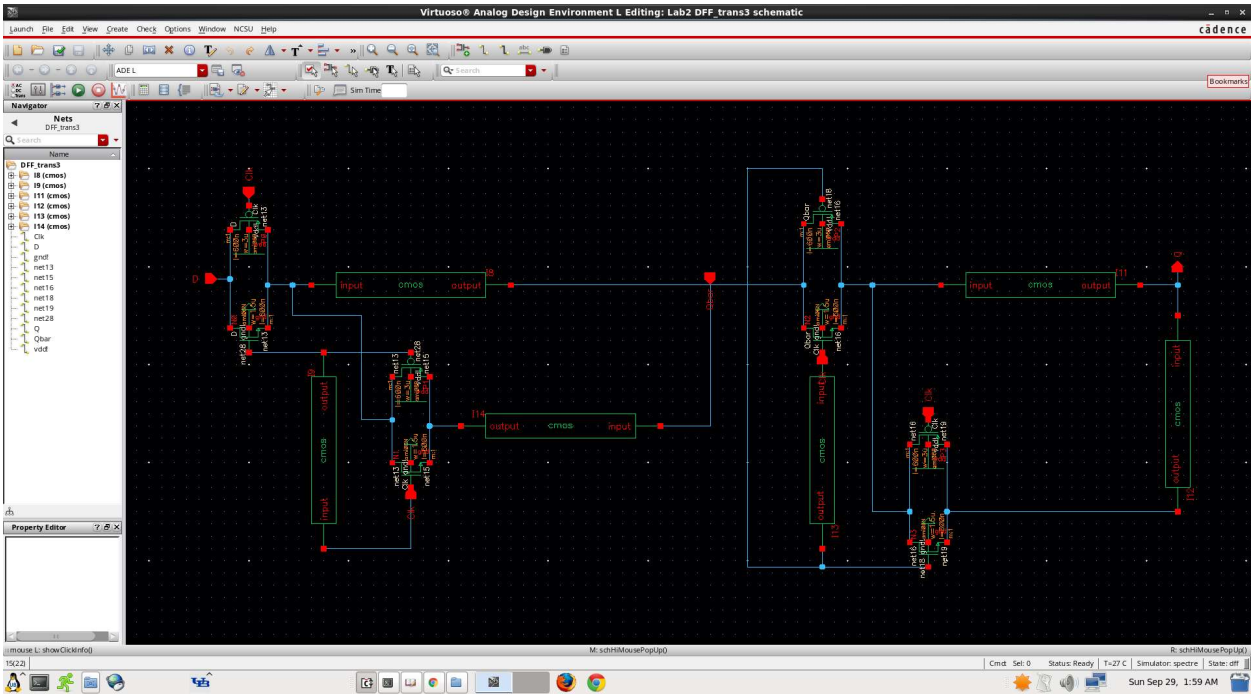



## Truth Table:

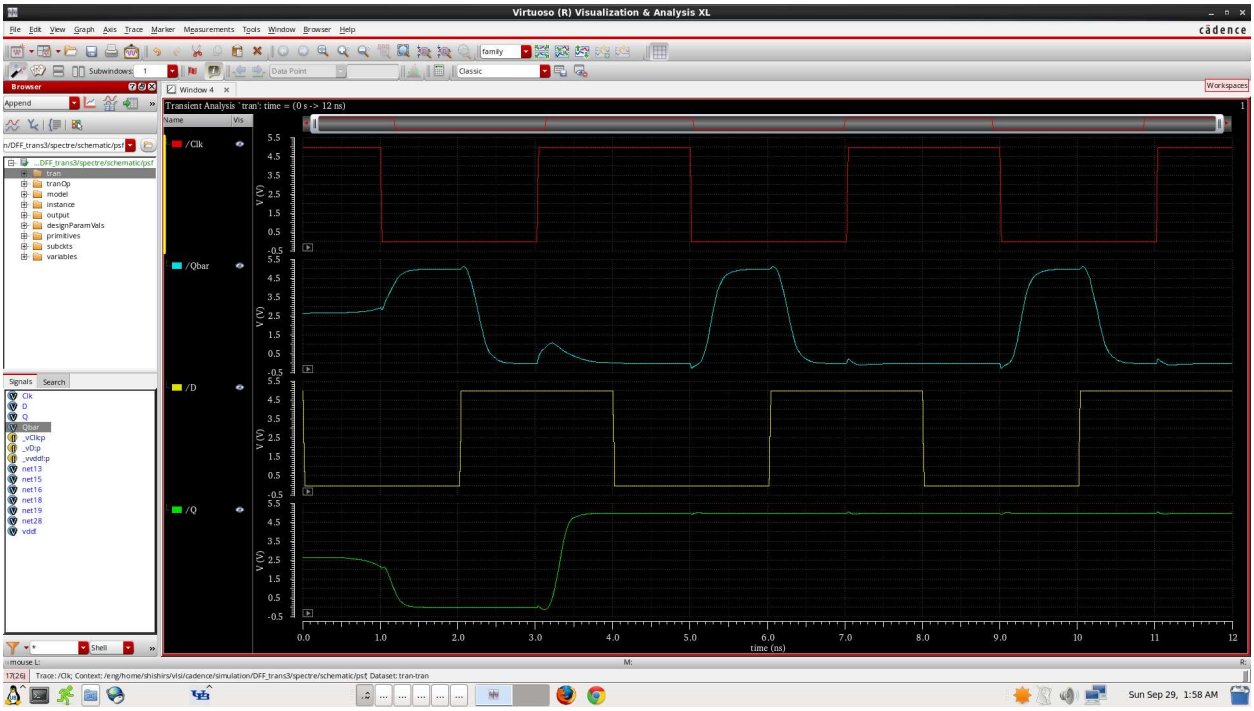
| Clk | D | Q | | Description |
|---|---|---|---|---|
| ↓ » 0 | X | Q | $\overline{Q}$ | Memory no change |
| ↑ » 1 | 0 | 0 | 1 | Reset Q » 0 |
| ↑ » 1 | 1 | 1 | 0 | Set Q » 1 |

# D Flip Flop using Transmission Gates:

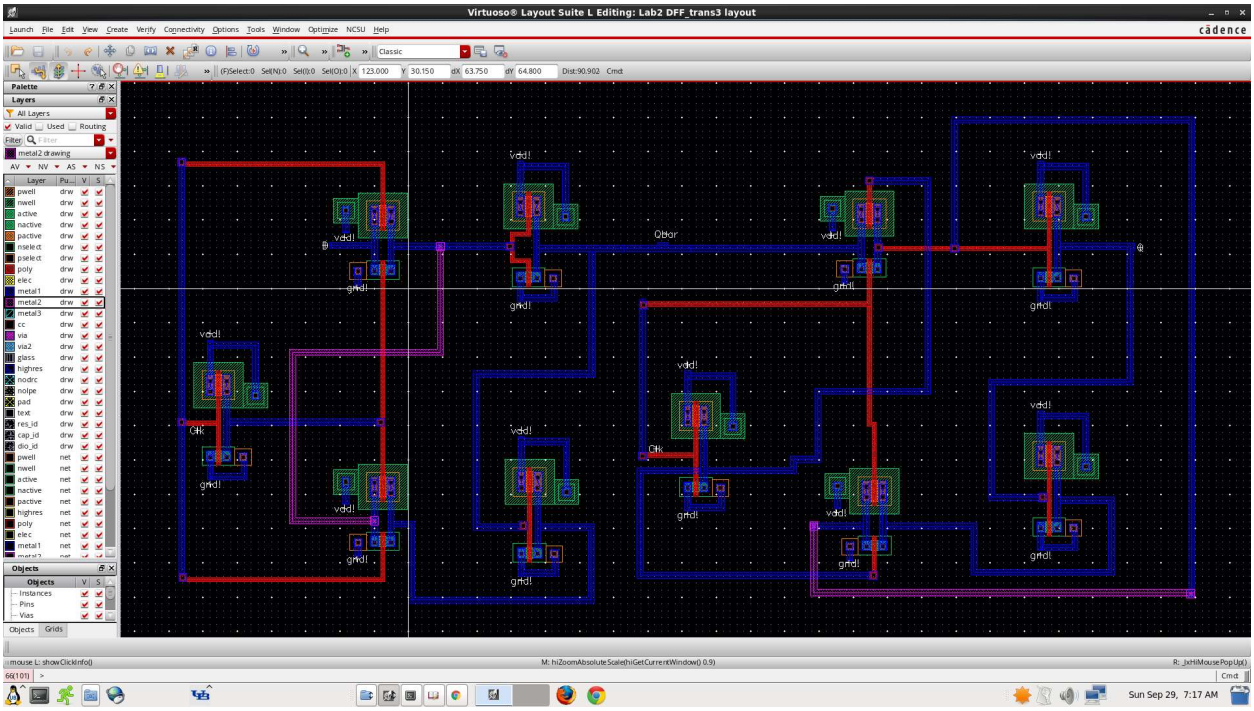
## Schematic View:



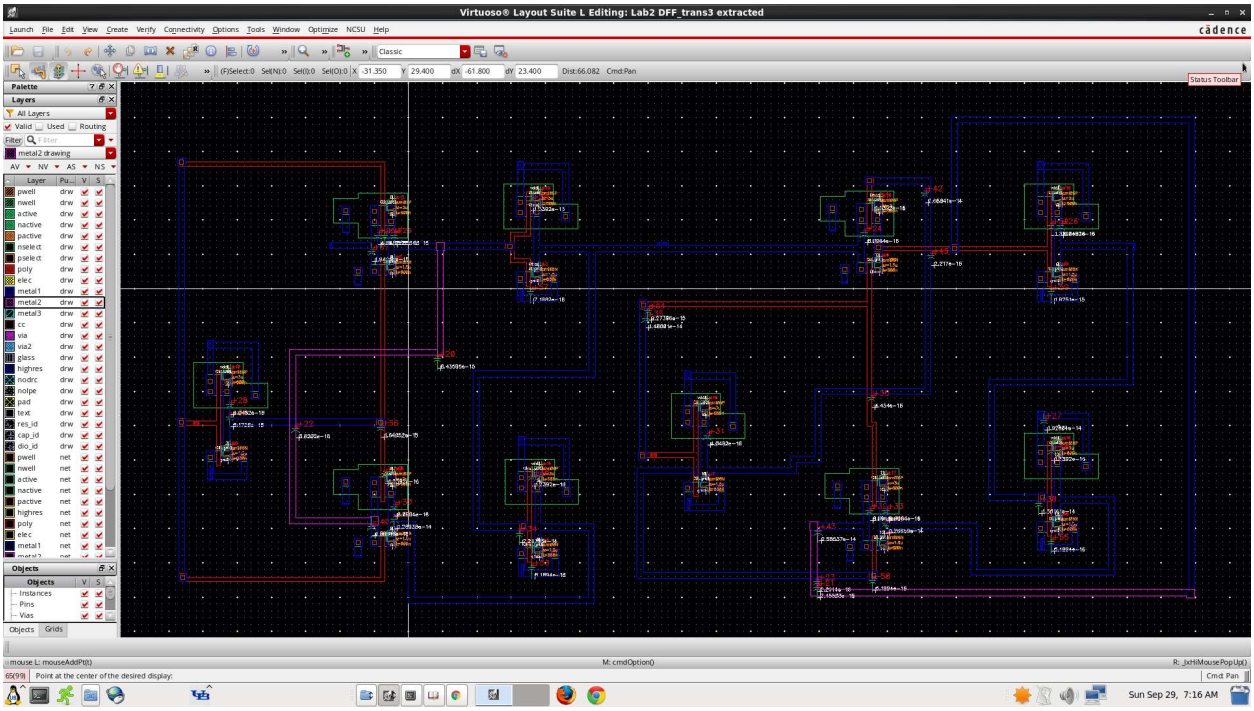

## Schematic View Simulation:



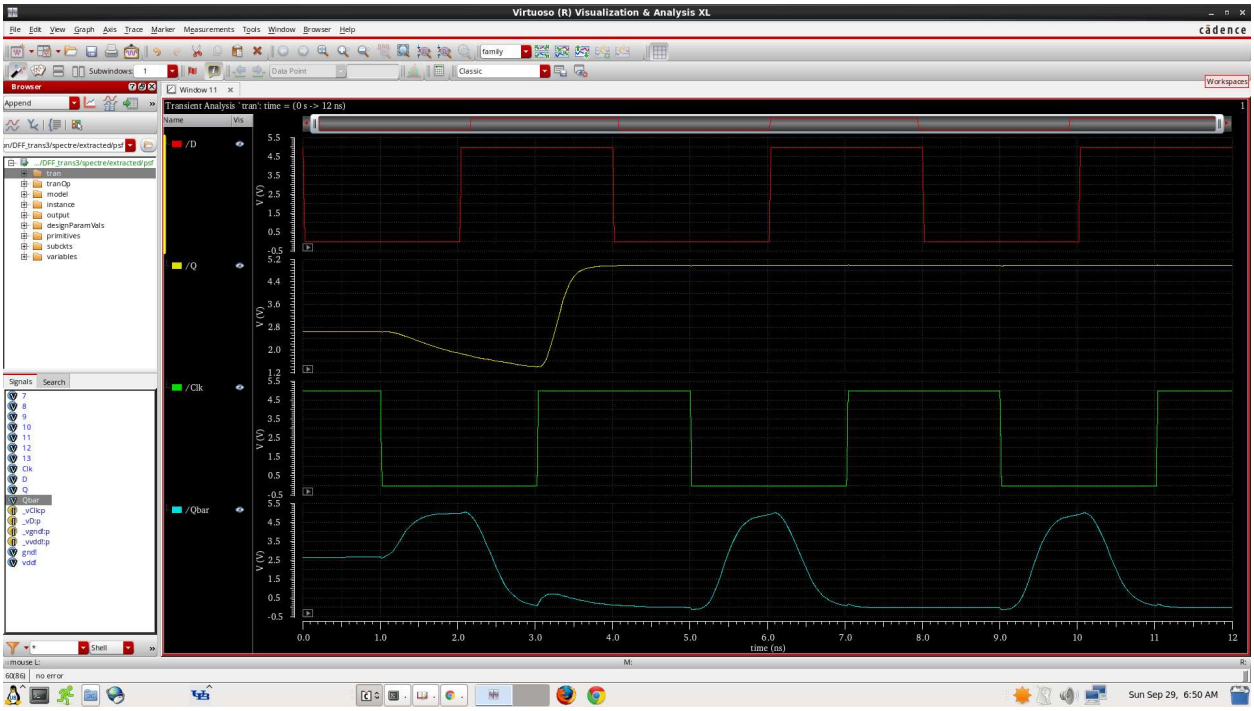
## Layout View:




## Extracted View:



## Extracted View Simulation:

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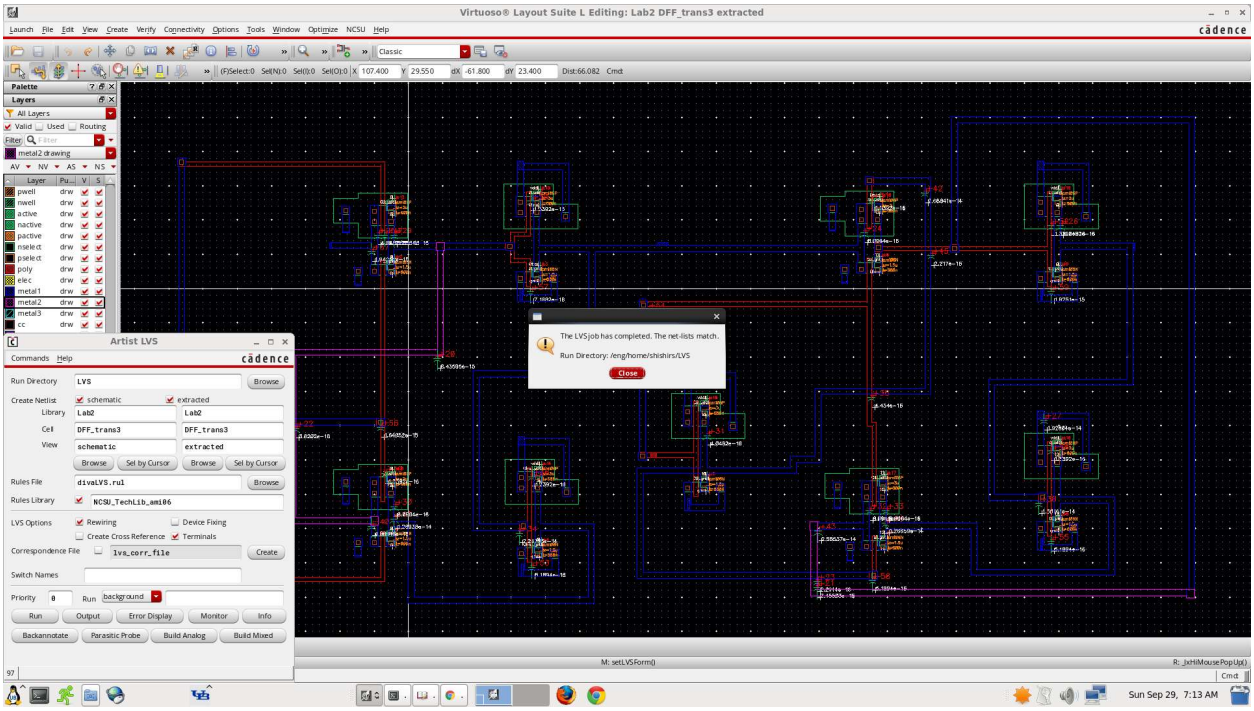

Truth Table:

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## Working of circuit:

- The D Flip Flop circuit can be used to store memory where the output is dependent on the clock signal i.e clock is a control signal
- When the clock signal is high, the output follows the input signal. When the clock signal is low, the input doesn't affect the output
- circuit can be constructed using two D latches
- D Flip Flop can be used in many applications such as shift registers and frequency registers

## Inference and Conclusion:

- The working of D Flip Flop circuit was learnt using circuit design techniques
- The working of D Latch circuit was learnt using circuit design techniques
- The difference between D Latch and D Flip flop was observed
- It was observed that the transmission gate implementation of the Flip Flop was more efficient than the normal CMOS implementation due to **lesser delay** in output w.r.t clock signal
- The schematic and Layout versions of the gates were implemented in the form of circuits in Cadence
- The correctness of the circuit design was verified using simulation tools and output was recorded
- LVS (Layout vs Schematic) check was performed to check if both versions of a gate matched