Lab 4: Magnitude Comparator

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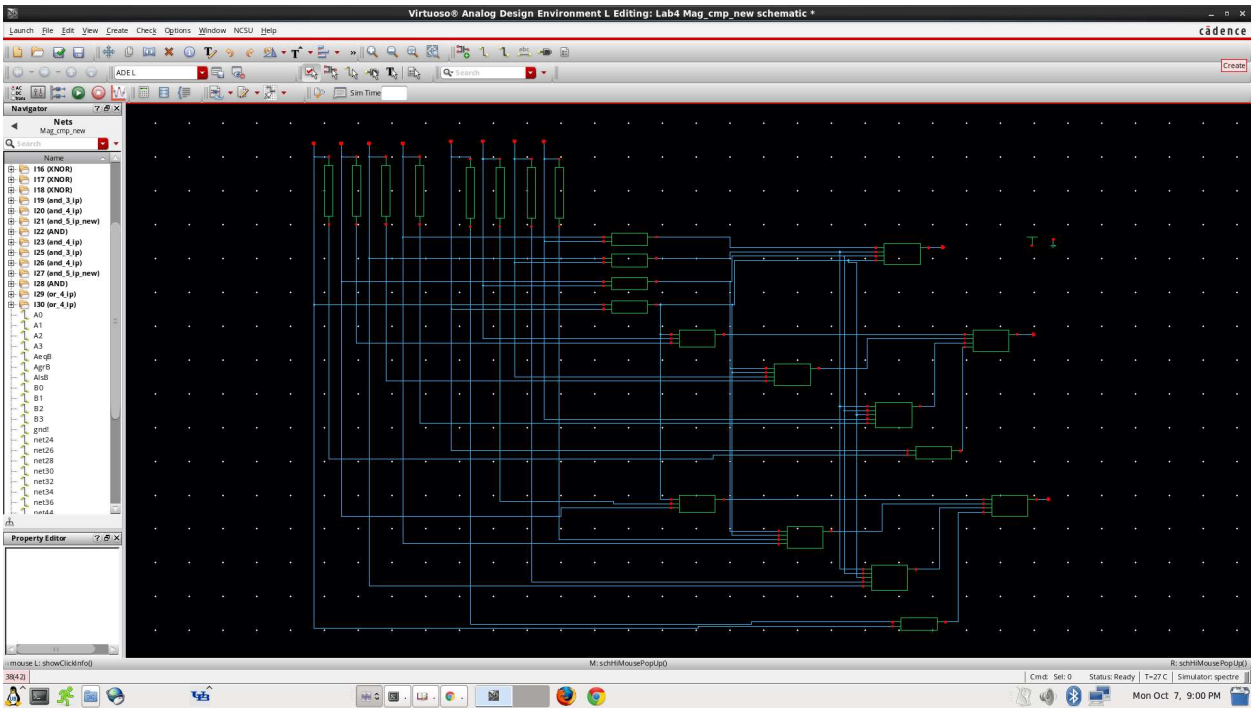
Objective:

- To understand the working and design of 4 Bit Magnitude Comparator
- To implement the schematic and layout versions using Cadence
- Prepare a report to summarize the results of the lab activity

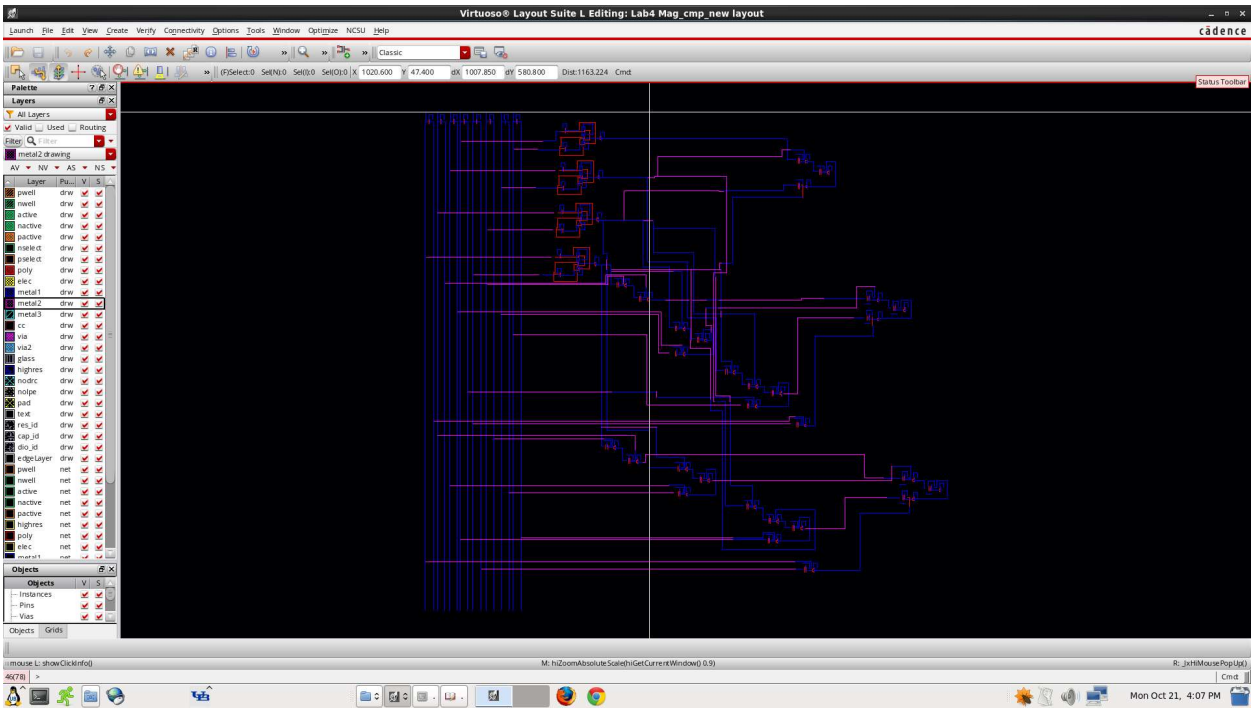
4 bit Magnitude Comparator:

Schematic View:

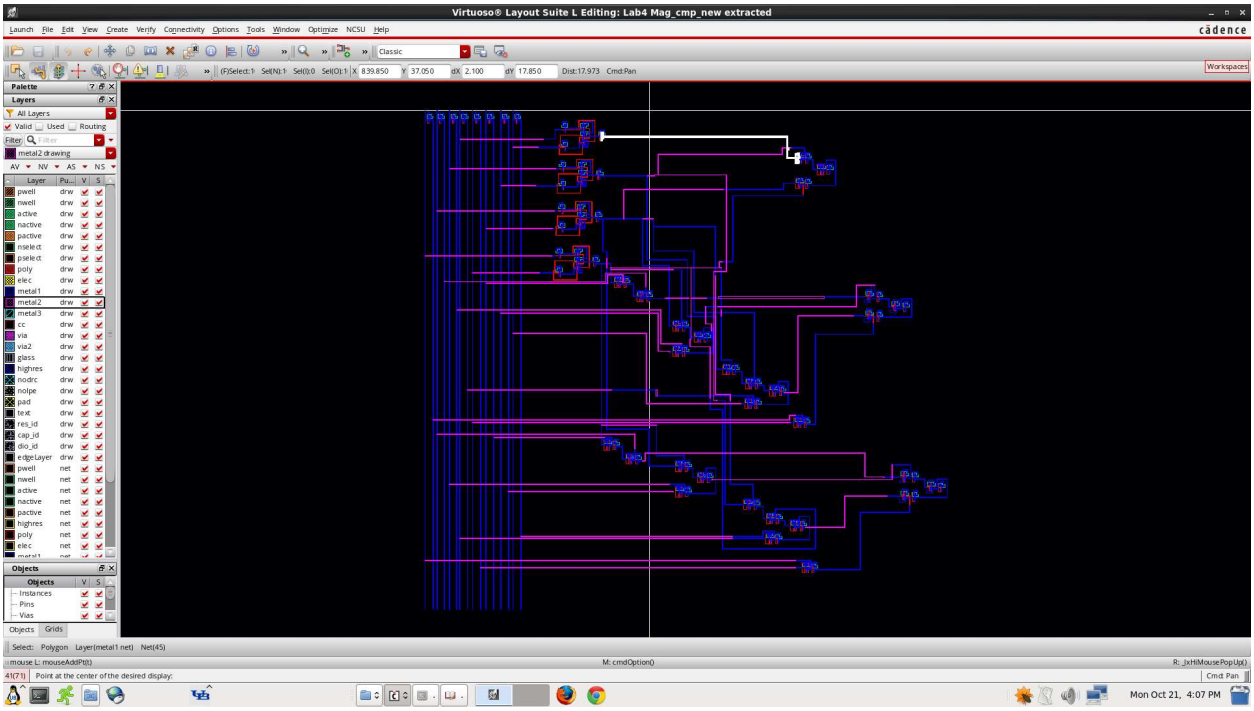


Schematic View Simulation:

Layout View:

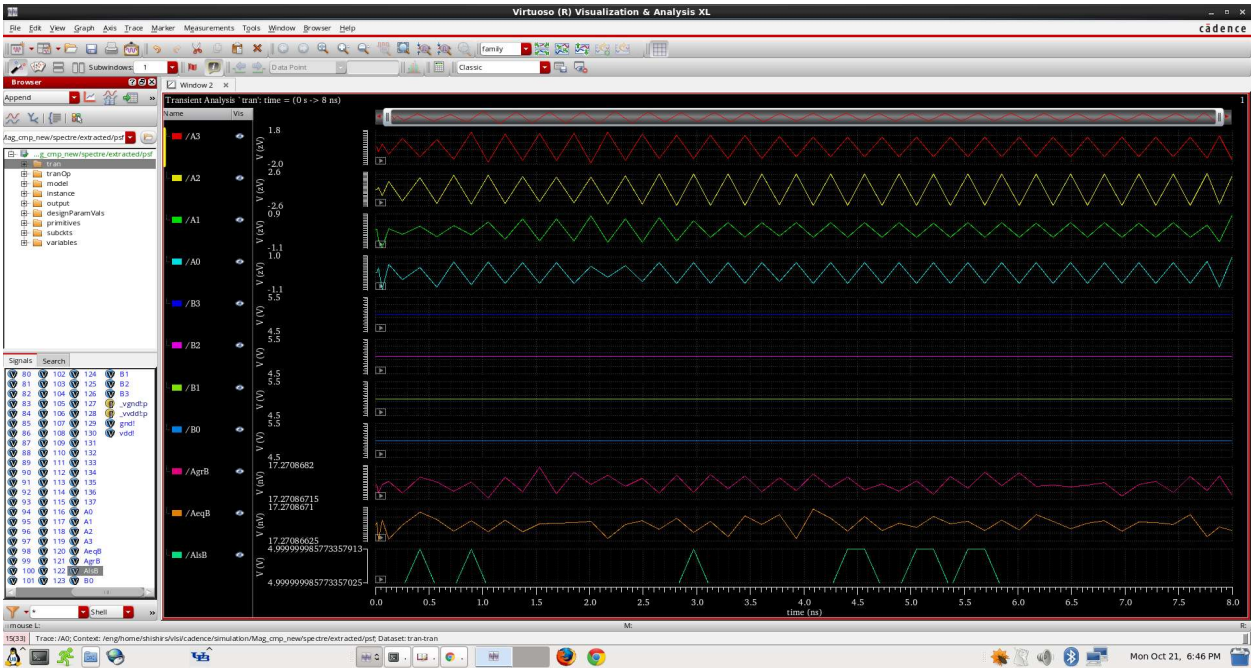


Extracted View:

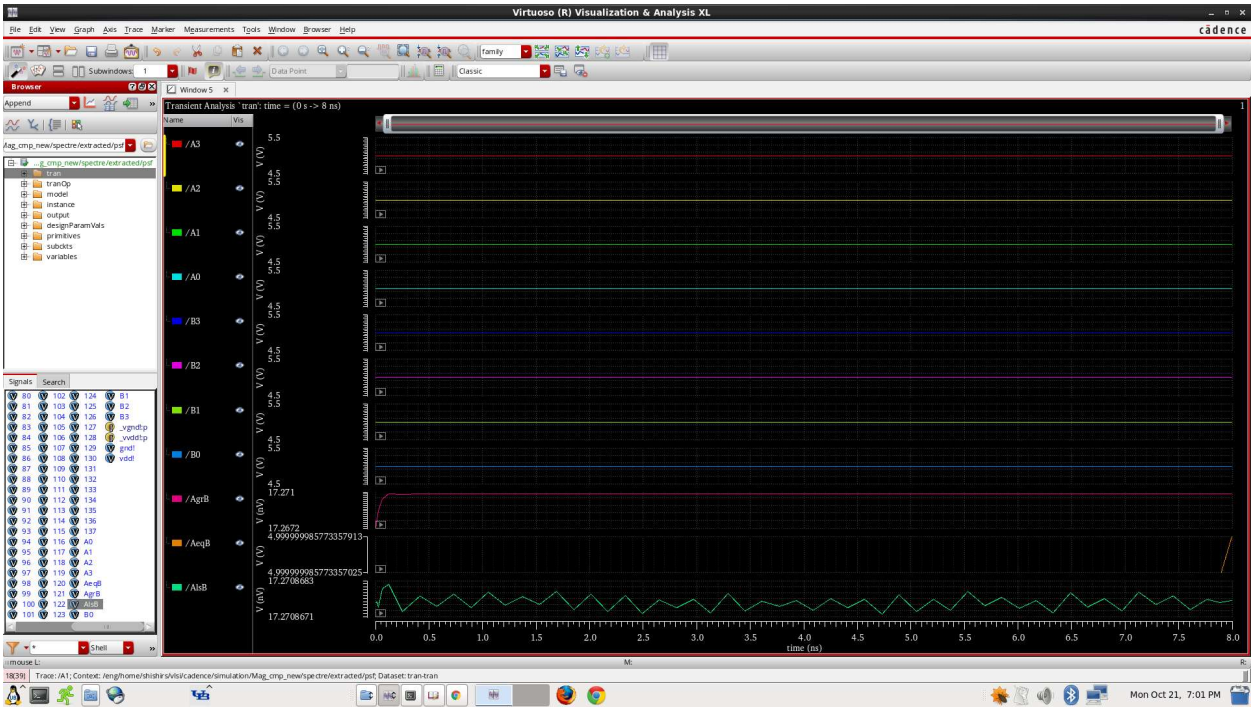


Extracted View Simulation:

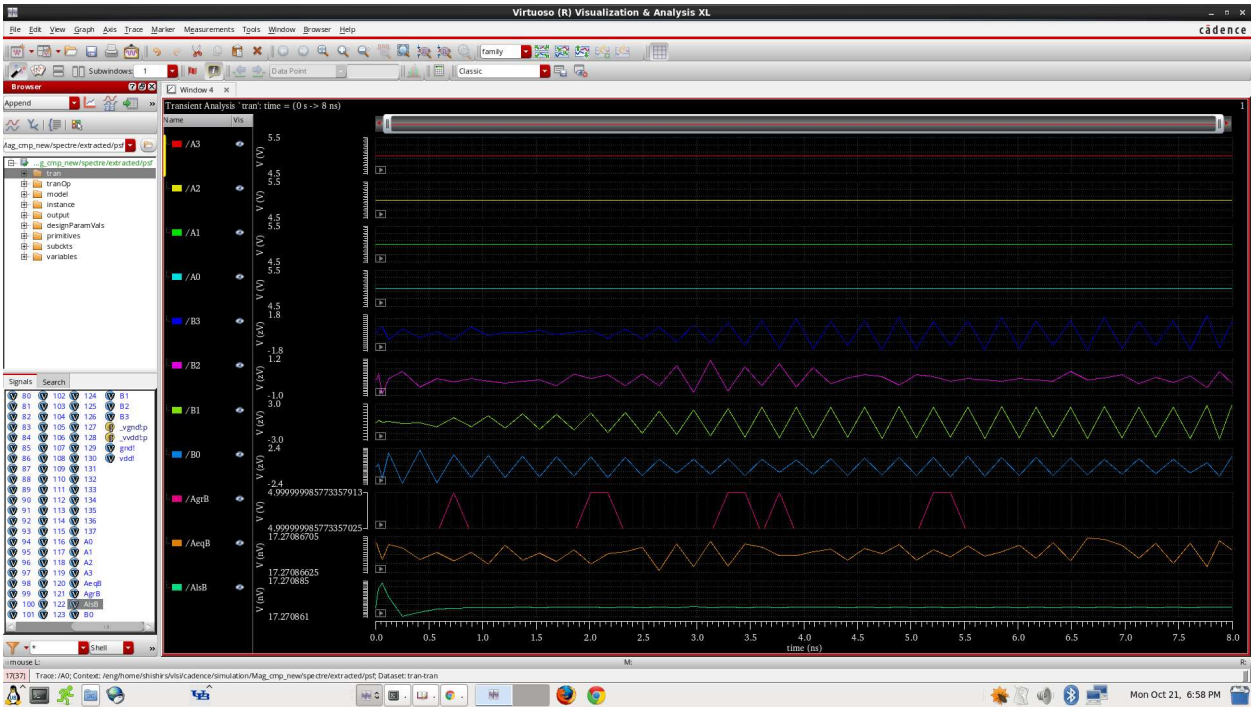
A is lesser than B(AlsB is high)



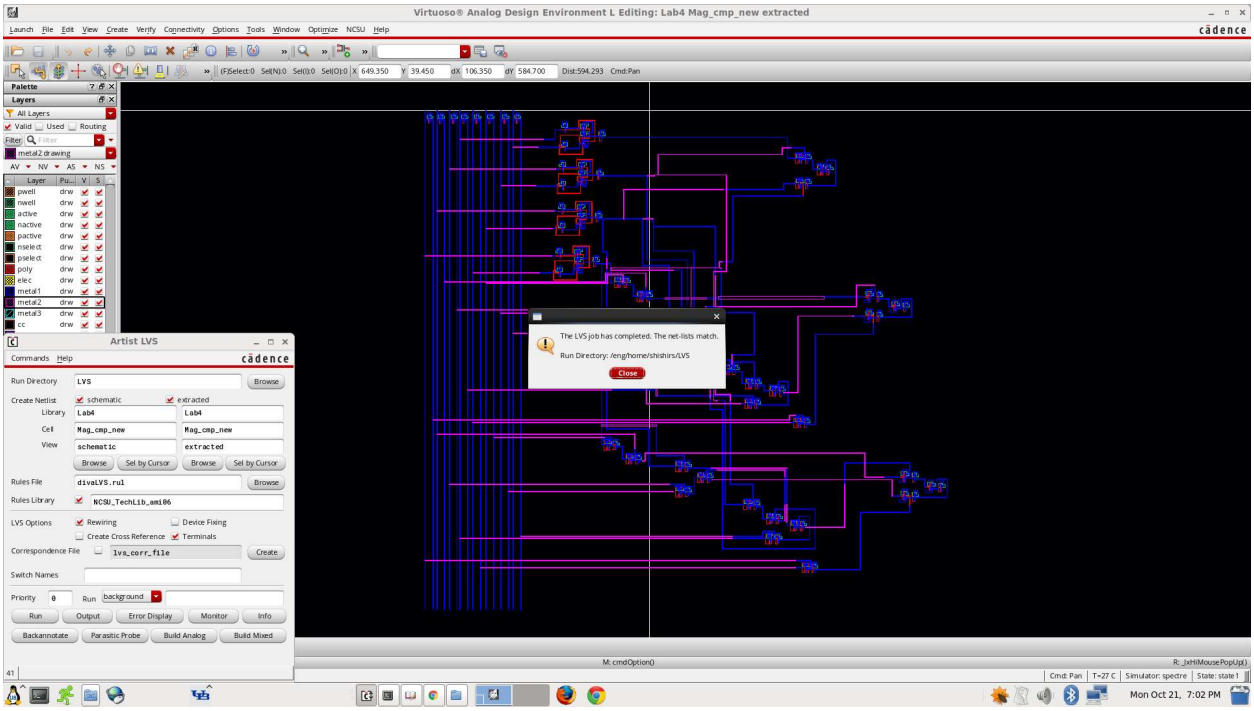
A equals B(AeqB is high)



A greater than B(AgrB is high)



LVS match between Layout and Extracted views:



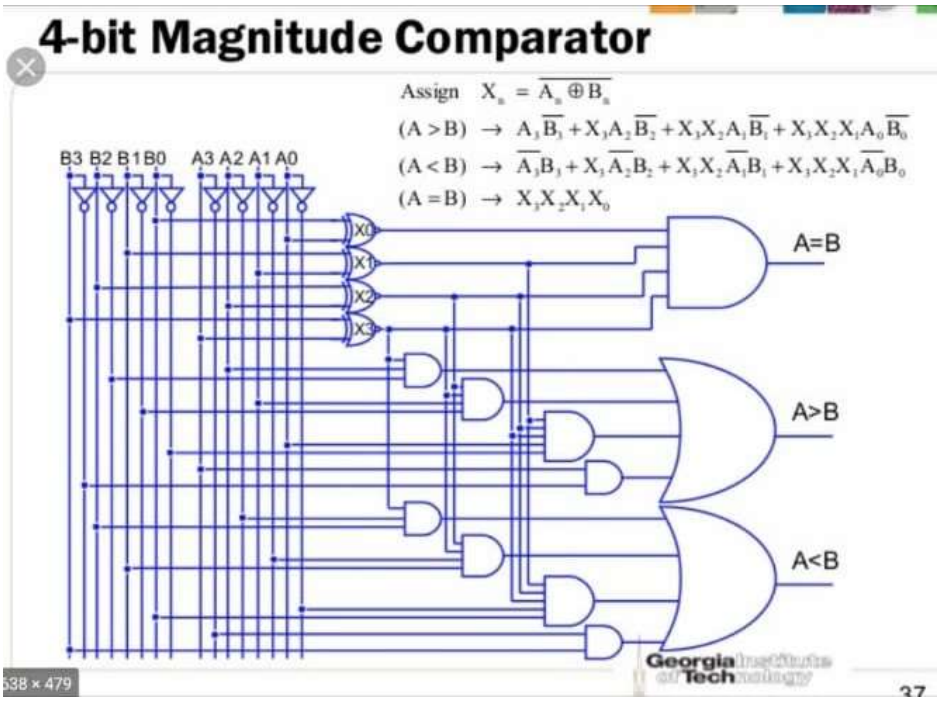
Truth Table:

A3	A2	A1	A0	B3	B2	B1	B0
0	1	0	1	0	0	0	0
0	0	1	1	0	0	1	1
0	0	0	0	0	1	1	0
1	1	1	1	1	1	1	1

Working of circuit:

- A Comparator is a digital circuit that takes two binary numbers and compares their values
- It outputs values as to whether A is greater than B, A is equal to B or A is lesser than B
- It is an important component of processors
- It is made using a combination of multi-input gates including 3,4 and 5 input versions of AND gate and 4 input version of OR gate
- Based on one of the conditions that have been achieved in output, an operation can be set to be performed. This is a useful application of the magnitude comparator

Circuit Diagram:



Inference and Conclusion:

- The working of magnitude comparator was learnt using circuit design techniques
- The schematic and Layout versions of the gates were implemented in the form of circuits in Cadence
- The correctness of the circuit design was verified using simulation tools and output was recorded
- LVS (Layout vs Schematic) check was obtained to verify that both versions of the gate matched