Lab 1: Implementation of Basic Logic Gates

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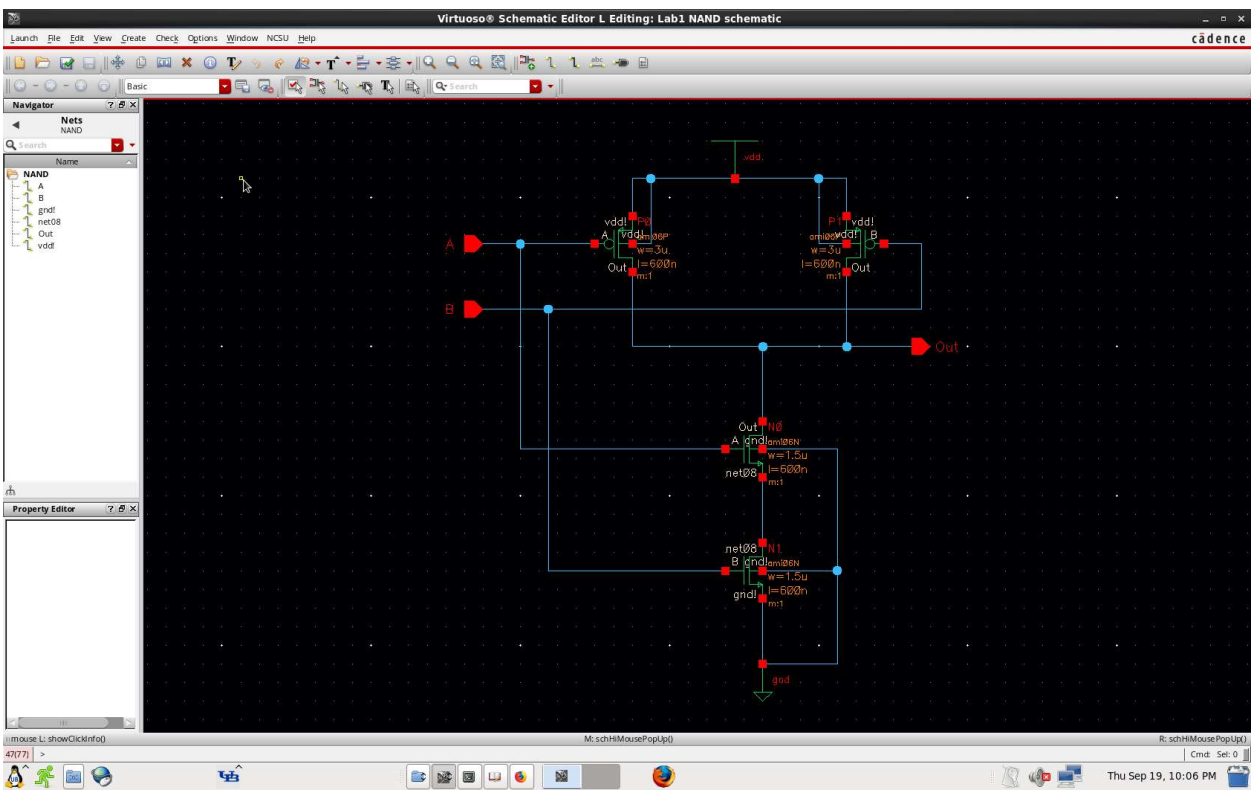
Objective:

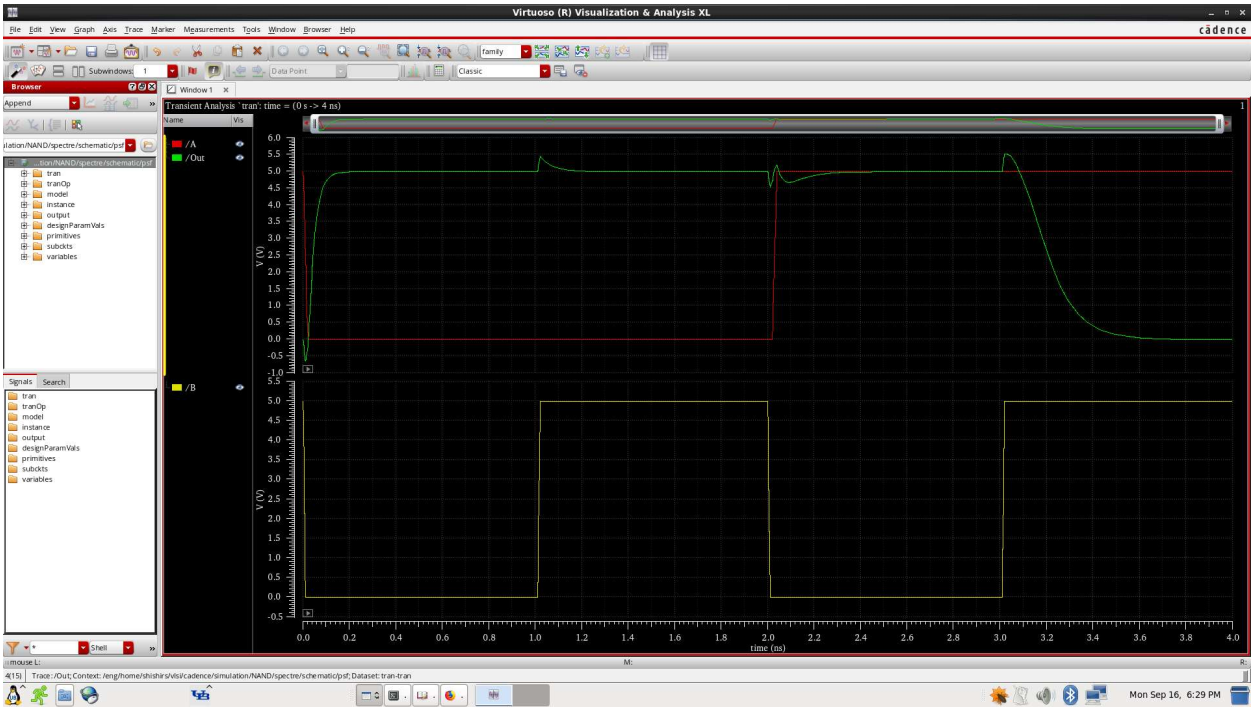
- To understand the working and design of basic digital logic gates
- To implement their schematic and layout versions using Cadence
- Prepare a report to summarize the results of the lab activity

NAND:

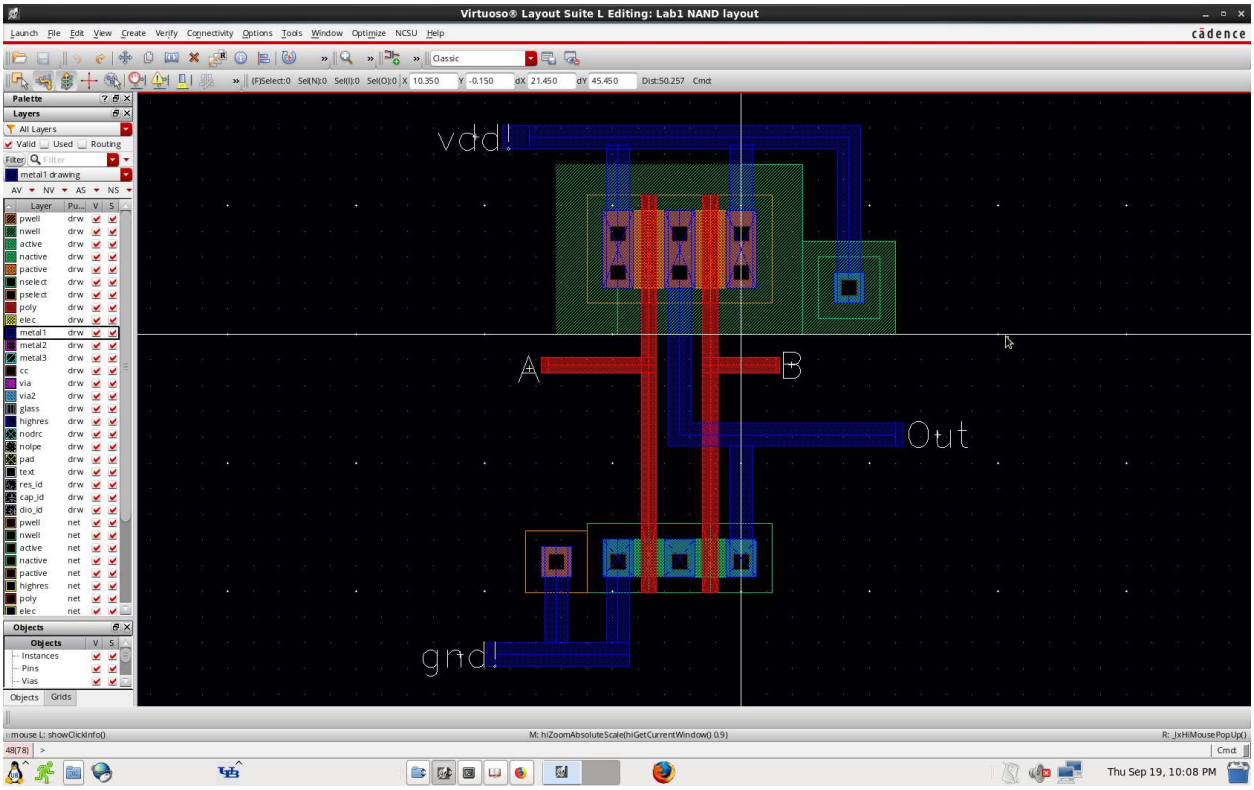
Schematic View:



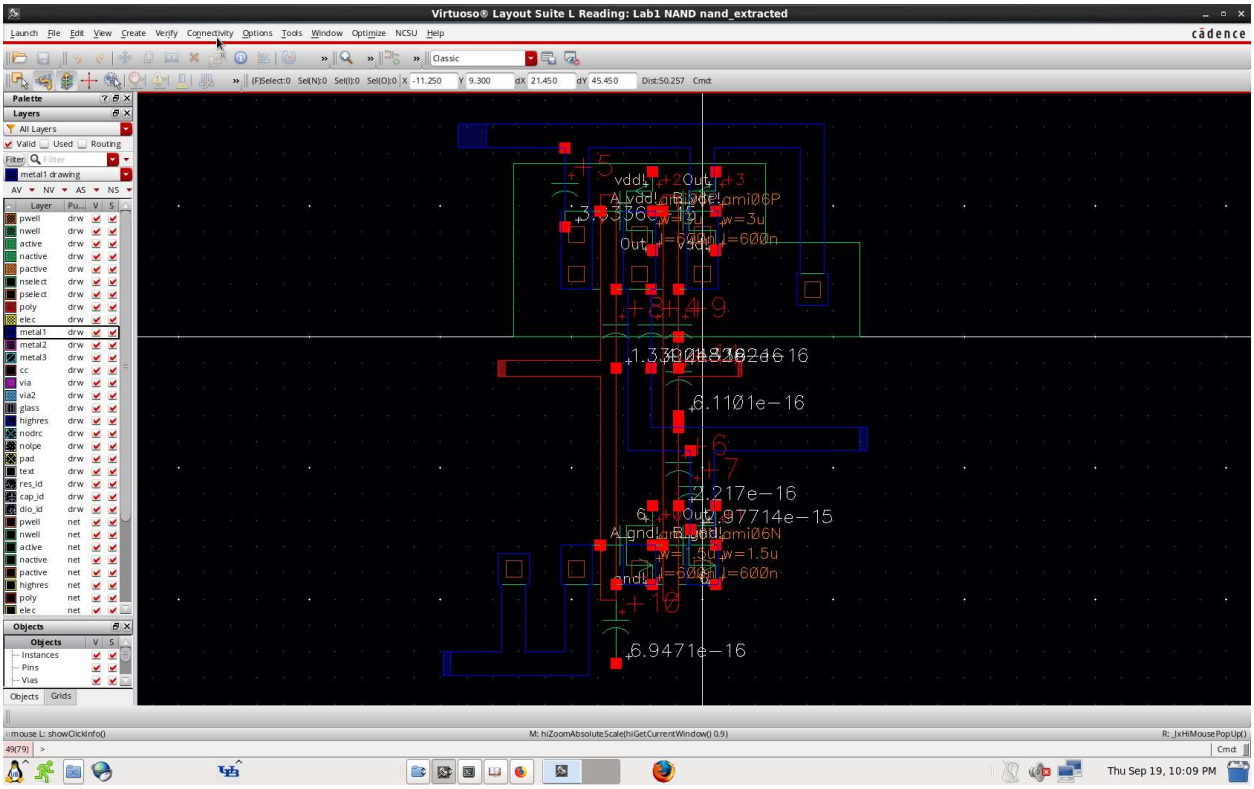
Schematic View Simulation:



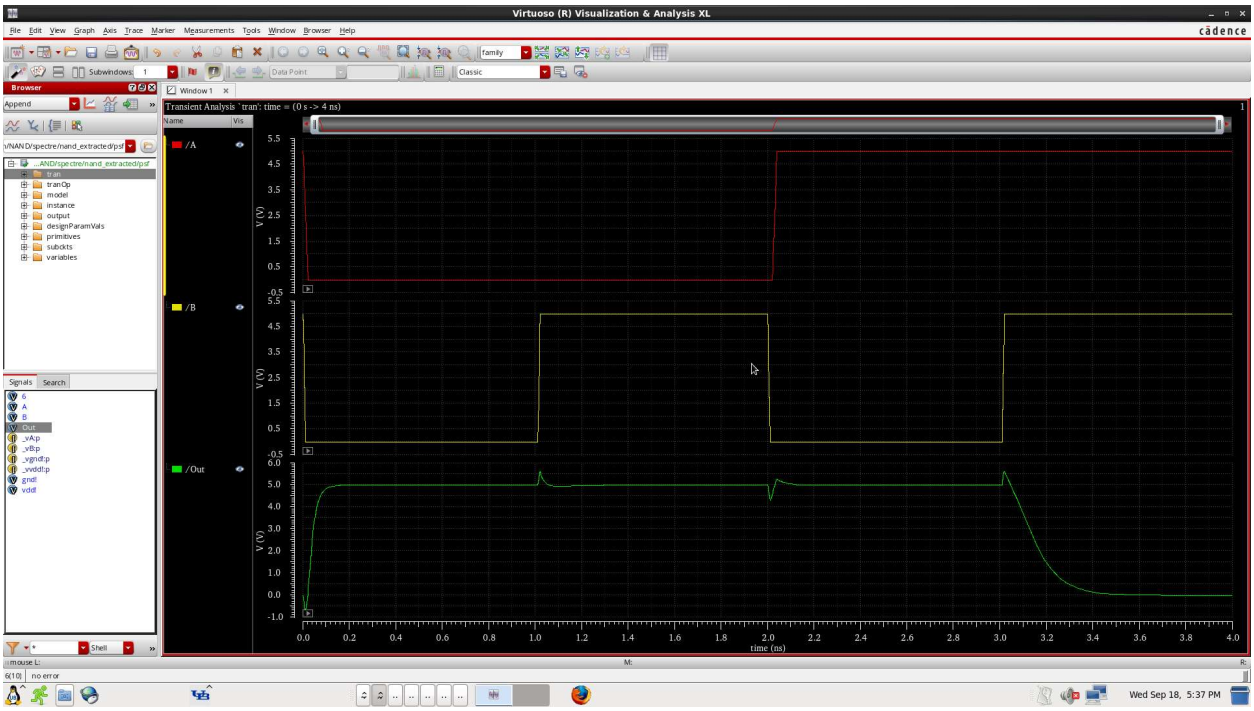
Layout View:



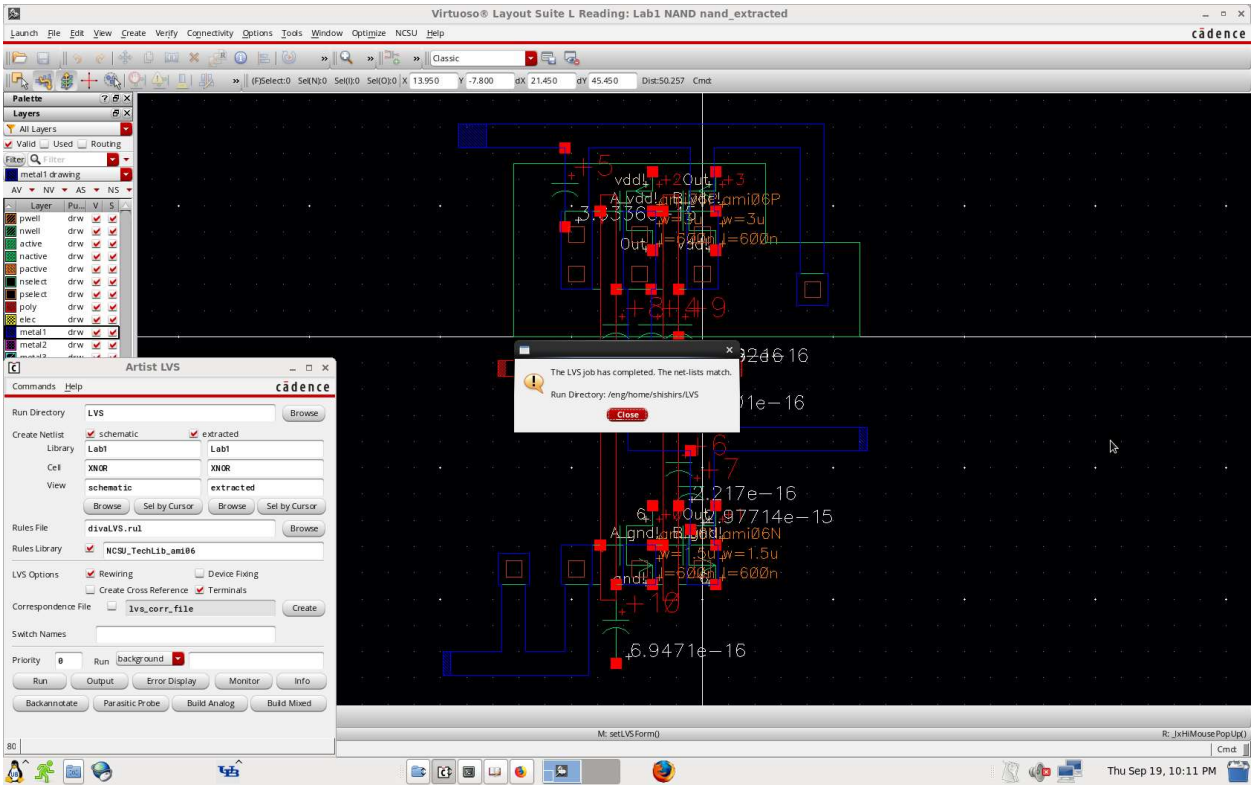
Extracted View:



Extracted View Simulation:



LVS Match between Schematic and Extracted Views:



Truth Table:

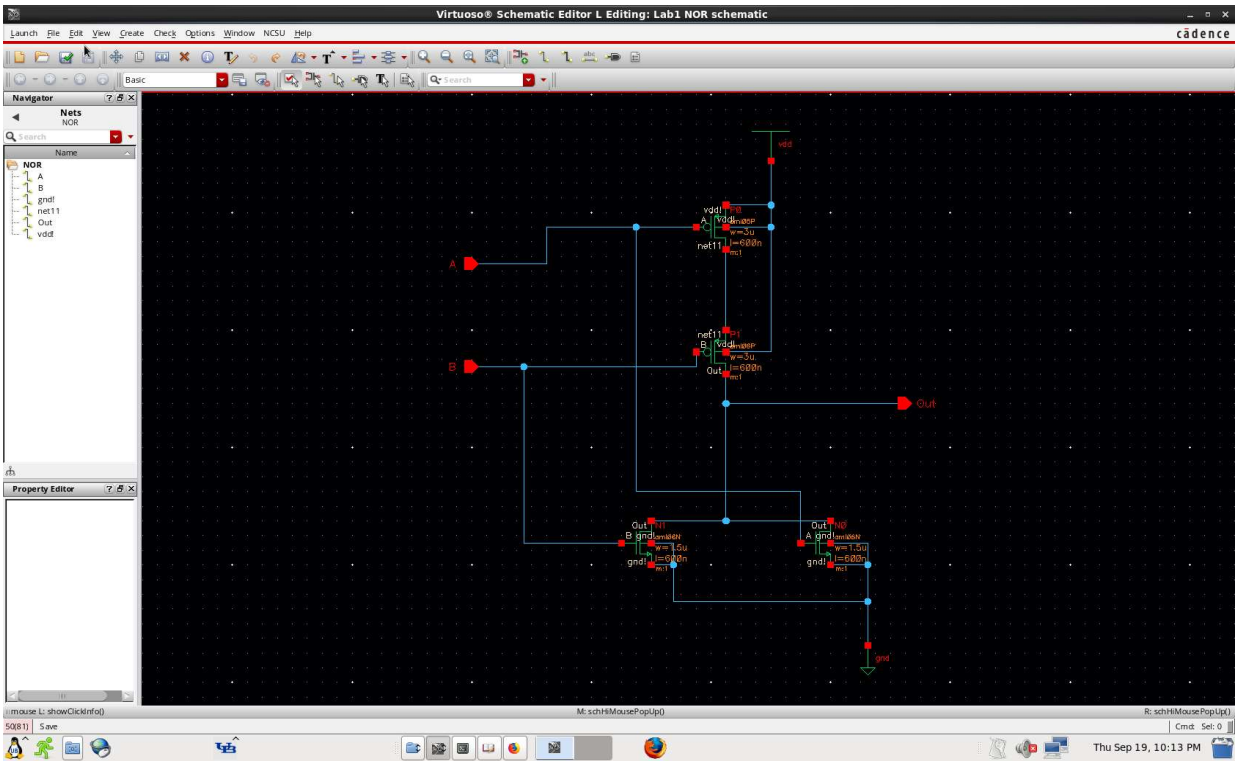
Input A	Input B	Output Q
0	0	1
0	1	1
1	0	1
1	1	0

Working:

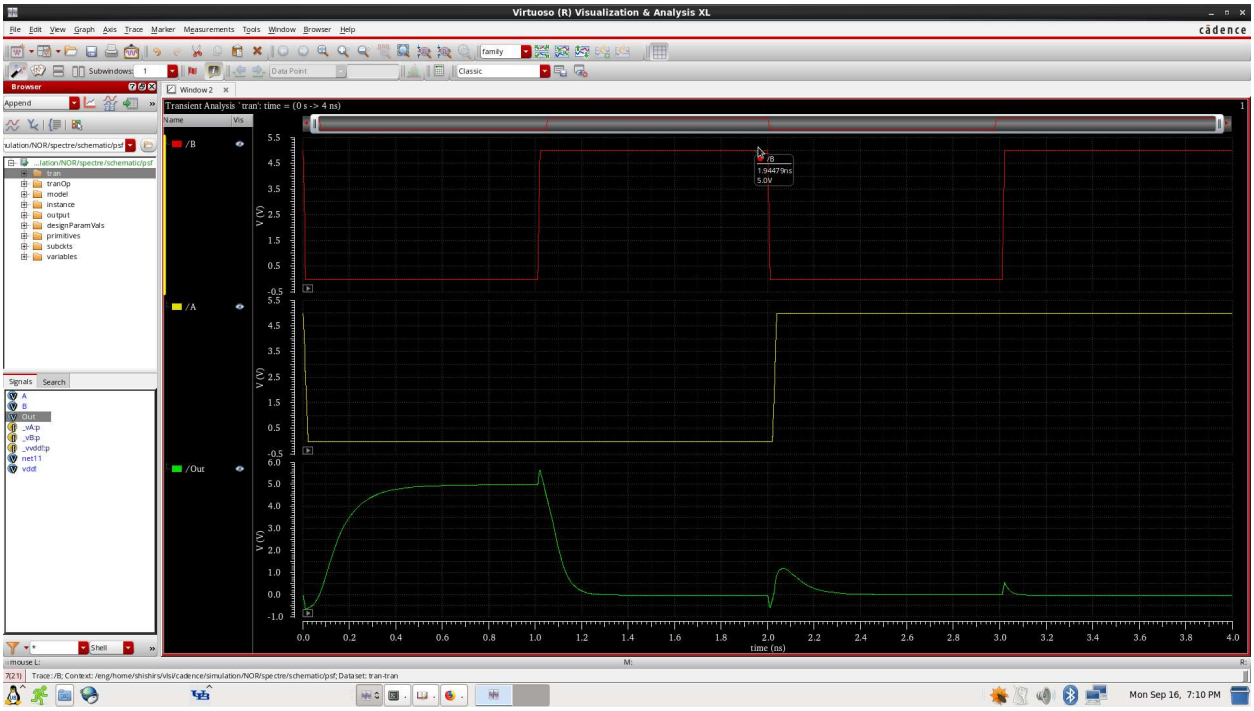
- NAND gate is an AND gate whose output is inverted
- If either input is not true, then Output for gate is True

NOR:

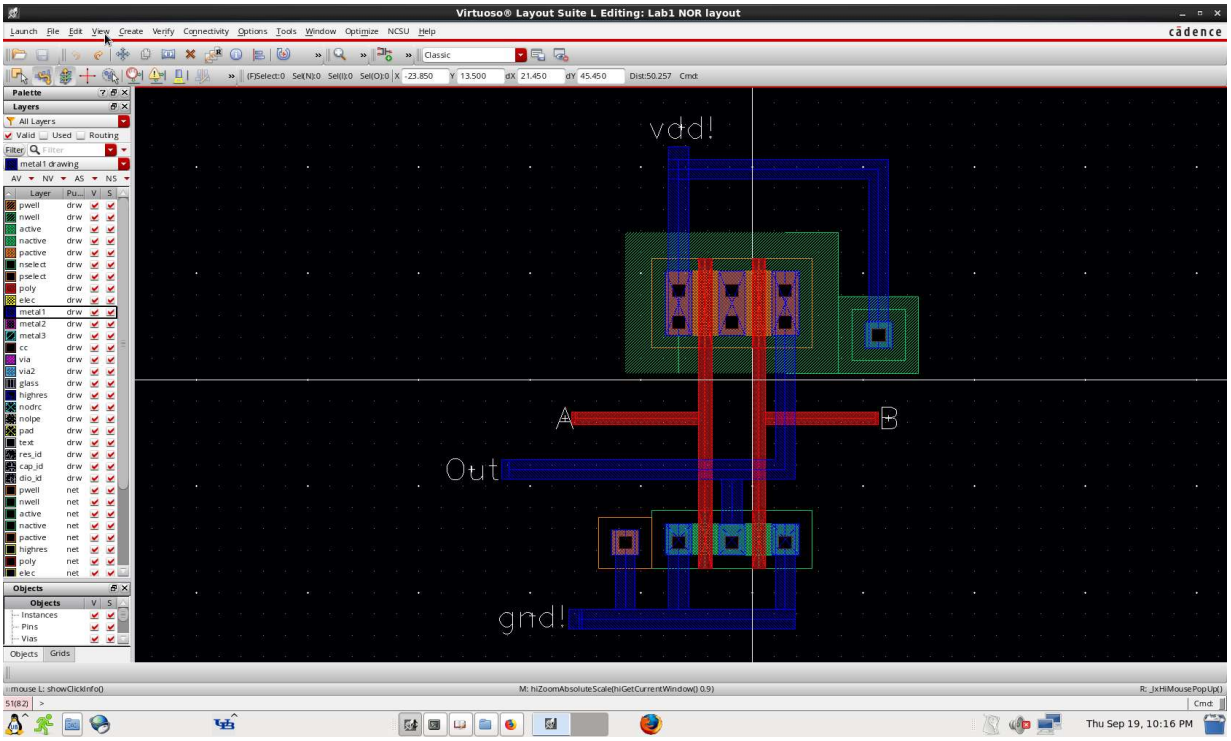
Schematic View:



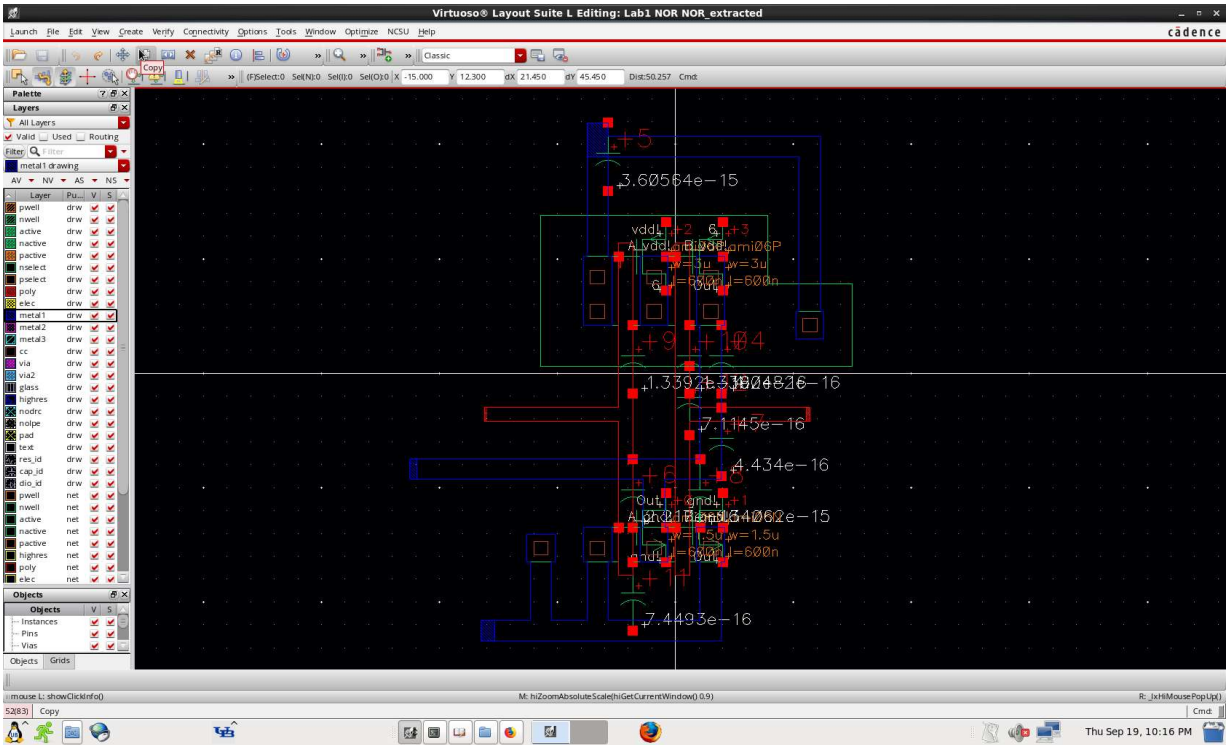
Schematic View Simulation:



Layout View:



Extracted View:



Extracted View Simulation:

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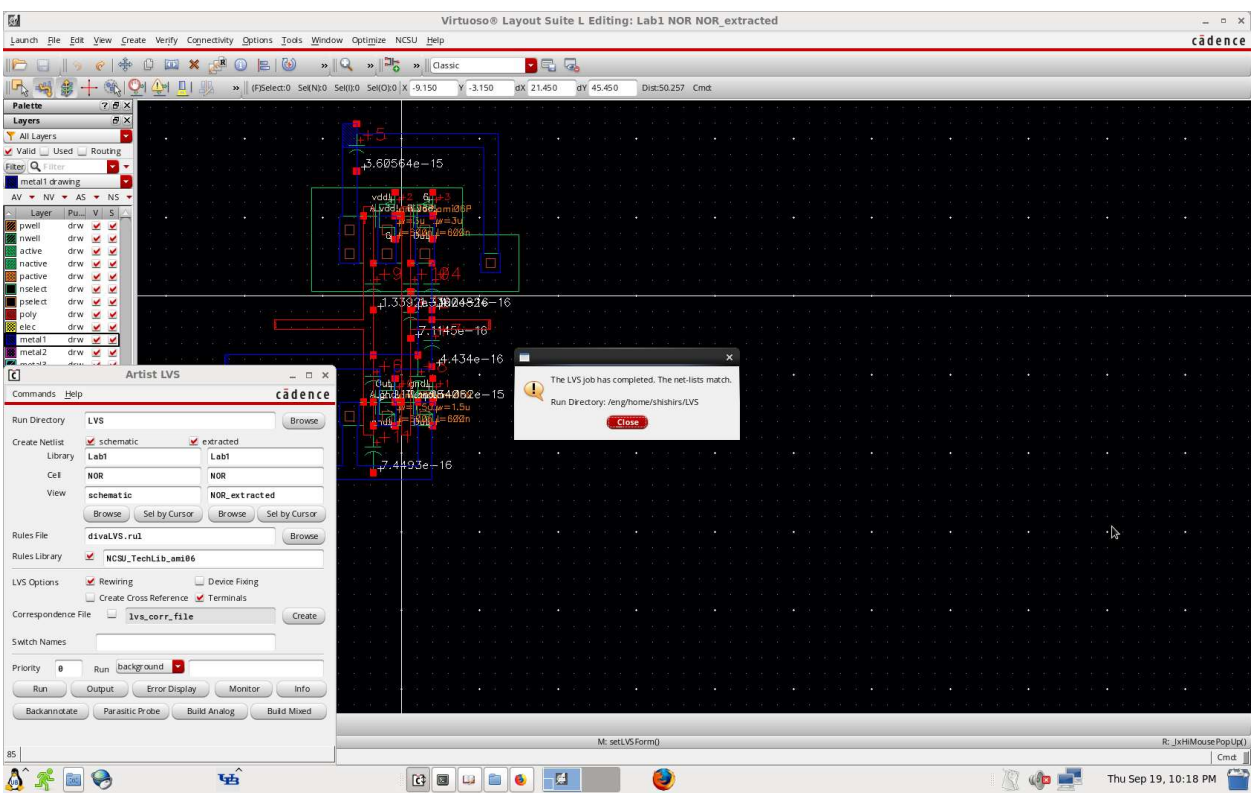


Truth Table:

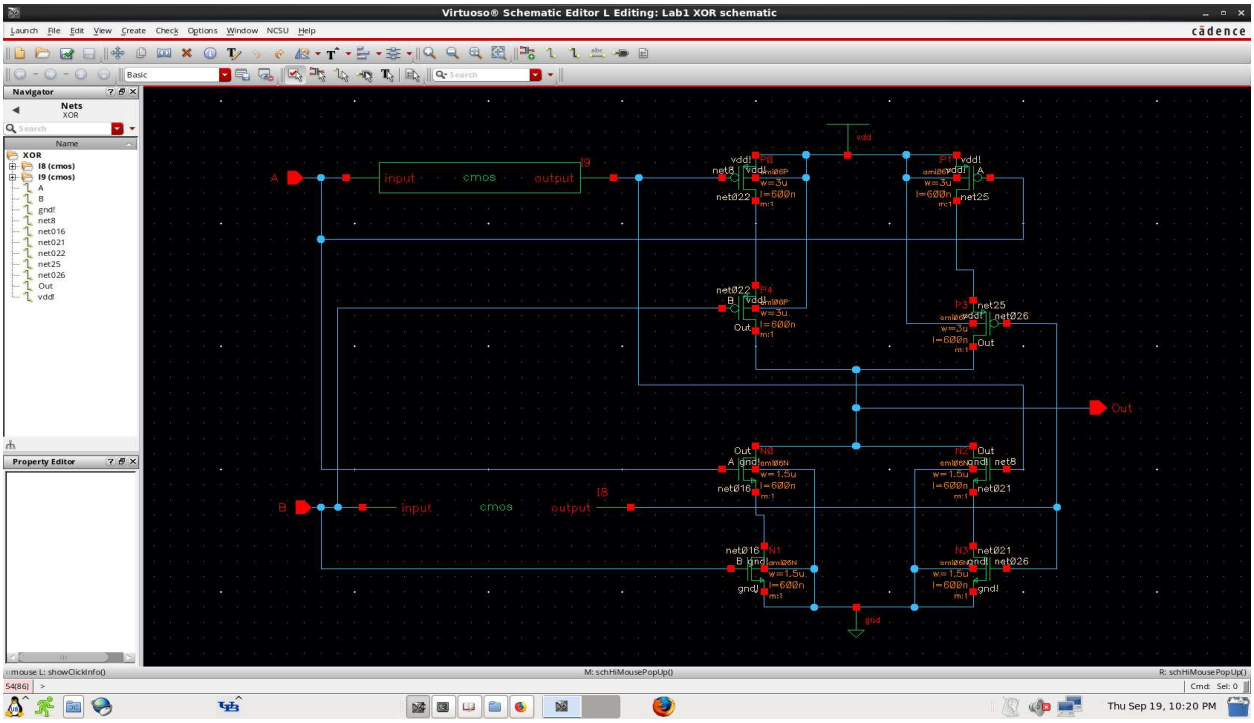
Input A	Input B	Output Q
0	0	1
0	1	0
1	0	0
1	1	0

Working:

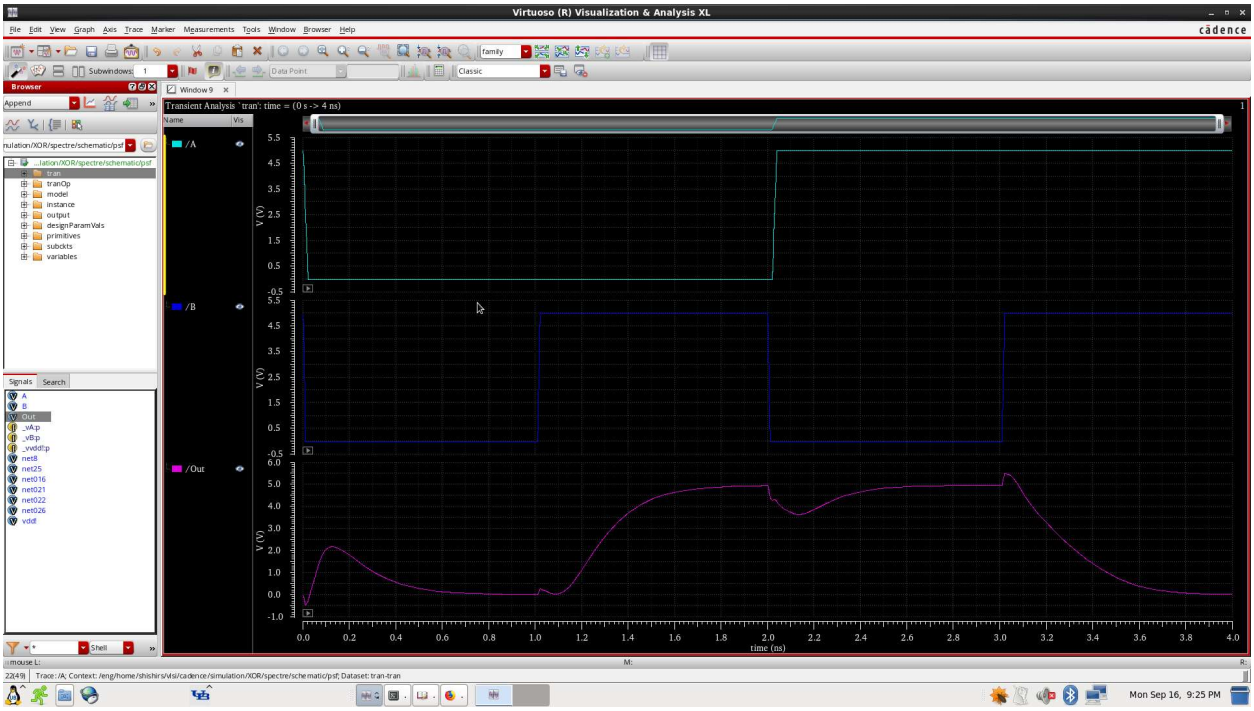
- NOR gate is an OR gate with its output inverted.
- If no inputs are true, then the output is true

XOR:

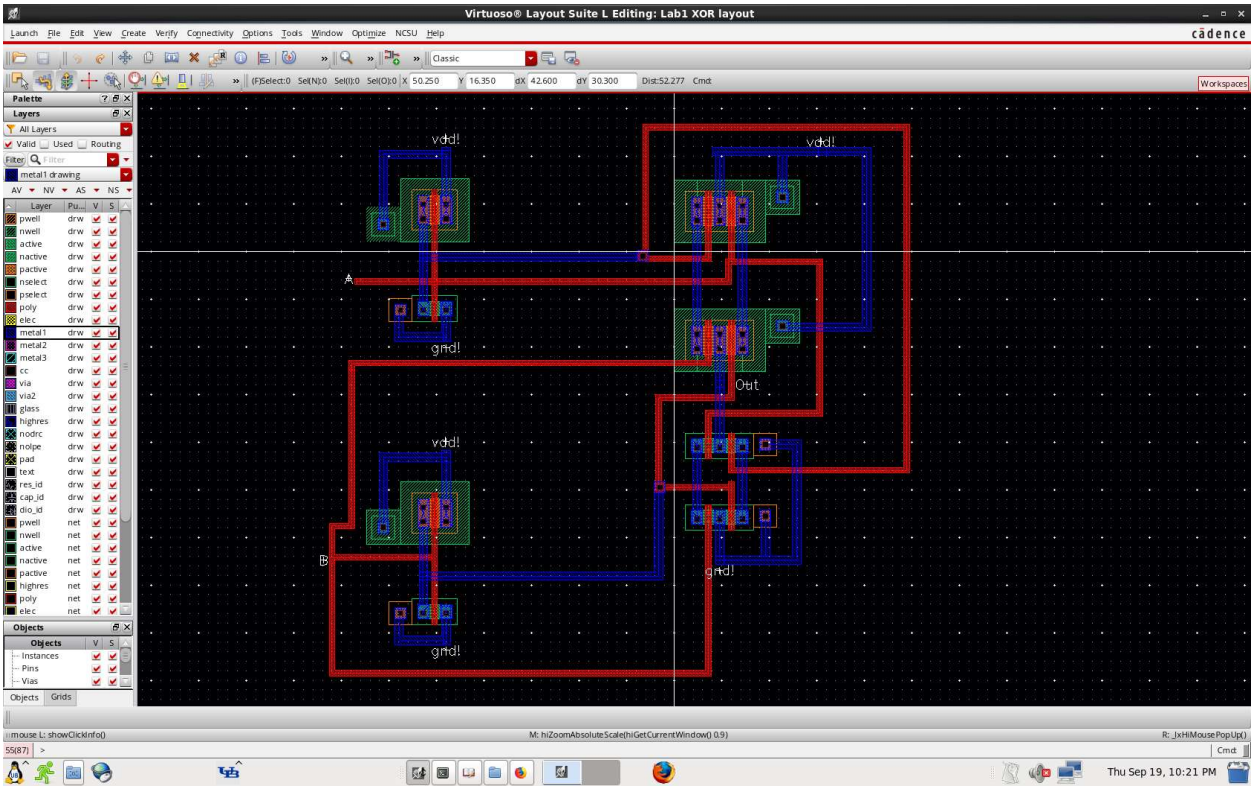
Schematic View:



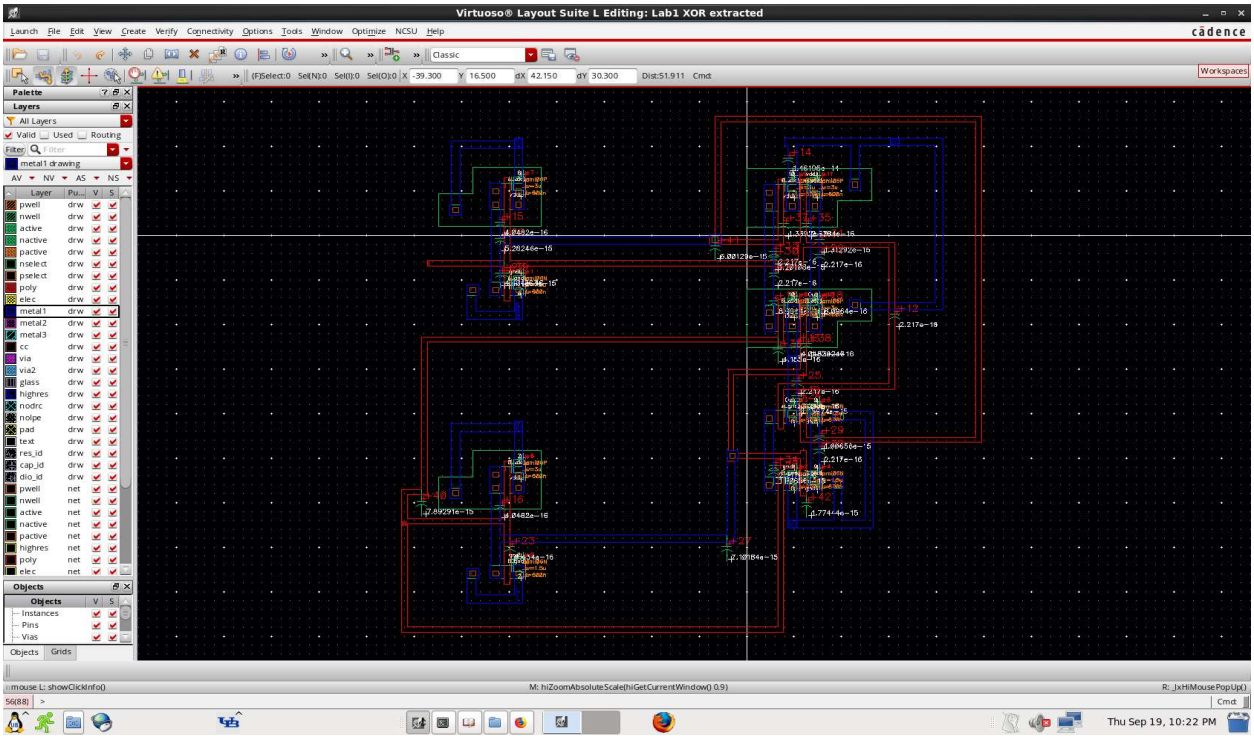
Schematic View Simulation:



Layout View:



Extracted View:



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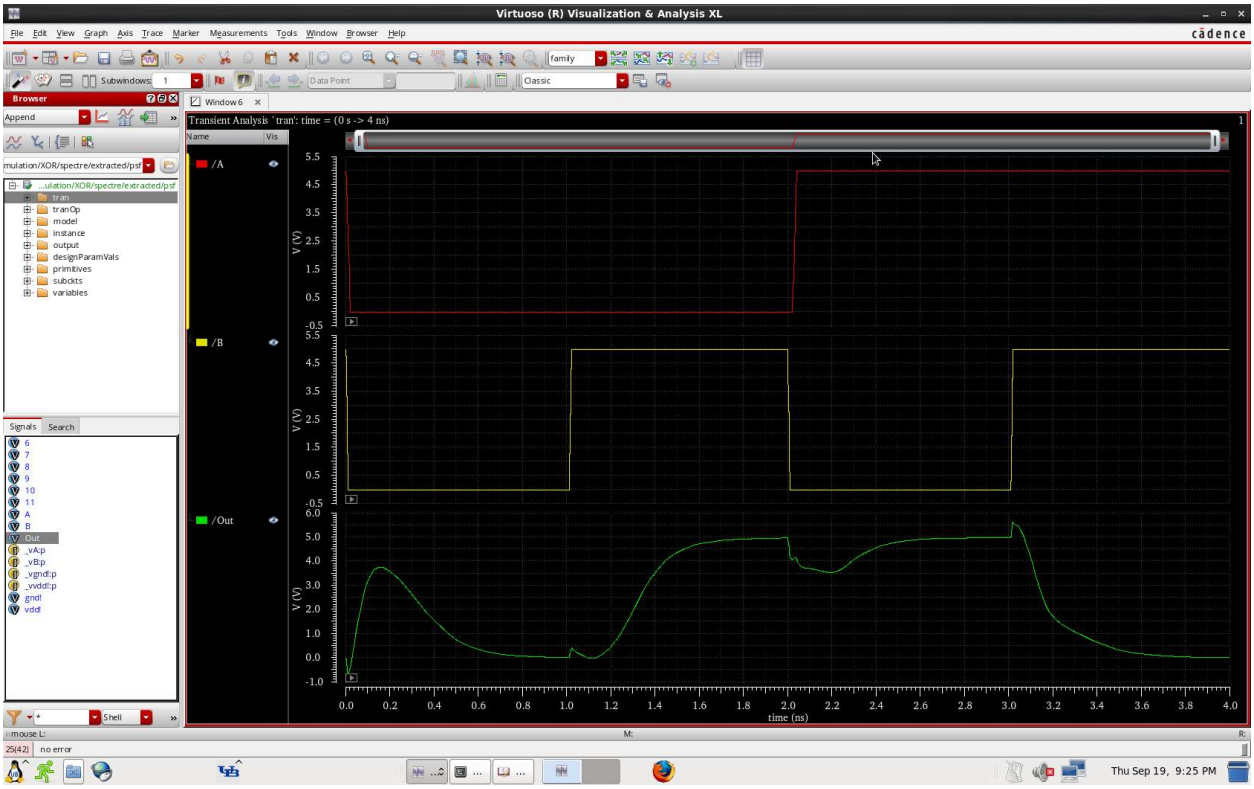
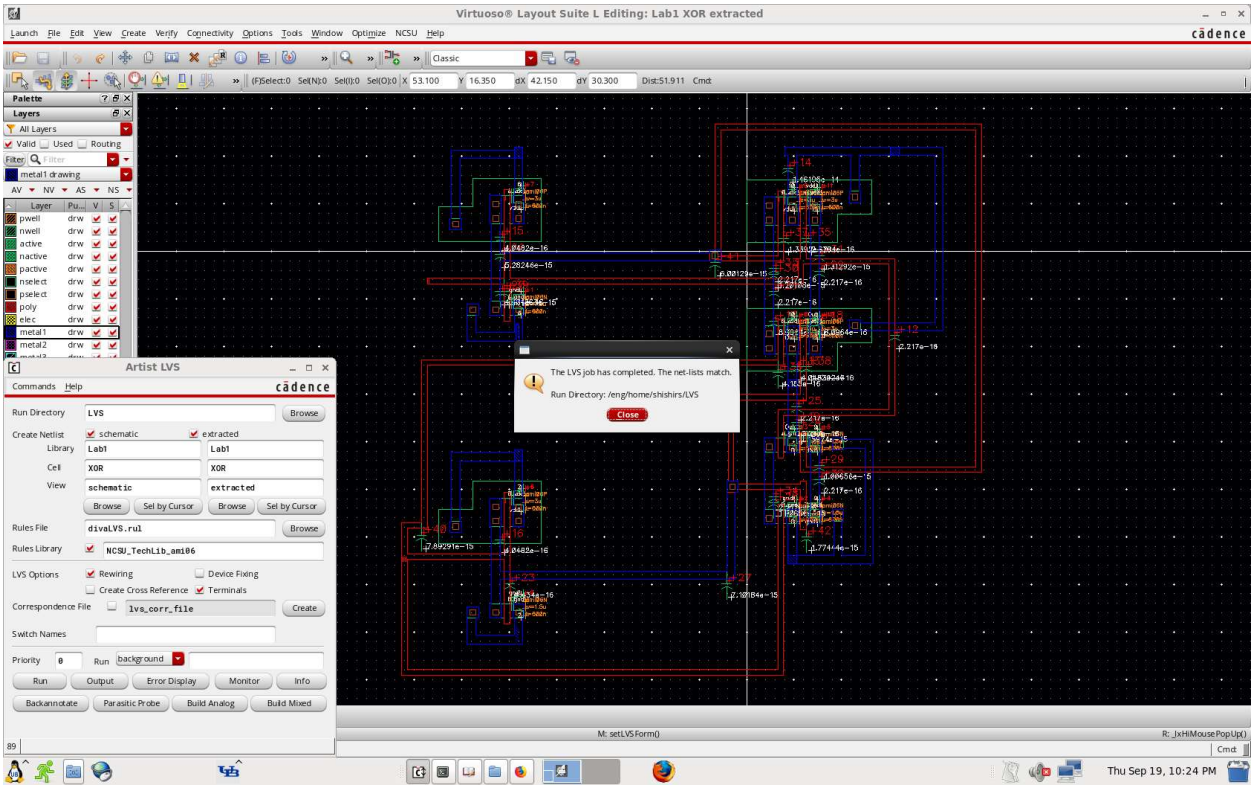


LVS Match between Schematic and Extracted Views:



Truth Table:

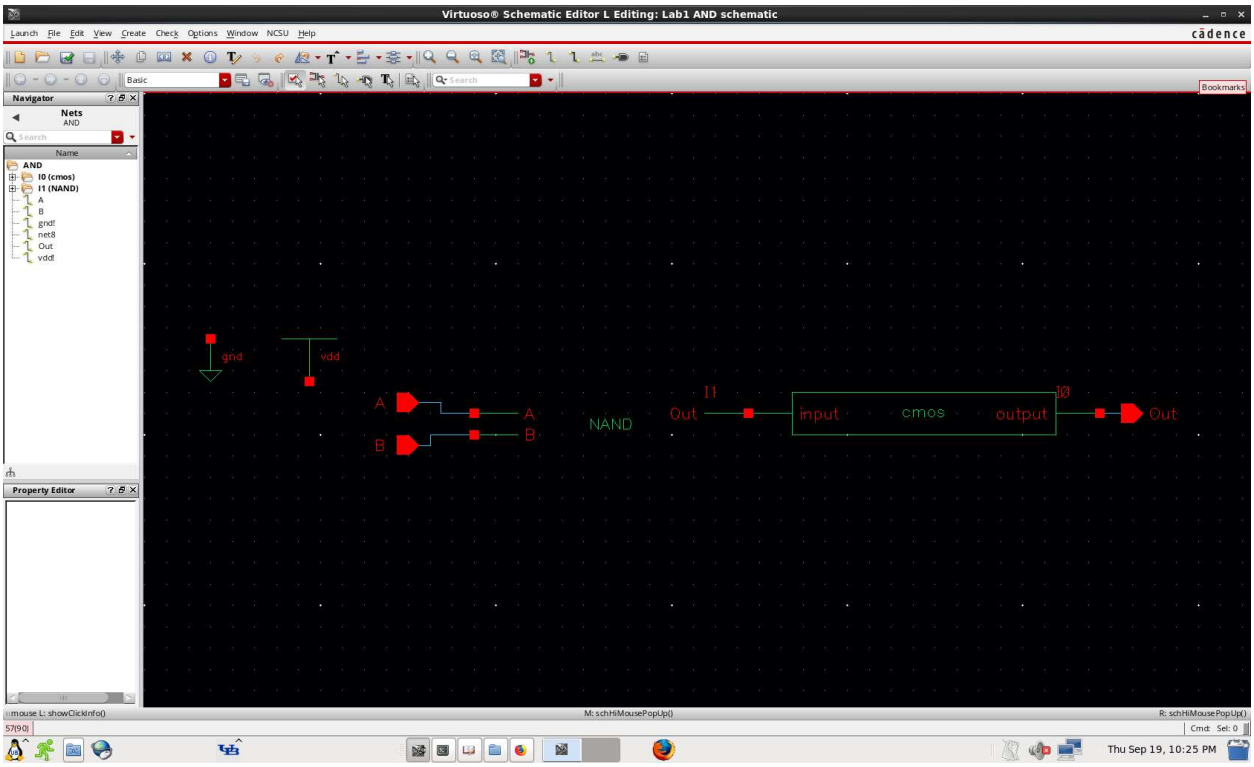
Input A	Input B	Output Q
0	0	0
0	1	1
1	0	1
1	1	0

Working:

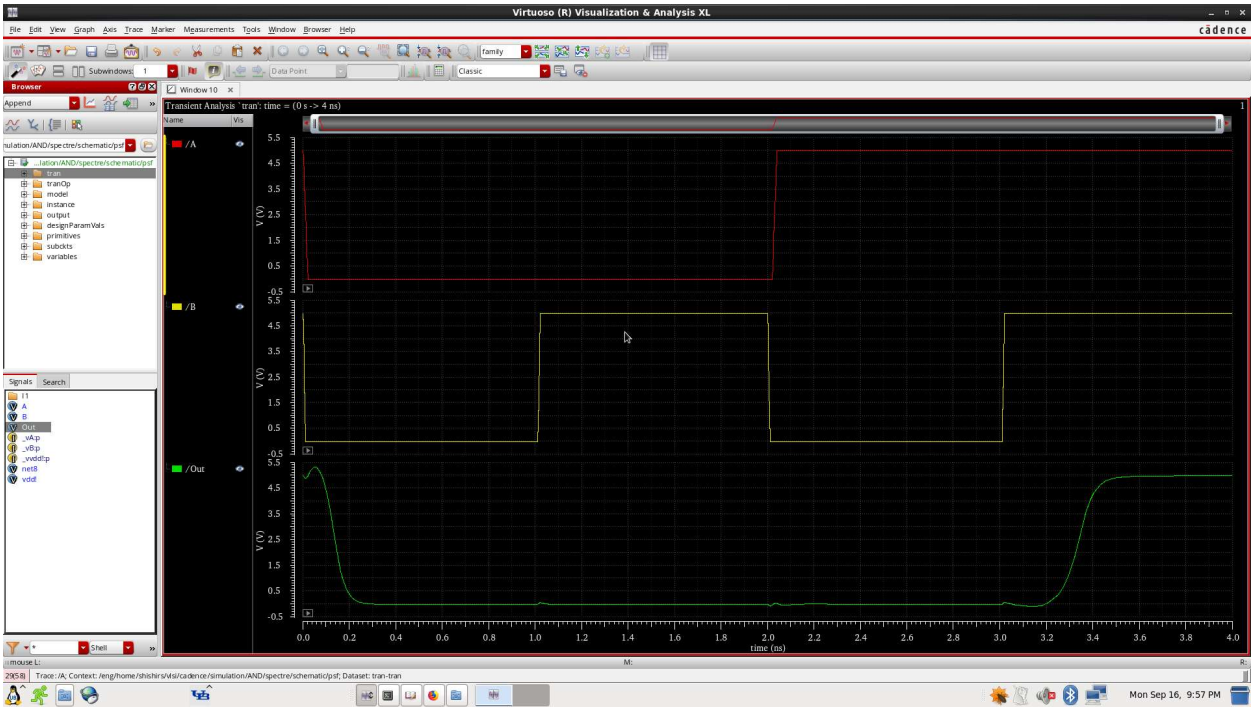
- Exclusive OR gate whose output is true only when both inputs are different from each other

AND:

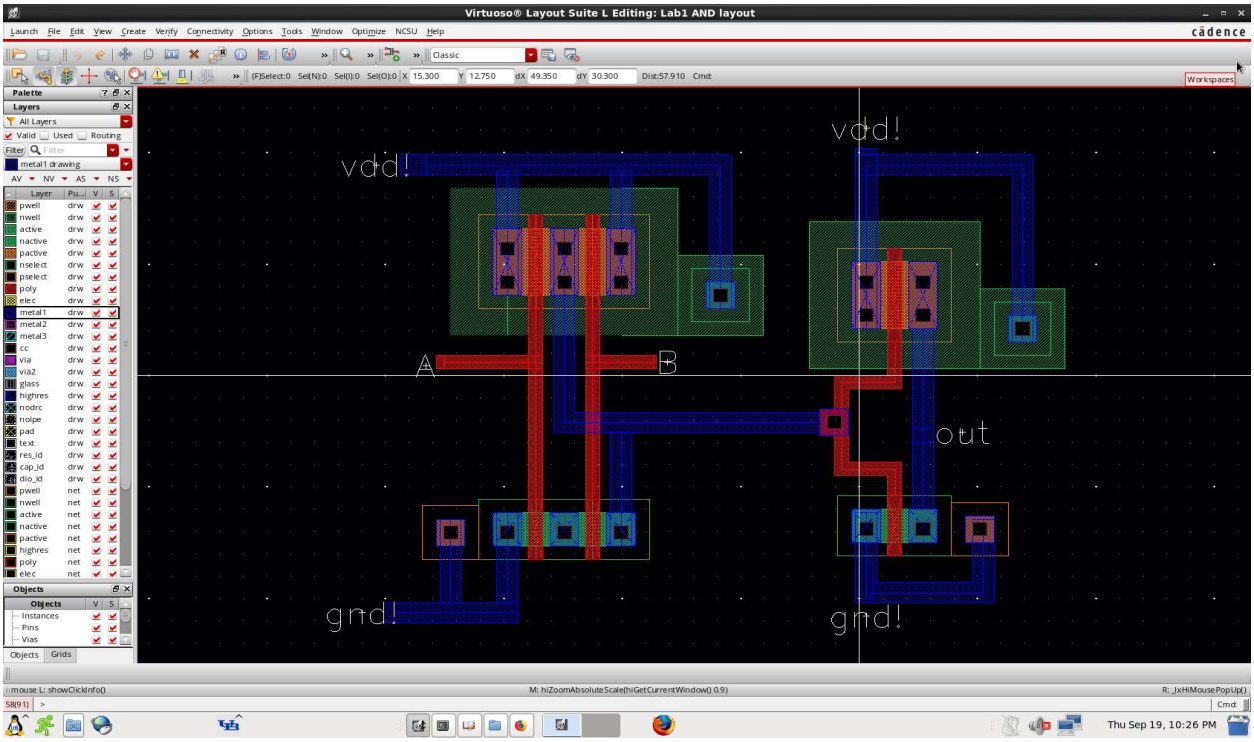
Schematic View:



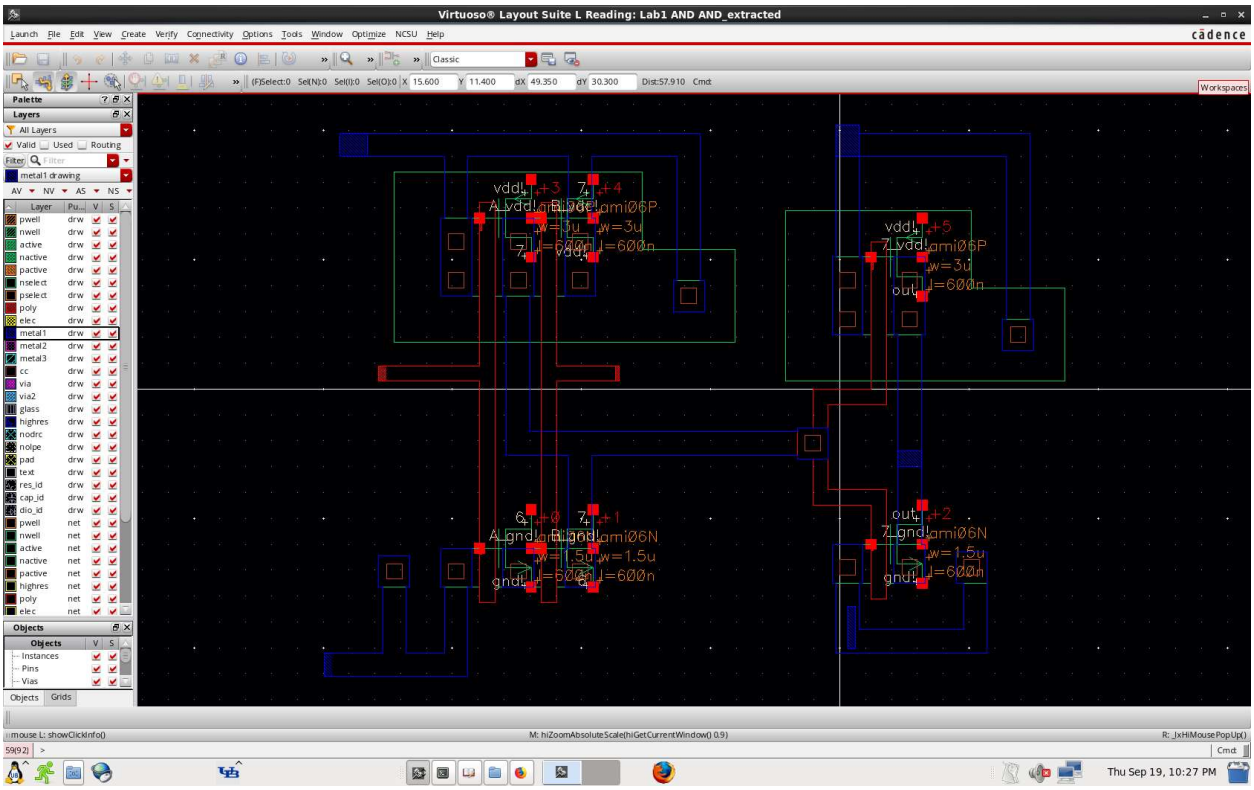
Schematic View Simulation:



Layout View:

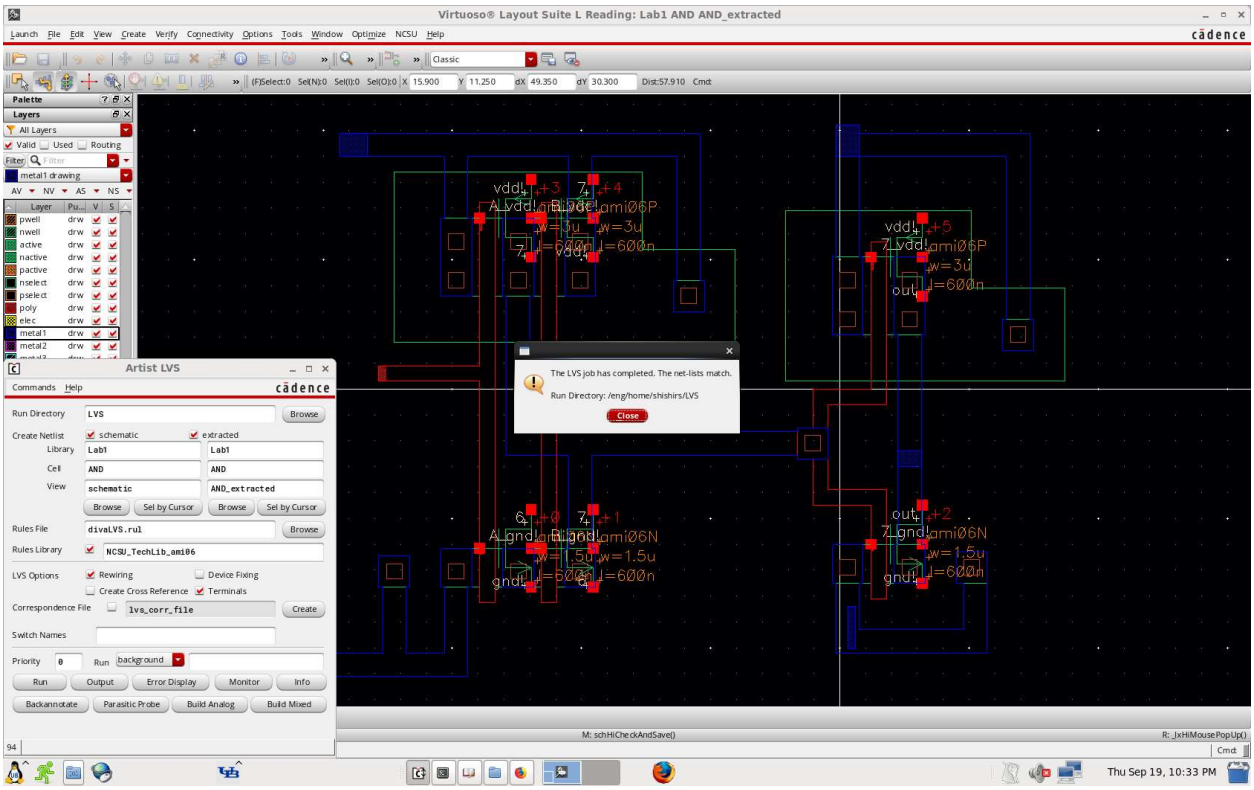


Extracted View:



Extracted View Simulation:

LVS Match between Schematic and Extracted Views:



Truth Table:

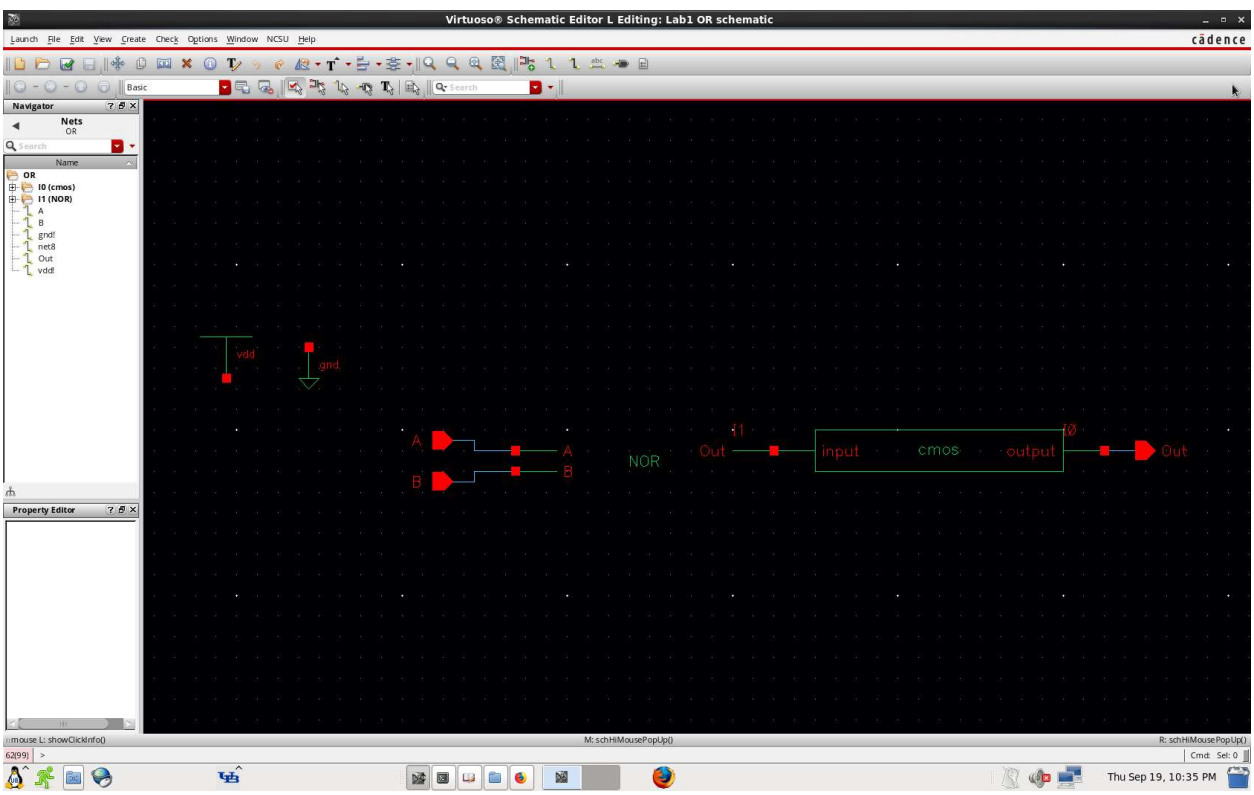
Input A	Input B	Output Q
0	0	0
0	1	0
1	0	0
1	1	1

Working:

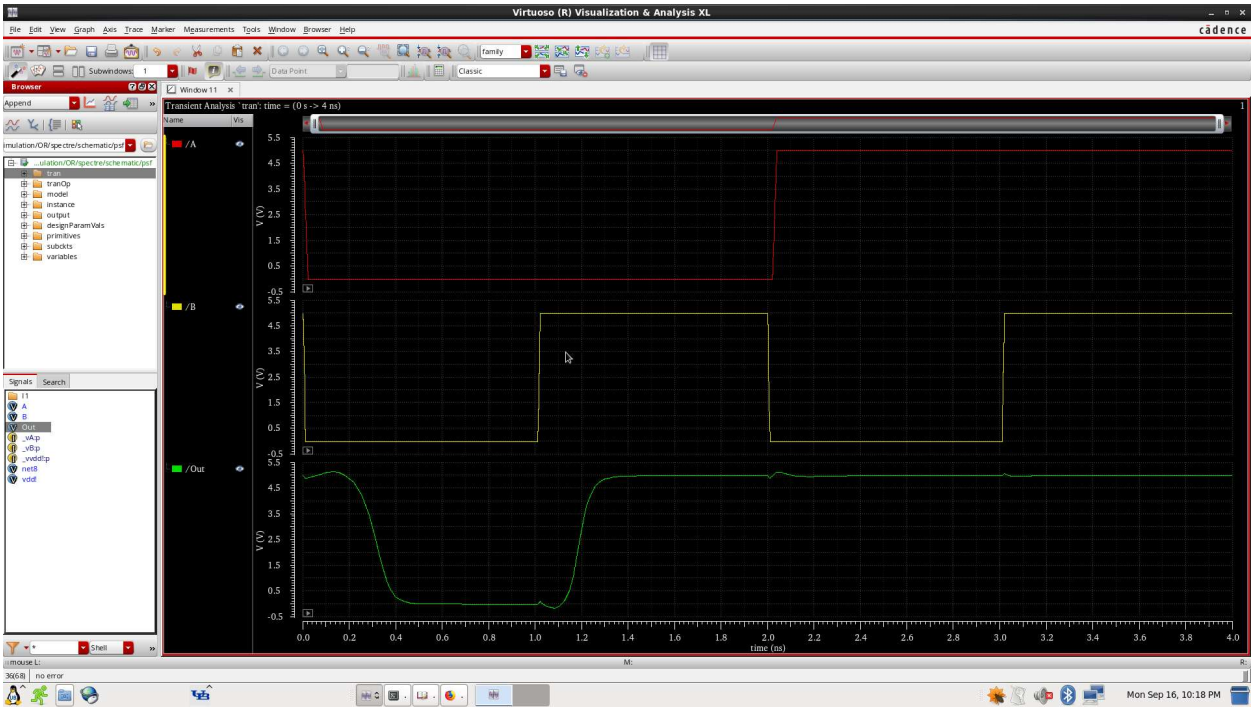
- The AND gate produces an output of true if ALL the inputs are true

OR:

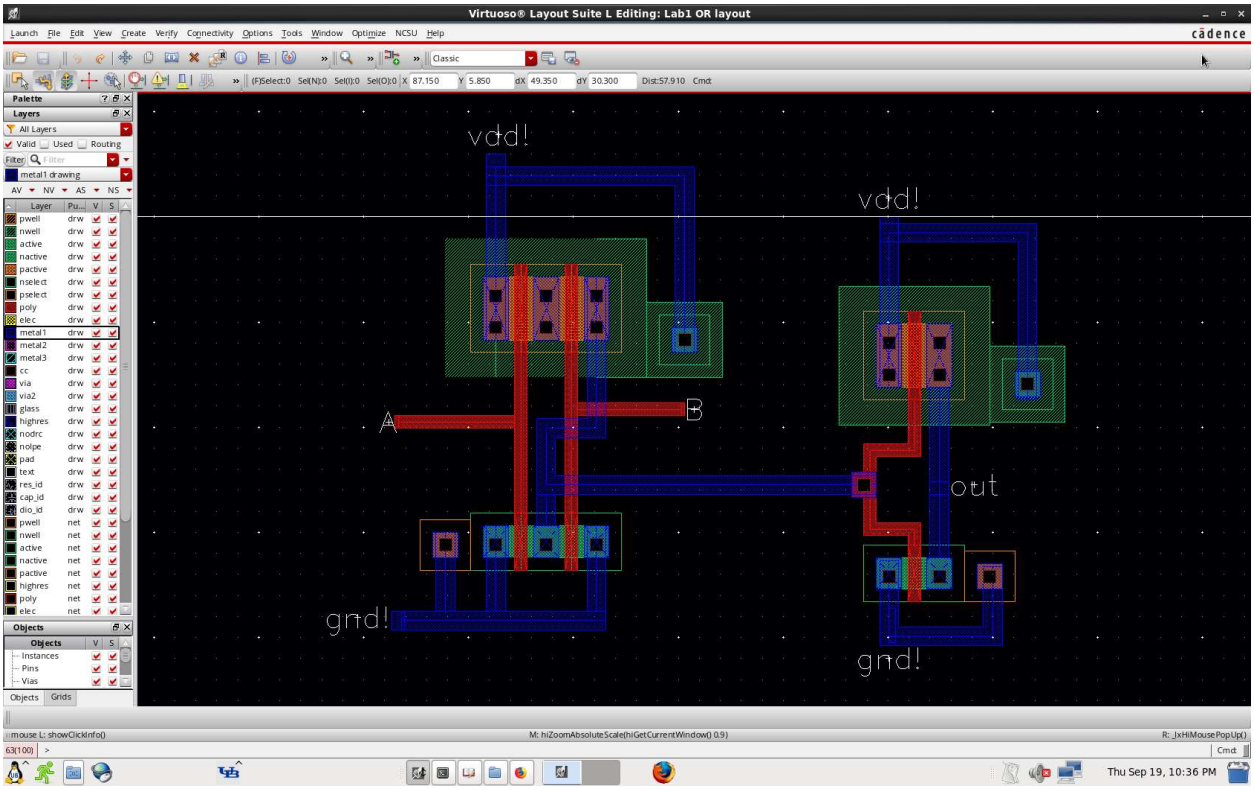
Schematic View:



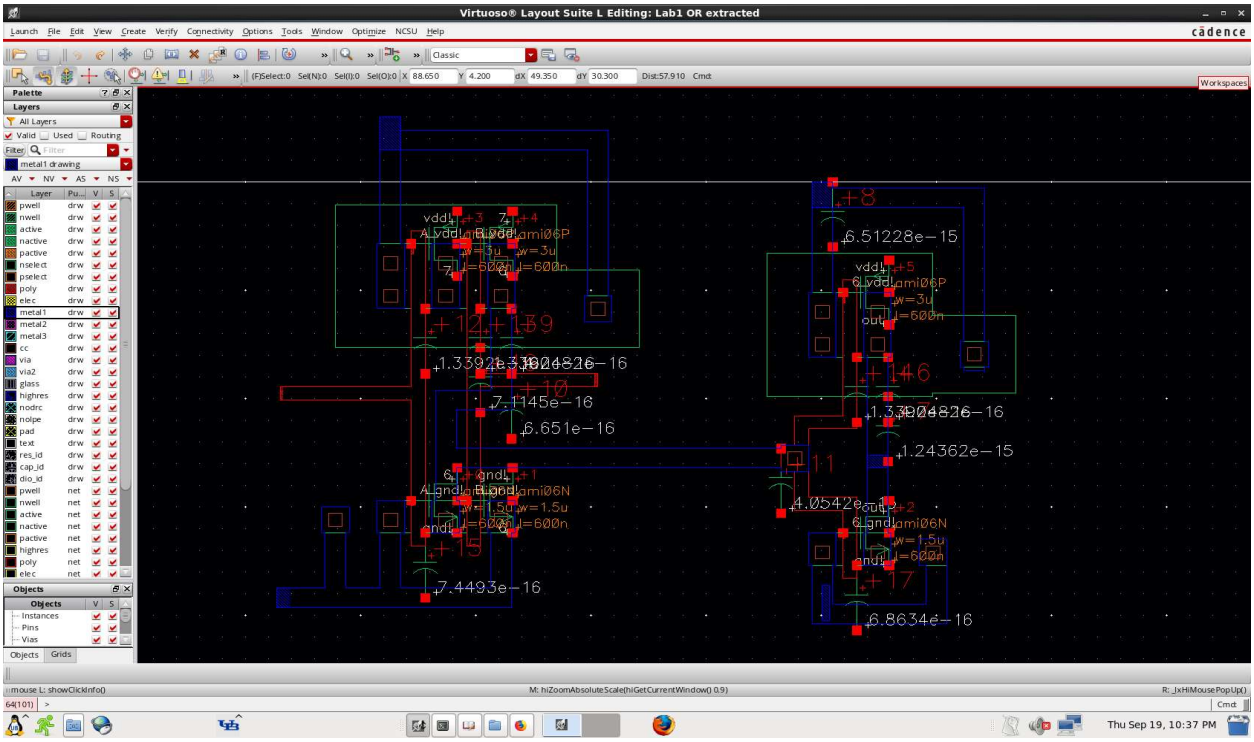
Schematic View Simulation:



Layout View:

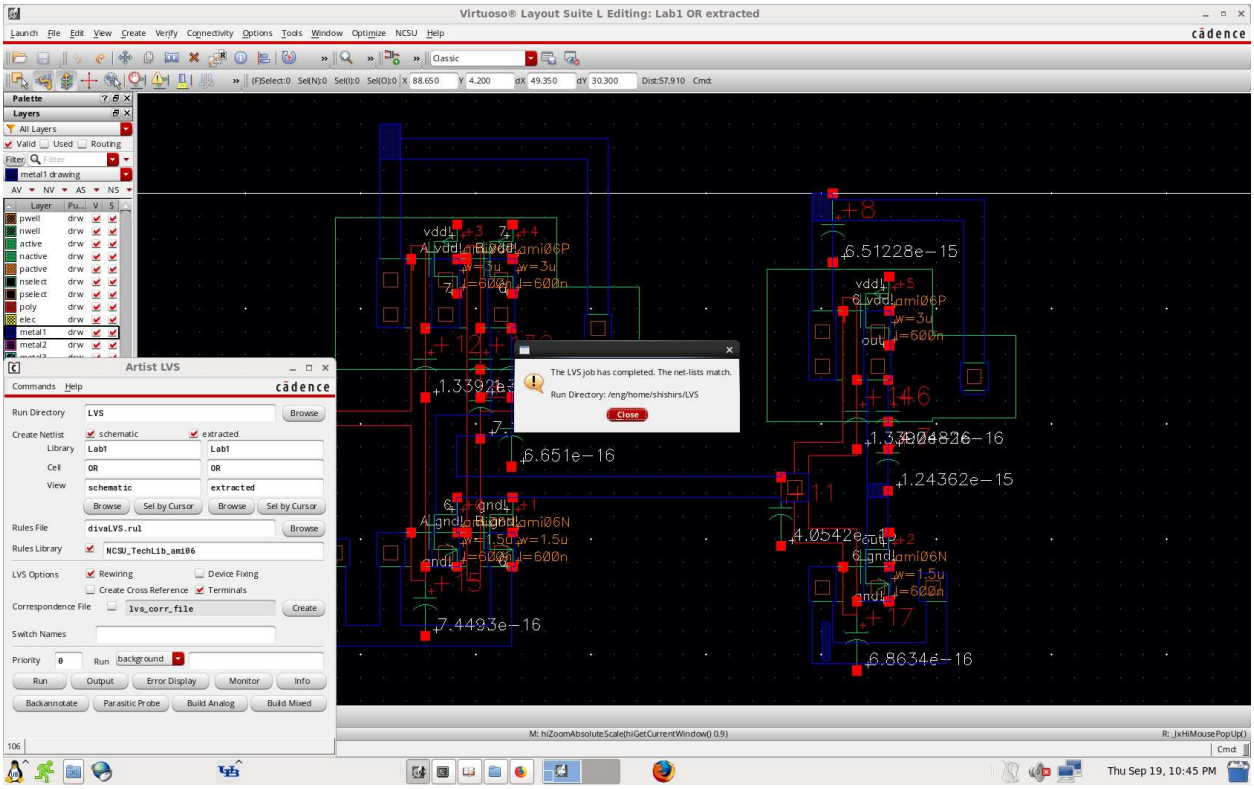


Extracted View:



Extracted View Simulation:

LVS Match between Schematic and Extracted Views:



Truth Table:

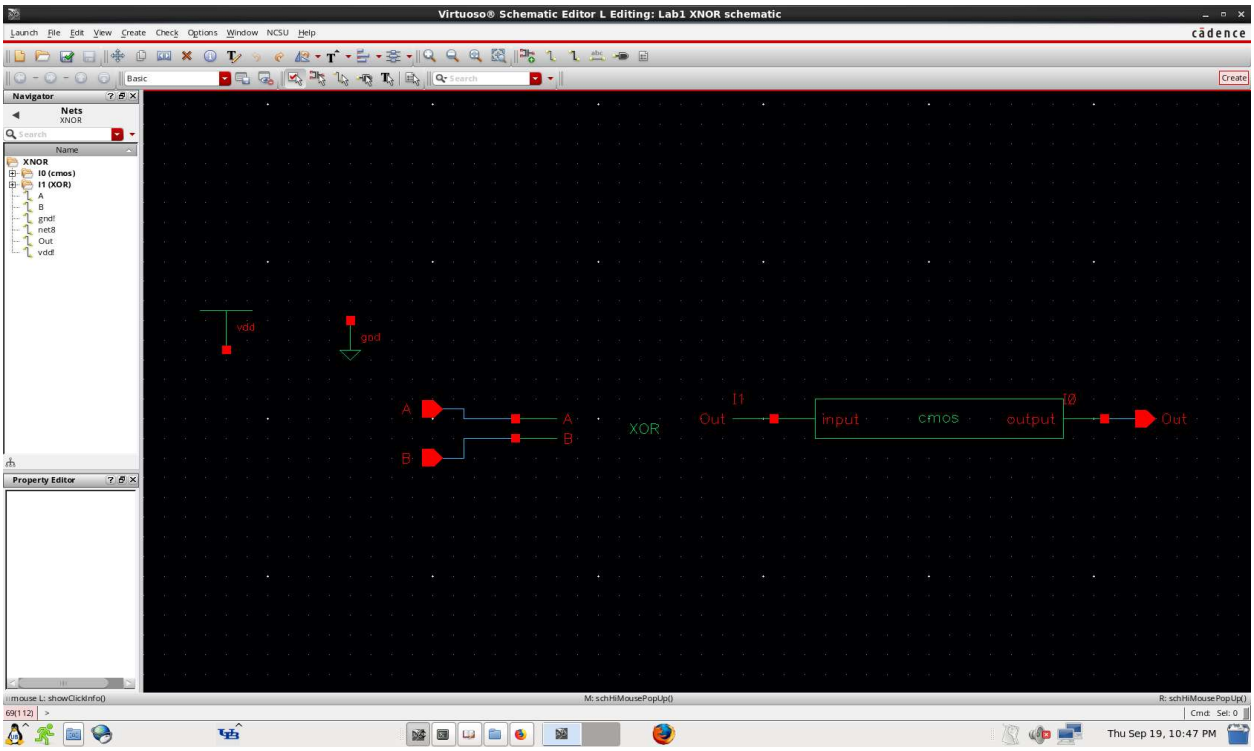
Input A	Input B	Output Q
0	0	0
0	1	1
1	0	1
1	1	1

Working:

- The OR gate produces an output of True if either of the inputs are True

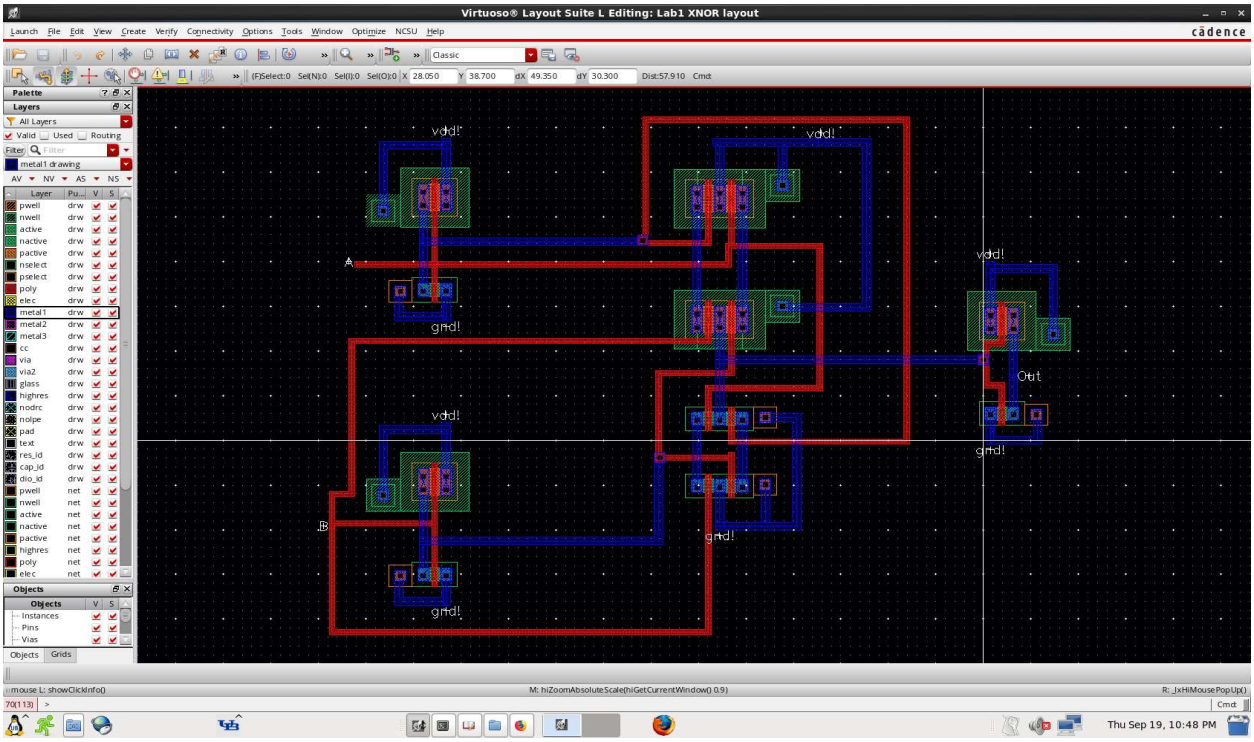
XNOR:

Schematic View:

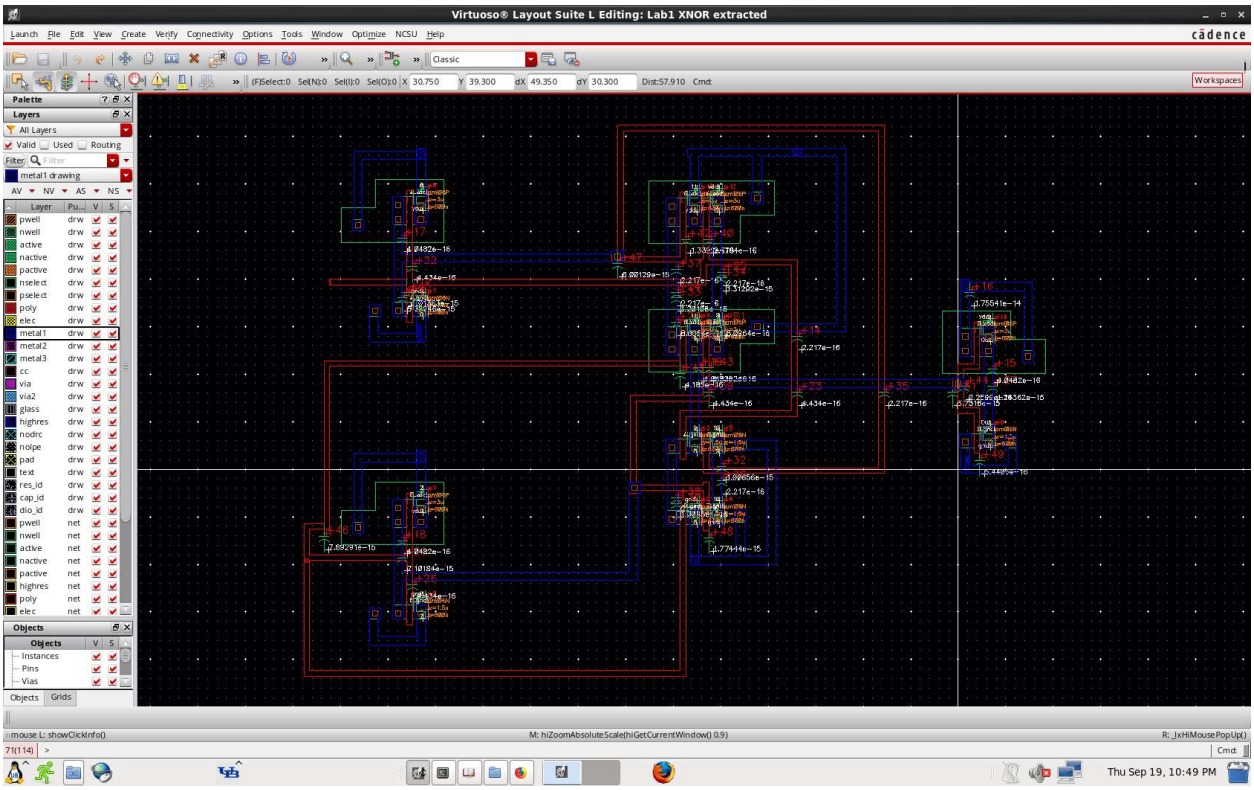


Schematic View Simulation:

Layout View:

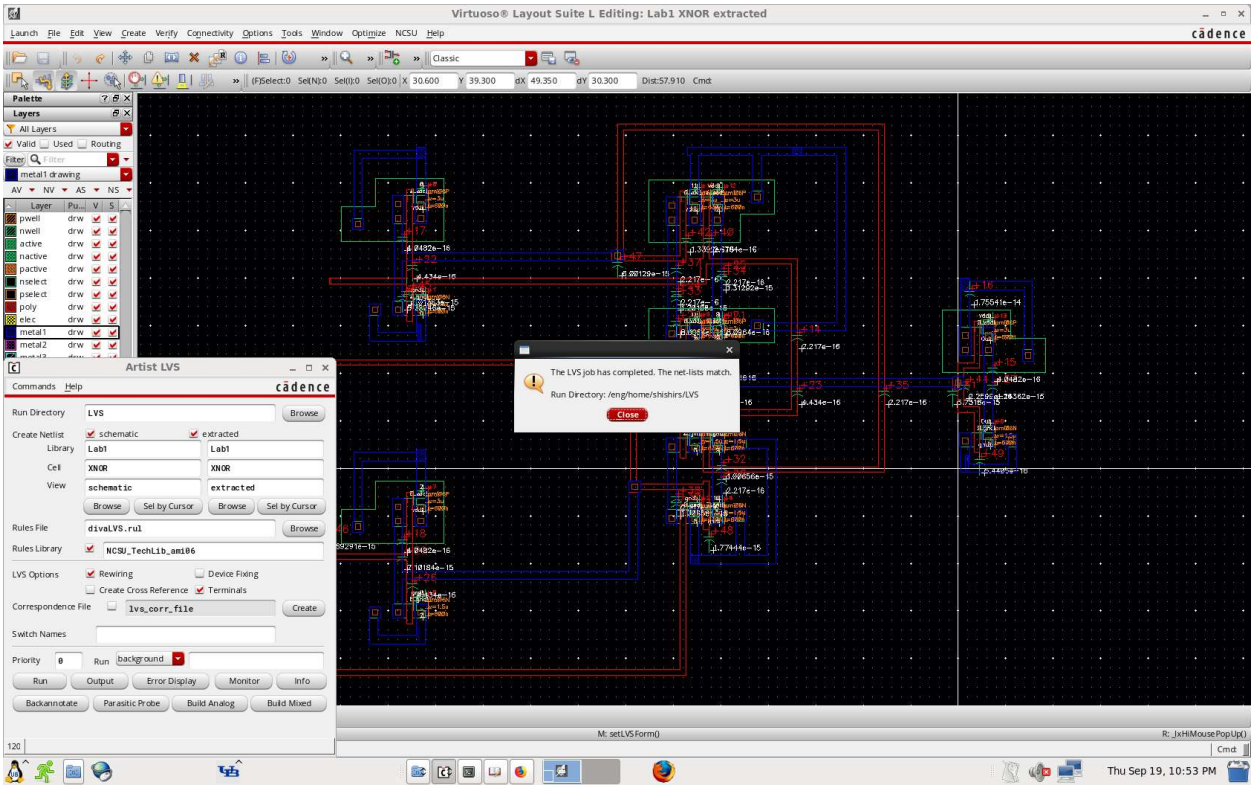


Extracted View:



Extracted View Simulation:

LVS Match between Schematic and Extracted Views:



Truth Table:

Input A	Input B	Output Q
0	0	1
0	1	0
1	0	0
1	1	1

Working:

- The XNOR gate stands for Exclusive-NOR. It is the opposite of XOR gate and produces an output of True if both inputs are the SAME

Inference and Conclusion:

- The working of all basic logic gates was learnt using circuit design techniques
- The schematic and Layout versions of the gates were implemented in the form of circuits in Cadence
- The correctness of the circuit design was verified using simulation tools and output was recorded
- LVS (Layout vs Schematic) check was performed to check if both versions of a gate matched