MEMORY ARRAY USING 6T SRAM CELL

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INTRODUCTION TO VLSI ELECTRONICS

CSE - 593

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INTRODUCTION:

Today, there is a great need for efficient memory structures which can provide good performance while consuming less power. SRAM stands for Static Random Access Memory. It is static in the sense that its value doesn't need to be refreshed.

It holds its value as long as supply voltage is given. SRAM is popular in the industry because of its reliability, performance, low idle power consumption.

WHAT IS SRAM?

SRAM stands for Static Random Access Memory. It is a subtype of the more general Access Memory (RAM). One of the main characteristics of SRAM is that it can hold its contents as long as power is being supplied. In other words, data bits are retained as long as supply voltage is active.

SRAM has some important advantages over Dynamic Random Access Memory (DRAM). It is much faster than DRAM as it provides access to data at higher speeds. Unlike DRAM, it is a static memory and can hold its state without needing to be refreshed. DRAM on the other hand, might need to be refreshed hundreds of times per second. Other practical advantages include reliable performance and low idle power consumption making it an efficient form of memory.

However, SRAM is also significantly more expensive than DRAM. Hence, it is more useful for applications like CPU caches while DRAM is more useful as main memory.

There are two types of SRAM – synchronous and asynchronous. Synchronous RAM is the faster of the two, as it is able to synch with the microprocessor or CPU's clock speed.

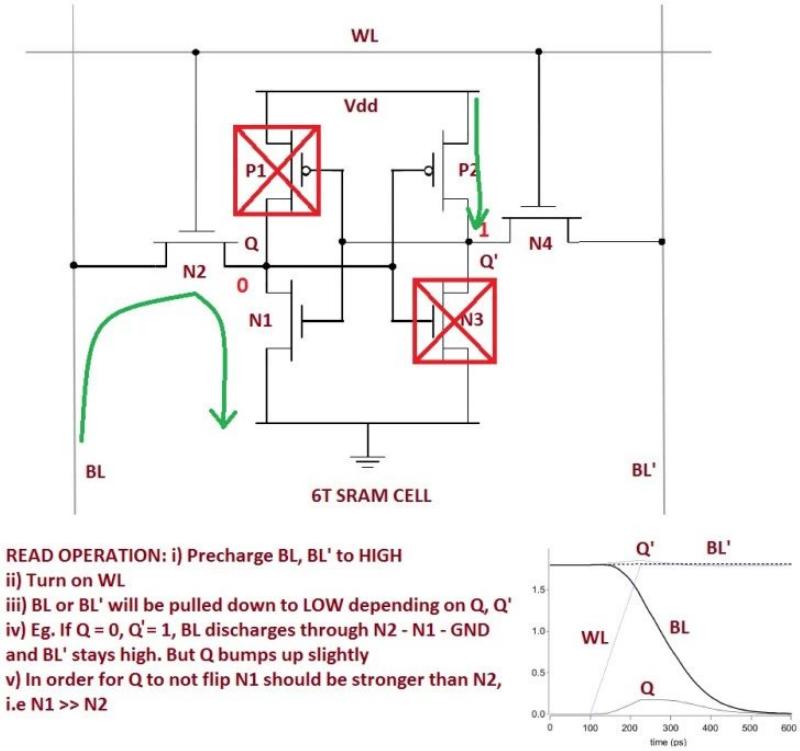
SRAM cell is a volatile memory and the data is lost when the power is cut off. But unlike DRAM, it doesn't have leakage and holds its value in a stable value when active. Hence, it doesn't need to be refreshed.

6T SRAM CELL:

Depending on the number of transistors in the cell, SRAM cell may be 6T, 7T or 8T. A 6T SRAM cell consists of six MOSFET transistors. Four of these transistors are used to constitute two inverters which are cross coupled with each other. The other two transistors are used as access transistors. It uses bi-stable flip flop circuits and holds two stable states, 0 and 1.

The access transistors are activated when the Word-Line is high.

READ OPERATION:



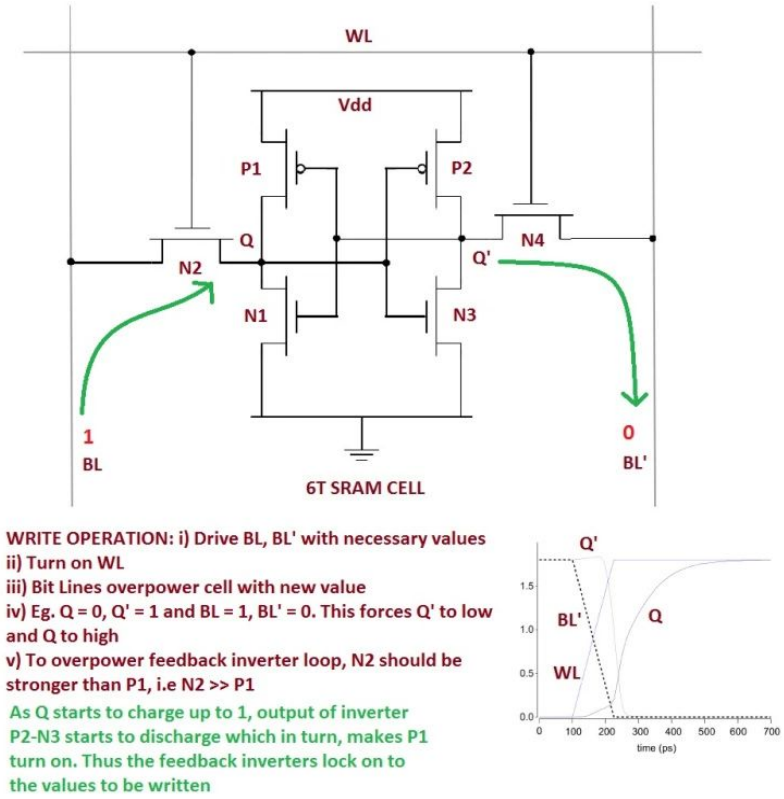
The Read operation is one of the two main operations of the SRAM cell. Both the read and write operations are facilitated by the activations of the two bitlines.(Bitline and Bitline'). This occurs when the Word-Line is active.

Depending upon the values of Q and Q', BL and BL' can be pulled down provided they have been pre-charged to high. If Q=0 and Q'=1, then BL discharges through the path N2 then N1 and then ground. BL' stays high.

The value of Q will not flip provided that access transistor N1 is stronger than N2. This change in voltage is read by the Sense Amplifier which reads the decrease in voltage BL' and shows a high output for Q.

This is a Read operation for the cell.

WRITE OPERATION:



In the write operation bit and bit' are input lines. Consider the memory bits consists of Q=0 and Q'=1. Initially word line is high and hence write operation can be performed.

As we have control on the bit lines, initially make the BLB connected to ground so that we can have the voltage difference between Q' and BLB.

To write 1 into the SRAM cell, M1 must be stronger than M2, this can be achieved by changing the aspect ratio of the transistors. Hence Q will be 1. Initially Q=0 after the operation Q=1, hence we write successfully into the memory.

SRAM ARCHITECTURE:

SRAM array consists of SRAM cell, write driver circuit, precharge circuit, sense amplifier and row/column decoder. A SRAM cell is capable of storing one bit of binary information. SRAM array consists of horizontal rows and vertical columns. In array architecture, there are 2N rows that are called as word lines and 2M columns that are called as bitlines. The total number of memory cells in the array is 2(N+M). For this implementation, we have a write driver circuit and sense amplifier dedicated for one column.

ADDRESS DECODER:

In digital electronics, an address decoder is a binary decoder that has two or more inputs for address bits and one or more outputs for device selection signals.When the address for a particular device appears on the address inputs, the decoder asserts the selection output for that device. A dedicated, single-output address decoder may be incorporated into each device on an address bus, or a single address decoder may serve multiple devices.

A single address decoder with n address input bits can serve up to 2n devices. The name “Decoder” means to translate or decode coded information from one format into another, so a binary decoder transforms “n” binary input signals into an equivalent code using 2n outputs.

Binary Decoders are another type of digital logic device that has inputs of 2-bit, 3-bit or 4-bit codes depending upon the number of data input lines, so a decoder that has a set of two or more bits will be defined as having an n-bit code, and therefore it will be possible to represent 2n possible values. Thus, a decoder generally decodes a binary value into a non-binary one by setting exactly one of its n outputs to logic “1”.

If a binary decoder receives n inputs (usually grouped as a single Binary or Boolean number) it activates one and only one of its 2n outputs based on that input with all other outputs deactivated.

Generally a decoders output code normally has more bits than its input code and practical “binary decoder” circuits include, 2-to-4, 3-to-8 and 4-to-16 line configurations.

For the purpose of this project we use two 2-to-4 line address decoders, namely, **a row decoder** and a column **decoder.** These two address decoders are employed to decode the given address and alter the actual row or column. Row and column decoder is employed to pick out a specific WL and that of an SRAM array. Figure shows the diagram of decoder that have two inputs (A and B) and four outputs.

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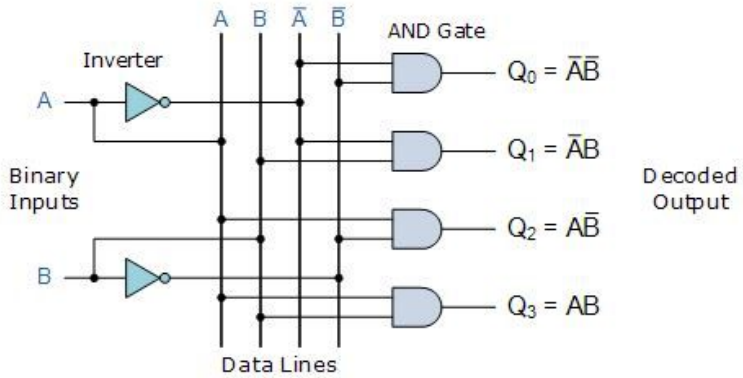
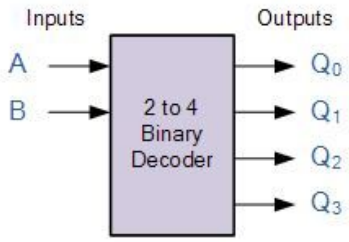
A 2-to-4 Binary Decoders



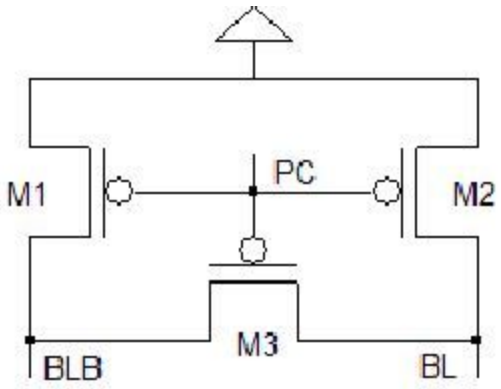


Truth Table

A	B	Q_0	Q_1	Q_2	Q_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

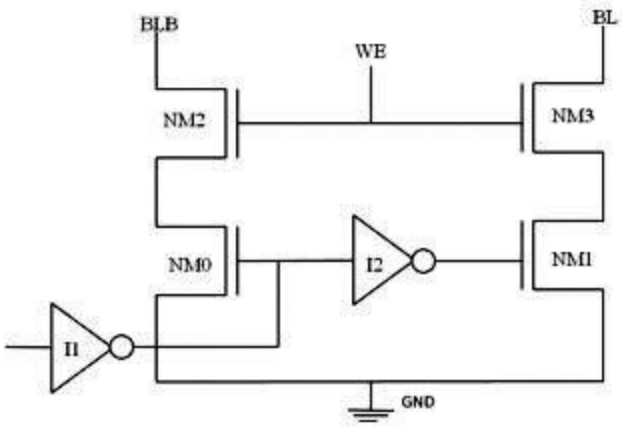
PRECHARGE CIRCUIT:

The pre-charge circuit is the main component that is implemented in SRAM array. following figure represents the circuit diagram of pre-charge circuit. Pre-charge circuit consists of three PMOS transistors. Two upper transistors are used for pre-charging and the lower one is used for equalization. The main role of pre-charge circuit is to charge both the bit lines up to VDD before a read and write operations. Each column incorporates a single pre-charge circuit within the array.



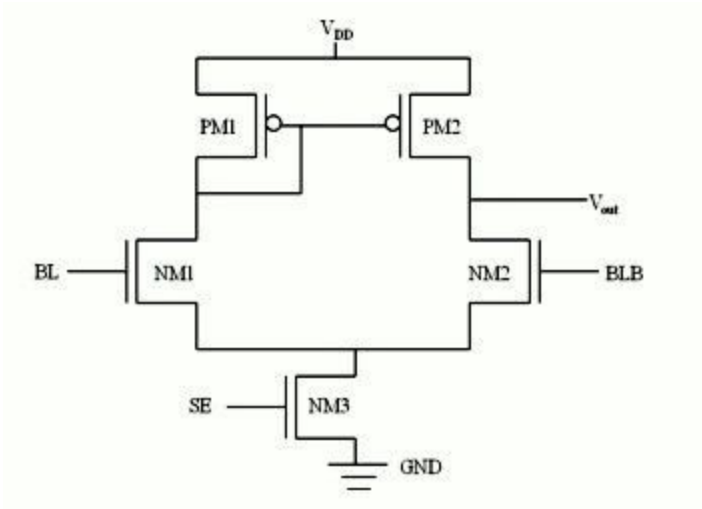
WRITE DRIVER CIRCUIT:

The main role of write driver circuit is to complete discharge one of the bitlines from the precharge level. Write driver is enabled by a Write Enable (WE) signal. Only one write driver circuit is required for each column in the array. Write driver circuit shows in the following figure. It consists of two inverters (I1 and I2) and four NMOS (NM0, NM1, NM2 and NM3) transistors. Channel length of NMOS transistor is 5μm and channel width is 200nm is considered.



SENSE AMPLIFIER:

Sense electronic equipment is an important element of SRAM. Figure below shows the circuit diagram of Differential Sense electronic equipment. It's conjointly referred to as voltage mode sense electronic equipment.



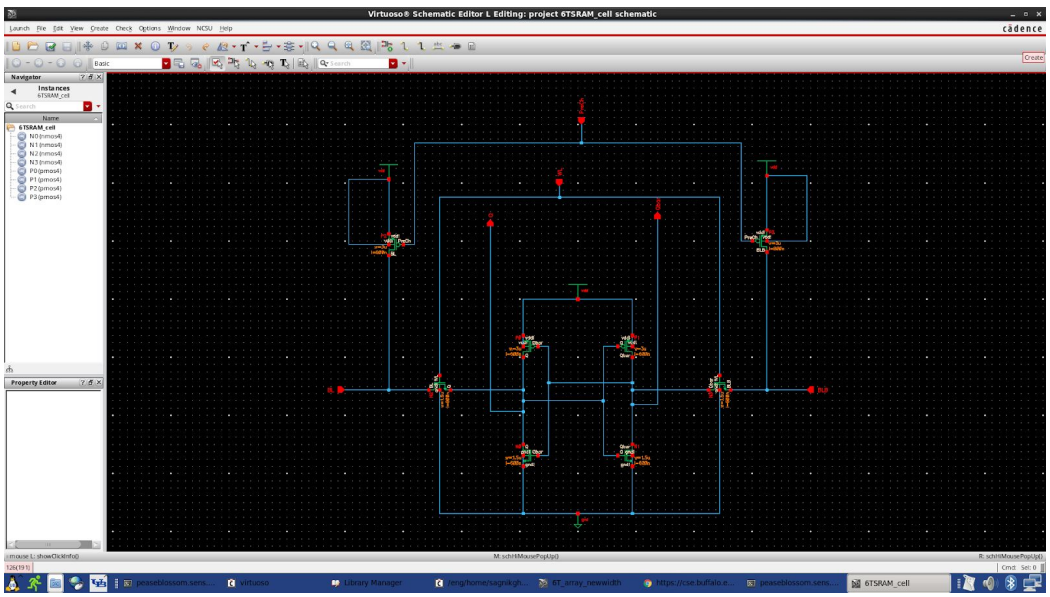
Sense amplifiers detects the voltage difference between the bit-lines and show which data value stored in the memory cell. The circuit consists of cross coupled inverters that converts the bit-line voltage

difference at their input to full swing output. BL and BLB inputs are coupled to the column bit-lines of the cell.

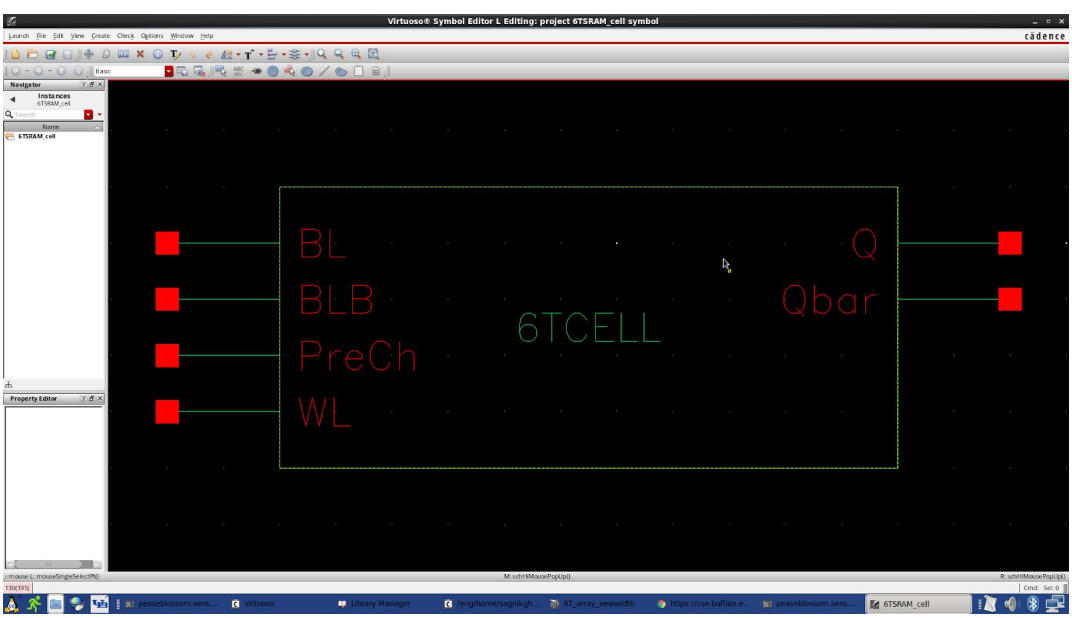
To read a bit from a particular memory cell, the word line along the cell's row is turned on, activating all the cells in the row. The stored value (Logic 0 or 1) from the cell then comes to the Bit-lines associated with it. The sense amplifier at the end of the two complementary bit-lines amplify the small voltages to a normal logic level. The bit from the desired cell is then latched from the cell's sense amplifier into a buffer, and put on the output bus.

SCREENSHOTS AND OUTPUTS

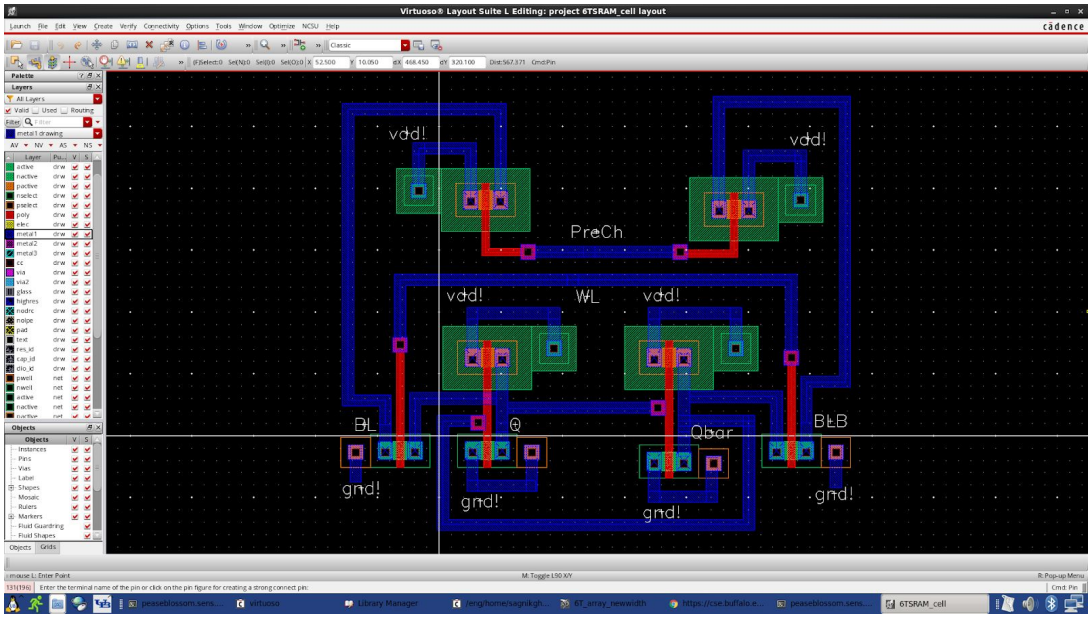
- **6T Cell**



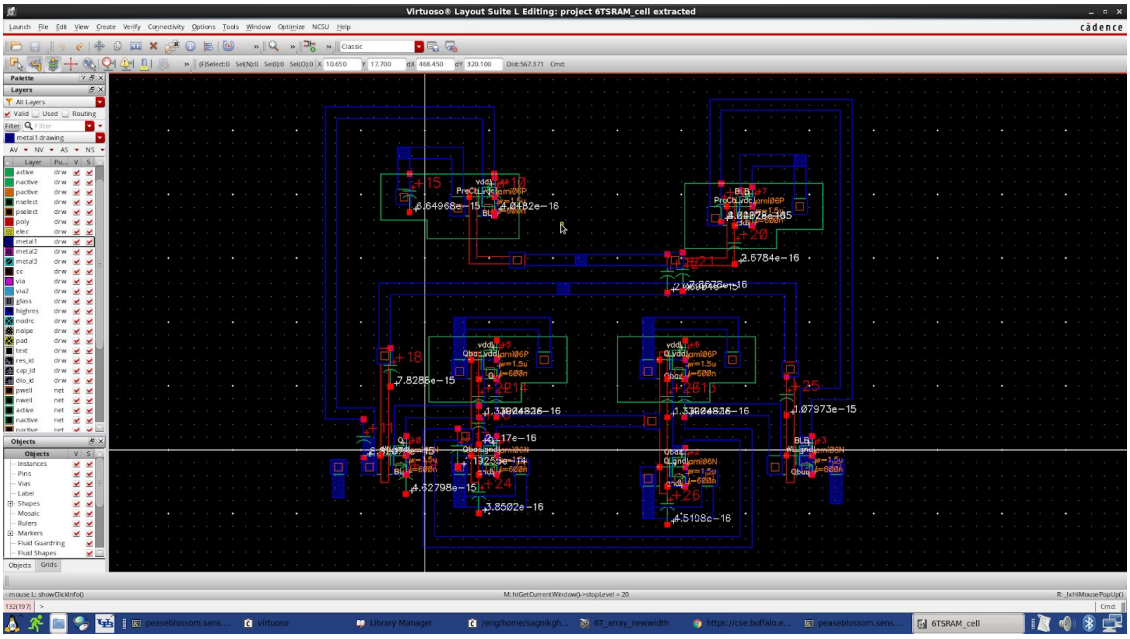
Schematic Diagram



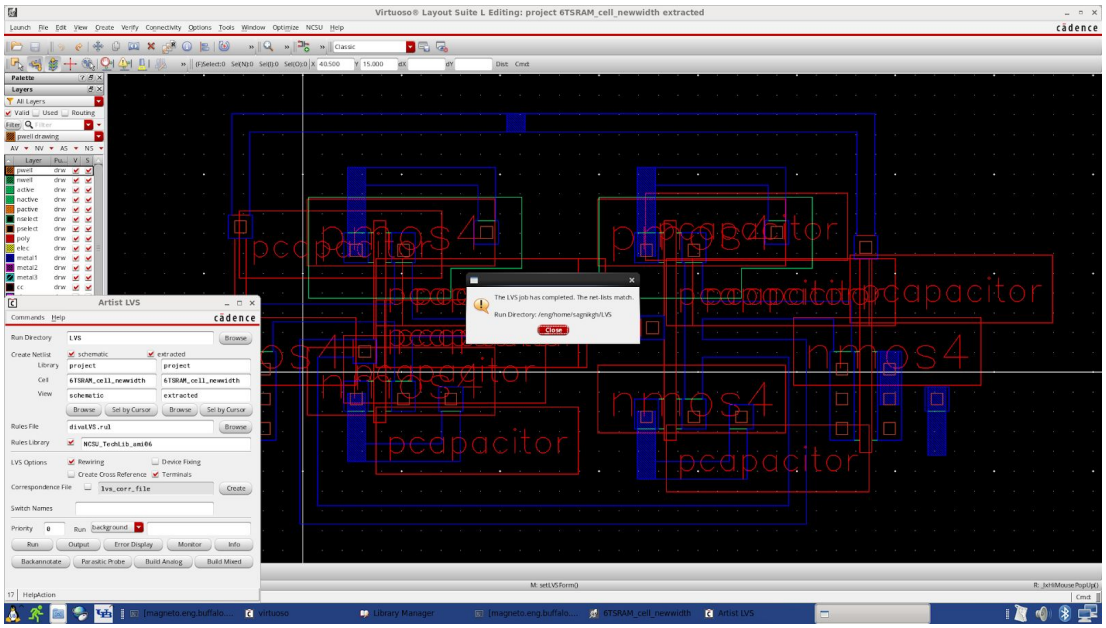
Symbol



Layout View



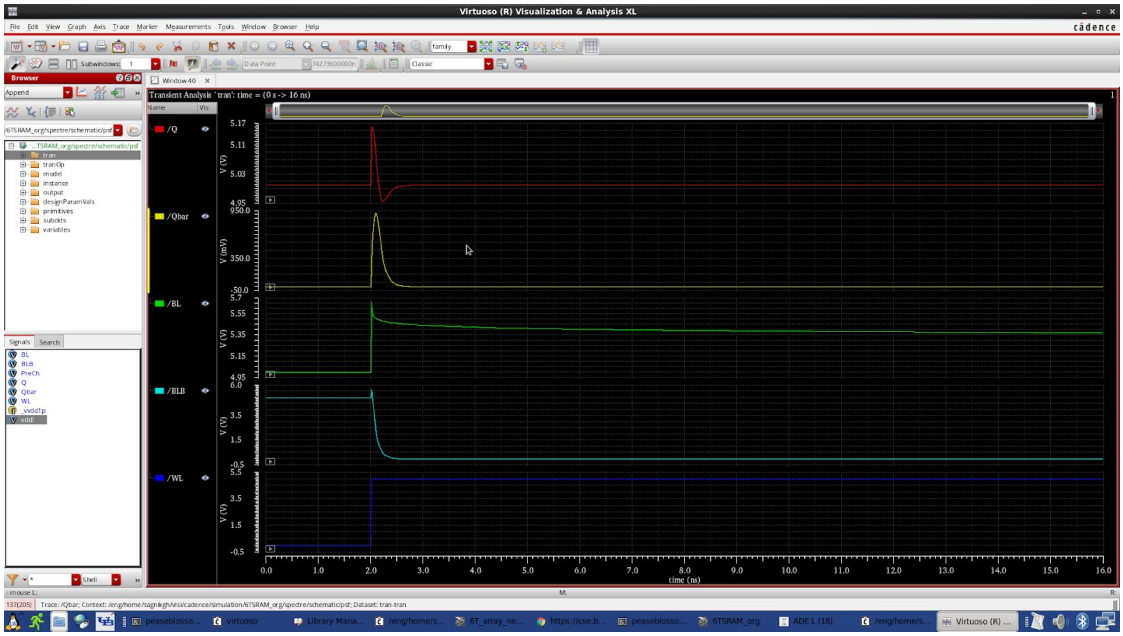
Extracted View



LVS match

Simulation (Write Operation)

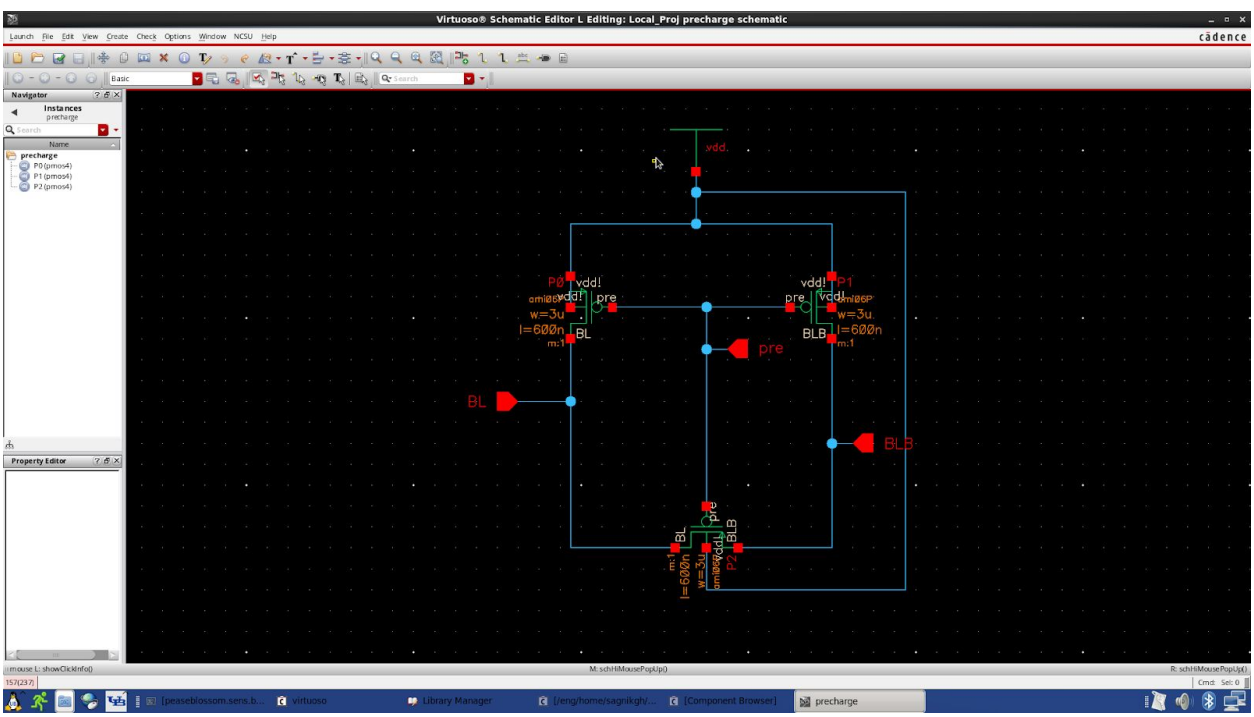
Q is going from Low to high and Q' which was initially set to high is going to low. Which means Q' is discharging and a value is being written in Q.



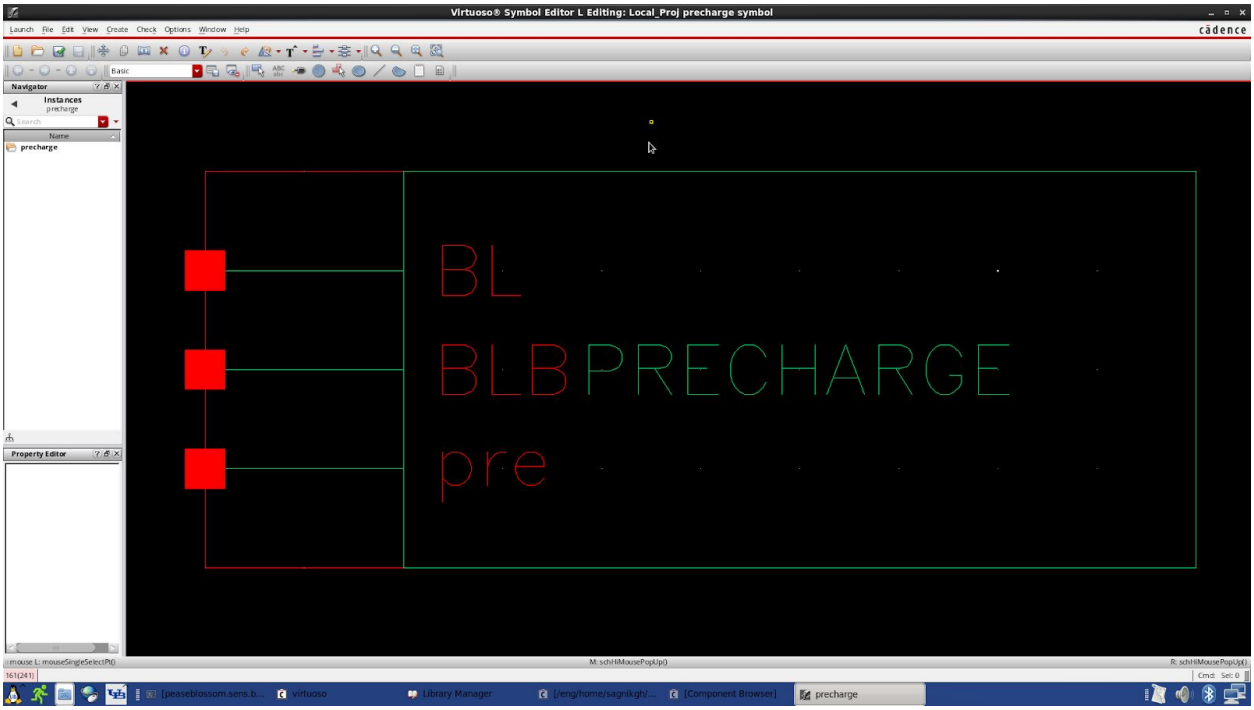
The above simulation explains the read operation of the 6T SRAM cell. Here, the value of BL is constantly high but BL' is discharging and there is no voltage difference BL and Q, i.e. Q is storing a high value.

Simulation (Read Operation)

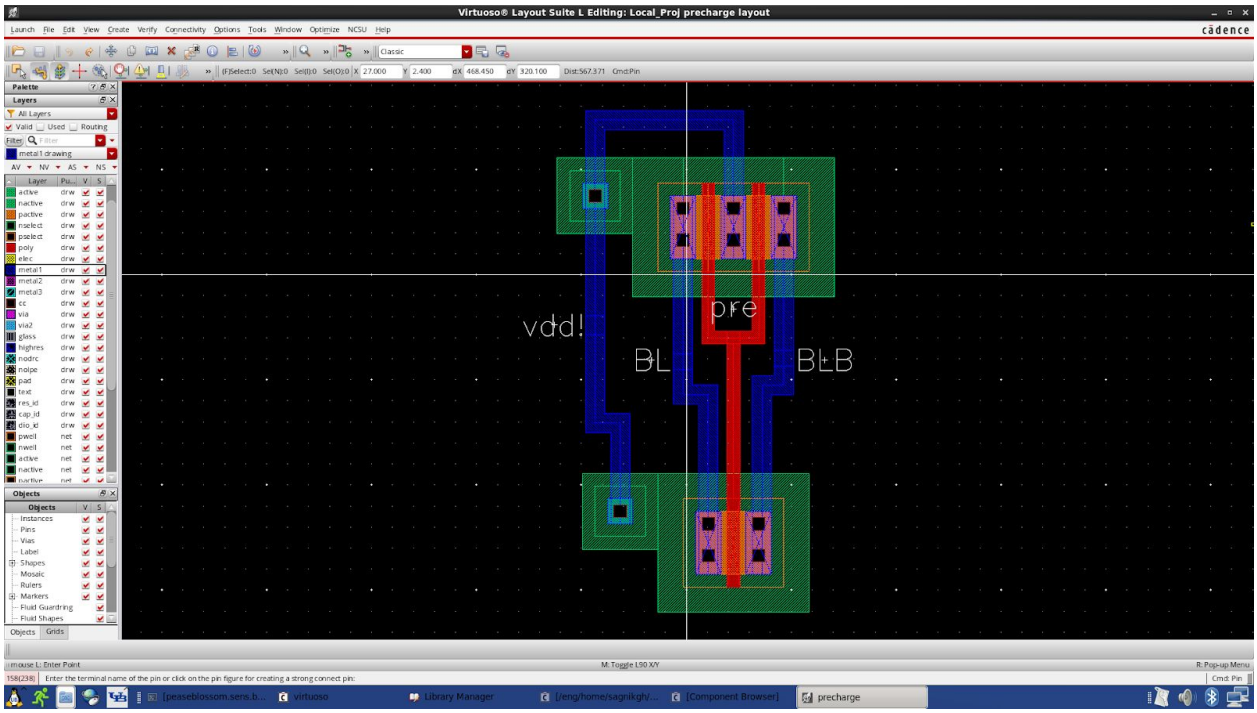
- ## Precharge Circuit



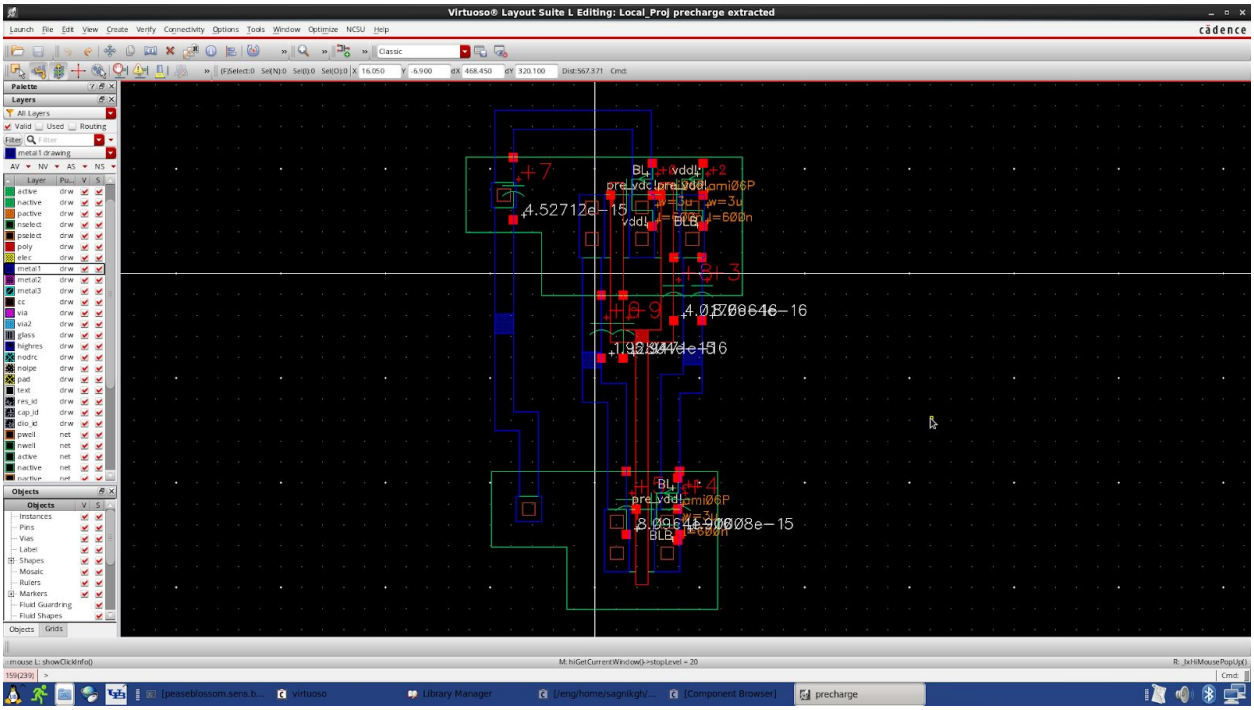
Schematic Diagram



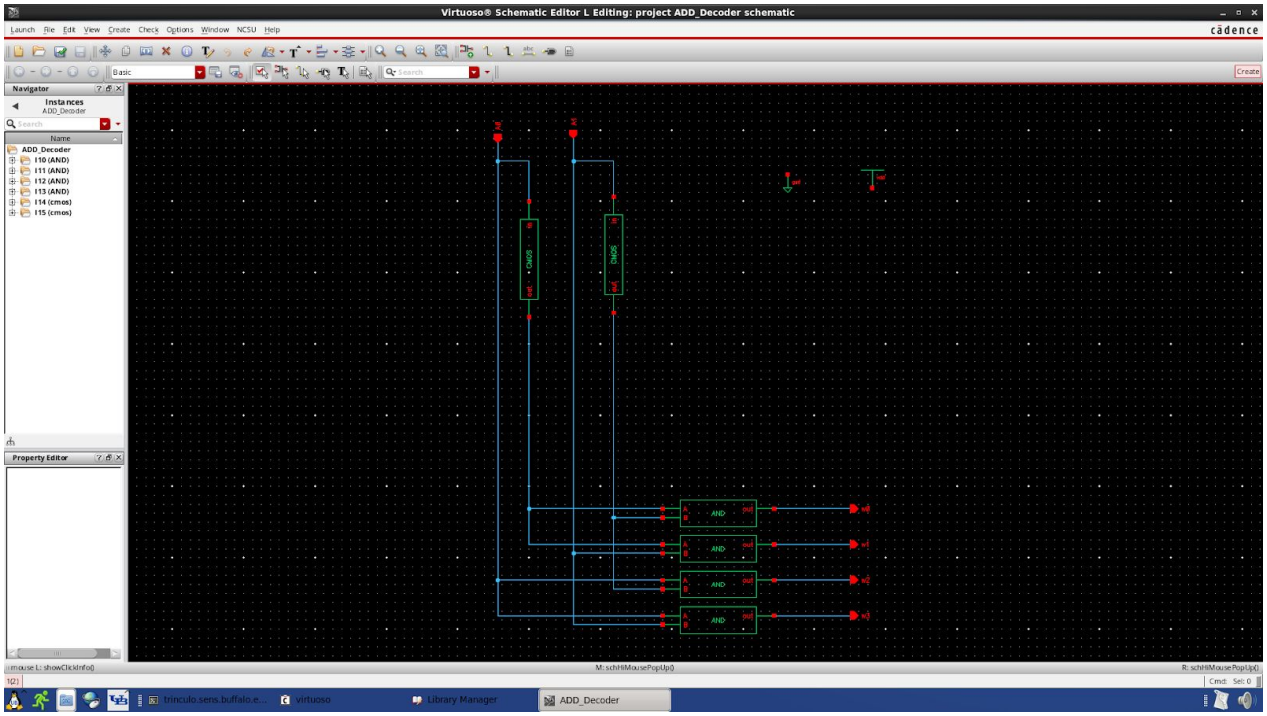
Symbol



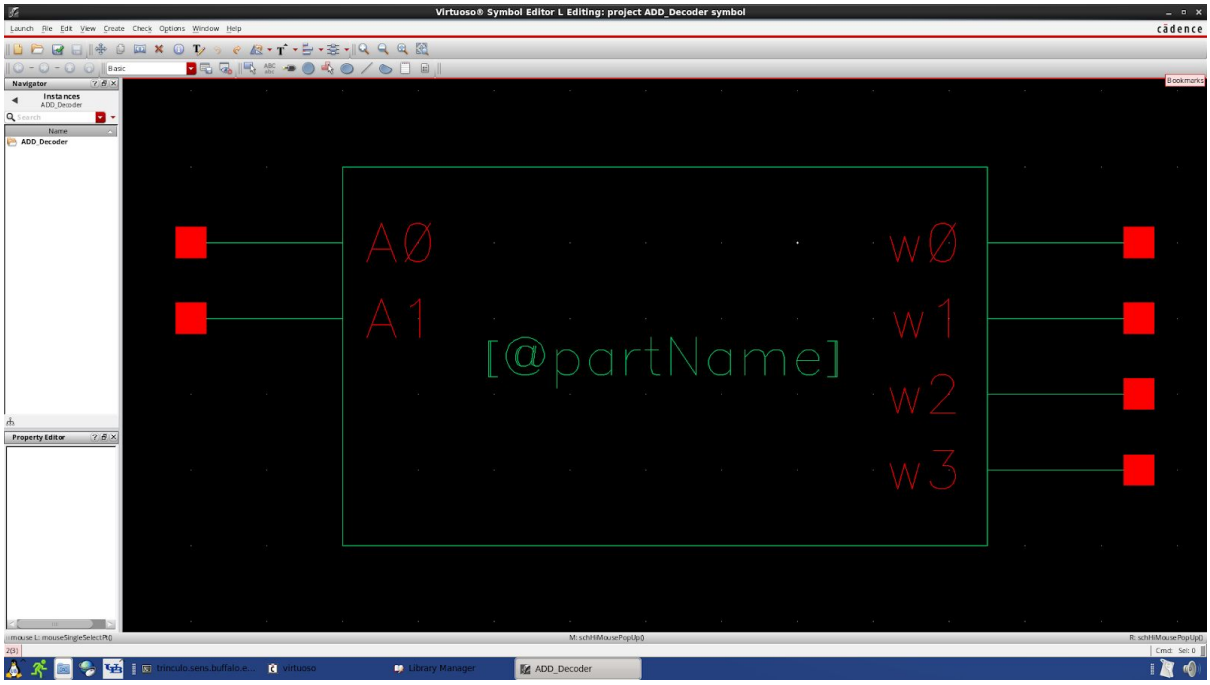
Layout View



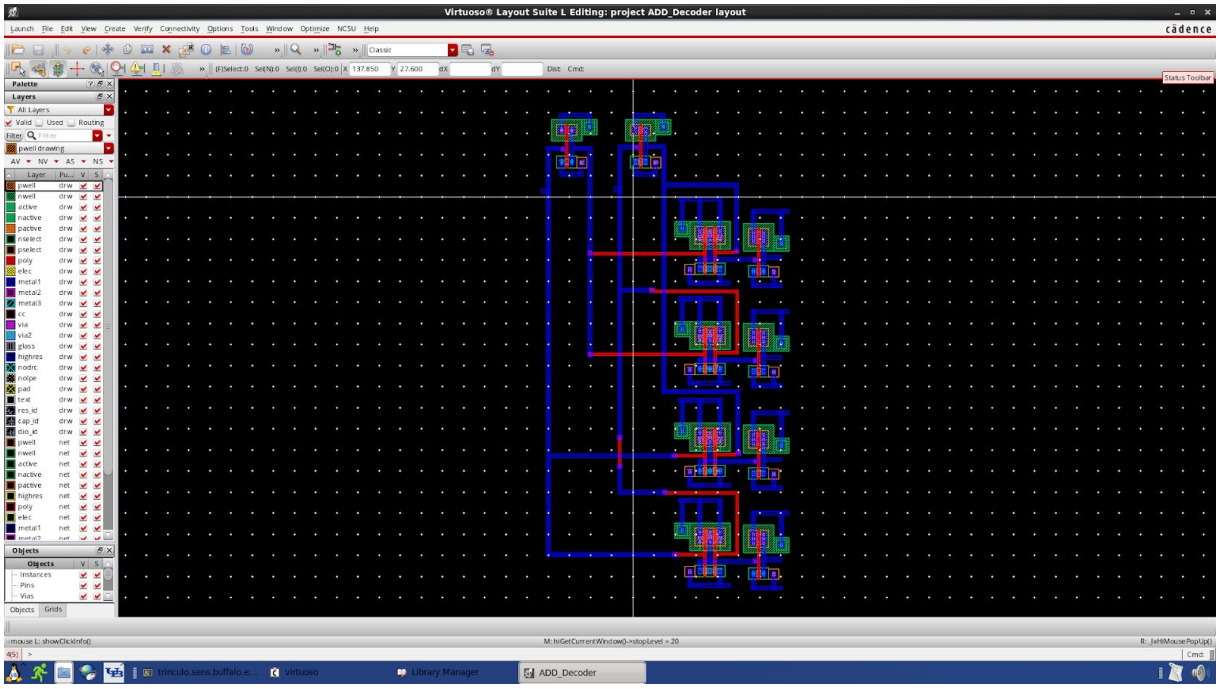
Extracted View



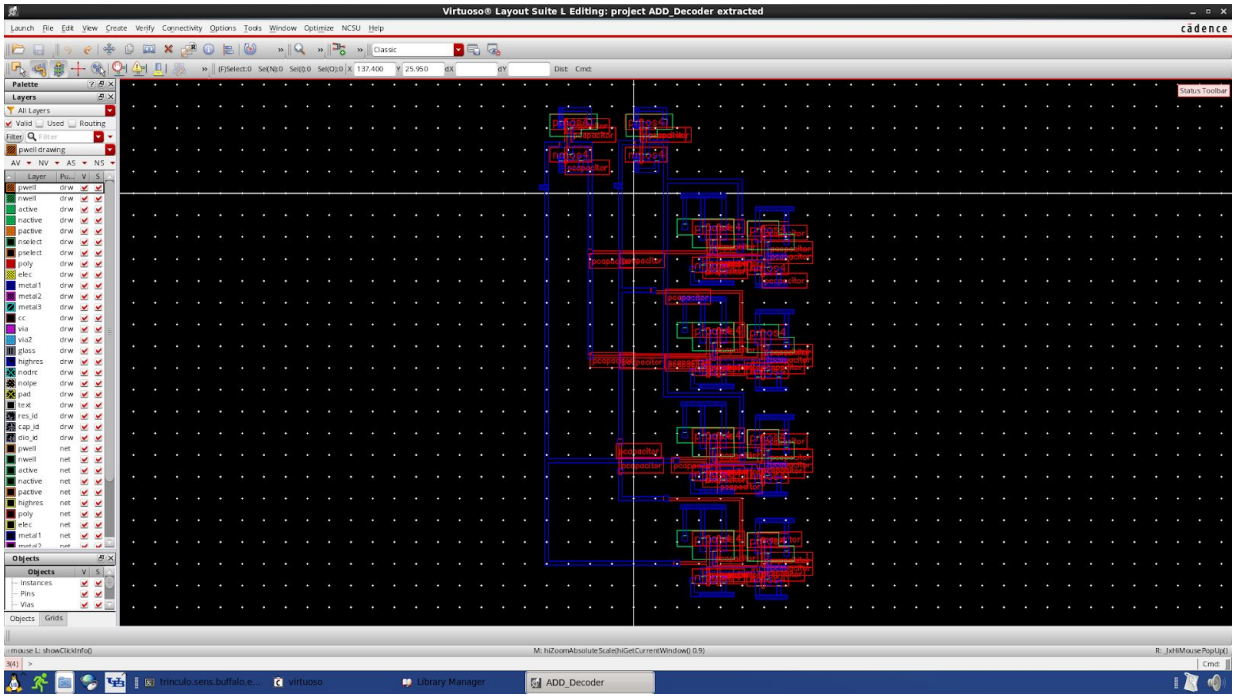
Schematic Diagram



Symbol

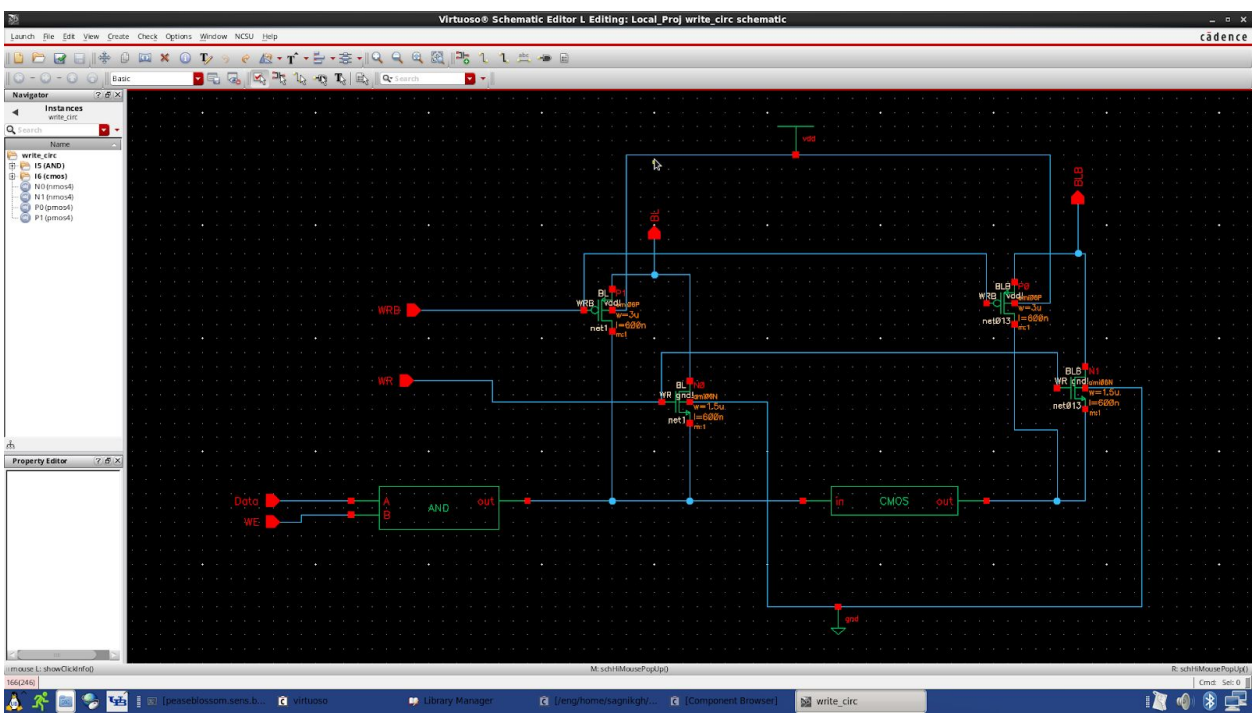


Layout View

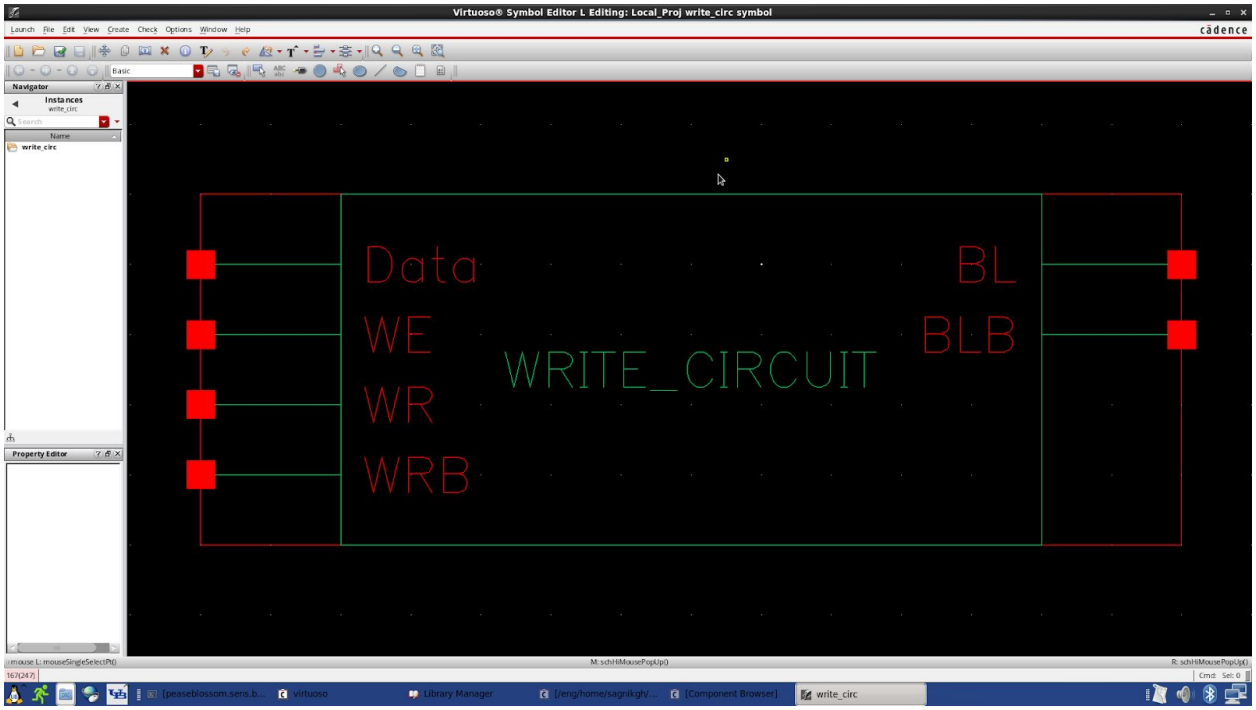


Extracted View

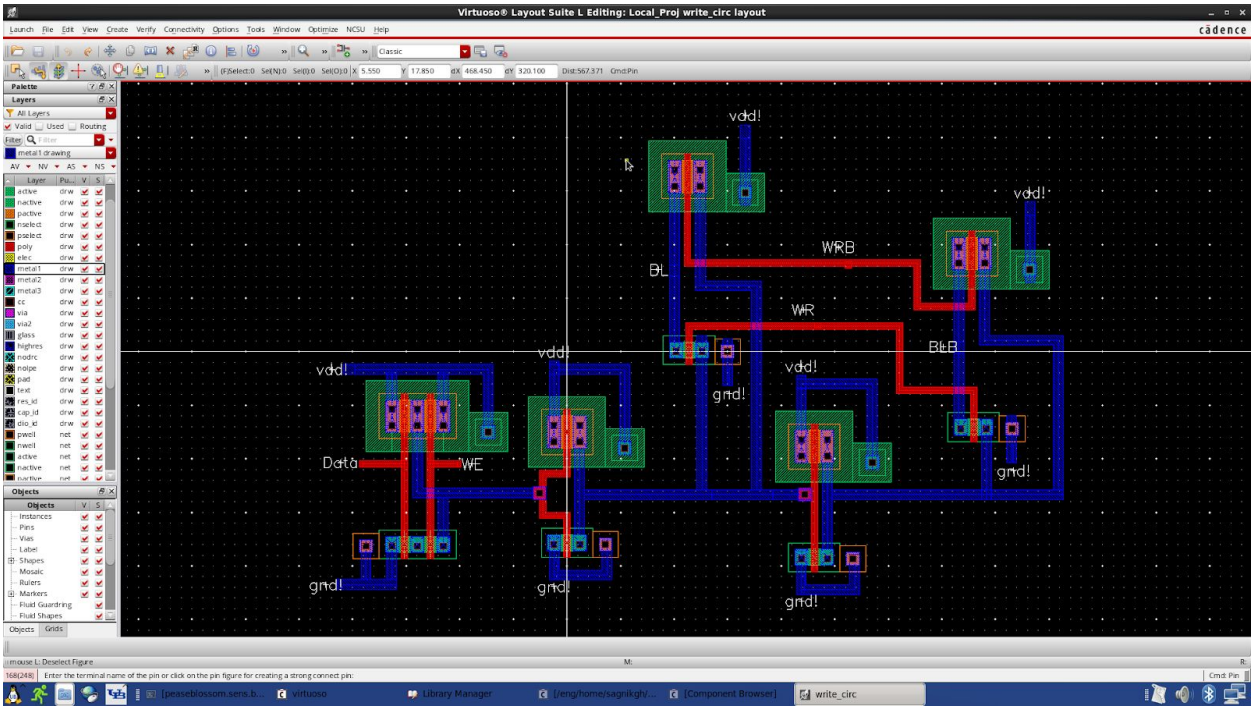
- ## Write Driver Circuit



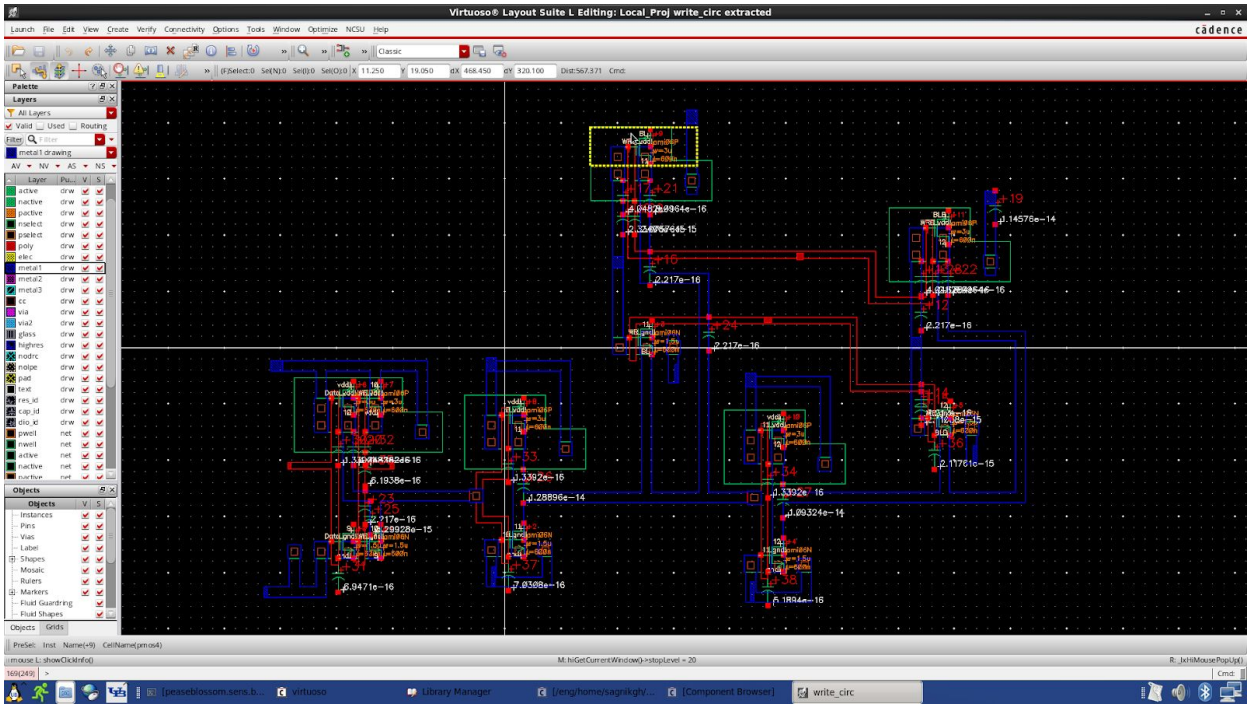
Schematic Diagram



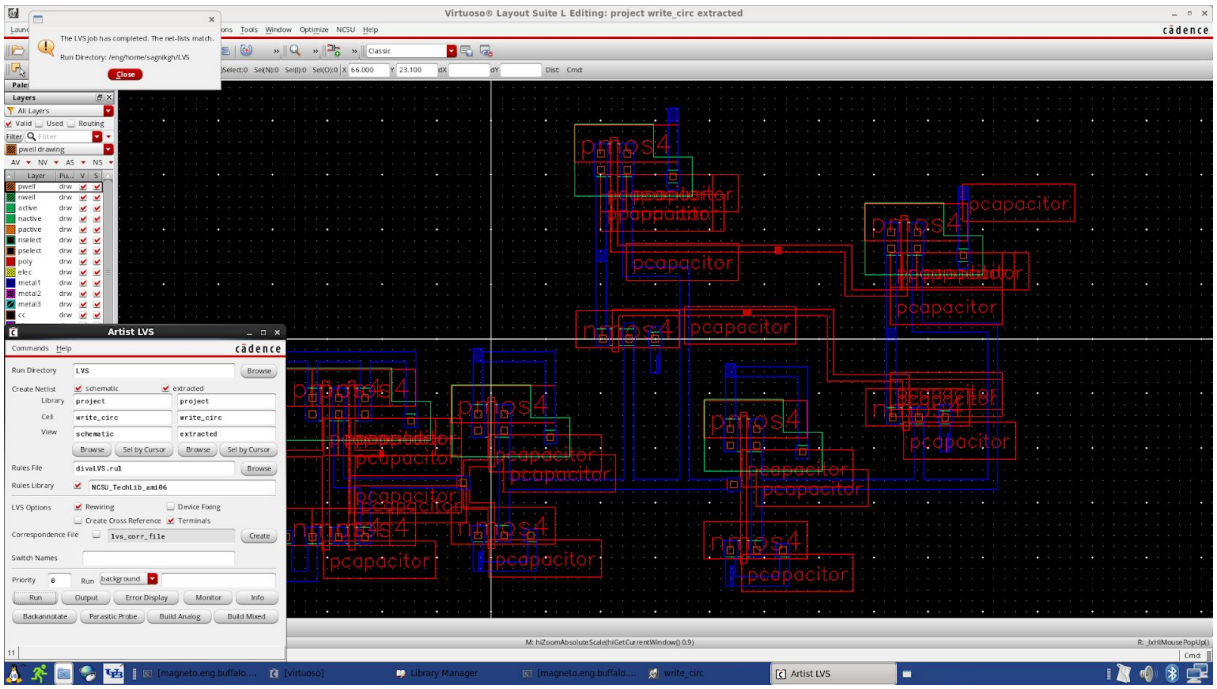
Symbol



Layout View

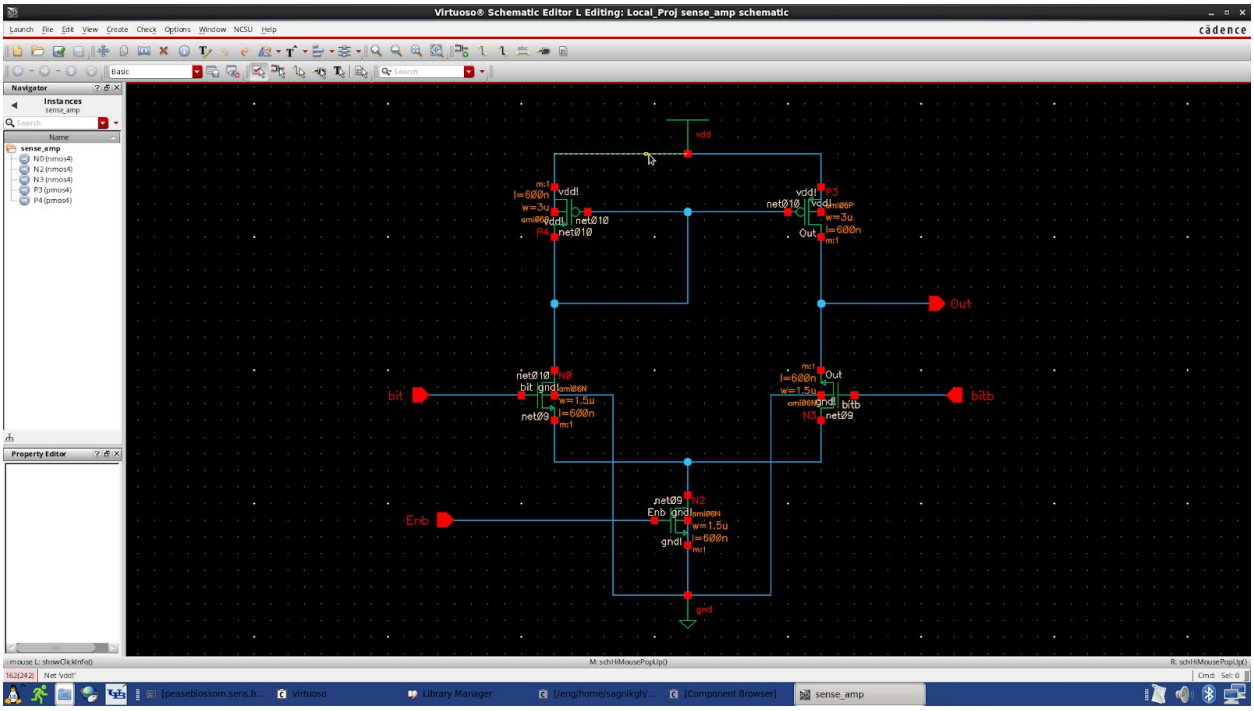


Extracted View

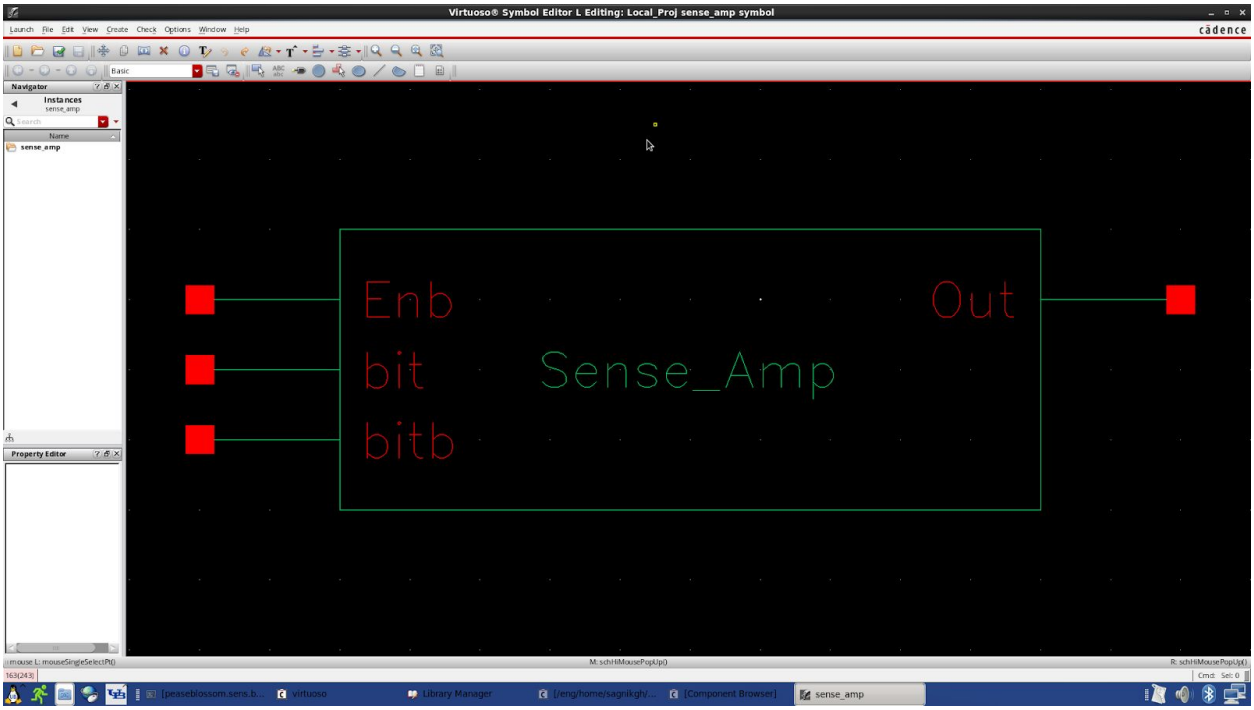


LVS Match

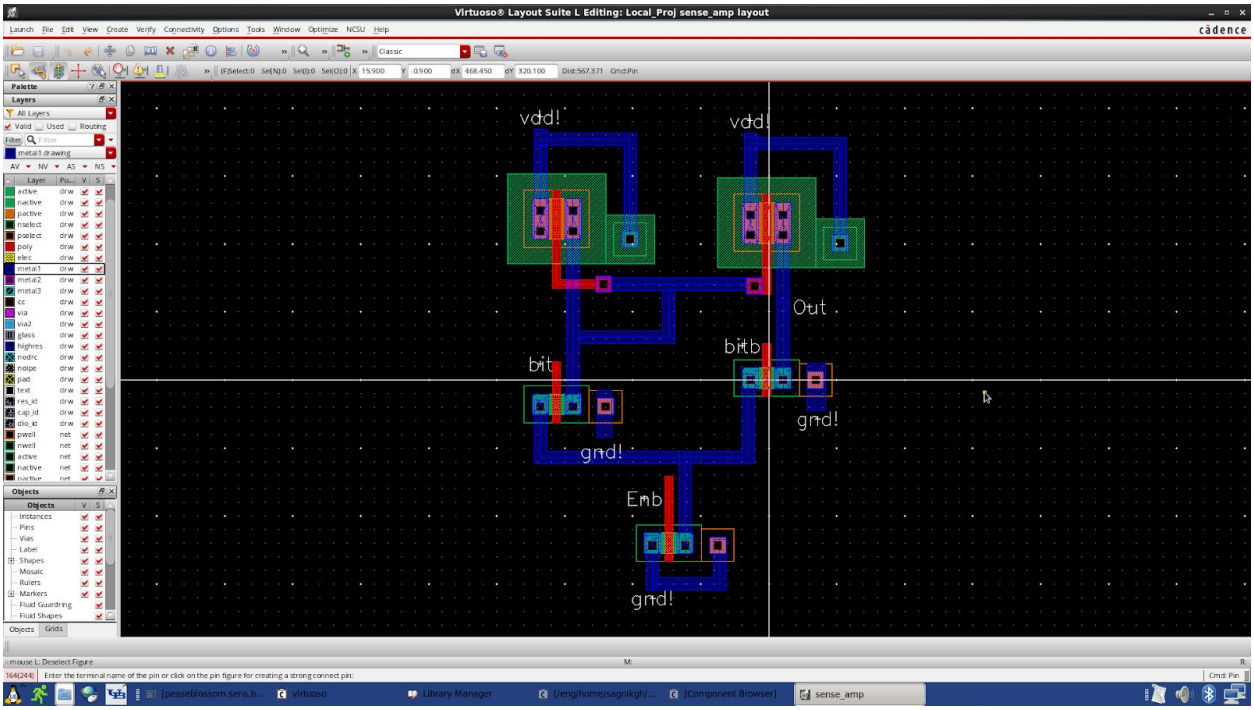
- ## Sense Amplifier



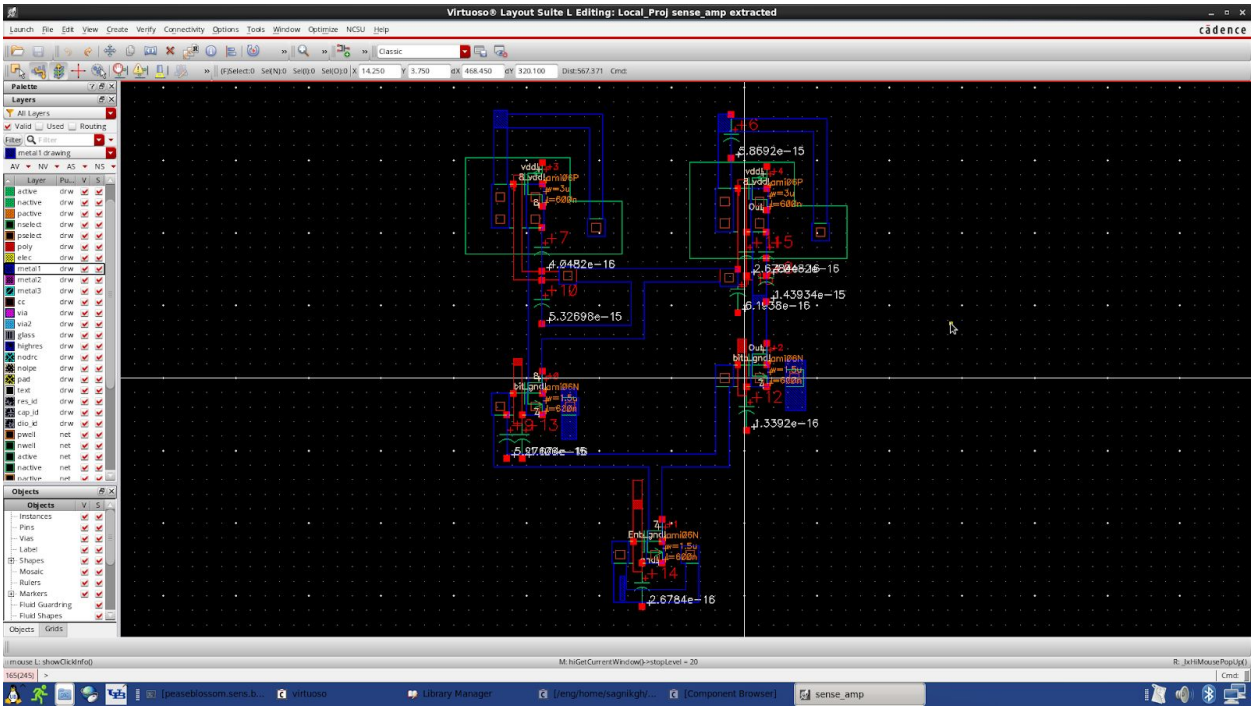
Schematic Diagram



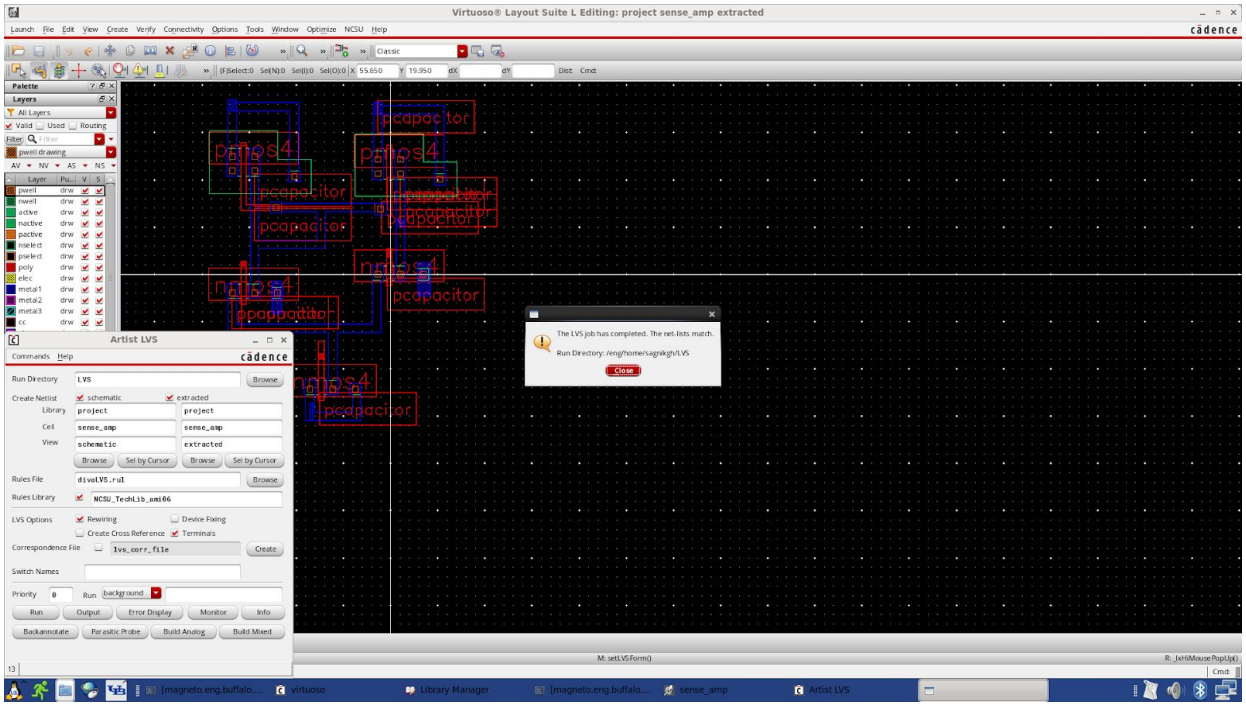
Symbol



Layout View

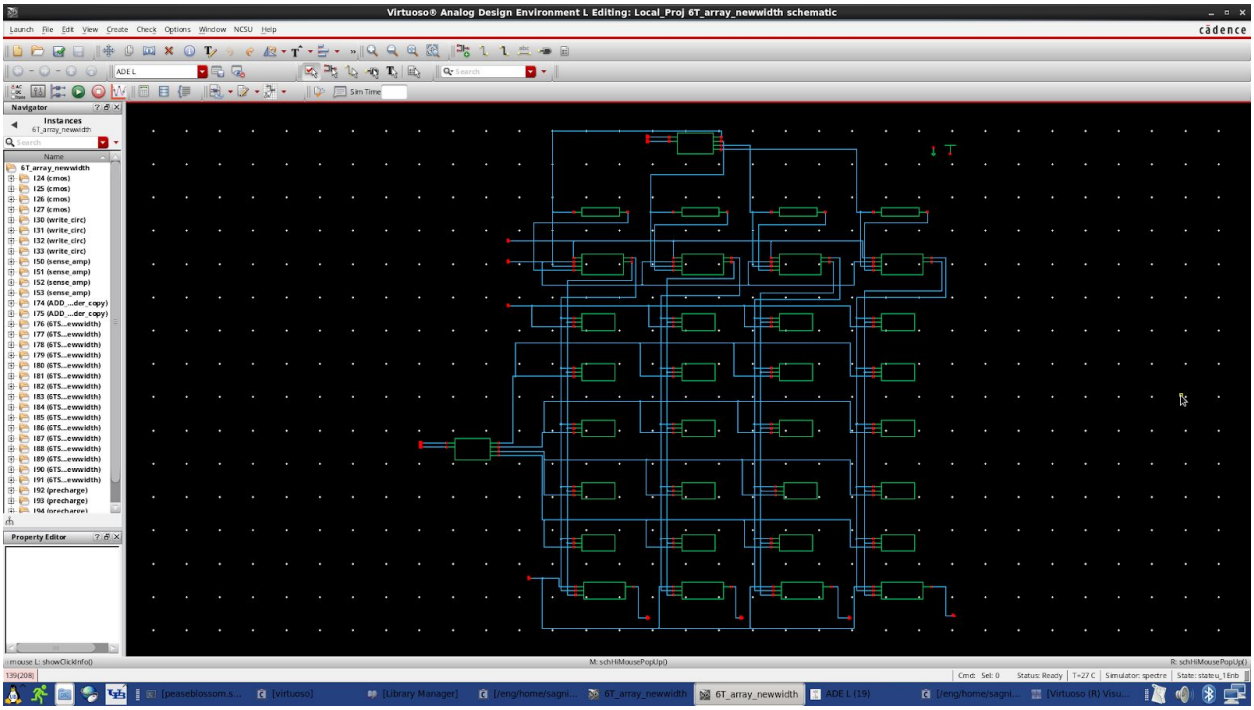


Extracted View

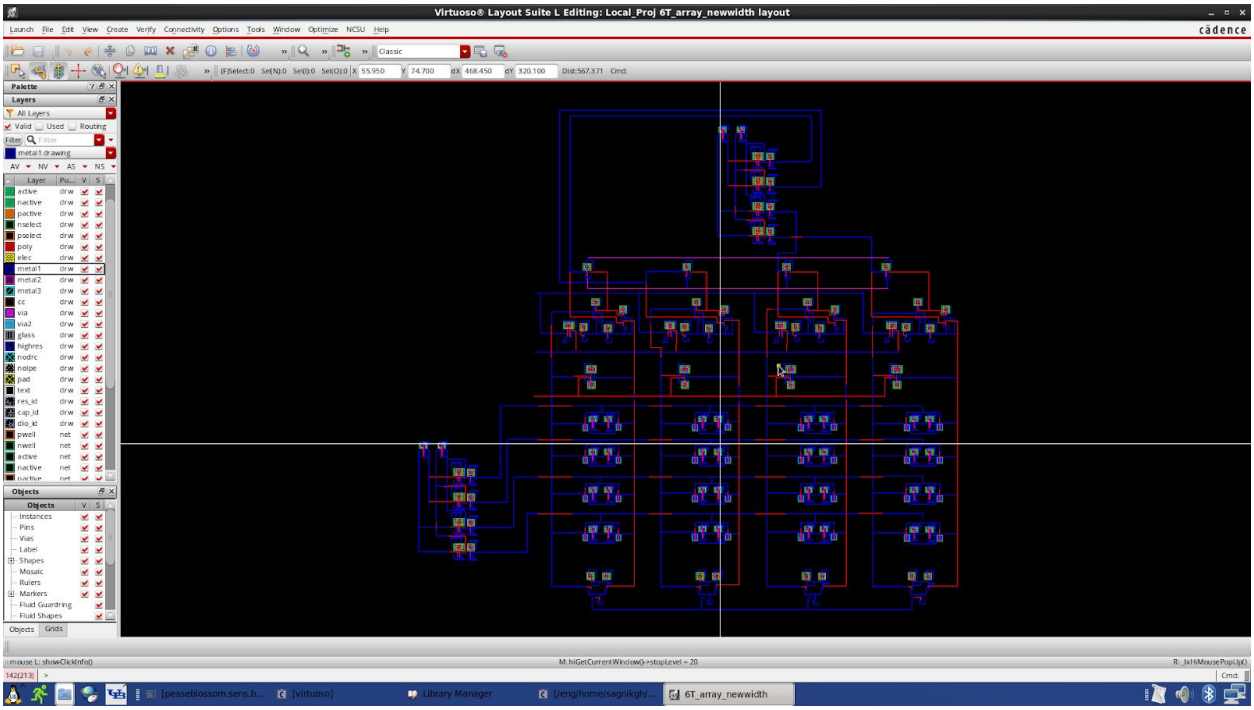


LVS Match

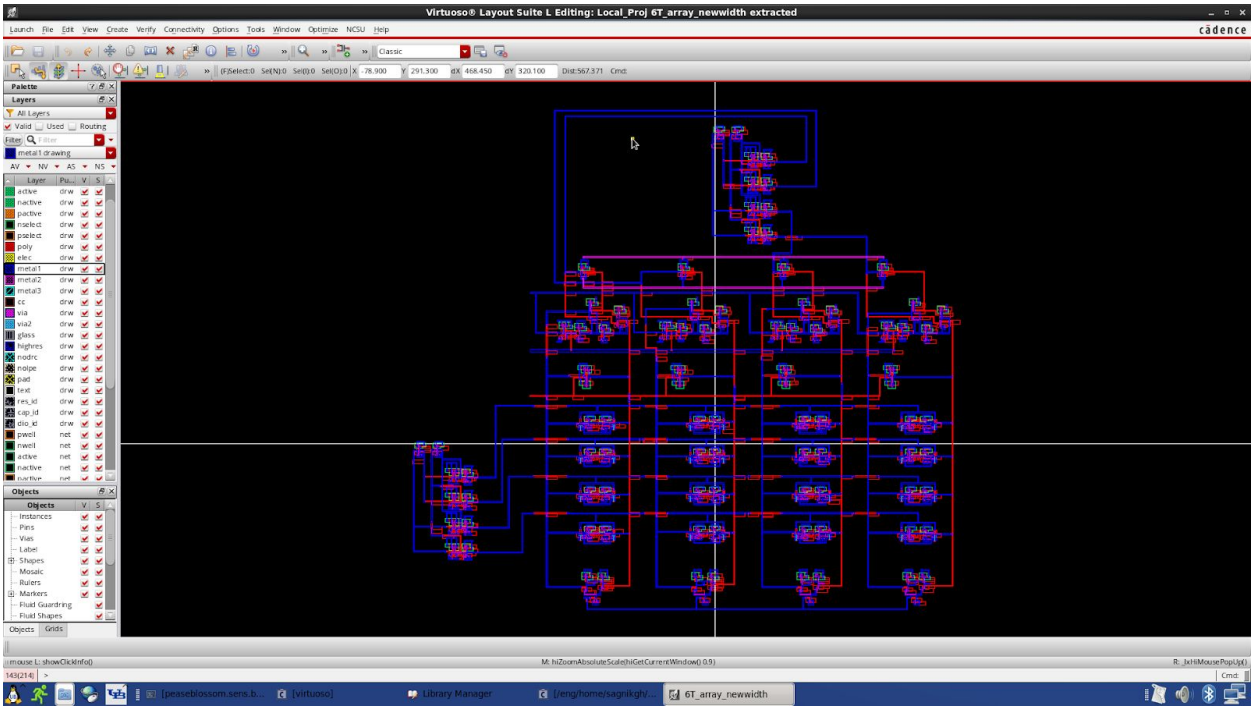
- ## 4X4 MEMORY ARRAY USING 6T SRAM CELL



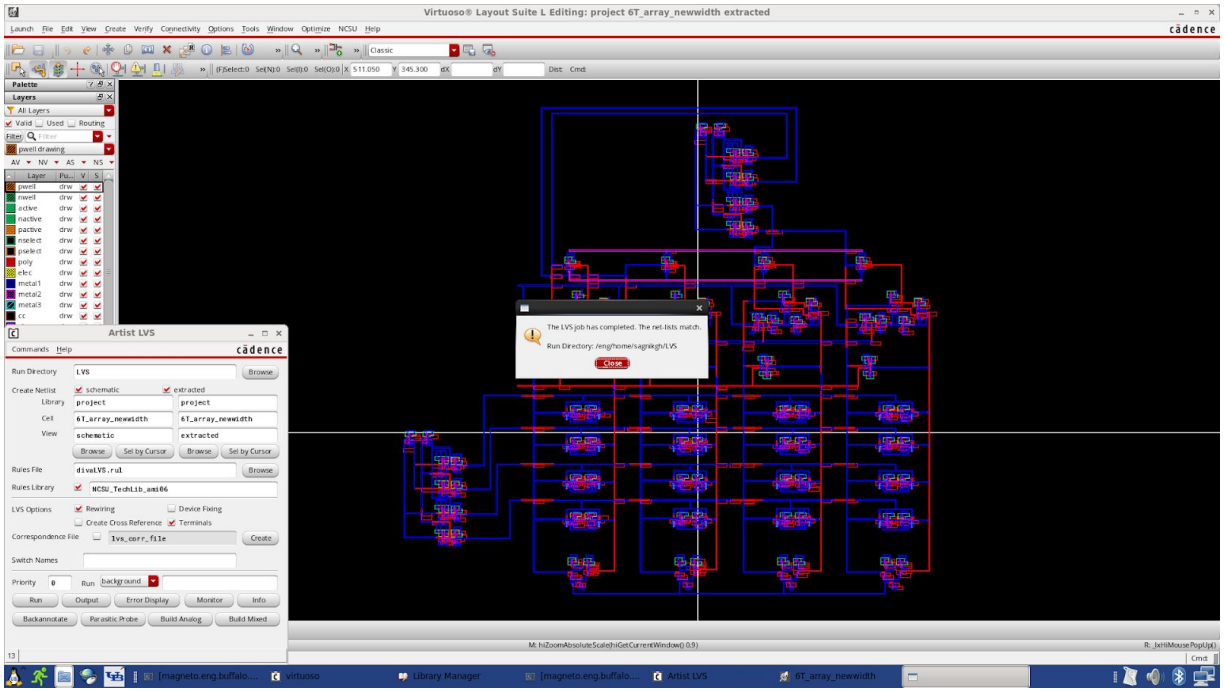
Schematic Diagram



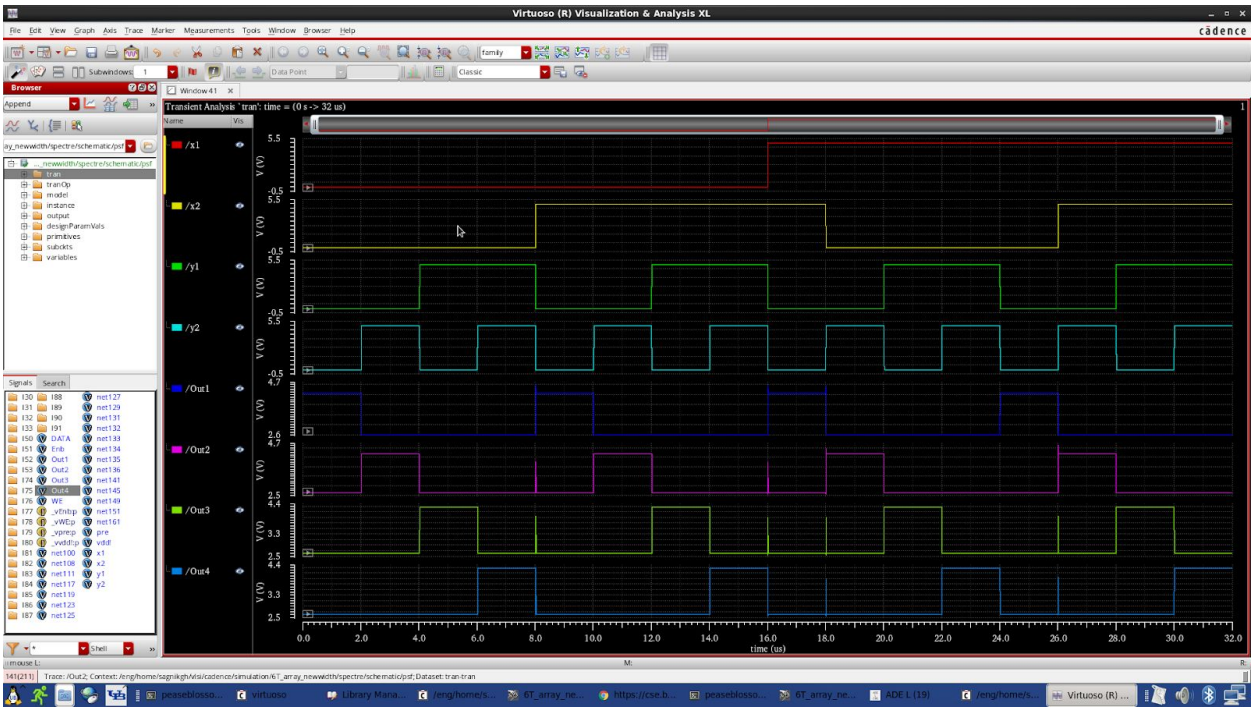
Layout View



Extracted View

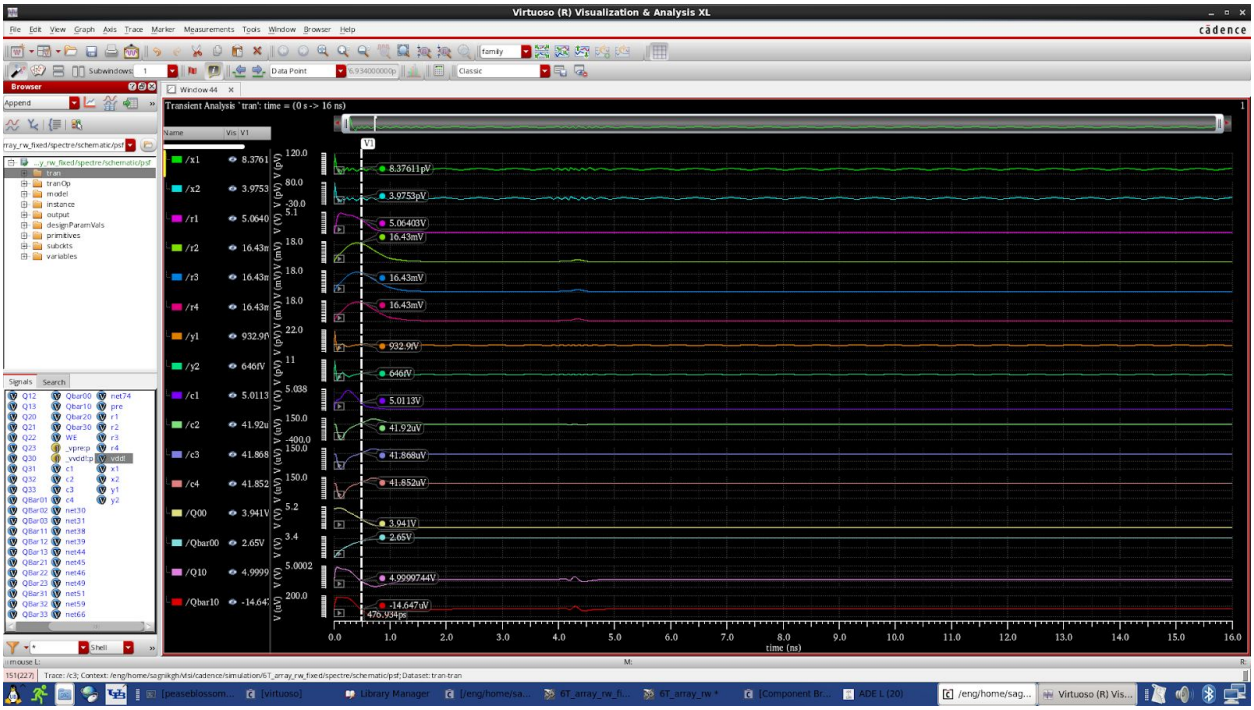


LVS Match

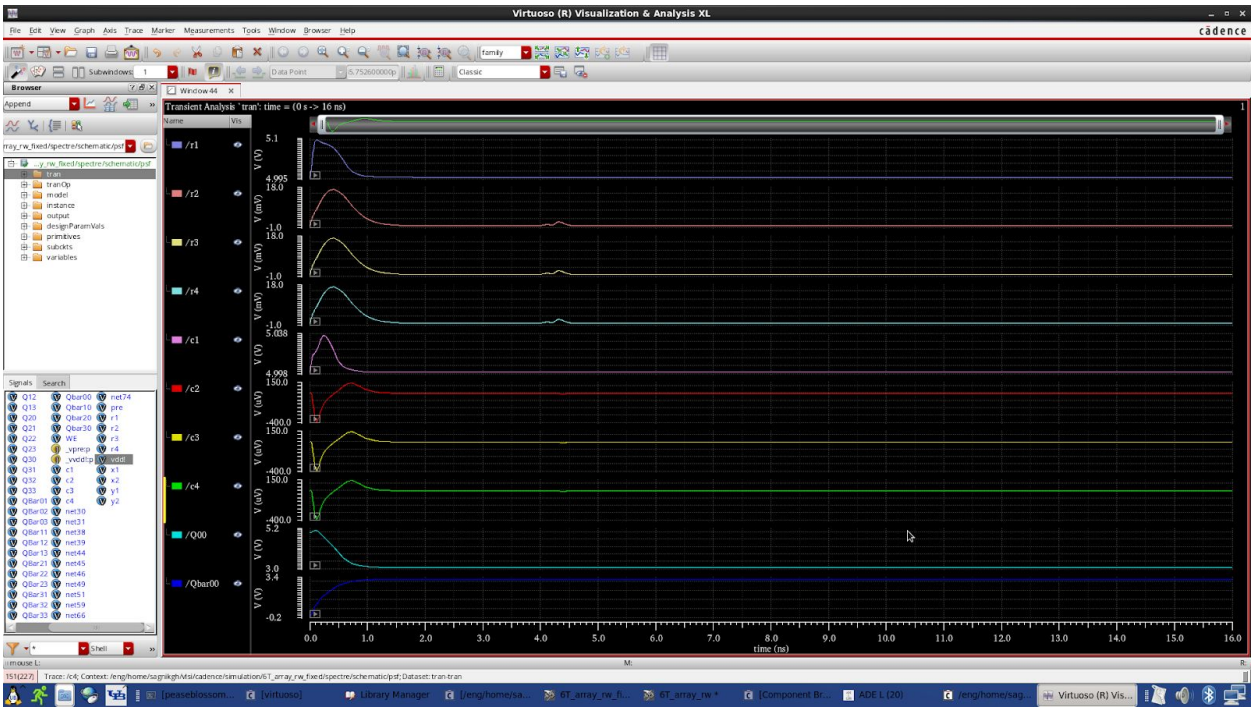


Simulation

The above simulation explains the working of the SRAM array and the address decoders. When both x1 x2 are low first row and first column is selected and so on. When x1= 0 and x2 = 1, second column is selected and so on. Similarly when y1 = y2 = 0 first column is selected and so on.



Simulation (Write Circuit)



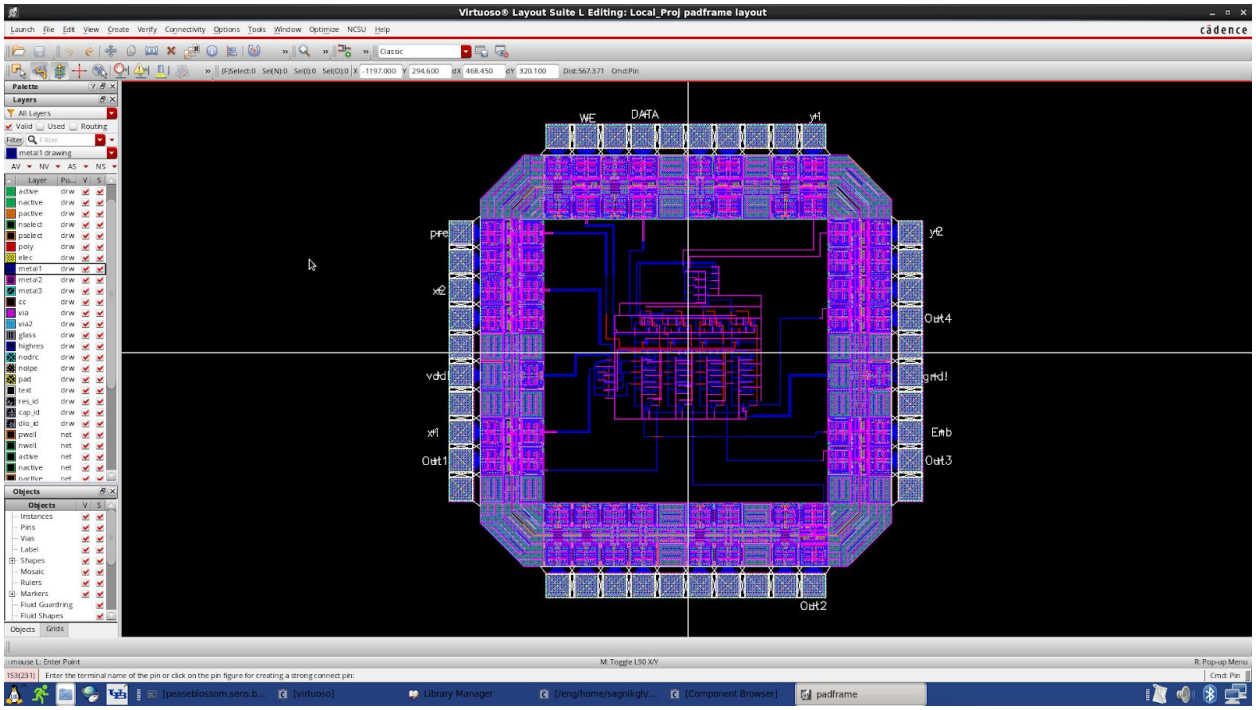
Simulation (Write Operation - Cell 00)

Above simulation explains the write operation of the SRAM array, when all inputs of the address decoders are low (x1=x2=y1=y2=0) then the top left cell is activated and as it is visible, write operation is happening in that particular cell only .

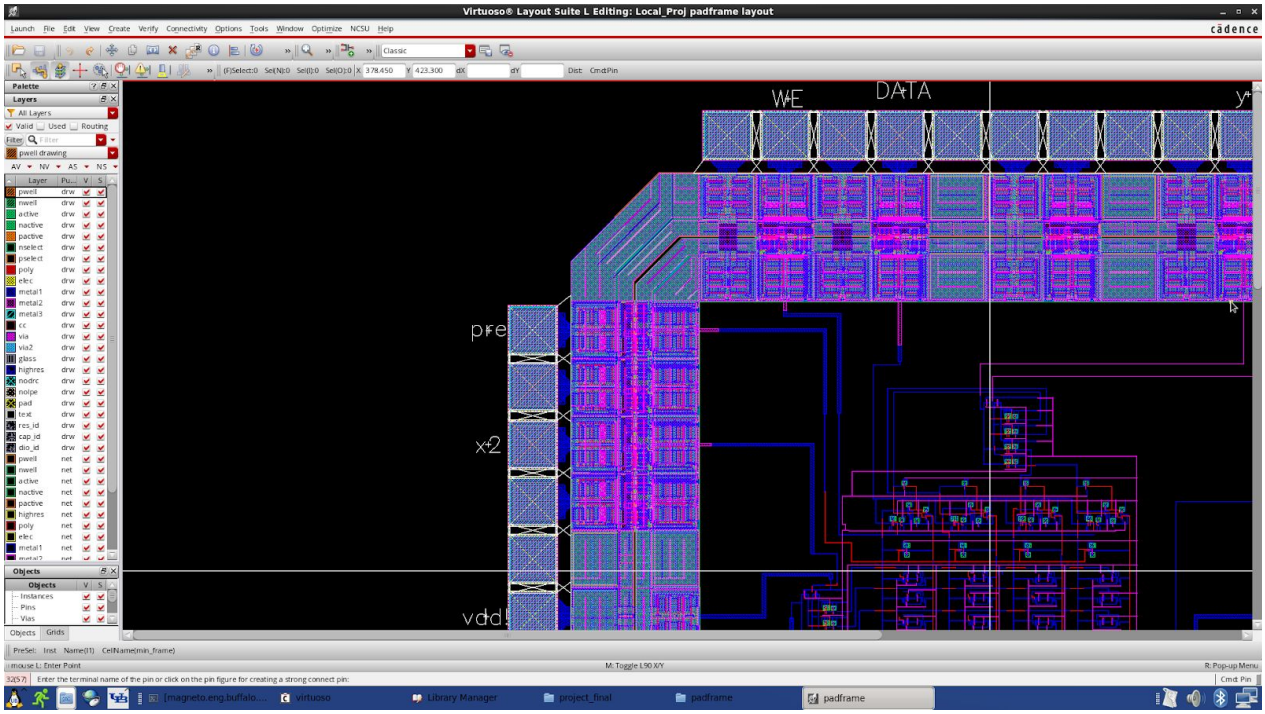
Simulation (Write Operation - Cell 00 Vs. Cell 10)

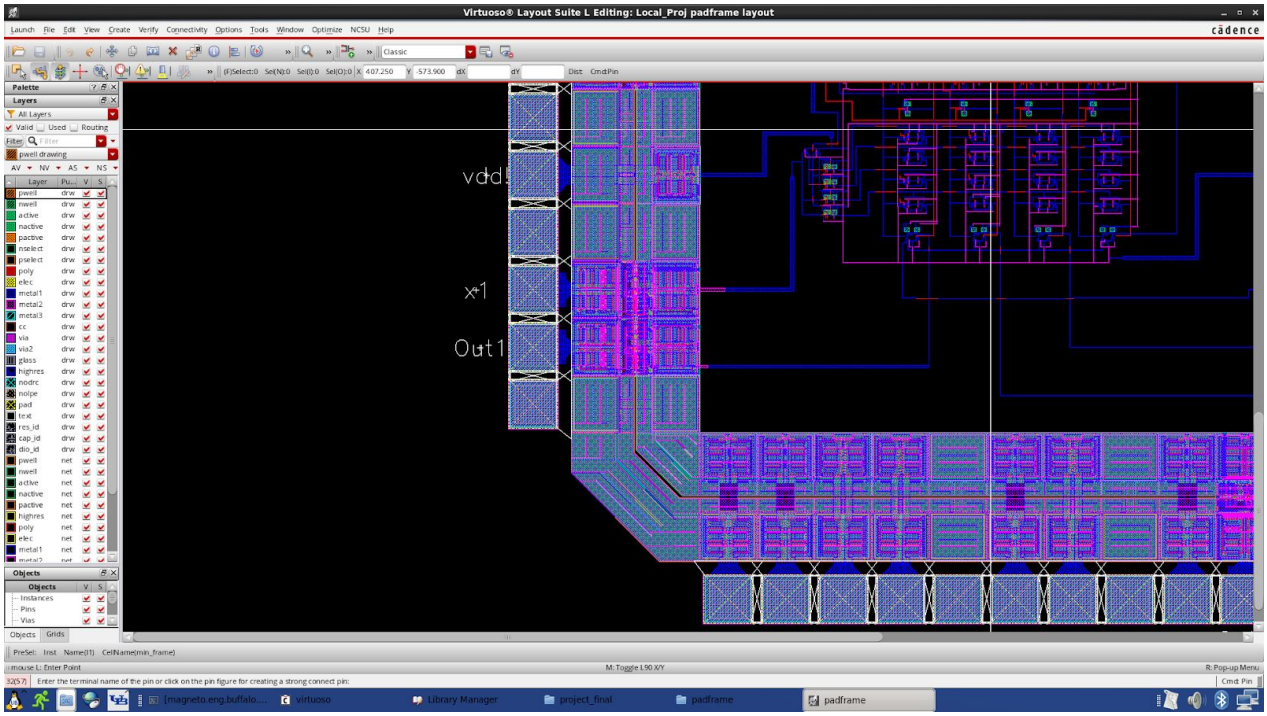
This is the comparison of two cells of the same column. This diagrams describes that while writing to a particular cell, other cells are unaffected.

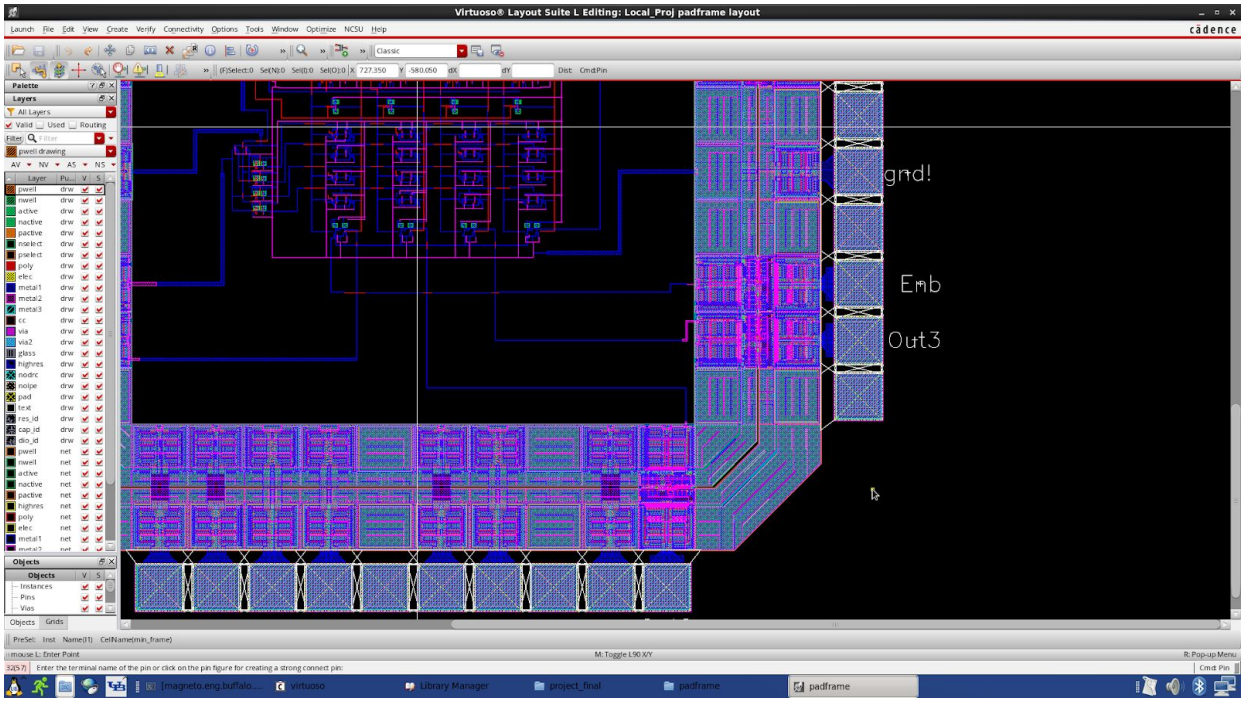
- ## 4X4 MEMORY ARRAY FITTED IN PADFRAME

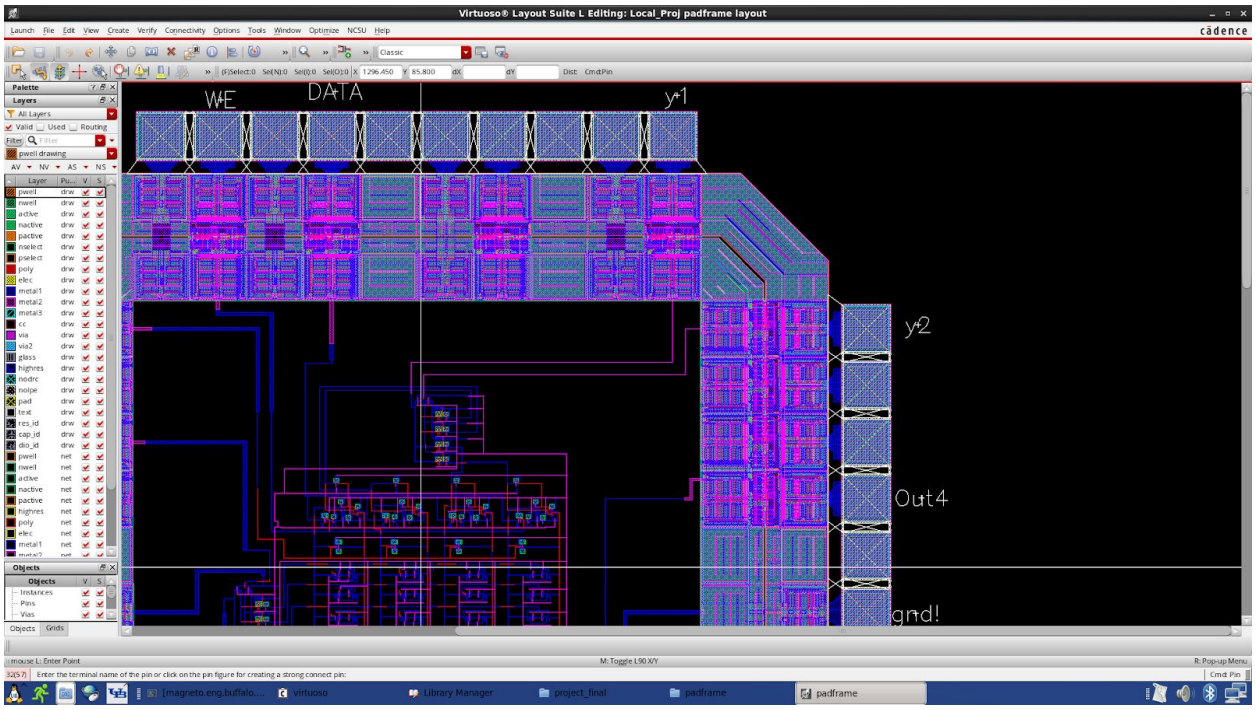


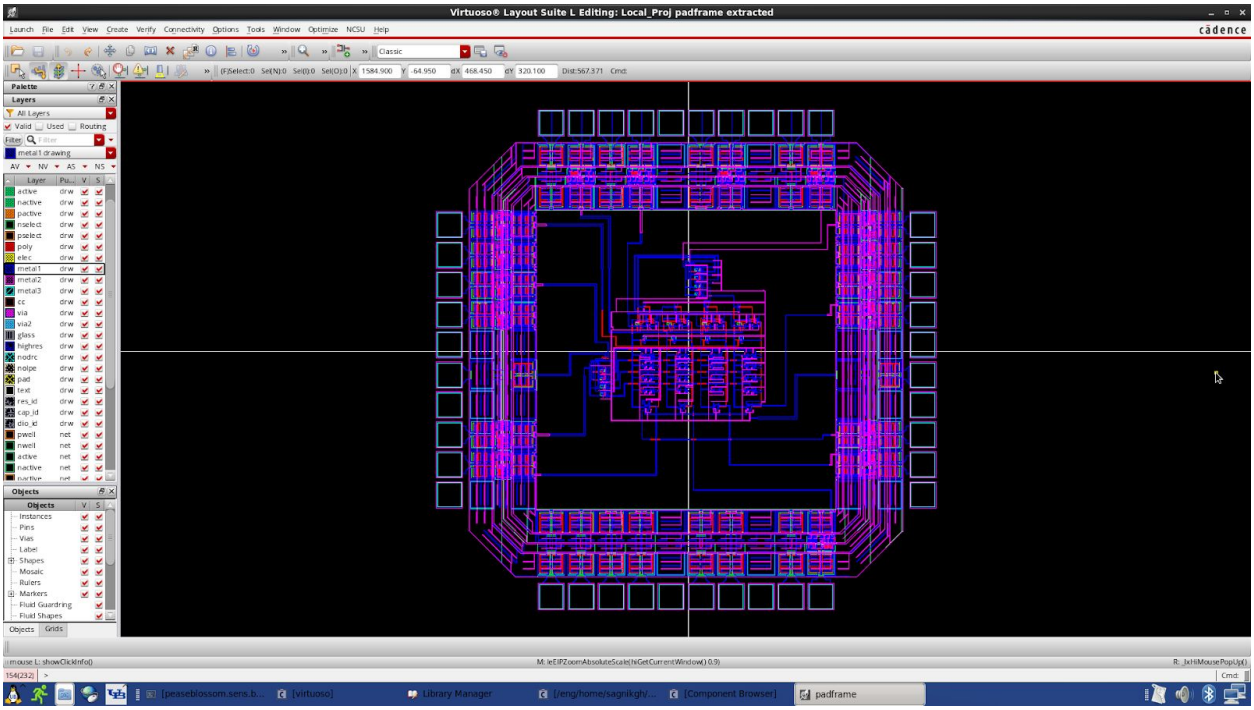
Layout View


Virtuoso® Layout Suite L Editing: Local_Proj padframe layout
WE
DATA
pre
x2
vdd!

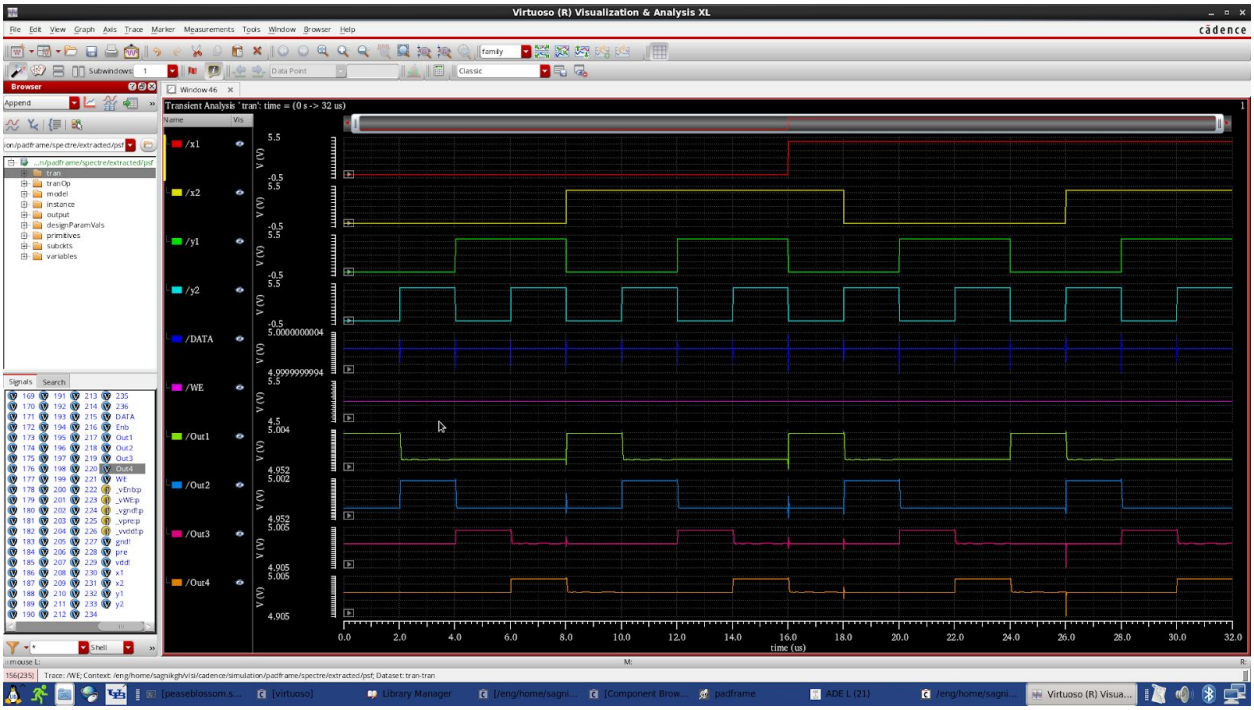

Virtuoso® Layout Suite L Editing: Local_Proj padframe layout
vdd!
x1
Out1


Virtuoso® Layout Suite L Editing: Local_Proj padframe layout
gnd!
Emb
Out3


Virtuoso® Layout Suite L Editing: Local_Proj padframe layout
WE
DATA
y1
y2
Out4
gnd!



Extracted View



Simulation

Above is the simulation of the 6T SRAM array circuit fitted in the pad frame, as it is visible, the waveform is similar to the simulation waveform of the circuit without the padframe.When both x1 x2 are low first row and first column is selected and so on. When x1= 0 and x2 = 1, second column is selected and so on. Similarly when y1 = y2 = 0 first column is selected and so on.

FUTURE SCOPE:

•Apart from storage, this architecture can also be used for Machine Learning tasks and can be modified to perform classification tasks.
•For example, in order to perform image digit classification on the popular MNIST dataset, we can develop a specialized component called the Word-Line DAC.
•It is connected to each word-line in the array (at each row) and it converts the features obtained from digital values to analog voltage
•A binary linear classifier is based on taking inner product between input feature vectors and a weight vector "w"
•Initially weight matrix is stored in the SRAM array. Then all WLs are driven at once with the feature values obtained from data-set in order to perform inner product and get the desired classification

CONCLUSION

The schematic is designed for storage capacity of 16bits i.e. 4x4 Memory array. The complete array which includes peripheral components such as memory bit cell, write driver circuit, pre-charge circuit, Sense amplifier are designed and integrated. The functioning of various components within the array and how they are enabled was understood.

The relation of one component with the other and how they function as a whole was learnt.

REFERENCES

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