# PROJECT 3: BJT BASED AMPLIFIERS

*ELEC ENG 2EI4 - Electronic Devices and Circuits I*

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1. Project Overview

   "Design, simulate, and build an amplifier that can take an input of ±0.5V from a source with an internal resistance of 100 Ω and deliver it to a 100 Ω load with good linearity and less than 10% attenuation." [1]

2. Design Guidelines/Criteria

   a) For my choice of transistor, I decided to choose a single BJT, specifically the 2N3904 NPN BJT. One of the main reasons is the fact that it was available in our kits and is simpler to implement and use in the design, as although a MOSFET is usable, considering that our kit has a MOSFET IC, wiring and implementing the build could become complex, so a BJT would suffice. Secondly, BJTs are known to have a higher transconductance than MOSFETs, which would allow for a better voltage gain which is what we're looking for in this project, considering that we're constructing an amplifier. As seen in **Figure 1**, the calculated transconductance ($g_m$) for this transistor was approximately 990 ms, which is fairly high and out of the range of MOSFETs, but more attainable for BJTs. Additionally, considering that our input voltage is ± 0.5 V, a MOSFET may not fully operate in the active region efficiently. Lastly, BJTs require less current due to their overall improved linearity, which is required for this design.

   b) In terms of amplifier topology, I decided to use the Common Collector (CC) type, as there is little to no voltage gain between the input and

output, and given the load resistor to be 100 Ω, it fits the Common Collector design guide, as the load resistor is typically a very low value.

c) The values of the load ($R_L$) and series ($R_S$) resistance were given, which was 100Ω. For the values of the two capacitors, they were given which was 10μF, and for the two resistors, $R_1$ and $R_2$, their criteria was for them to be a large value, which was chosen to be 10KΩ.

The calculated input resistance ($R_{IN}$) using the formulas given was calculated to be greater than or equal to 3.33kΩ. Using values of current gain ($\beta$), which was found using the 2N3904 data sheet [2], the common-base current gain ($\alpha$), and $g_m$ (transconductance), were calculated using the given formula, and the value of collector current ($I_C$) from the 2N3904 data sheet.

The gain (G) was calculated by using the formula in **Figure 1**, giving a theoretical gain of approximately 0.97, which was an acceptable value and fell within the 10% actuation range.

The signal swing was also confirmed and validated with the numbers provided and calculated, proving that the design-build with those numbers was valid and would meet the design criteria.

To confirm and validate these results, Gain (G) can be calculated using:

$$G = \frac{V_{OUT}}{V_{IN}} \geq 0.90$$

With input resistance ($R_{IN}$) being calculated and verified by:

$$R_{IN} = \frac{V_{IN}}{I_{IN}} \geq 3330\ \Omega$$

1. $g_m$

$|V_{in}| = (0.2)(x)(1 + g_m R_L)$ ➡ $x = V_t = 25\ mV$ (RST)

$|0.51| = (0.2)(25 \cdot 10^{-3})(1 + g_m(100))$

$\left(\frac{0.5}{(0.2)(25 \cdot 10^{-3})} - 1\right) \div 100 = g_m$

$g_m \geq 0.99\ S$

$g_m \geq 990\ mS$

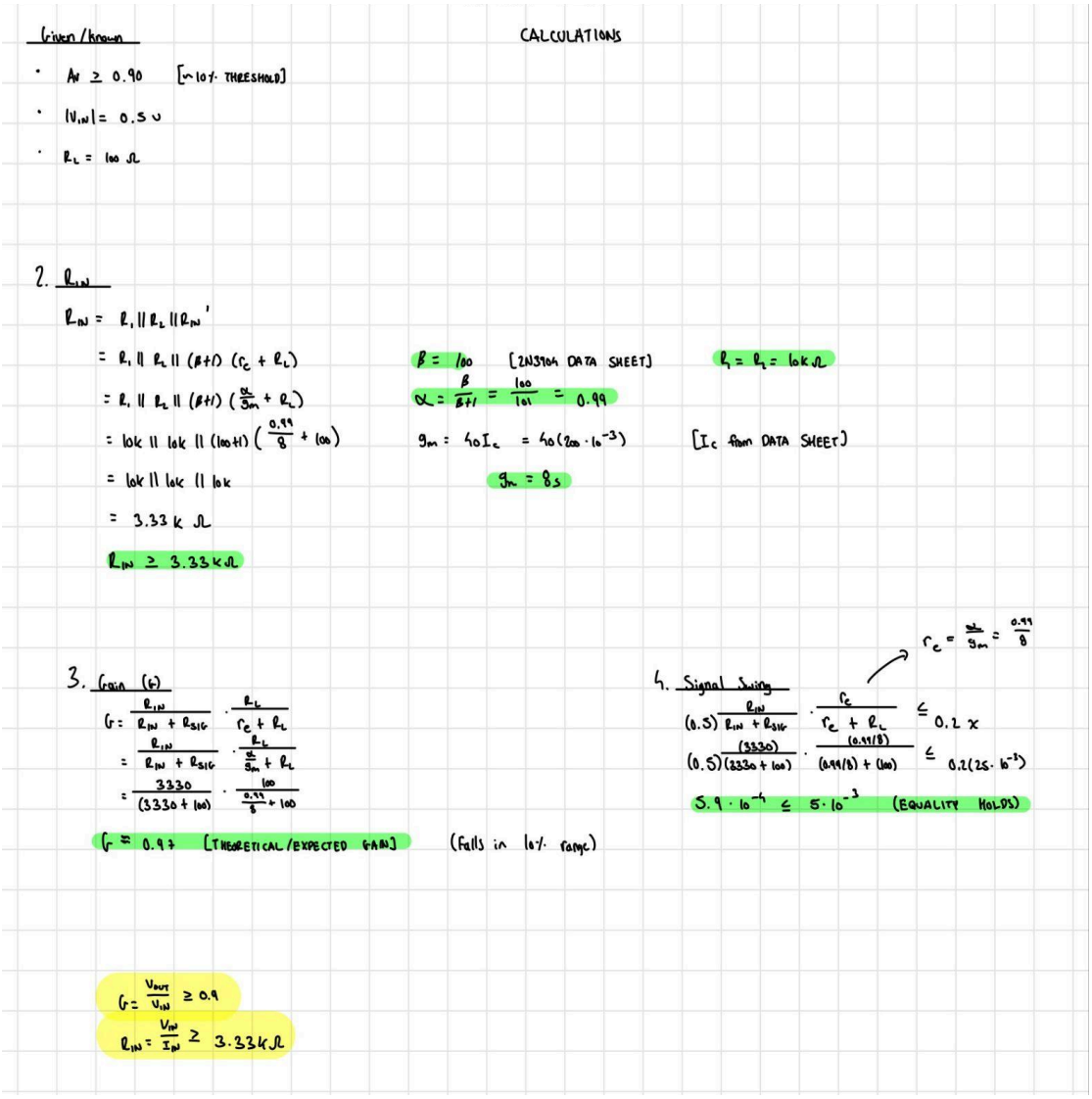



**Figure 1**: Calculations to implement design guide

3. Circuit Schematic & Simulations

    a. LTSpice has NPN BJTs in its software, and to specify my selection, 29N3904, I listed it in the BJT name (**Figure 2**) and it behaved and performed accordingly and as expected.

    b. For simulation settings, the input voltage source had a sinusoidal wave, with a DC offset of 0, amplitude of 0.5 V, which adheres to the project requirements, and a frequency of 1000 Hz (1 kHz).

    For the actual simulation, I decided to use a transient analysis, with a runtime of 5ms, and given that my chosen frequency was 1000 Hz, the simulation would run for 5 cycles. Additionally, I chose no step time, as LTSpice would give the most accurate and appropriate scale for the graph. I chose these parameters as they have worked in previous projects and LTSpice simulations and gave accurate data for this project as well.

    c. Considering the circuit schematic simulation (**Figure 2**), gain can be calculated using the formula from **Figure 1** and the values from **Figure 3**.

$$G = \frac{V_{OUT}}{V_{IN}} \geq 0.90$$

$$G = \frac{(0.482)}{(0.50)}$$

$$G = 0.964$$

$$G = 0.964 \geq 0.90$$

The resistance was calculated to be 4307 Ω, which met the greater than or equal to the value of 3330 Ω.

d. Input resistance ($R_{IN}$) was calculated using the numbers from **Figure 4**:

$$R_{IN} = \frac{V_{IN}}{I_{IN}} \geq 3330\ \Omega$$

$$R_{IN} = \frac{(0.50)}{(116.1\ \mu A)}$$

$$R_{IN} = 4307\Omega$$

$$R_{IN} = 4307 \geq 3330\ \Omega$$

The $R_{IN}$ value fits the parameter that was set, further proving this design is implemented correctly.

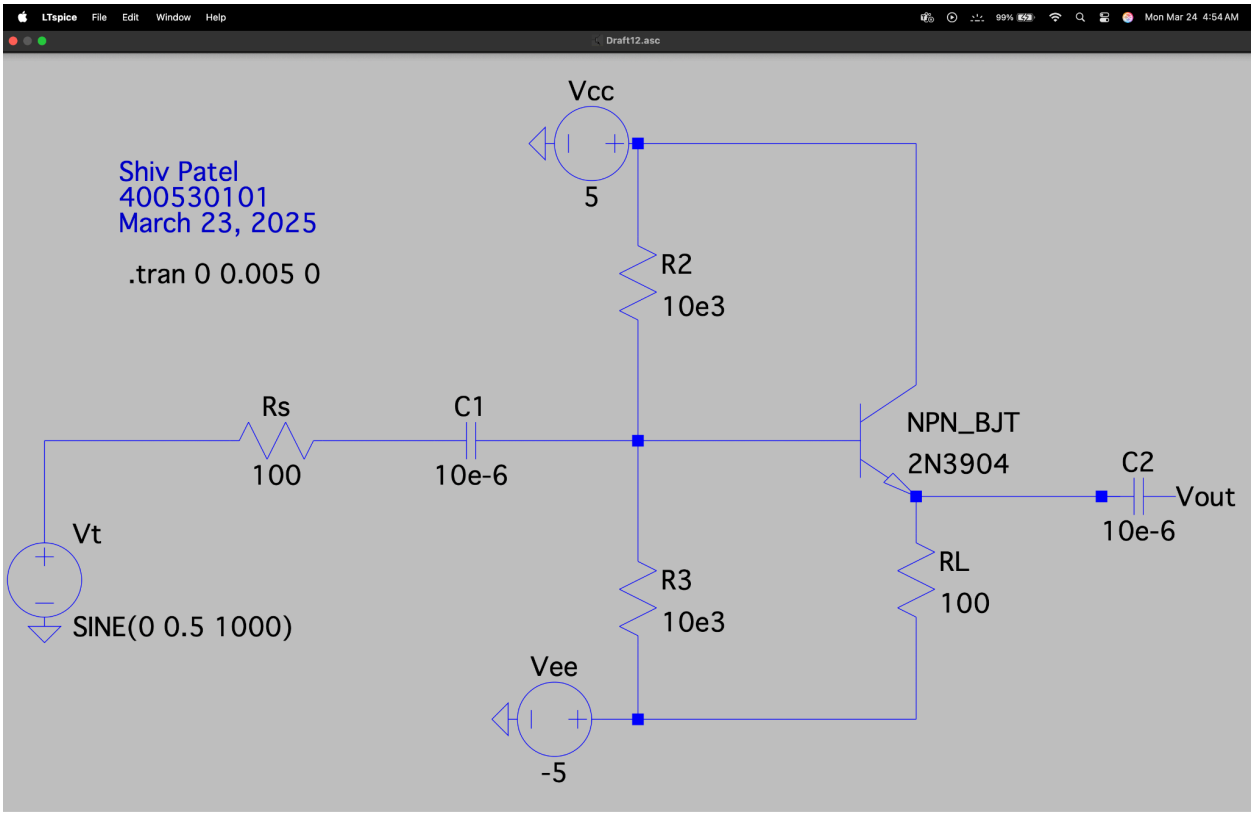



**Figure 2**: Circuit schematic on LTSpice (with the date of screenshot)

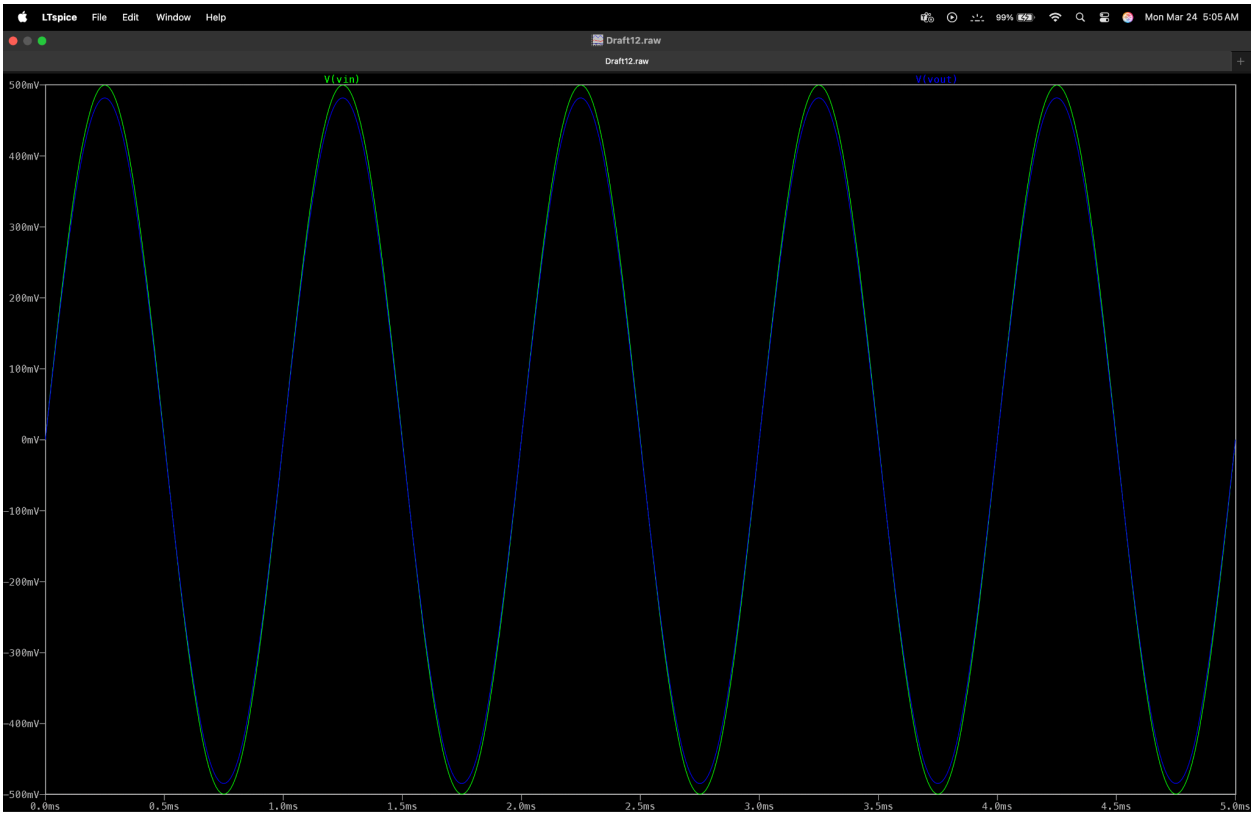



**Figure 3**: Circuit simulation on LTSpice (with the date of screenshot)

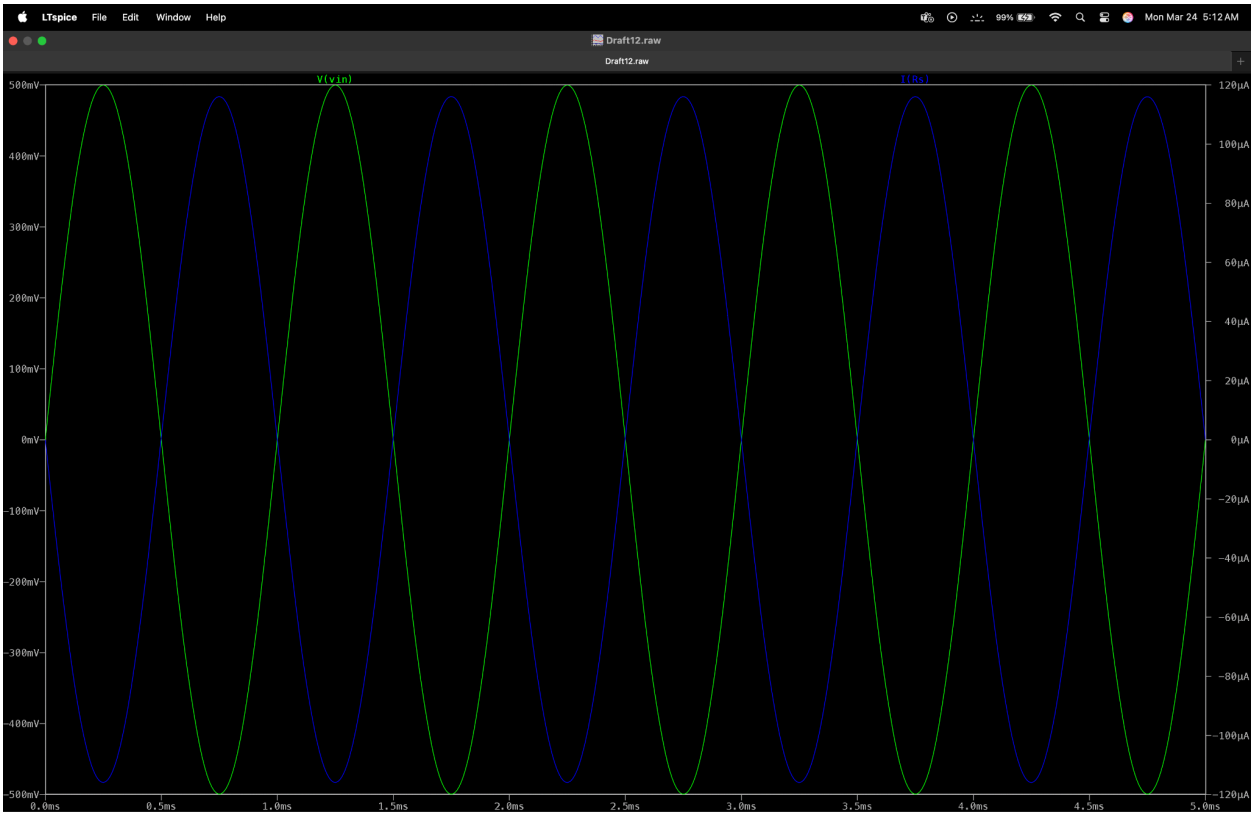



**Figure 4**: Circuit simulation on LTSpice with $I_{IN}$ (with the date of screenshot)

4. Physical Circuit

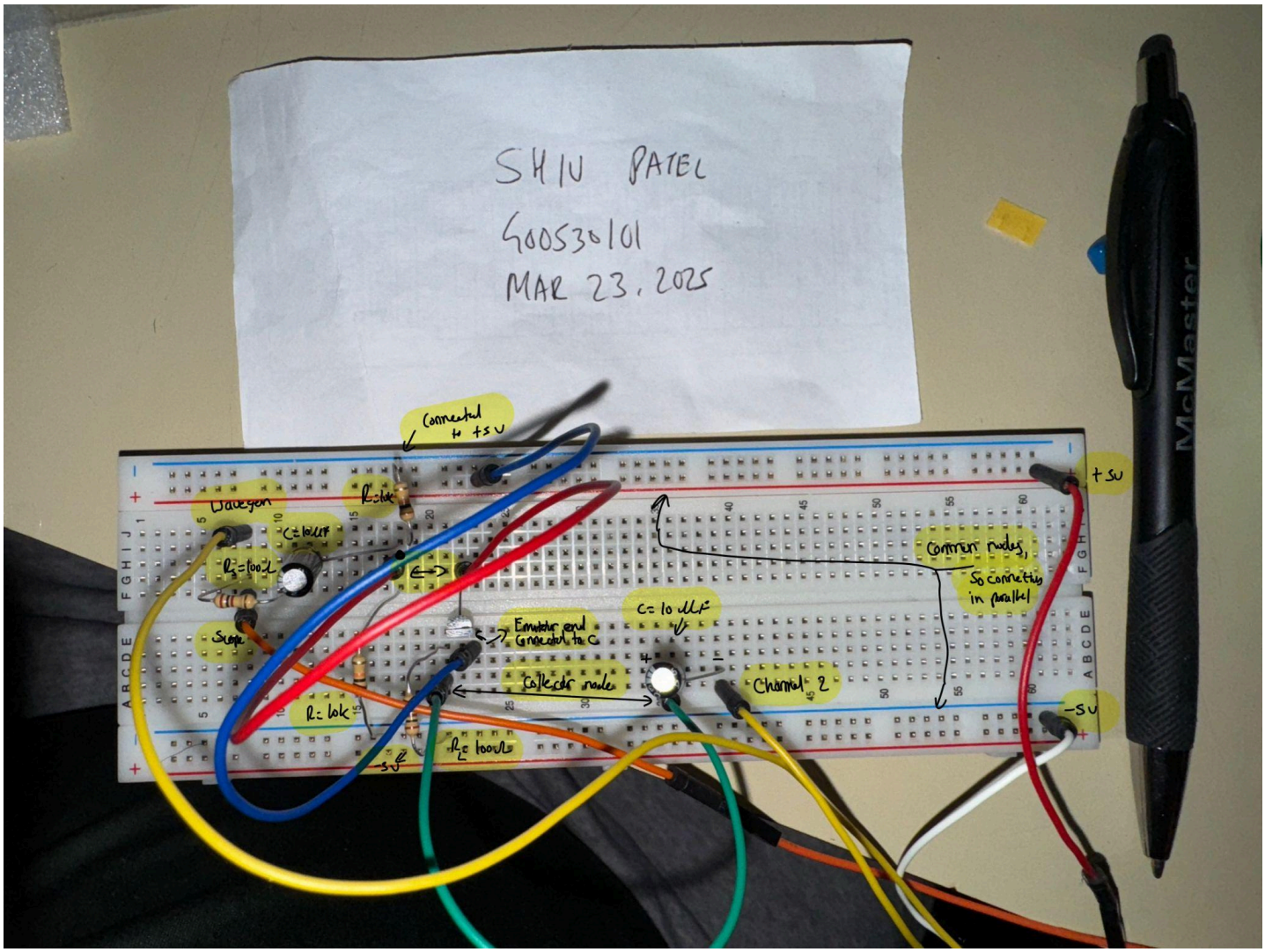



**Figure 5**: Physical Circuit Build (with labeling)

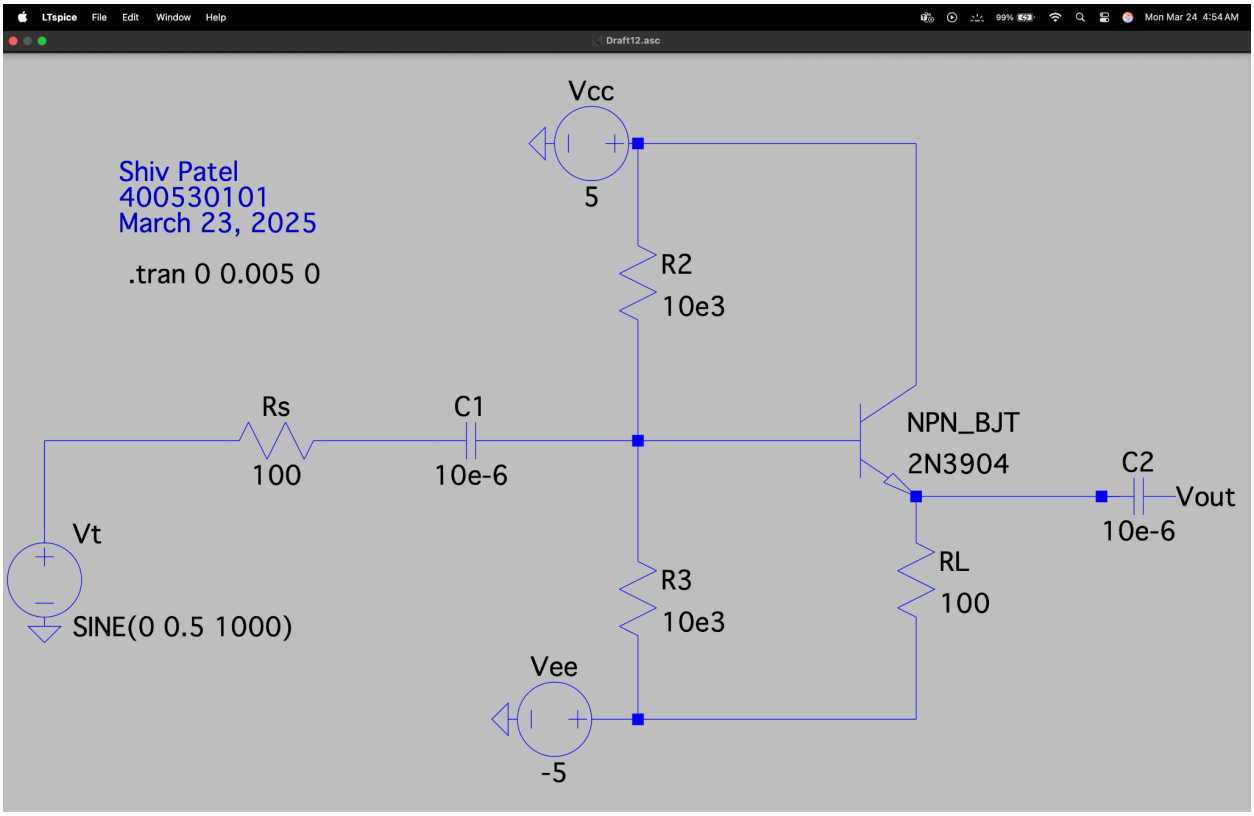



**Figure 2**: Circuit schematic on LTSpice (with the date of screenshot)

5. WaveForms Simulation

    a. For the physical simulation, I generated a sinusoidal wave as seen in **Figure 6** with the same settings as the simulation, followed by a ± 5 V supply (**Figure 7**). To obtain and verify the results, I used the scope feature, as it allowed me to simultaneously check both channels of $V_{IN}$ and $V_{OUT}$ and ensure they were similar and accurate (**Figure 8**). Additionally, the scope feature also has a measurements tab, which gives automatic values of peak-to-peak voltage, maximums, minimums, and frequency, of each channel, which was straightforward to compare and contrast between the two channels. The phase angle, which was added through a custom global measurement, was measured to be around 0.53°, which shows there is some discrepancy and not complete linearity (which was visible as channel 2's voltage did not reach 0.5 V), but the deviation isn't too drastic.

    b. For the midband gain, using the measurements feature on the scope, I was able to do a single run after allowing the circuits to reach a steady state and allow the capacitors to charge up. Then, I was able to use the peak value for channel 2, which represented $V_{OUT}$ and the same for channel 1, which represented $V_{IN}$, and was able to use the formula determined in **Figure 1**. Using the values from the single run in **Figure 8**:

$$G = \frac{V_{OUT}}{V_{IN}} \geq 0.90$$

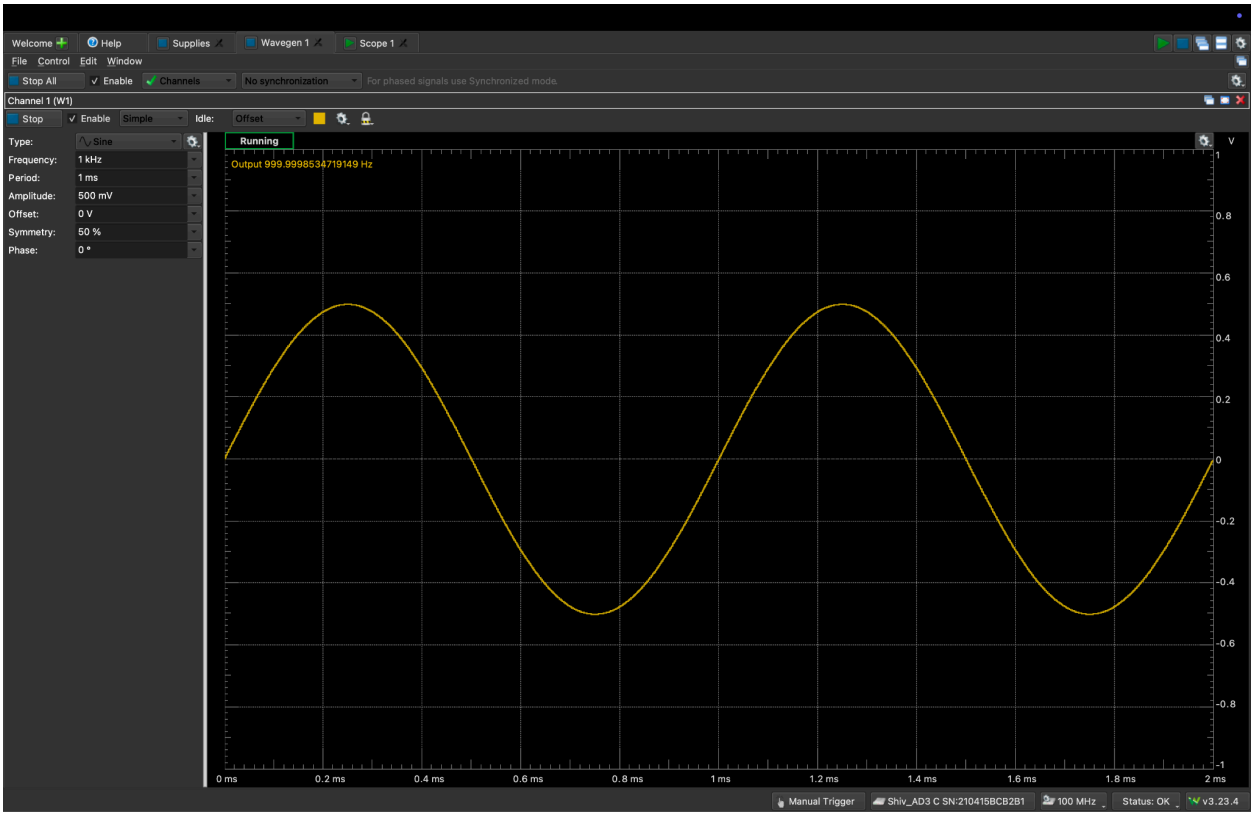
$$G = \frac{(480.37\ mV)}{(0.50)}$$

$$G = 0.961$$

$$G = 0.961 \geq 0.90$$

Comparing the real circuit results to the simulation results, and the theoretical results, they are nearly accurate, off by the smallest margin. The gain (G) from the WaveForms simulation was calculated to be 0.961, whereas the LTSpice simulation gain was 0.964, and the theoretical was calculated to be approximately 0.97. All of these values meet the design criteria, which is having a gain of over 0.9 (or less than a 10% discrepancy), and the overall difference being of less than 4% for the physical run and simulation.

c. To demonstrate linearity at an input amplitude of 0.5 V, I used the spectrum feature on WaveForms (**Figure 9**). An input amplitude of 0.5 V is the equivalent of -50 dBV and on that graph, both channels have an identical shape, proving linearity. Although the graph of channel 2 is shifted up, this could be due to a gain difference, which is possible as the gain was not completely 1 and the maximum voltage for channel 2 was measured at approximately 0.480 V. But in terms of linear, yes linearity is proven, as both graphs are within the appropriate range and have an identical output with little to no abnormal spikes.



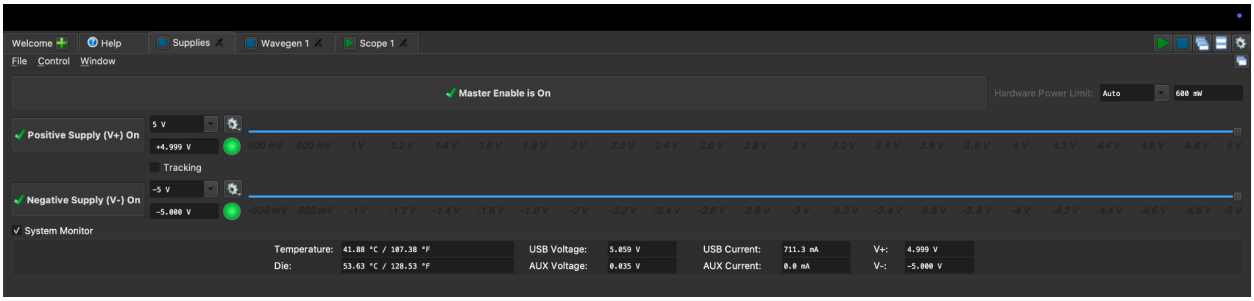




**Figure 6, 7:** WaveForms Configuration Screenshots

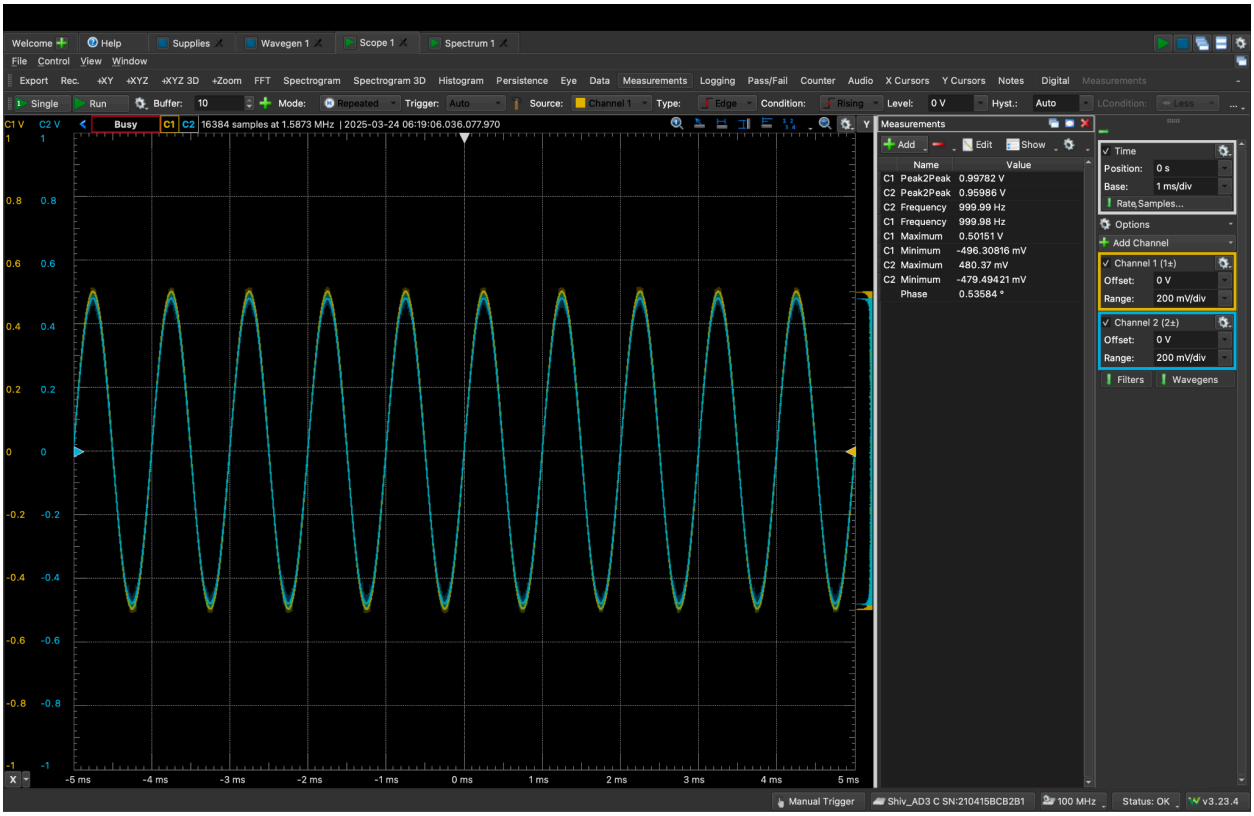



**Figure 8:** WaveForms Wavegen Screenshot

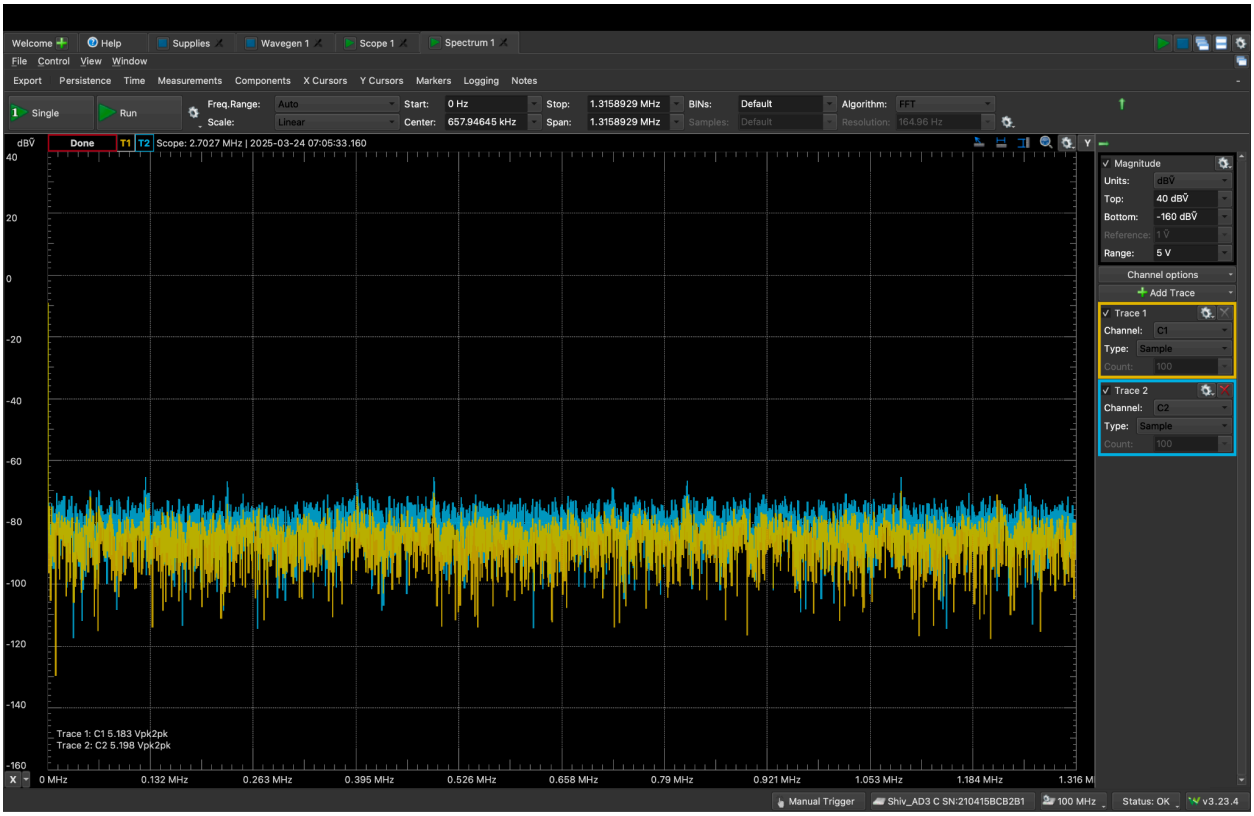



**Figure 9:** WaveForms Spectrum Screenshot

**References**

[1] ELEC ENG 2EI5: Design Project #3. Accessed: March 23, 2025. [Online]. Available: https://avenue.cllmcmaster.ca/d2l/le/content/638927/fullscreen/5010089/View.

[2] STMicroelectronics, BJT Data Sheets - 2N3904. Feb. 2003. Accessed: March 23, 2025. [Online]. Available: http://www.st.com.