In the Name of God

Logical Circuit Design

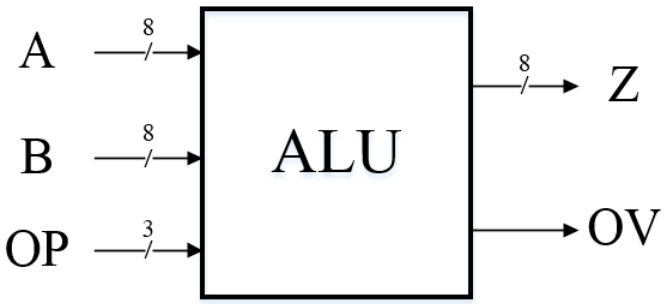
(396-1)

Project:

ALU Design with Verilog HDL

Project Description

In this project you're supposed to design an ALU which operates on two 8 bit numbers, A and B, and gives the result as an 8 bit number Z. The ALU has a 3 bit input signal OP which specifies which operation should be done on the two inputs. In addition to the output Z, there is a 1 bit OV output which becomes 1 if there is an overflow in the addition or subtraction, and zero otherwise.



Design your ALU based on the table below.

OP	Operation
0	Z = A+B
1	Z = A-B
2	Z = max(A,B)
3	Z = min(A,B)
4	Z = A<<<2
5	Z = B >>>3

* >>> and <<< are arithmetic shift to right and left operators, respectively.

Notes:

- The module declaration should be as follows

```
module ALU(A,B,OP,Z,OV);
    input [7:0] A,B;
    input [2:0] OP;
    output [7:0] Z;
    output OV;

    //the body of the module

endmodule
```

- You should provide one Verilog code containing your ALU module and the testbench.

- The codes and the validity of your design will be checked in-person, some days after the final exam day (the exact time will be announced later).
- This project has a bonus point.

Good luck!

Shahshahani, S.M.R.