Analog Circuits EE301

PROJECT REPORT

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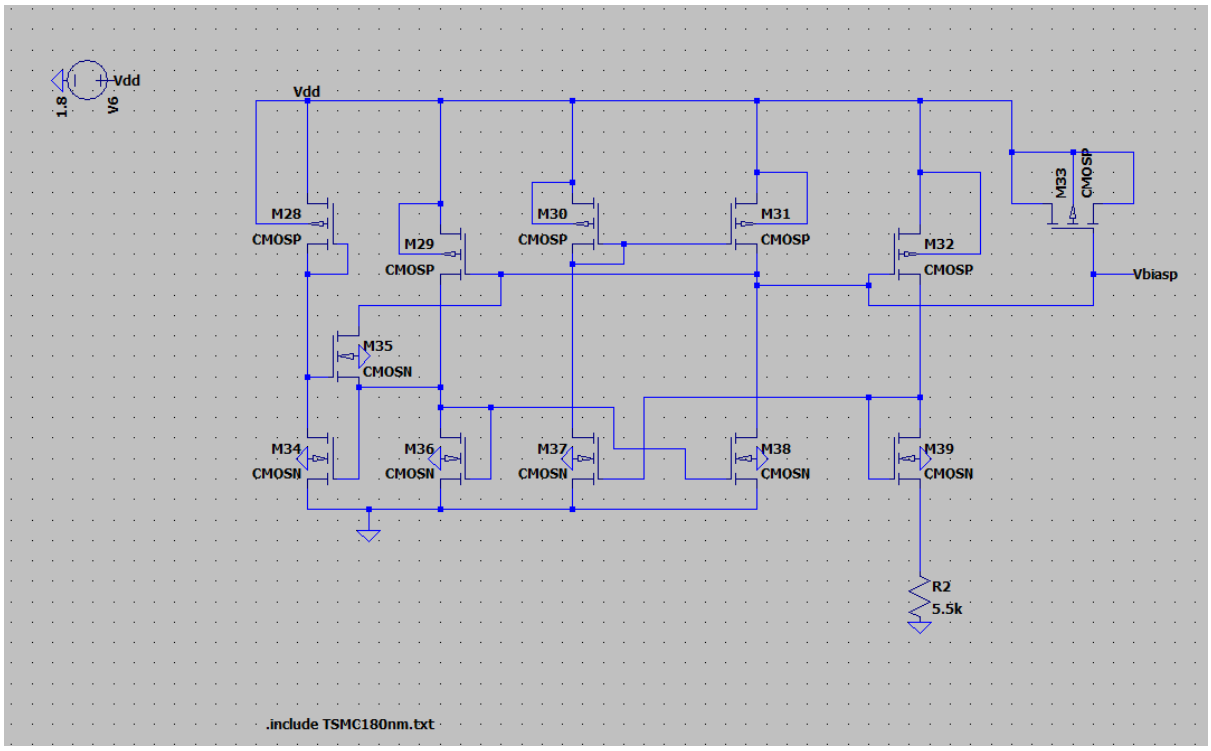
ENTRYNO: 2022EEB1191

COURSE INSTRUCTOR: Dr. Mahendra Sakare

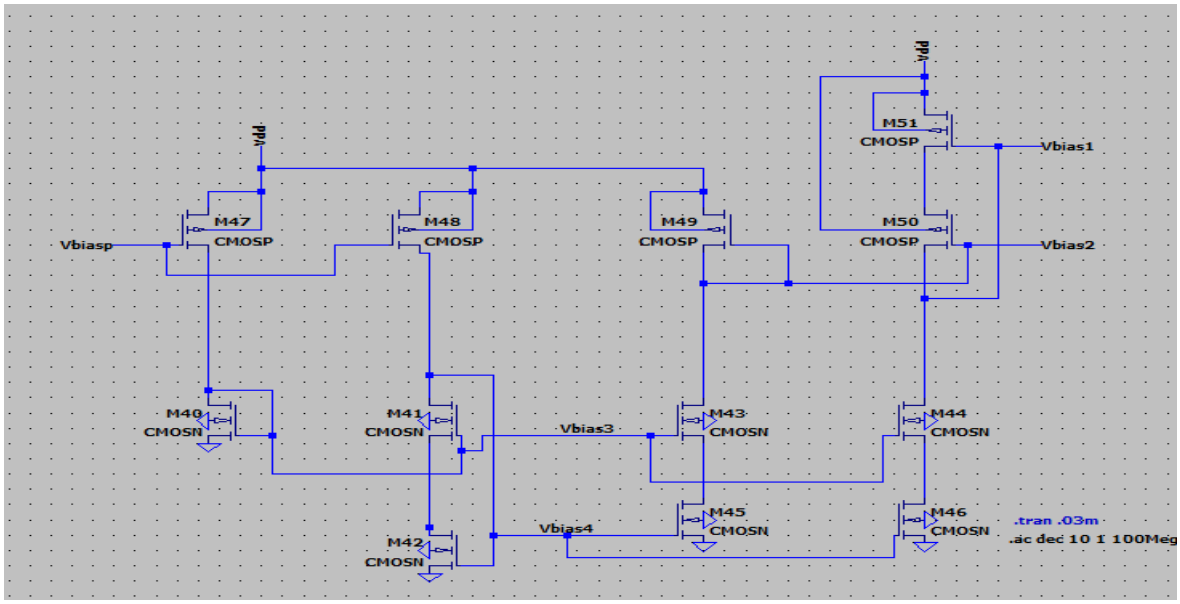
OBJECTIVE: Design of cascode amplifier and cascode current mirror in schematic and layout using LTspice or Cadence and Magic/Cadence tools in 180nm (supply 1.8V) technology and only schematic of cascode amplifier, beta multiplier and cascode current mirror in 22nm (supply 0.8V) technology node to see the effect of lowering the technology node.

LTSPICE SCHEMATICS:

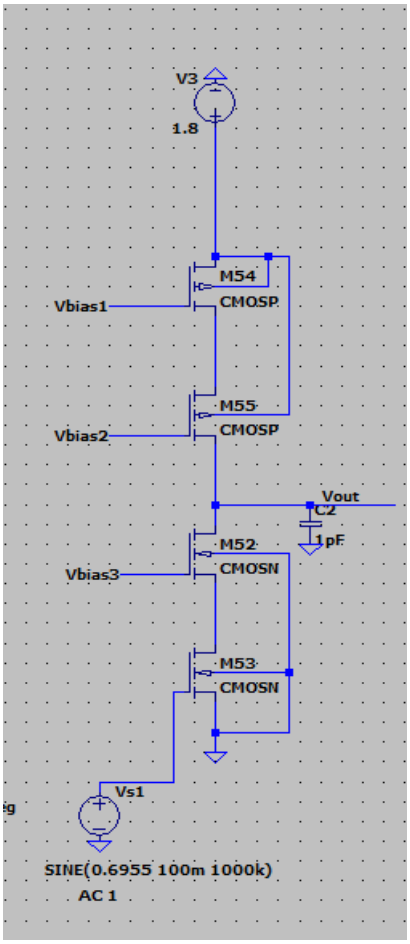
FOR 180nm txt file:



BETA MULTIPLIER

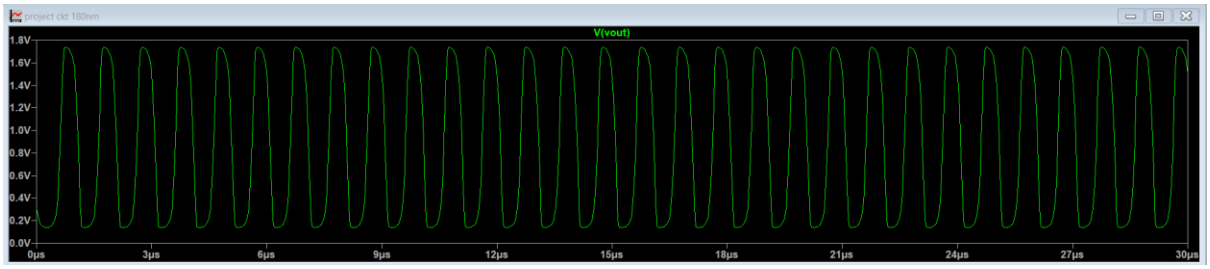


CASCODE CURRENT MIRROR

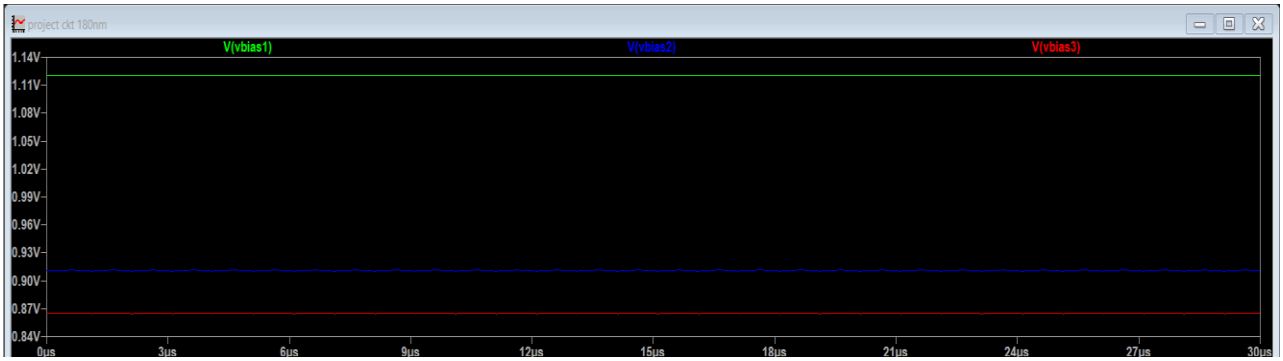


CASCODE AMPLIFIER

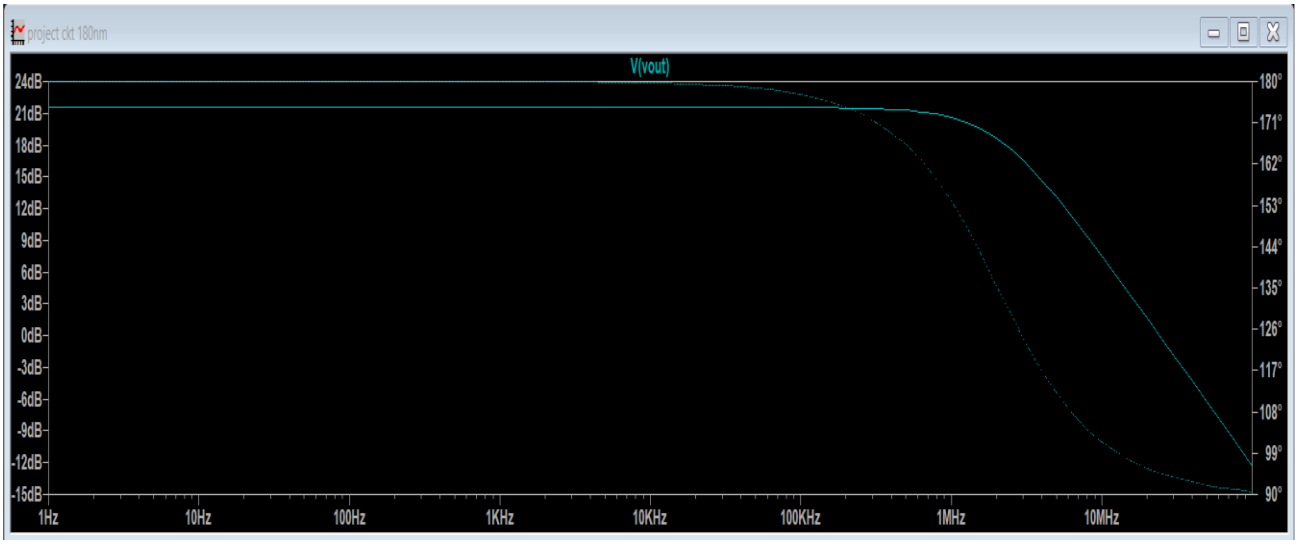
OUTPUT WAVEFORMS:



VOUT



Vbias1,Vbias2,Vbias3



GAIN FREQUENCY RESPONSE

Calculations:

The following calculations were done to find W/L ratio for Cascode Amplifier.

$\mu_p C_{ox} = 71.2\ \mu A/V^2$ gain(A_v) = 20 $V_{DD} = 1.8V$

$\mu_n C_{ox} = 350.8\ \mu A/V^2$ Load capacitance (C_L) = 1pF $\lambda = 0.09$

$V_{th} = 0.5V$

Calculation:- (for 180nm)

$$f_p = \frac{1}{2\pi R_{out} C}$$

(Suitable gain $= 20\log_{10}^{20} \approx 26dB$)

$$R_{out} = \frac{1}{2\pi f_p C}$$

Assume $f_p = 2.4MHz$ $R_{out} = \frac{1}{2\pi \times 2.4\times10^6 \times 10^{-12}} = 66,314.5\Omega$

$g_m = A_V / R_{out}$

(By considering All mosfets at saturation)

$$g_m = \frac{A_V}{R_{out}} = \frac{20}{66314.5} \Rightarrow 0.0003015\ S$$

$$g_m = \mu_n C_{ox} \frac{W}{L} V_{ov}$$

$$0.0003015 = 350.8 \times \frac{W}{L} \times 10^{-6} \times 0.2$$

$$\left(\frac{W}{L}\right)_{nmos} = 4.297$$

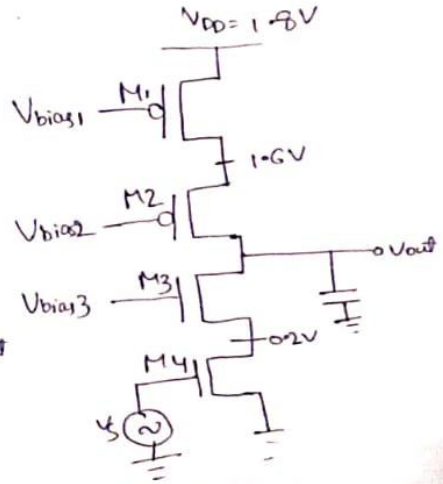
assume drop of 0.2V on each mosfet

$V_{DS} \geq V_{GS} - V_{TH}$ (saturation)

$V_d = 0.2$, $V_S = 0$, $V_{ds} = 0.2V$

$0.2 \geq V_S - V_{th}$

$V_S \leq 0.7V$ indicates input of sinewave of input is 0.7V



M_3 NMOS :-

$V_d = 0.4V$, $V_S = 0.2V$ $\quad 0.2 \geq V_{bias_3} - 0.2 - 0.5t$

$V_{bias_3} \leq 0.91$

I_d is same for all Mosfets because of saturation

$$I_d = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \times (V_{OV})^2 (1 + \lambda V_{DS})$$

$$I_d = \frac{1}{2} \times 350.8 \times \frac{\mu A}{V^2} \times 4.297 \times (0.2)^2 (1 + 0.018)$$

$$\Rightarrow 30.622 \mu A$$

As current is same for PMOS as well

$$I_D = \frac{1}{2} \mu_p C_{ox} \times \left(\frac{W}{L}\right)' V_{ov}^2 (1 + \lambda V_{DS})$$

$$30.622 = \frac{1}{2} \times 71.2 \times 0.04 \times 1.018 \times \left(\frac{W}{L}\right)'$$

$$\left(\frac{W}{L}\right)_{Pmos} = 21.1864$$

Power Dissipation $= V_{DD} \times I_D \Rightarrow 1.8 \times 30.622 \mu$

$\Rightarrow 0.0551 mW$

PMOS :-

$$V_{sd} \geq V_{sg} - |V_{tnp}|$$

$V_S = 1.6V$ $\quad V_d = 1.4V$

$0.2 \geq 1.6 - V_{bias_2} - 0.5t$

$$\boxed{V_{bias_2} \geq 0.89V}$$

for M_1 $V_S = 1.8V$, $V_d = 1.6$

$V_{Sd} = 0.2$ $\quad 0.2 \geq 1.8 - V_{bias_1} - 0.5t$

$$\boxed{V_{bias_1} \geq 1.09V}$$

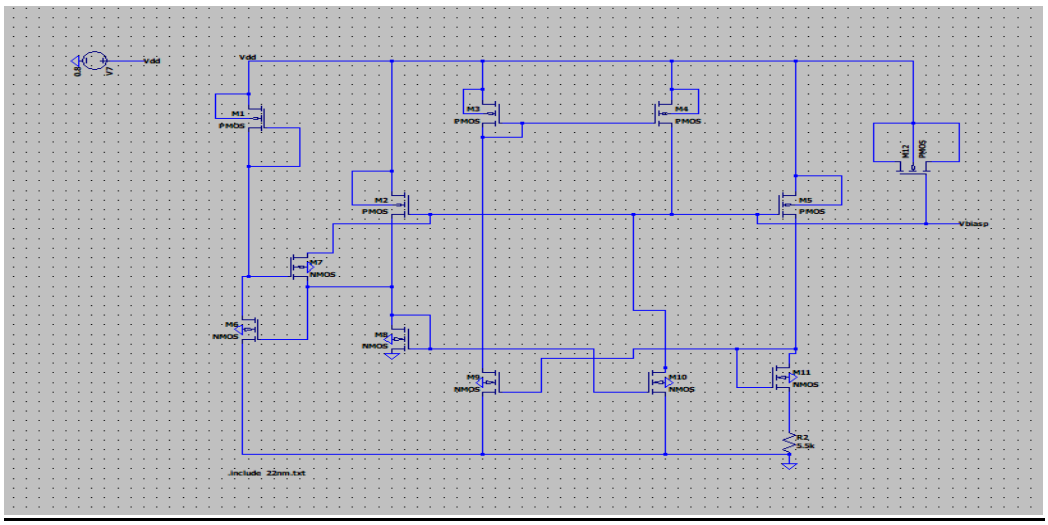
Simulation Results and Theoretical Values For 180nm:

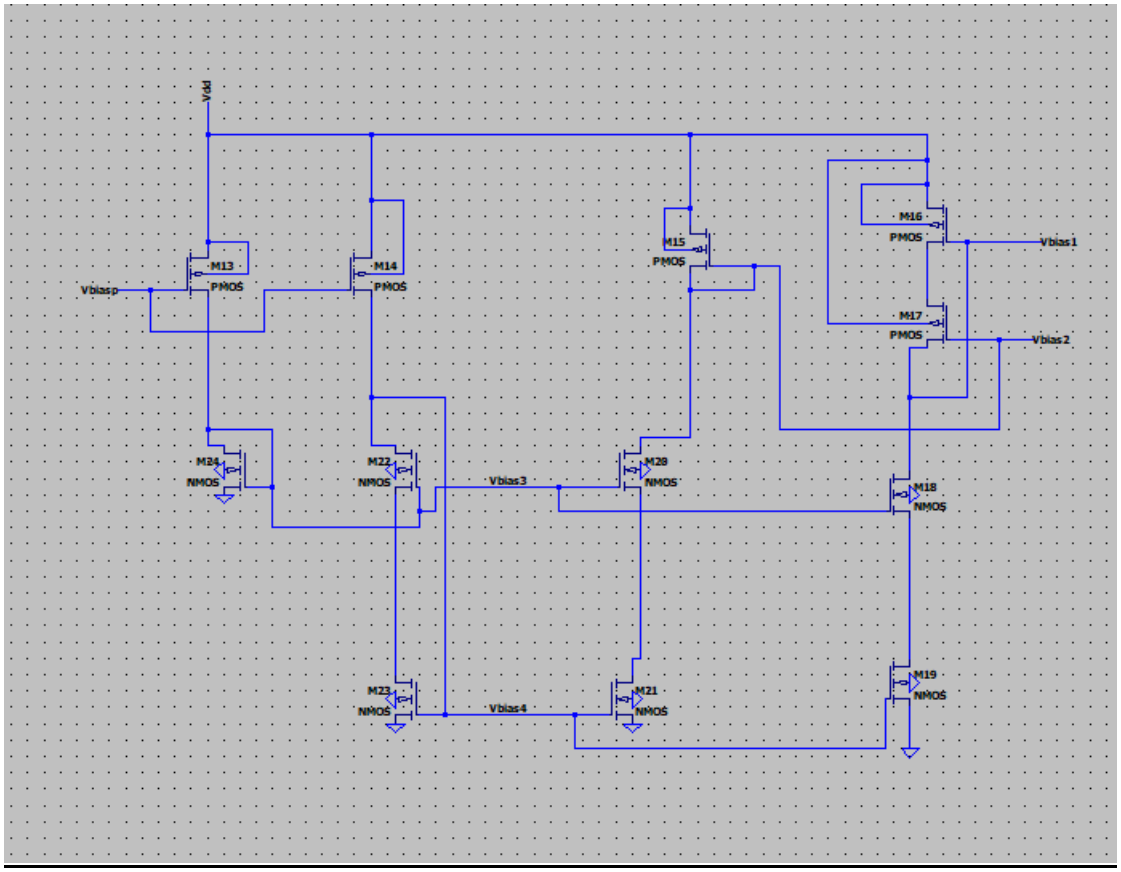
For 180nm

	Theoretical Values	Simulation Results
Vbiasp		1.223V
Vbias1	≥1.1V	1.12V
Vbias2	≥0.9V	0.91V
Vbias3	≤0.9V	0.864V
Av	≈26dB	25 dB
ID	30.622μA	28μAmp
UGB	>500KHz	25MHz
Power Dissipation	<5mW =0.0551mW	0.0504mW (28μX1.8)

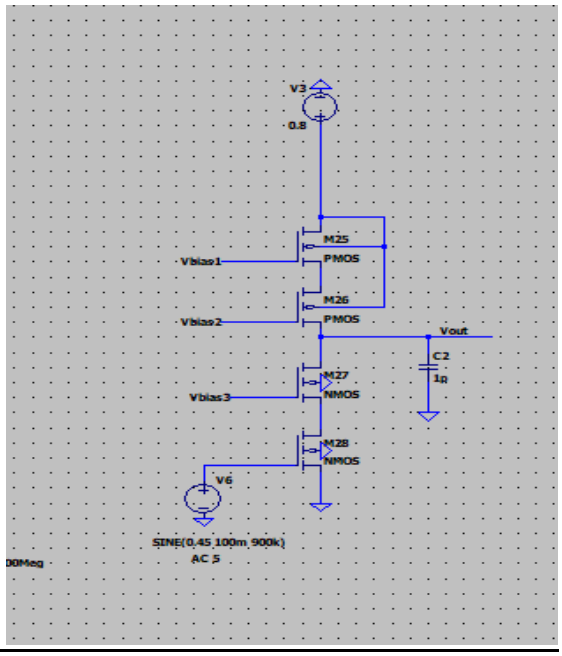
22 nm Technology:

BETA MULTIPLIER



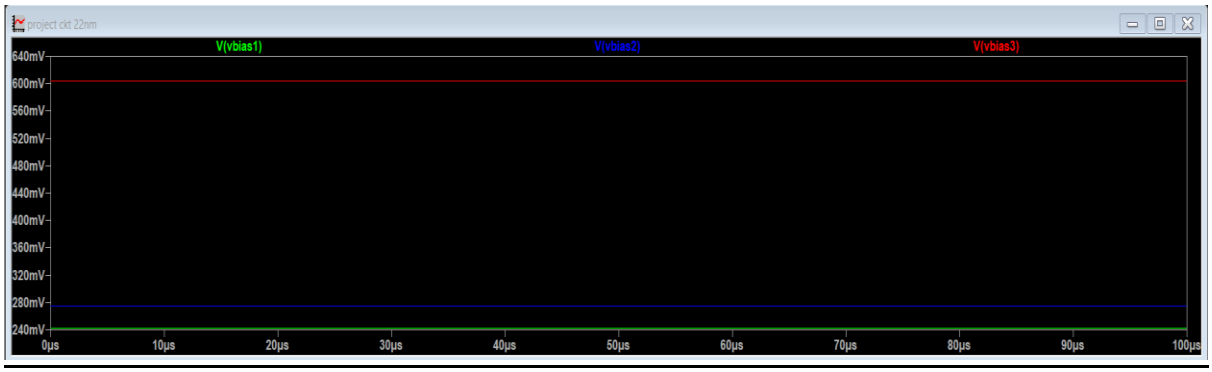


CASCODE CURRENT MIRROR

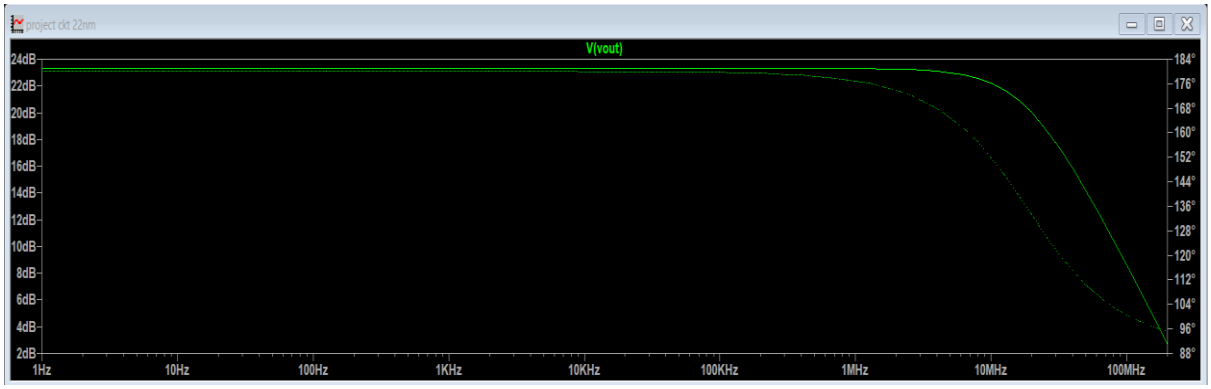


CASCODE AMPLIFIER

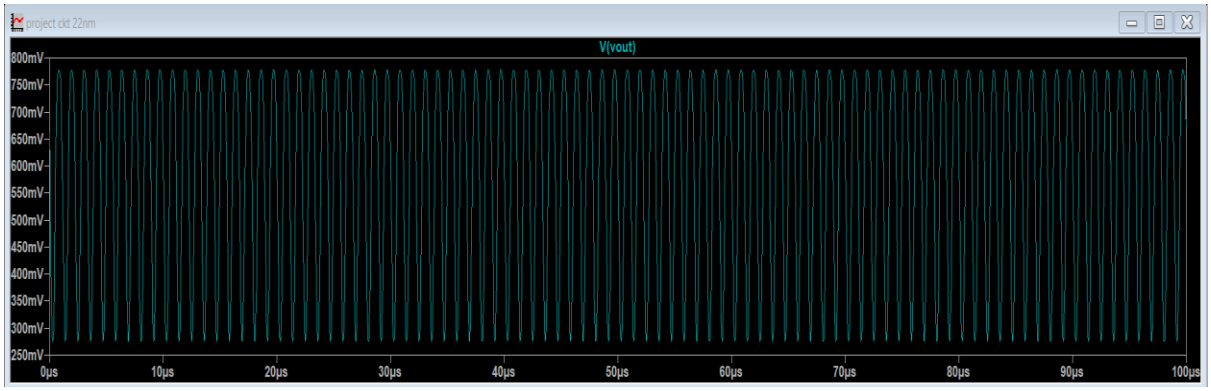
Output :



Vbias123



Frequency response



Vout

CALCULATIONS:

For 22nm:-

$A_V = 20$, $V_{DD} = 0.8V$, $C_L = 1pF$

$|V_{tn}| = 0.3V$, $\mu_p C_{ox} = 50\mu A/V^2$, $\mu_n C_{ox} = 100\mu A/V^2$

$V_{OV} = 0.2V$

assume $f_p = 2.8MHz$

$$R_{out} = \frac{1}{2\pi f_p C_L} = \frac{1}{2\pi \times 2.8 \times 10^6 \times 10^{-12}} = 56841.05\Omega$$

$A_V = g_m R_{out}$ $\quad g_m = \frac{20}{56841.05} = 0.0003518S$

$g_m = \mu_n C_{ox} \frac{W}{L} V_{OV}$

$$\left(\frac{W}{L}\right) = \frac{0.0003518}{0.2 \times 100 \times 10^{-6}} = 17.55$$

$$\boxed{\left(\frac{W}{L}\right)_{NMOS} = 17.55}$$

Current $I_D = \frac{1}{2} \times 100 \times 10^{-6} \times 17.55 \times 0.04$

$= 3.51 \times 10^{-6} \Rightarrow 35.1\mu A$

Same current in both Pmos & NMOS (saturation)

$$35.1 \times 10^{-6} = \frac{1}{2} \times 50 \times 10^{-6} \times \left(\frac{W}{L}\right)' \times 0.04$$

$$\left(\frac{W}{L}\right)_{PMOS} = \frac{35.1 \times 10^{-6} \times 2}{50 \times 0.04 \times 10^{-6}}$$

$= 35.1$

$\Rightarrow$ Power dissipation :- $V_{DD} \times I_D \Rightarrow 0.8 \times 35.1\mu$

$\Rightarrow \boxed{0.028\ mW}$

$\left(\frac{W}{L}\right)_{Nmos} = 17.55$ & $\left(\frac{W}{L}\right)_{pmos} = 35.1$

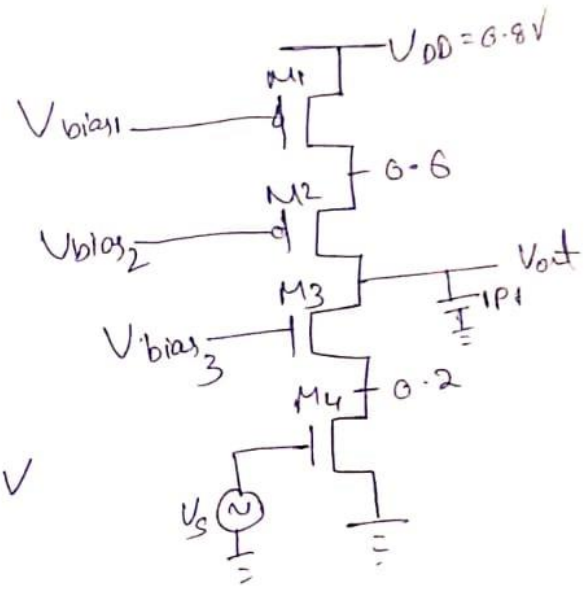
Saturation condn:-

for M4:-

$V_s = 0 \quad V_{ds} = 200mV$

$0.2 \geq V_g - V_{th}$

$\boxed{V_s \leq 0.5V}$



For M3

$V_d = 400\,mV; V_s = 200mV$

$V_{dg} = 200mV$

$V_{dg} > V_{gs} - V_{th} \Rightarrow 200 \geq V_{bias3} - 0.2 - 0.3$

$\boxed{V_{bias3} \leq 0.7V}$

For M_2 PMOS: $V_{ds} \leq V_{gs} - V_{th}$

$V_{sd} \geq V_{sg} - |V_{thp}|$

$0.2 \geq 0.6 - V_{bias2} - 0.3$

$\boxed{V_{bias2} \geq 0.1V}$

For M_1 :- $V_{sd} \geq V_{sg} - |V_{thp}|$

$0.2 \geq 0.8 - V_{bias1} - 0.3$

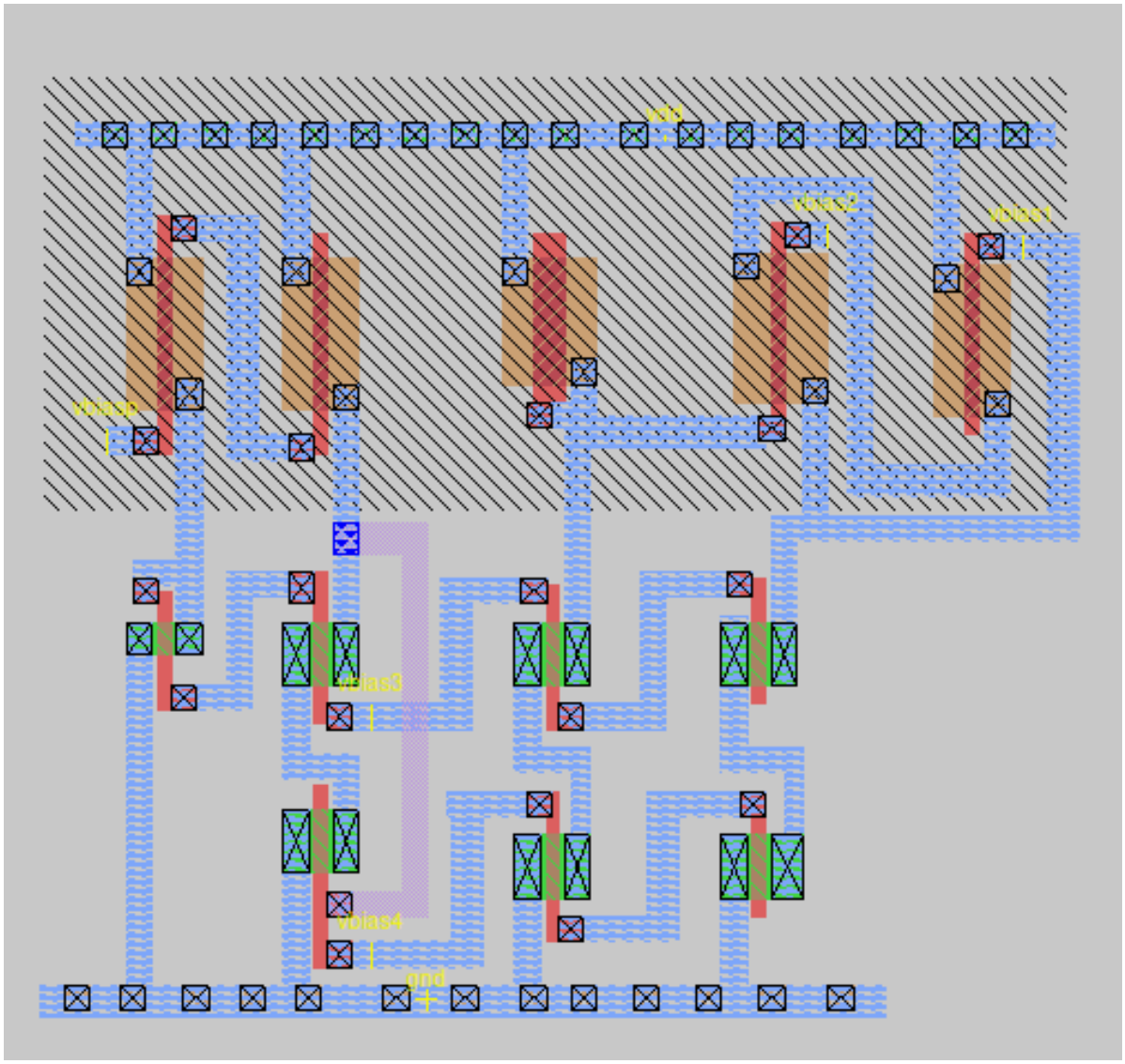
$V_{bias1} \geq 0.3V$

Simulation Results and Theoretical Values For 22nm:

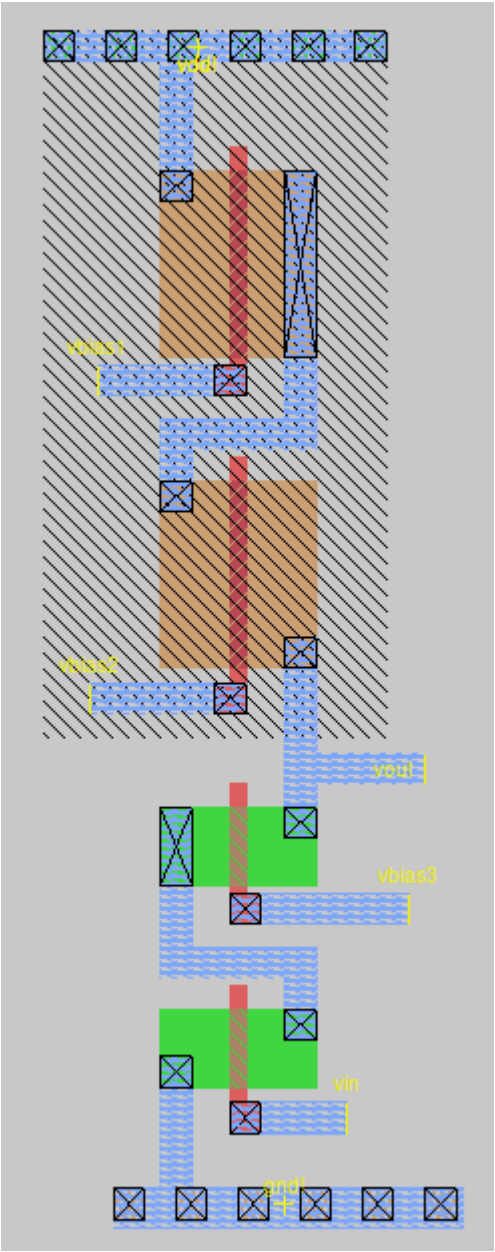
For 22nm:-

	Theoretical values	Simulation Results
V_{biasp}		0.24847 V
V_{bias1}	$\geq$ 0.3V	0.243053 V
V_{bias2}	$\geq$ 0.1V	0.274505 V
V_{bias3}	$\leq$ 0.7V	0.604538 V
A_V	$\approx$ 26dB	23.03dB
ID	35.1μA	30μA
UGB	>500KHz	270MHz
Power Dissipation	<5mW $\approx$0.028mW	0.024 mW

Magic Layout (for 180nm Technology):



Cascode Current Mirror



Cascode amplifier

specifications Required:

- Gain: The desired gain is 20log(20) dB, equating to 26 dB. The simulations achieved a gain of 21.5dB for 180nm technology and 23.03 dB for 22nm technology.
- Power Dissipation: The target is under 5mW, with simulated values of 0.0504mW for 180nm technology and 0.024mW for 22nm technology.

- Unity Gain Bandwidth (UGB): The requirement is greater than 500KHz, with achieved UGB values of 25 MHz for 180nm and 270 MHz for 22nm technology.
- Frequency Response: Both simulations exhibit a low-pass filter response.

Differences Observed between 180nm and 22nm Technology:

- Generally, all Vbias values are lower in 22nm technology, resulting in lower power consumption compared to 180nm technology.
- The Unity Gain Bandwidth (UGB) and, therefore, the cutoff frequency, are higher for 22nm technology.
- Due to their smaller size (approximately 8 times smaller than 180nm), 22nm MOSFETs can be placed closer together in the layout, allowing more transistors to fit on a single chip, which enhances performance.
- However, the smaller size of 22nm MOSFETs makes layout design more challenging, potentially increasing production costs.

Conclusion:

In this study, we simulated the Beta Multiplier, Cascode Current Mirror, and Cascode Amplifier using both 180nm and 22nm technology nodes in LTspice. The simulation outcomes closely matched theoretical predictions, meeting all specified performance requirements. Additionally, we designed the layouts for the Cascode Current Mirror and Cascode Amplifier using the Magic layout tool, focusing on the 180nm technology.

Finally, a comparative analysis was conducted between the 180nm and 22nm technologies based on LTspice simulation results and Magic layout designs. This comparison highlighted the performance variations and layout considerations inherent in each technology.