R-2R LADDER DAC USING OP-AMP IN CADENCE

Parushuram M, Shivabasavesh A S

Department of Electronics and Communication ,NIE South , Mysore

2022ec_shivabasaveshas_b@nie.ac.in ,2022ec_parushuramm_a@nie.ac.in

***Abstract*— This paper presents the design and realization of a 4-bit R-2R Digital-to-Analog Converter (DAC) using a two-stage CMOS operational amplifier in Cadence Virtuoso. The DAC uses a resistor ladder structure that simplifies binary-weighted digital-to-analog conversion. A two-stage operational amplifier—consisting of a differential amplifier and a gain stage—is designed to convert the ladder output current into a stable analog voltage. The complete workflow includes schematic design, simulation analysis, layout implementation, and physical verification through DRC and LVS. Simulation results validate the performance of both the op-amp and the DAC.**

***Keywords*— R-2R DAC, Two-Stage Op-Amp, CMOS Analog Design, Cadence Virtuoso, Schematic and Layout.**

I. INTRODUCTION

Digital-to-analog conversion is a fundamental requirement in mixed-signal systems such as communication devices, sensor interfaces, audio equipment, and microcontroller-driven circuits. Among various DAC architectures, the R-2R ladder DAC remains a popular choice due to its structural simplicity, requirement of only two resistor values, and excellent scalability for higher resolutions.

A DAC alone cannot generate a stable analog voltage without proper load driving. Therefore, a two-stage CMOS operational amplifier is paired with the R-2R network. The op-amp converts the binary-weighted ladder current into a continuous analog voltage output with high gain and stability.

This project focuses on:

- Designing a 4-bit R-2R ladder DAC
- Developing a two-stage CMOS op-amp
- Simulating the DAC–op-amp combination
- Creating layout and performing DRC/LVS checks

All design and analyses were carried out in Cadence Virtuoso using the gpdk180 (180 nm CMOS) technology.

II COMPONENTS

1. NMOS Transistors (gpdk180)
2. PMOS Transistors (gpdk180)
3. Precision Resistors (1 kΩ and 2 kΩ)
4. Compensation Capacitor
5. VDC and Vref Sources (1.8 V)
6. Digital Bit Input Sources (0–1.8 V Square Waves)

A. Technical Specifications:

NMOS:
W/L ratios used: 10 µm/1 µm, 3 µm/1 µm
Threshold voltage: approx. 0.45–0.5 V
Drain current rating suitable for low-power analog design

PMOS:
W/L ratios used: 50 µm/1 µm, 15 µm/1 µm
High output swing and better load-driving characteristics

R and 2R Resistors:
Resistance values:
– R = 1 kΩ
– 2R = 2 kΩ
Tolerance: ±1%
Temperature Range: −55°C to +155°C

Capacitor (Compensation):
Range: 1 pF to 5 pF
Used for Miller compensation

Vref and Supply:
VDD = 1.8 V
Vref = 1.8 V

B. Stages of the DAC System.

1. R-2R Ladder Network
The R-2R ladder forms the core of the DAC. It generates binary-weighted current contributions based on the digital input bits. Each bit switches between Vref (logic 1) and GND (logic 0).

2. Operational Amplifier

The op-amp converts the current output of the R-2R ladder into a corresponding analog voltage. It is designed as a two-stage amplifier to ensure high gain and stability.

3. Output Buffering

The op-amp output is used as the final analog voltage, representing the digital input in analog form.

Circuit Daigram:

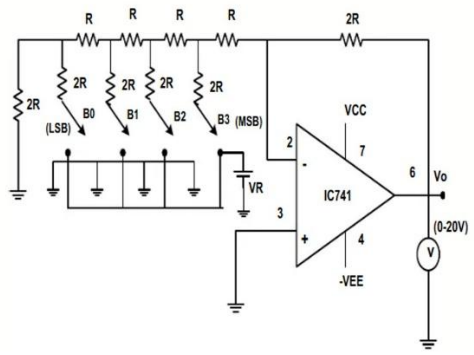

Fig: 4-bit R2R DAC

III WORKING AND ANALYSIS

A. Circuit Design

The R-2R ladder DAC consists of multiple resistor branches arranged in a repeating pattern of R and 2R.

The output voltage of a 4-bit DAC is given by:

$$V_{out} = V_{ref}\left(\frac{b_3}{2} + \frac{b_2}{4} + \frac{b_1}{8} + \frac{b_0}{16}\right)$$

Where b_3 is the MSB and b_0 is the LSB.

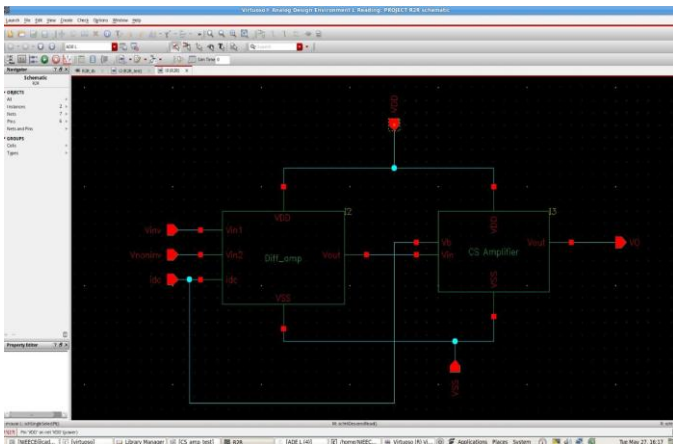

Fig.1 Schematic of Two-Stage Op-Amp

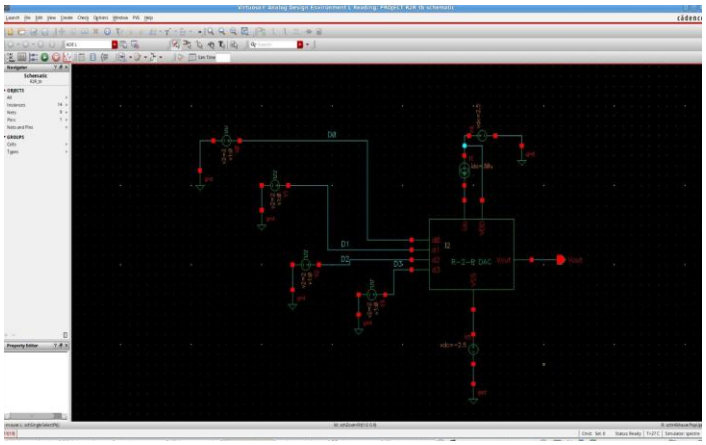

Fig.2 Testbench of Op-Amp

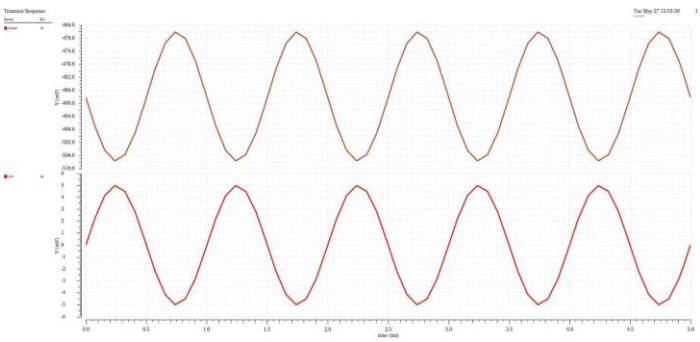

Fig.3 Transient Analysis of Op-Amp

B. DAC Description

The R-2R network generates currents proportional to digital bit weights. These currents sum at the op-amp input.

The op-amp (configured as an inverting I-to-V converter) translates this current into a proportional analog voltage.

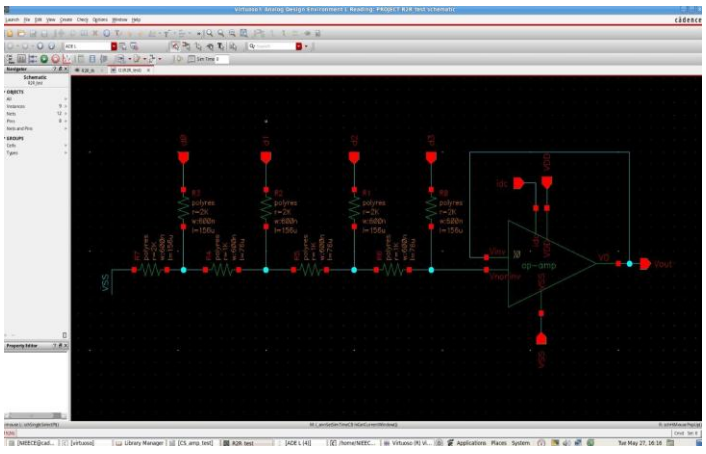

Fig.4 Schematic of R-2R DAC

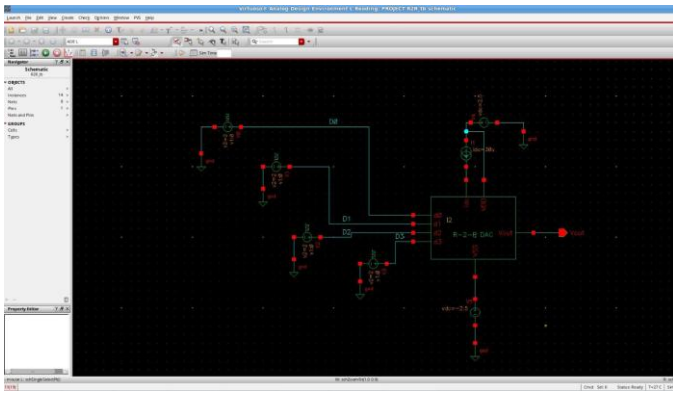

Fig.5 Testbench of R-2R DAC

C. Simulation Results

1. Transient Analysis

The DAC produces a staircase waveform where each step corresponds to a binary input.

2. AC Analysis

The op-amp exhibits high gain (>60 dB) and good phase margin (>60°), ensuring stable operation.

3. Stage-Wise AC Analysis

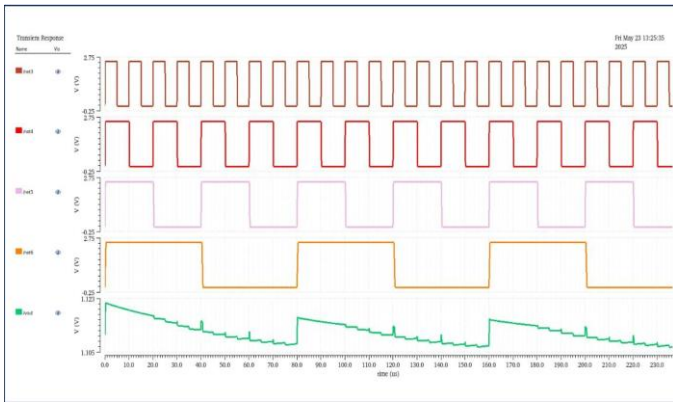

Fig.6 Transient Output of DAC

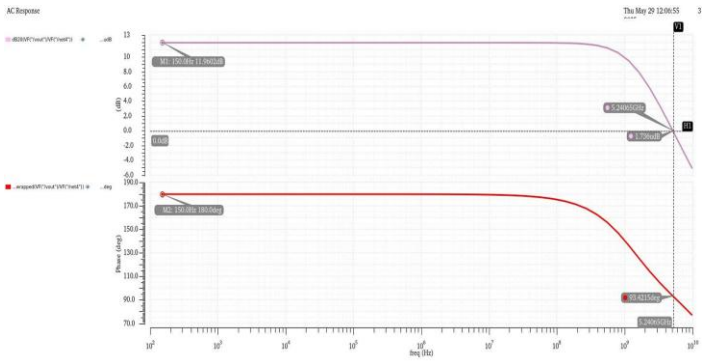

Fig.7 AC Analysis of Common-Source Stage

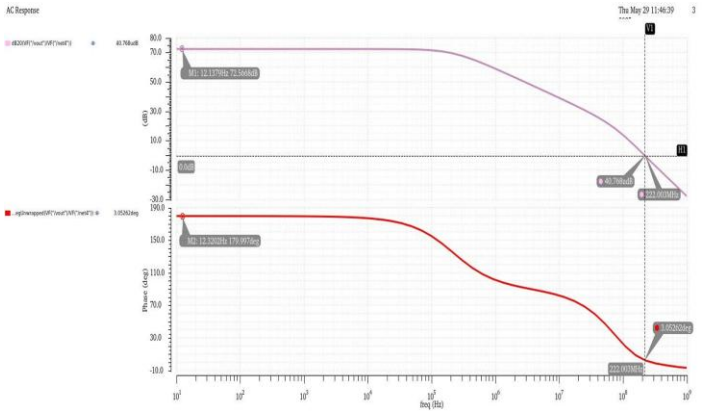

Fig.8 AC Analysis of Differential Stage

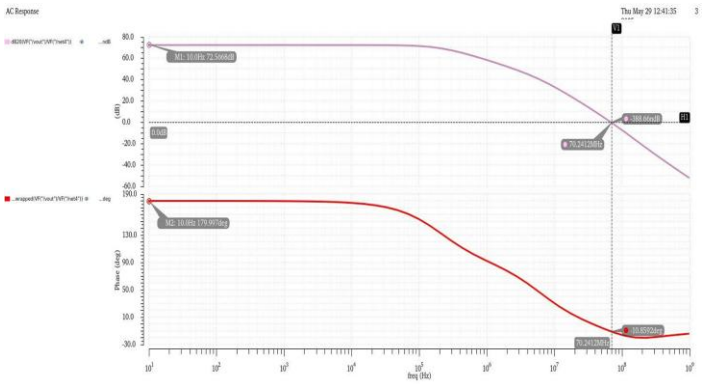

Fig.9 AC Analysis of Overall Op-Amp

- IV. CONCLUSION

In conclusion, the 4-bit R-2R DAC combined with a two-stage CMOS operational amplifier was successfully designed and tested using Cadence Virtuoso. Simulation results verified accurate digital-to-analog conversion and stable amplifier behavior. The layout passed DRC and LVS checks, confirming fabrication readiness. This system demonstrates an efficient, low-component analog conversion architecture suitable for low-power mixed-signal applications.

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