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## 1.1

Addressing Modes (18) top1.1.1 Addressing Modes: GATE CSE 1987 | Question: 1-V top

The most relevant addressing mode to write position-independent codes is:

- A. Direct mode
- B. Indirect mode
- C. Relative mode
- D. Indexed mode

gate1987 co-and-architecture addressing-modes

**Answer key** top

1.1.2 Addressing Modes: GATE CSE 1988 | Question: 9iii top

In the program scheme given below indicate the instructions containing any operand needing relocation for position independent behaviour. Justify your answer.

$$Y = 10$$

MOV  $X(R_0), R_1$

MOV  $X, R_0$

MOV  $2(R_0), R_1$

MOV  $Y(R_0), R_5$

.

.

.

$X : \text{WORD } 0,0,0$

gate1988 normal descriptive co-and-architecture addressing-modes

**Answer key** top

1.1.3 Addressing Modes: GATE CSE 1989 | Question: 2-ii top

Match the pairs in the following questions:

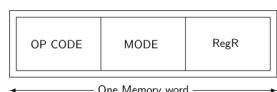
(A) Base addressing	(p) Reentrancy
(B) Indexed addressing	(q) Accumulator
(C) Stack addressing	(r) Array
(D) Implied addressing	(s) Position independent

gate1989 match-the-following co-and-architecture addressing-modes easy

**Answer key** top

1.1.4 Addressing Modes: GATE CSE 1993 | Question: 10 top

The instruction format of a CPU is:



Mode and RegR together specify the operand. RegR specifies a CPU register and Mode specifies an addressing mode. In particular, Mode = 2 specifies that 'the register RegR contains the address of the operand, after fetching the operand, the contents of RegR are incremented by 1'.

An instruction at memory location 2000 specifies Mode = 2 and the RegR refers to program counter (PC).

- A. What is the address of the operand?

B. Assuming that is a non-jump instruction, what are the contents of PC after the execution of this instruction?

gate1993 co-and-architecture addressing-modes normal descriptive

Answer key 

### 1.1.5 Addressing Modes: GATE CSE 1996 | Question: 1.16, ISRO2016-42 [top](#)

Relative mode of addressing is most relevant to writing:

- A. Co – routines
- B. Position – independent code
- C. Shareable code
- D. Interrupt Handlers

gate1996 co-and-architecture addressing-modes easy isro2016

Answer key 

### 1.1.6 Addressing Modes: GATE CSE 1998 | Question: 1.19 [top](#)

Which of the following addressing modes permits relocation without any change whatsoever in the code?

- A. Indirect addressing
- B. Indexed addressing
- C. Base register addressing
- D. PC relative addressing

gate1998 co-and-architecture addressing-modes easy

Answer key 

### 1.1.7 Addressing Modes: GATE CSE 1999 | Question: 2.23 [top](#)

A certain processor supports only the immediate and the direct addressing modes. Which of the following programming language features cannot be implemented on this processor?

- A. Pointers
- B. Arrays
- C. Records
- D. Recursive procedures with local variable

gate1999 co-and-architecture addressing-modes normal multiple-selects

Answer key 

### 1.1.8 Addressing Modes: GATE CSE 2000 | Question: 1.10 [top](#)

The most appropriate matching for the following pairs

- |                              |              |
|------------------------------|--------------|
| X: Indirect addressing       | 1: Loops     |
| Y: Immediate addressing      | 2: Pointers  |
| Z: Auto decrement addressing | 3: Constants |

is

- A.  $X - 3, Y - 2, Z - 1$
- B.  $X - 1, Y - 3, Z - 2$
- C.  $X - 2, Y - 3, Z - 1$
- D.  $X - 3, Y - 1, Z - 2$

gatecse-2000 co-and-architecture normal addressing-modes

Answer key 

### 1.1.9 Addressing Modes: GATE CSE 2001 | Question: 2.9 [top](#)

Which is the most appropriate match for the items in the first column with the items in the second column:

X. Indirect Addressing	I. Array implementation
Y. Indexed Addressing	II. Writing relocatable code
Z. Base Register Addressing	III. Passing array as parameter

- A. (X, III), (Y, I), (Z, II)
- B. (X, II), (Y, III), (Z, I)
- C. (X, III), (Y, II), (Z, I)
- D. (X, I), (Y, III), (Z, II)

gatecse-2001 co-and-architecture addressing-modes normal

[Answer key](#)

### 1.1.10 Addressing Modes: GATE CSE 2002 | Question: 1.24 top



In the absolute addressing mode:

- A. the operand is inside the instruction
- B. the address of the operand is inside the instruction
- C. the register containing the address of the operand is specified inside the instruction
- D. the location of the operand is implicit

gatecse-2002 co-and-architecture addressing-modes easy

[Answer key](#)

### 1.1.11 Addressing Modes: GATE CSE 2004 | Question: 20 top



Which of the following addressing modes are suitable for program relocation at run time?

- I. Absolute addressing
  - II. Based addressing
  - III. Relative addressing
  - IV. Indirect addressing
- |               |                 |
|---------------|-----------------|
| A. I and IV   | B. I and II     |
| C. II and III | D. I, II and IV |

gatecse-2004 co-and-architecture addressing-modes easy

[Answer key](#)

### 1.1.12 Addressing Modes: GATE CSE 2005 | Question: 65 top



Consider a three word machine instruction

**ADDA[R<sub>0</sub>], @B**

The first operand (destination) “A[R<sub>0</sub>]” uses indexed addressing mode with R<sub>0</sub> as the index register. The second operand (source) “@B” uses indirect addressing mode. A and B are memory addresses residing at the second and third words, respectively. The first word of the instruction specifies the opcode, the index register designation and the source and destination addressing modes. During execution of ADD instruction, the two operands are added and stored in the destination (first operand).

The number of memory cycles needed during the execution cycle of the instruction is:

- A. 3                    B. 4                    C. 5                    D. 6

gatecse-2005 co-and-architecture addressing-modes normal

[Answer key](#)

### 1.1.13 Addressing Modes: GATE CSE 2005 | Question: 66 top



Match each of the high level language statements given on the left hand side with the most natural addressing mode from those listed on the right hand side.

- |   |   |
|---|---|
| (1) A[I] = B[J]<br>(2) while (*A++);<br>(3) int temp = *x | (a) Indirect addressing<br>(b) Indexed addressing<br>(c) Auto increment |
|---|---|

- |                      |                      |
|----------------------|----------------------|
| A. (1,c),(2,b),(3,a) | B. (1,c),(2,c),(3,b) |
| C. (1,b),(2,c),(3,a) | D. (1,a),(2,b),(3,c) |

gatecse-2005 co-and-architecture addressing-modes easy

[Answer key](#)

### 1.1.14 Addressing Modes: GATE CSE 2008 | Question: 33, ISRO2009-80 [top](#)



Which of the following is/are true of the auto-increment addressing mode?

- I. It is useful in creating self-relocating code
  - II. If it is included in an Instruction Set Architecture, then an additional ALU is required for effective address calculation
  - III. The amount of increment depends on the size of the data item accessed
- A. I only      B. II only      C. III only      D. II and III only

gatecse-2008 addressing-modes co-and-architecture normal isro2009

[Answer key](#)

### 1.1.15 Addressing Modes: GATE CSE 2011 | Question: 21 [top](#)



Consider a hypothetical processor with an instruction of type **LW R1, 20(R2)**, which during execution reads a 32-bit word from memory and stores it in a 32-bit register **R1**. The effective address of the memory location is obtained by the addition of a constant 20 and the contents of register **R2**. Which of the following best reflects the addressing mode implemented by this instruction for the operand in memory?

- A. Immediate addressing  
C. Register Indirect Scaled Addressing      B. Register addressing  
D. Base Indexed Addressing

gatecse-2011 co-and-architecture addressing-modes easy

[Answer key](#)

### 1.1.16 Addressing Modes: GATE CSE 2017 Set 1 | Question: 11 [top](#)



Consider the *C* struct defined below:

```
struct data {  
    int marks [100];  
    char grade;  
    int cnumber;  
};  
struct data student;
```

The base address of student is available in register **R1**. The field **student.grade** can be accessed efficiently using:

- A. Post-increment addressing mode,  $(R1) +$
- B. Pre-decrement addressing mode,  $-(R1)$
- C. Register direct addressing mode,  $R1$
- D. Index addressing mode,  $X(R1)$ , where  $X$  is an offset represented in 2's complement 16-bit representation

gatecse-2017-set1 co-and-architecture addressing-modes

[Answer key](#)

### 1.1.17 Addressing Modes: GATE IT 2006 | Question: 39, ISRO2009-42 [top](#)



Which of the following statements about relative addressing mode is FALSE?

- A. It enables reduced instruction size
- B. It allows indexing of array element with same instruction
- C. It enables easy relocation of data
- D. It enables faster address calculation than absolute addressing

gateit-2006 co-and-architecture addressing-modes normal isro2009

[Answer key](#)

### 1.1.18 Addressing Modes: GATE IT 2006 | Question: 40 [top](#)



The memory locations 1000, 1001 and 1020 have data values 18, 1 and 16 respectively before the

following program is executed.

```
MOVI    Rs, 1          ; Move immediate
LOAD    Rd, 1000(Rs) ; Load from memory
ADDI    Rd, 1000       ; Add immediate
STOREI   0(Rd), 20     ; Store immediate
```

Which of the statements below is TRUE after the program is executed ?

- A. Memory location 1000 has value 20  
C. Memory location 1021 has value 20
- B. Memory location 1020 has value 20  
D. Memory location 1001 has value 20

gateit-2006 co-and-architecture addressing-modes normal

[Answer key](#)

## 1.2

### Assembly Code (1) [top](#)

#### 1.2.1 Assembly Code: GATE CSE 2023 | Question: 31 [top](#)



Consider the given C-code and its corresponding assembly code, with a few operands U1-U4 being unknown. Some useful information as well as the semantics of each unique assembly instruction is annotated as inline comments in the code. The memory is byte-addressable.

```
//C-code
;assembly-code (; indicates comments)
;r1-r5 are 32-bit integer registers
;initialize r1=0, r2=10
;initialize r3, r4 with base address of a, b

int a[10], b[10], i;
// int is 32-bit
for (i=0; i<10; i++)
    a[i] = b[i] * 8;

L01: jeq r1, r2, end ;if(r1==r2) goto end
L02: lw r5, 0(r4)      ;r5 <- Memory[r4+0]
L03: shl r5, r5, U1    ;r5 <- r5 << U1
L04: sw r5, 0(r3)      ;Memory[r3+0] <- r5
L05: add r3, r3, U2    ;r3 <- r3+U2
L06: add r4, r4, U3    ;r4 <- r4+U3
L07: add r1, r1, 1      ;r1 <- r1+1
L08: jmp U4            ;goto U4
L09: end
```

Which one of the following options is a CORRECT replacement for operands in the position (U1, U2, U3, U4) in the above assembly code?

- A. (8,4,1,L02)      B. (3,4,4,L01)      C. (8,1,1,L02)      D. (3,1,1,L01)

gatecse-2023 co-and-architecture assembly-code 2-marks

[Answer key](#)

## 1.3

### Cache Memory (66) [top](#)

#### 1.3.1 Cache Memory: GATE CSE 1987 | Question: 4b [top](#)



What is cache memory? What is rationale of using cache memory?

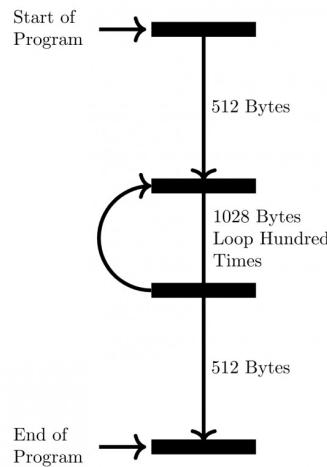
gate1987 co-and-architecture cache-memory descriptive

[Answer key](#)

#### 1.3.2 Cache Memory: GATE CSE 1989 | Question: 6a [top](#)



A certain computer system was designed with cache memory of size 1 Kbytes and main memory size of 256 Kbytes. The cache implementation was fully associative cache with 4 bytes per block. The CPU memory data path was 16 bits and the memory was 2-way interleaved. Each memory read request presents two 16-bit words. A program with the model shown below was run to evaluate the cache design.



Answer the following questions:

- What is the hit ratio?
- Suggest a change in the program size of model to improve the hit ratio significantly.

gate1989 descriptive co-and-architecture cache-memory

[Answer key](#)

### 1.3.3 Cache Memory: GATE CSE 1990 | Question: 7a [top](#)

A block-set associative cache memory consists of 128 blocks divided into four block sets. The main memory consists of 16,384 blocks and each block contains 256 eight bit words.

- How many bits are required for addressing the main memory?
- How many bits are needed to represent the TAG, SET and WORD fields?

gate1990 descriptive co-and-architecture cache-memory

[Answer key](#)

### 1.3.4 Cache Memory: GATE CSE 1992 | Question: 5-a [top](#)

The access times of the main memory and the Cache memory, in a computer system, are 500 n sec and 50 nsec, respectively. It is estimated that 80% of the main memory request are for read the rest for write. The hit ratio for the read access only is 0.9 and a write-through policy (where both main and cache memories are updated simultaneously) is used. Determine the average time of the main memory (in ns).

gate1992 co-and-architecture cache-memory normal numerical-answers

[Answer key](#)

### 1.3.5 Cache Memory: GATE CSE 1993 | Question: 11 [top](#)

In the three-level memory hierarchy shown in the following table,  $p_i$  denotes the probability that an access request will refer to  $M_i$ .

Hierarchy Level ( $M_i$ )	Access Time ( $t_i$ )	Probability of Access ( $p_i$ )	Page Transfer Time ( $T_i$ )
$M_1$	$10^{-6}$	0.99000	0.001 sec
$M_2$	$10^{-5}$	0.00998	0.1 sec
$M_3$	$10^{-4}$	0.00002	—

If a miss occurs at level  $M_i$ , a page transfer occurs from  $M_{i+1}$  to  $M_i$  and the average time required for such a

page swap is  $T_i$ . Calculate the average time  $t_A$  required for a processor to read one word from this memory system.

gate1993 co-and-architecture cache-memory normal descriptive

Answer key 

### 1.3.6 Cache Memory: GATE CSE 1995 | Question: 1.6



The principle of locality justifies the use of:

- A. Interrupts      B. DMA      C. Polling      D. Cache Memory

gate1995 co-and-architecture cache-memory easy

Answer key 

### 1.3.7 Cache Memory: GATE CSE 1995 | Question: 2.25



A computer system has a  $4 K$  word cache organized in block-set-associative manner with 4 blocks per set, 64 words per block. The number of bits in the SET and WORD fields of the main memory address format is:

- A. 15,40      B. 6,4      C. 7,2      D. 4,6

gate1995 co-and-architecture cache-memory normal

Answer key 

### 1.3.8 Cache Memory: GATE CSE 1996 | Question: 26



A computer system has a three-level memory hierarchy, with access time and hit ratios as shown below:

Level 1 (Cache memory)		Level 2 (Main memory)		Level 3	
Size	Hit ratio	Size	Hit ratio	Size	Hit ratio
8M bytes	0.80	4M bytes	0.98	260M bytes	1.0
16M bytes	0.90	16M bytes	0.99		
64M bytes	0.95	64M bytes	0.995		

- A. What should be the minimum sizes of level 1 and 2 memories to achieve an average access time of less than  $100\text{nsec}$ ?  
B. What is the average access time achieved using the chosen sizes of level 1 and level 2 memories?

gate1996 co-and-architecture cache-memory normal

Answer key 

### 1.3.9 Cache Memory: GATE CSE 1998 | Question: 18



For a set-associative Cache organization, the parameters are as follows:

$t_c$	Cache Access Time
$t_m$	Main memory access time
$l$	Number of sets
$b$	Block size
$k \times b$	Set size

Calculate the hit ratio for a loop executed 100 times where the size of the loop is  $n \times b$ , and  $n = k \times m$  is a non-zero integer and  $1 \leq m \leq l$ .

Give the value of the hit ratio for  $l = 1$ .

gate1998 co-and-architecture cache-memory descriptive

[Answer key](#)

### 1.3.10 Cache Memory: GATE CSE 1999 | Question: 1.22 [top](#)

The main memory of a computer has  $2^m$  blocks while the cache has  $2^c$  blocks. If the cache uses the set associative mapping scheme with 2 blocks per set, then block  $k$  of the main memory maps to the set:

- A.  $(k \bmod m)$  of the cache
- B.  $(k \bmod c)$  of the cache
- C.  $(k \bmod 2c)$  of the cache
- D.  $(k \bmod 2^{cm})$  of the cache

gate1999 co-and-architecture cache-memory normal

[Answer key](#)



### 1.3.11 Cache Memory: GATE CSE 2001 | Question: 1.7, ISRO2008-18 [top](#)

More than one word are put in one cache block to:

- A. exploit the temporal locality of reference in a program
- B. exploit the spatial locality of reference in a program
- C. reduce the miss penalty
- D. none of the above

gatecse-2001 co-and-architecture easy cache-memory isro2008

[Answer key](#)



### 1.3.12 Cache Memory: GATE CSE 2001 | Question: 9 [top](#)

A CPU has  $32 - bit$  memory address and a  $256 KB$  cache memory. The cache is organized as a  $4 - way$  set associative cache with cache block size of 16 bytes.

- A. What is the number of sets in the cache?
- B. What is the size (in bits) of the tag field per cache block?
- C. What is the number and size of comparators required for tag matching?
- D. How many address bits are required to find the byte offset within a cache block?
- E. What is the total amount of extra memory (in bytes) required for the tag bits?

gatecse-2001 co-and-architecture cache-memory normal descriptive

[Answer key](#)



### 1.3.13 Cache Memory: GATE CSE 2002 | Question: 10 [top](#)

In a C program, an array is declared as  $\text{float } A[2048]$ . Each array element is 4 Bytes in size, and the starting address of the array is  $0x00000000$ . This program is run on a computer that has a direct mapped data cache of size 8 Kbytes, with block (line) size of 16 Bytes.

- A. Which elements of the array conflict with element  $A[0]$  in the data cache? Justify your answer briefly.
- B. If the program accesses the elements of this array one by one in reverse order i.e., starting with the last element and ending with the first element, how many data cache misses would occur? Justify your answer briefly. Assume that the data cache is initially empty and that no other data or instruction accesses are to be considered.

gatecse-2002 co-and-architecture cache-memory normal descriptive

[Answer key](#)



### 1.3.14 Cache Memory: GATE CSE 2004 | Question: 65 [top](#)

Consider a small two-way set-associative cache memory, consisting of four blocks. For choosing the block to be replaced, use the least recently used (LRU) scheme. The number of cache misses for the following sequence of block addresses is:

8, 12, 0, 12, 8.

- A. 2
- B. 3
- C. 4
- D. 5

gatecse-2004 co-and-architecture cache-memory normal

[Answer key](#)



### 1.3.15 Cache Memory: GATE CSE 2005 | Question: 67 top



Consider a direct mapped cache of size  $32\text{ KB}$  with block size  $32\text{ bytes}$ . The  $CPU$  generates  $32\text{ bit}$  addresses. The number of bits needed for cache indexing and the number of tag bits are respectively,

- A. 10,17      B. 10,22      C. 15,17      D. 5,17

gatecse-2005 co-and-architecture cache-memory easy

[Answer key](#)

### 1.3.16 Cache Memory: GATE CSE 2006 | Question: 74 top



Consider two cache organizations. First one is  $32\text{ KB}$  2-way set associative with  $32\text{ byte}$  block size, the second is of same size but direct mapped. The size of an address is  $32\text{ bits}$  in both cases. A 2-to-1 multiplexer has latency of  $0.6\text{ ns}$  while a  $k$ -bit comparator has latency of  $\frac{k}{10}\text{ ns}$ . The hit latency of the set associative organization is  $h_1$  while that of direct mapped is  $h_2$ .

The value of  $h_1$  is:

- A.  $2.4\text{ ns}$       B.  $2.3\text{ ns}$       C.  $1.8\text{ ns}$       D.  $1.7\text{ ns}$

gatecse-2006 co-and-architecture cache-memory normal

[Answer key](#)

### 1.3.17 Cache Memory: GATE CSE 2006 | Question: 75 top



Consider two cache organizations. First one is  $32\text{ kB}$  2-way set associative with  $32\text{ byte}$  block size, the second is of same size but direct mapped. The size of an address is  $32\text{ bits}$  in both cases. A 2-to-1 multiplexer has latency of  $0.6\text{ ns}$  while a  $k$ -bit comparator has latency of  $\frac{k}{10}\text{ ns}$ . The hit latency of the set associative organization is  $h_1$  while that of direct mapped is  $h_2$ .

The value of  $h_2$  is:

- A.  $2.4\text{ ns}$       B.  $2.3\text{ ns}$       C.  $1.8\text{ ns}$       D.  $1.7\text{ ns}$

gatecse-2006 co-and-architecture cache-memory normal

[Answer key](#)

### 1.3.18 Cache Memory: GATE CSE 2006 | Question: 80 top



A CPU has a  $32KB$  direct mapped cache with  $128\text{ byte-block}$  size. Suppose  $A$  is two dimensional array of size  $512 \times 512$  with elements that occupy  $8\text{-bytes}$  each. Consider the following two C code segments,  $P1$  and  $P2$ .

P1:

```
for (i=0; i<512; i++)
{
    for (j=0; j<512; j++)
    {
        x += A[i][j];
    }
}
```

P2:

```
for (i=0; i<512; i++)
{
    for (j=0; j<512; j++)
    {
        x += A[j][i];
    }
}
```

$P1$  and  $P2$  are executed independently with the same initial state, namely, the array  $A$  is not in the cache and  $i, j, x$  are in registers. Let the number of cache misses experienced by  $P1$  be  $M_1$  and that for  $P2$  be  $M_2$ .

The value of  $M_1$  is:

A. 0

B. 2048

C. 16384

D. 262144

gatecse-2006 co-and-architecture cache-memory normal

Answer key 

### 1.3.19 Cache Memory: GATE CSE 2006 | Question: 81



A CPU has a  $32\text{ KB}$  direct mapped cache with  $128$  byte-block size. Suppose  $A$  is two dimensional array of size  $512 \times 512$  with elements that occupy  $8 - \text{bytes}$  each. Consider the following two  $C$  code segments,  $P1$  and  $P2$ .

$P1$ :

```
for (i=0; i<512; i++)
{
    for (j=0; j<512; j++)
    {
        x += A[i][j];
    }
}
```

$P2$ :

```
for (i=0; i<512; i++)
{
    for (j=0; j<512; j++)
    {
        x += A[j][i];
    }
}
```

$P1$  and  $P2$  are executed independently with the same initial state, namely, the array  $A$  is not in the cache and  $i, j, x$  are in registers. Let the number of cache misses experienced by  $P1$  be  $M_1$  and that for  $P2$  be  $M_2$ .

The value of the ratio  $\frac{M_1}{M_2}$ :

A. 0

B.  $\frac{1}{16}$

C.  $\frac{1}{8}$

D. 16

co-and-architecture cache-memory normal gatecse-2006

Answer key 

### 1.3.20 Cache Memory: GATE CSE 2007 | Question: 10



Consider a 4-way set associative cache consisting of  $128$  lines with a line size of  $64$  words. The CPU generates a  $20 - \text{bit}$  address of a word in main memory. The number of bits in the TAG, LINE and WORD fields are respectively:

A. 9,6,5

B. 7,7,6

C. 7,5,8

D. 9,5,6

gatecse-2007 co-and-architecture cache-memory normal

Answer key 

### 1.3.21 Cache Memory: GATE CSE 2007 | Question: 80



Consider a machine with a byte addressable main memory of  $2^{16}$  bytes. Assume that a direct mapped data cache consisting of  $32$  lines of  $64$  bytes each is used in the system. A  $50 \times 50$  two-dimensional array of bytes is stored in the main memory starting from memory location  $1100H$ . Assume that the data cache is initially empty. The complete array is accessed twice. Assume that the contents of the data cache do not change in between the two accesses.

How many data misses will occur in total?

A. 48

B. 50

C. 56

D. 59

gatecse-2007 co-and-architecture cache-memory normal

Answer key 

### 1.3.22 Cache Memory: GATE CSE 2007 | Question: 81 [top](#)



Consider a machine with a byte addressable main memory of  $2^{16}$  bytes. Assume that a direct mapped data cache consisting of 32 lines of 64 bytes each is used in the system. A  $50 \times 50$  two-dimensional array of bytes is stored in the main memory starting from memory location  $1100H$ . Assume that the data cache is initially empty. The complete array is accessed twice. Assume that the contents of the data cache do not change in between the two accesses.

Which of the following lines of the data cache will be replaced by new blocks in accessing the array for the second time?

- A. line 4 to line 11
- B. line 4 to line 12
- C. line 0 to line 7
- D. line 0 to line 8

gatecse-2007 co-and-architecture cache-memory normal

[Answer key](#)

### 1.3.23 Cache Memory: GATE CSE 2008 | Question: 35 [top](#)



For inclusion to hold between two cache levels  $L_1$  and  $L_2$  in a multi-level cache hierarchy, which of the following are necessary?

- I.  $L_1$  must be write-through cache
- II.  $L_2$  must be a write-through cache
- III. The associativity of  $L_2$  must be greater than that of  $L_1$
- IV. The  $L_2$  cache must be at least as large as the  $L_1$  cache

- A. IV only
- B. I and IV only
- C. I, II and IV only
- D. I, II, III and IV

gatecse-2008 co-and-architecture cache-memory normal

[Answer key](#)

### 1.3.24 Cache Memory: GATE CSE 2008 | Question: 71 [top](#)



Consider a machine with a 2-way set associative data cache of size 64Kbytes and block size 16bytes. The cache is managed using 32 bit virtual addresses and the page size is 4Kbytes. A program to be run on this machine begins as follows:

```
double ARR[1024][1024];
int i, j;
/*Initialize array ARR to 0.0 */
for(i = 0; i < 1024; i++)
    for(j = 0; j < 1024; j++)
        ARR[i][j] = 0.0;
```

The size of double is 8Bytes. Array ARR is located in memory starting at the beginning of virtual page 0xFF000 and stored in row major order. The cache is initially empty and no pre-fetching is done. The only data memory references made by the program are those to array ARR.

The total size of the tags in the cache directory is:

- A. 32Kbits
- B. 34Kbits
- C. 64Kbits
- D. 68Kbits

gatecse-2008 co-and-architecture cache-memory normal

[Answer key](#)

### 1.3.25 Cache Memory: GATE CSE 2008 | Question: 72 [top](#)



Consider a machine with a 2-way set associative data cache of size 64 Kbytes and block size 16 bytes. The cache is managed using 32 bit virtual addresses and the page size is 4 Kbytes. A program to be run on this machine begins as follows:

```
double ARR[1024][1024];
int i, j;
/*Initialize array ARR to 0.0 */
for(i = 0; i < 1024; i++)
    for(j = 0; j < 1024; j++)
        ARR[i][j] = 0.0;
```

The size of double is 8 bytes. Array ARR is located in memory starting at the beginning of virtual page 0xFF000 and stored in row major order. The cache is initially empty and no pre-fetching is done. The only data memory references made by the program are those to array ARR.

Which of the following array elements have the same cache index as ARR[0][0]?

- A. ARR[0][4]      B. ARR[4][0]      C. ARR[0][5]      D. ARR[5][0]

gatecse-2008 co-and-architecture cache-memory normal

Answer key ↗

#### 1.3.26 Cache Memory: GATE CSE 2008 | Question: 73 top ↗

Consider a machine with a 2-way set associative data cache of size 64 Kbytes and block size 16 bytes. The cache is managed using 32 bit virtual addresses and the page size is 4 Kbytes. A program to be run on this machine begins as follows:

```
double ARR[1024][1024];
int i, j;
/*Initialize array ARR to 0.0 */
for(i = 0; i < 1024; i++)
    for(j = 0; j < 1024; j++)
        ARR[i][j] = 0.0;
```

The size of double is 8 bytes. Array ARR is located in memory starting at the beginning of virtual page 0xFF000 and stored in row major order. The cache is initially empty and no pre-fetching is done. The only data memory references made by the program are those to array ARR.

The cache hit ratio for this initialization loop is:

- A. 0%      B. 25%      C. 50%      D. 75%

gatecse-2008 co-and-architecture cache-memory normal

Answer key ↗

#### 1.3.27 Cache Memory: GATE CSE 2009 | Question: 29 top ↗

Consider a 4-way set associative cache (initially empty) with total 16 cache blocks. The main memory consists of 256 blocks and the request for memory blocks are in the following order:

0, 255, 1, 4, 3, 8, 133, 159, 216, 129, 63, 8, 48, 32, 73, 92, 155.

Which one of the following memory block will NOT be in cache if LRU replacement policy is used?

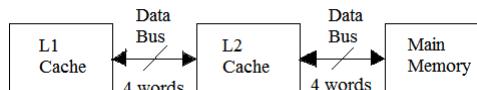
- A. 3      B. 8      C. 129      D. 216

gatecse-2009 co-and-architecture cache-memory normal

Answer key ↗

#### 1.3.28 Cache Memory: GATE CSE 2010 | Question: 48 top ↗

A computer system has an *L1* cache, an *L2* cache, and a main memory unit connected as shown below. The block size in *L1* cache is 4 words. The block size in *L2* cache is 16 words. The memory access times are 2 nanoseconds, 20 nanoseconds and 200 nanoseconds for *L1* cache, *L2* cache and the main memory unit respectively.

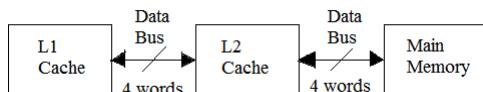


When there is a miss in *L1* cache and a hit in *L2* cache, a block is transferred from *L2* cache to *L1* cache. What is the time taken for this transfer?

- A. 2 nanoseconds      B. 20 nanoseconds  
C. 22 nanoseconds      D. 88 nanoseconds

**Answer key****1.3.29 Cache Memory: GATE CSE 2010 | Question: 49**

A computer system has an  $L_1$  cache, an  $L_2$  cache, and a main memory unit connected as shown below. The block size in  $L_1$  cache is 4 words. The block size in  $L_2$  cache is 16 words. The memory access times are 2 nanoseconds, 20 nanoseconds and 200 nanoseconds for  $L_1$  cache,  $L_2$  cache and the main memory unit respectively.



When there is a miss in both  $L_1$  cache and  $L_2$  cache, first a block is transferred from main memory to  $L_2$  cache, and then a block is transferred from  $L_2$  cache to  $L_1$  cache. What is the total time taken for these transfers?

- A. 222 nanoseconds      B. 888 nanoseconds  
 C. 902 nanoseconds      D. 968 nanoseconds

**Answer key****1.3.30 Cache Memory: GATE CSE 2011 | Question: 43**

A n 8KB direct-mapped write-back cache is organized as multiple blocks, each size of 32-bytes. The processor generates 32-bit addresses. The cache controller contains the tag information for each cache block comprising of the following.

- 1 valid bit
- 1 modified bit
- As many bits as the minimum needed to identify the memory block mapped in the cache.

What is the total size of memory needed at the cache controller to store meta-data (tags) for the cache?

- A. 4864 bits      B. 6144 bits      C. 6656 bits      D. 5376 bits

**Answer key****1.3.31 Cache Memory: GATE CSE 2012 | Question: 54**

A computer has a 256-KByte, 4-way set associative, write back data cache with block size of 32-Bytes. The processor sends 32-bit addresses to the cache controller. Each cache tag directory entry contains, in addition to address tag, 2 valid bits, 1 modified bit and 1 replacement bit.

The number of bits in the tag field of an address is

- A. 11      B. 14      C. 16      D. 27

**Answer key****1.3.32 Cache Memory: GATE CSE 2012 | Question: 55**

A computer has a 256-KByte, 4-way set associative, write back data cache with block size of 32 Bytes. The processor sends 32 bit addresses to the cache controller. Each cache tag directory entry contains, in addition to address tag, 2 valid bits, 1 modified bit and 1 replacement bit.

The size of the cache tag directory is:

- A. 160 Kbits      B. 136 Kbits      C. 40 Kbits      D. 32 Kbits

**Answer key**

### 1.3.33 Cache Memory: GATE CSE 2013 | Question: 20

In a  $k$ -way set associative cache, the cache is divided into  $v$  sets, each of which consists of  $k$  lines. The lines of a set are placed in sequence one after another. The lines in set  $s$  are sequenced before the lines in set  $(s + 1)$ . The main memory blocks are numbered 0 onwards. The main memory block numbered  $j$  must be mapped to any one of the cache lines from

- A.  $(j \bmod v) * k$  to  $(j \bmod v) * k + (k - 1)$
- B.  $(j \bmod v)$  to  $(j \bmod v) + (k - 1)$
- C.  $(j \bmod k)$  to  $(j \bmod k) + (v - 1)$
- D.  $(j \bmod k) * v$  to  $(j \bmod k) * v + (v - 1)$

gatecse-2013 co-and-architecture cache-memory normal

[Answer key](#) 

### 1.3.34 Cache Memory: GATE CSE 2014 Set 1 | Question: 44

An access sequence of cache block addresses is of length  $N$  and contains  $n$  unique block addresses. The number of unique block addresses between two consecutive accesses to the same block address is bounded above by  $k$ . What is the miss ratio if the access sequence is passed through a cache of associativity  $A \geq k$  exercising least-recently-used replacement policy?

- A.  $\left(\frac{n}{N}\right)$
- B.  $\left(\frac{1}{N}\right)$
- C.  $\left(\frac{1}{A}\right)$
- D.  $\left(\frac{k}{n}\right)$

gatecse-2014-set1 co-and-architecture cache-memory normal

[Answer key](#) 

### 1.3.35 Cache Memory: GATE CSE 2014 Set 2 | Question: 43

In designing a computer's cache system, the cache block (or cache line) size is an important parameter. Which one of the following statements is correct in this context?

- A. A smaller block size implies better spatial locality
- B. A smaller block size implies a smaller cache tag and hence lower cache tag overhead
- C. A smaller block size implies a larger cache tag and hence lower cache hit time
- D. A smaller block size incurs a lower cache miss penalty

gatecse-2014-set2 co-and-architecture cache-memory normal

[Answer key](#) 

### 1.3.36 Cache Memory: GATE CSE 2014 Set 2 | Question: 44

If the associativity of a processor cache is doubled while keeping the capacity and block size unchanged, which one of the following is guaranteed to be NOT affected?

- A. Width of tag comparator
- B. Width of set index decoder
- C. Width of way selection multiplexer
- D. Width of processor to main memory data bus

gatecse-2014-set2 co-and-architecture cache-memory normal

[Answer key](#) 

### 1.3.37 Cache Memory: GATE CSE 2014 Set 2 | Question: 9

A 4-way set-associative cache memory unit with a capacity of 16 KB is built using a block size of 8 words. The word length is 32 bits. The size of the physical address space is 4 GB. The number of bits for the TAG field is \_\_\_\_\_

gatecse-2014-set2 co-and-architecture cache-memory numerical-answers normal

[Answer key](#) 

### 1.3.38 Cache Memory: GATE CSE 2014 Set 3 | Question: 44 top



The memory access time is 1 nanosecond for a read operation with a hit in cache, 5 nanoseconds for a read operation with a miss in cache, 2 nanoseconds for a write operation with a hit in cache and 10 nanoseconds for a write operation with a miss in cache. Execution of a sequence of instructions involves 100 instruction fetch operations, 60 memory operand read operations and 40 memory operand write operations. The cache hit-ratio is 0.9. The average memory access time (in nanoseconds) in executing the sequence of instructions is \_\_\_\_\_.

gatecse-2014-set3 co-and-architecture cache-memory numerical-answers normal

Answer key

### 1.3.39 Cache Memory: GATE CSE 2015 Set 2 | Question: 24 top



Assume that for a certain processor, a read request takes 50 nanoseconds on a cache miss and 5 nanoseconds on a cache hit. Suppose while running a program, it was observed that 80% of the processor's read requests result in a cache hit. The average read access time in nanoseconds is \_\_\_\_\_.

gatecse-2015-set2 co-and-architecture cache-memory easy numerical-answers

Answer key

### 1.3.40 Cache Memory: GATE CSE 2015 Set 3 | Question: 14 top



Consider a machine with a byte addressable main memory of  $2^{20}$  bytes, block size of 16 bytes and a direct mapped cache having  $2^{12}$  cache lines. Let the addresses of two consecutive bytes in main memory be  $(E201F)_{16}$  and  $(E2020)_{16}$ . What are the tag and cache line addresses (in hex) for main memory address  $(E201F)_{16}$ ?

- A. E, 201      B. F, 201      C. E, E20      D. 2, 01F

gatecse-2015-set3 co-and-architecture cache-memory normal

Answer key

### 1.3.41 Cache Memory: GATE CSE 2016 Set 2 | Question: 32 top



The width of the physical address on a machine is 40 bits. The width of the tag field in a 512 KB 8-way set associative cache is \_\_\_\_\_ bits.

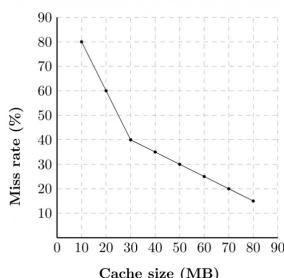
gatecse-2016-set2 co-and-architecture cache-memory normal numerical-answers

Answer key

### 1.3.42 Cache Memory: GATE CSE 2016 Set 2 | Question: 50 top



A file system uses an in-memory cache to cache disk blocks. The miss rate of the cache is shown in the figure. The latency to read a block from the cache is 1 ms and to read a block from the disk is 10 ms. Assume that the cost of checking whether a block exists in the cache is negligible. Available cache sizes are in multiples of 10 MB.



The smallest cache size required to ensure an average read latency of less than 6 ms is \_\_\_\_\_ MB.

gatecse-2016-set2 co-and-architecture cache-memory normal numerical-answers

Answer key

### 1.3.43 Cache Memory: GATE CSE 2017 Set 1 | Question: 25 top

Consider a two-level cache hierarchy with  $L_1$  and  $L_2$  caches. An application incurs 1.4 memory accesses per instruction on average. For this application, the miss rate of  $L_1$  cache is 0.1; the  $L_2$  cache experiences, on average, 7 misses per 1000 instructions. The miss rate of  $L_2$  expressed correct to two decimal places is \_\_\_\_\_.

gatecse-2017-set1 co-and-architecture cache-memory numerical-answers

Answer key 

### 1.3.44 Cache Memory: GATE CSE 2017 Set 1 | Question: 54 top

A cache memory unit with capacity of  $N$  words and block size of  $B$  words is to be designed. If it is designed as a direct mapped cache, the length of the TAG field is 10 bits. If the cache unit is now designed as a 16-way set-associative cache, the length of the TAG field is \_\_\_\_\_ bits.

gatecse-2017-set1 co-and-architecture cache-memory normal numerical-answers

Answer key 

### 1.3.45 Cache Memory: GATE CSE 2017 Set 2 | Question: 29 top

In a two-level cache system, the access times of  $L_1$  and  $L_2$  caches are 1 and 8 clock cycles, respectively. The miss penalty from the  $L_2$  cache to main memory is 18 clock cycles. The miss rate of  $L_1$  cache is twice that of  $L_2$ . The average memory access time (AMAT) of this cache system is 2 cycles. The miss rates of  $L_1$  and  $L_2$  respectively are

- A. 0.111 and 0.056    B. 0.056 and 0.111    C. 0.0892 and 0.1784    D. 0.1784 and 0.0892

gatecse-2017-set2 cache-memory co-and-architecture normal

Answer key 

### 1.3.46 Cache Memory: GATE CSE 2017 Set 2 | Question: 45 top

The read access times and the hit ratios for different caches in a memory hierarchy are as given below:

Cache	Read access time (in nanoseconds)	Hit ratio
I-cache	2	0.8
D-cache	2	0.9
L2-cache	8	0.9

The read access time of main memory is 90 nanoseconds. Assume that the caches use the referred-word-first read policy and the write-back policy. Assume that all the caches are direct mapped caches. Assume that the dirty bit is always 0 for all the blocks in the caches. In execution of a program, 60% of memory reads are for instruction fetch and 40% are for memory operand fetch. The average read access time in nanoseconds (up to 2 decimal places) is \_\_\_\_\_

gatecse-2017-set2 co-and-architecture cache-memory numerical-answers

Answer key 

### 1.3.47 Cache Memory: GATE CSE 2017 Set 2 | Question: 53 top

Consider a machine with a byte addressable main memory of  $2^{32}$  bytes divided into blocks of size 32 bytes. Assume that a direct mapped cache having 512 cache lines is used with this machine. The size of the tag field in bits is \_\_\_\_\_

gatecse-2017-set2 co-and-architecture cache-memory numerical-answers

Answer key 

### 1.3.48 Cache Memory: GATE CSE 2018 | Question: 34 top



The size of the physical address space of a processor is  $2^P$  bytes. The word length is  $2^W$  bytes. The capacity of cache memory is  $2^N$  bytes. The size of each cache block is  $2^M$  words. For a  $K$ -way set-associative cache memory, the length (in number of bits) of the tag field is

- A.  $P - N - \log_2 K$   
B.  $P - N + \log_2 K$   
C.  $P - N - M - W - \log_2 K$   
D.  $P - N - M - W + \log_2 K$

gatecse-2018 co-and-architecture cache-memory normal 2-marks

Answer key

### 1.3.49 Cache Memory: GATE CSE 2019 | Question: 1 top



A certain processor uses a fully associative cache of size 16 kB. The cache block size is 16 bytes. Assume that the main memory is byte addressable and uses a 32-bit address. How many bits are required for the *Tag* and the *Index* fields respectively in the addresses generated by the processor?

- A. 24 bits and 0 bits  
B. 28 bits and 4 bits  
C. 24 bits and 4 bits  
D. 28 bits and 0 bits

gatecse-2019 co-and-architecture cache-memory normal 1-mark

Answer key

### 1.3.50 Cache Memory: GATE CSE 2019 | Question: 45 top



A certain processor deploys a single-level cache. The cache block size is 8 words and the word size is 4 bytes. The memory system uses a 60-MHz clock. To service a cache miss, the memory controller first takes 1 cycle to accept the starting address of the block, it then takes 3 cycles to fetch all the eight words of the block, and finally transmits the words of the requested block at the rate of 1 word per cycle. The maximum bandwidth for the memory system when the program running on the processor issues a series of read operations is \_\_\_\_\_  $\times 10^6$  bytes/sec.

gatecse-2019 numerical-answers co-and-architecture cache-memory 2-marks

Answer key

### 1.3.51 Cache Memory: GATE CSE 2020 | Question: 21 top



A direct mapped cache memory of 1 MB has a block size of 256 bytes. The cache has an access time of 3 ns and a hit rate of 94%. During a cache miss, it takes 20 ns to bring the first word of a block from the main memory, while each subsequent word takes 5 ns. The word size is 64 bits. The average memory access time in ns (round off to 1 decimal place) is \_\_\_\_\_.

gatecse-2020 numerical-answers co-and-architecture cache-memory 1-mark

Answer key

### 1.3.52 Cache Memory: GATE CSE 2020 | Question: 30 top



A computer system with a word length of 32 bits has a 16 MB byte-addressable main memory and a 64 KB, 4-way set associative cache memory with a block size of 256 bytes. Consider the following four physical addresses represented in hexadecimal notation.

- $A1 = 0x42C8A4$ ,
- $A2 = 0x546888$ ,
- $A3 = 0x6A289C$ ,
- $A4 = 0x5E4880$

Which one of the following is TRUE?

- A.  $A1$  and  $A4$  are mapped to different cache sets.  
B.  $A2$  and  $A3$  are mapped to the same cache set.  
C.  $A3$  and  $A4$  are mapped to the same cache set.  
D.  $A1$  and  $A3$  are mapped to the same cache set.

**Answer key****1.3.53 Cache Memory: GATE CSE 2021 Set 1 | Question: 22**

Consider a computer system with a byte-addressable primary memory of size  $2^{32}$  bytes. Assume the computer system has a direct-mapped cache of size 32 KB ( $1\text{ KB} = 2^{10}$  bytes), and each cache block is of size 64 bytes.

The size of the tag field is \_\_\_\_\_ bits.

**Answer key****1.3.54 Cache Memory: GATE CSE 2021 Set 2 | Question: 19**

Consider a set-associative cache of size 2KB ( $1\text{ KB} = 2^{10}$  bytes) with cache block size of 64 bytes. Assume that the cache is byte-addressable and a 32-bit address is used for accessing the cache. If the width of the tag field is 22 bits, the associativity of the cache is \_\_\_\_\_.

**Answer key****1.3.55 Cache Memory: GATE CSE 2021 Set 2 | Question: 27**

Assume a two-level inclusive cache hierarchy,  $L_1$  and  $L_2$ , where  $L_2$  is the larger of the two. Consider the following statements.

- $S_1$ : Read misses in a write through  $L_1$  cache do not result in writebacks of dirty lines to the  $L_2$
- $S_2$ : Write allocate policy *must* be used in conjunction with write through caches and no-write allocate policy is used with writeback caches.

Which of the following statements is correct?

- |                                     |                                      |
|-------------------------------------|--------------------------------------|
| A. $S_1$ is true and $S_2$ is false | B. $S_1$ is false and $S_2$ is true  |
| C. $S_1$ is true and $S_2$ is true  | D. $S_1$ is false and $S_2$ is false |

**Answer key****1.3.56 Cache Memory: GATE CSE 2022 | Question: 14**

Let WB and WT be two set associative cache organizations that use LRU algorithm for cache block replacement. WB is a write back cache and WT is a write through cache. Which of the following statements is/are FALSE?

- A. Each cache block in WB and WT has a dirty bit.
- B. Every write hit in WB leads to a data transfer from cache to main memory.
- C. Eviction of a block from WT will not lead to data transfer from cache to main memory.
- D. A read miss in WB will never lead to eviction of a dirty block from WB.

**Answer key****1.3.57 Cache Memory: GATE CSE 2022 | Question: 23**

A cache memory that has a hit rate of 0.8 has an access latency 10 ns and miss penalty 100 ns. An optimization is done on the cache to reduce the miss rate. However, the optimization results in an increase of cache access latency to 15 ns, whereas the miss penalty is not affected. The minimum hit rate (*rounded off to two decimal places*) needed after the optimization such that it should not increase the average memory access time is \_\_\_\_\_.

**Answer key****1.3.58 Cache Memory: GATE CSE 2023 | Question: 54**

An 8-way set associative cache of size 64 KB ( $1 \text{ KB} = 1024 \text{ bytes}$ ) is used in a system with 32-bit address. The address is sub-divided into TAG, INDEX, and BLOCK OFFSET.

The number of bits in the TAG is \_\_\_\_\_.

**Answer key****1.3.59 Cache Memory: GATE IT 2004 | Question: 12, ISRO2016-77**

Consider a system with 2 level cache. Access times of Level 1 cache, Level 2 cache and main memory are  $1 \text{ ns}$ ,  $10 \text{ ns}$ , and  $500 \text{ ns}$  respectively. The hit rates of Level 1 and Level 2 caches are 0.8 and 0.9, respectively. What is the average access time of the system ignoring the search time within the cache?

- A. 13.0      B. 12.8      C. 12.6      D. 12.4

**Answer key****1.3.60 Cache Memory: GATE IT 2004 | Question: 48**

Consider a fully associative cache with 8 cache blocks (numbered 0 – 7) and the following sequence of memory block requests:

4, 3, 25, 8, 19, 6, 25, 8, 16, 35, 45, 22, 8, 3, 16, 25, 7

If LRU replacement policy is used, which cache block will have memory block 7?

- A. 4      B. 5      C. 6      D. 7

**Answer key****1.3.61 Cache Memory: GATE IT 2005 | Question: 61**

Consider a 2-way set associative cache memory with 4 sets and total 8 cache blocks (0 – 7) and a main memory with 128 blocks (0 – 127). What memory blocks will be present in the cache after the following sequence of memory block references if LRU policy is used for cache block replacement. Assuming that initially the cache did not have any memory block from the current job?

0 5 3 9 7 0 16 55

- A. 0 3 5 7 16 55      B. 0 3 5 7 9 16 55  
C. 0 5 7 9 16 55      D. 3 5 7 9 16 55

**Answer key****1.3.62 Cache Memory: GATE IT 2006 | Question: 42**

A cache line is 64 bytes. The main memory has latency  $32 \text{ ns}$  and bandwidth  $1 \text{ GBytes/s}$ . The time required to fetch the entire cache line from the main memory is:

- A.  $32 \text{ ns}$       B.  $64 \text{ ns}$       C.  $96 \text{ ns}$       D.  $128 \text{ ns}$

**Answer key****1.3.63 Cache Memory: GATE IT 2006 | Question: 43**

A computer system has a level-1 instruction cache (1-cache), a level-1 data cache ( $D$ -cache) and a level-2 cache ( $L2$ -cache) with the following specifications:

	<b>Capacity</b>	<b>Mapping Method</b>	<b>Block Size</b>
<i>I</i> -Cache	4K words	Direct mapping	4 words
<i>D</i> -Cache	4K words	2-way set associative mapping	4 words
<i>L2</i> -Cache	64K words	4-way set associative mapping	16 words

The length of the physical address of a word in the main memory is 30 bits. The capacity of the tag memory in the *I*-cache, *D*-cache and *L2*-cache is, respectively,

- A. 1 K x 18-bit, 1 K x 19-bit, 4 K x 16-bit  
 C. 1 K x 16-bit, 512 x 18-bit, 1 K x 16-bit
- B. 1 K x 16-bit, 1 K x 19-bit, 4 K x 18-bit  
 D. 1 K x 18-bit, 512 x 18-bit, 1 K x 18-bit

gateit-2006 co-and-architecture cache-memory normal

[Answer key](#) 

#### 1.3.64 Cache Memory: GATE IT 2007 | Question: 37 [top](#)



Consider a Direct Mapped Cache with 8 cache blocks (numbered 0 – 7). If the memory block requests are in the following order

3, 5, 2, 8, 0, 63, 9, 16, 20, 17, 25, 18, 30, 24, 2, 63, 5, 82, 17, 24.

Which of the following memory blocks will not be in the cache at the end of the sequence ?

- A. 3                    B. 18                    C. 20                    D. 30

gateit-2007 co-and-architecture cache-memory normal

[Answer key](#) 

#### 1.3.65 Cache Memory: GATE IT 2008 | Question: 80 [top](#)



Consider a computer with a 4-ways set-associative mapped cache of the following characteristics: a total of 1 MB of main memory, a word size of 1 byte, a block size of 128 words and a cache size of 8 KB.

The number of bits in the TAG, SET and WORD fields, respectively are:

- A. 7,6,7                    B. 8,5,7                    C. 8,6,6                    D. 9,4,7

gateit-2008 co-and-architecture cache-memory normal

[Answer key](#) 

#### 1.3.66 Cache Memory: GATE IT 2008 | Question: 81 [top](#)



Consider a computer with a 4-ways set-associative mapped cache of the following characteristics: a total of 1 MB of main memory, a word size of 1 byte, a block size of 128 words and a cache size of 8 KB.

While accessing the memory location 0C795H by the CPU, the contents of the TAG field of the corresponding cache line is:

- A. 000011000                    B. 110001111                    C. 00011000                    D. 110010101

gateit-2008 co-and-architecture cache-memory normal

[Answer key](#) 

### 1.4

#### Cisc Risc Architecture (2) [top](#)



##### 1.4.1 Cisc Risc Architecture: GATE CSE 1999 | Question: 2.22 [top](#)

The main difference(s) between a CISC and a RISC processor is/are that a RISC processor typically

- A. has fewer instructions  
 C. has more registers
- B. has fewer addressing modes  
 D. is easier to implement using hard-wired logic

gate1999 co-and-architecture normal cisc-risc-architecture multiple-selects

[Answer key](#) 

## 1.4.2 Cisc Risc Architecture: GATE CSE 2018 | Question: 5 top ↗



Consider the following processor design characteristics:

- I. Register-to-register arithmetic operations only
- II. Fixed-length instruction format
- III. Hardwired control unit

Which of the characteristics above are used in the design of a RISC processor?

- A. I and II only      B. II and III only      C. I and III only      D. I, II and III

gatecse-2018 co-and-architecture cisc-risc-architecture easy 1-mark

**Answer key ↗**

## 1.5

## Clock Frequency (2) top ↗



### 1.5.1 Clock Frequency: GATE CSE 1992 | Question: 01-iii top ↗

Many microprocessors have a specified lower limit on clock frequency (apart from the maximum clock frequency limit) because \_\_\_\_\_

gate1992 normal co-and-architecture clock-frequency fill-in-the-blanks

**Answer key ↗**

### 1.5.2 Clock Frequency: GATE IT 2007 | Question: 36 top ↗



The floating point unit of a processor using a design  $D$  takes  $2t$  cycles compared to  $t$  cycles taken by the fixed point unit. There are two more design suggestions  $D_1$  and  $D_2$ .  $D_1$  uses 30% more cycles for fixed point unit but 30% less cycles for floating point unit as compared to design  $D$ .  $D_2$  uses 40% less cycles for fixed point unit but 10% more cycles for floating point unit as compared to design  $D$ . For a given program which has 80% fixed point operations and 20% floating point operations, which of the following ordering reflects the relative performances of three designs?

( $D_i > D_j$  denotes that  $D_i$  is faster than  $D_j$ )

- A.  $D_1 > D > D_2$   
B.  $D_2 > D > D_1$   
C.  $D > D_2 > D_1$   
D.  $D > D_1 > D_2$

gateit-2007 co-and-architecture normal clock-frequency

**Answer key ↗**

## 1.6

## Conflict Misses (1) top ↗



### 1.6.1 Conflict Misses: GATE CSE 2017 Set 1 | Question: 51 top ↗

Consider a 2-way set associative cache with 256 blocks and uses LRU replacement. Initially the cache is empty. Conflict misses are those misses which occur due to the contention of multiple blocks for the same cache set. Compulsory misses occur due to first time access to the block. The following sequence of access to memory blocks :

$\{0, 128, 256, 128, 0, 128, 256, 128, 1, 129, 257, 129, 1, 129, 257, 129\}$

is repeated 10 times. The number of *conflict misses* experienced by the cache is \_\_\_\_\_.

gatecse-2017-set1 co-and-architecture cache-memory conflict-misses normal numerical-answers

**Answer key ↗**

## 1.7

## Control Unit (1) top ↗



### 1.7.1 Control Unit: GATE CSE 1987 | Question: 1-vi top ↗

A microprogrammed control unit

- A. Is faster than a hard-wired control unit.
- B. Facilitates easy implementation of new instruction.
- C. Is useful when very small programs are to be run.

D. Usually refers to the control unit of a microprocessor.

gate1987 co-and-architecture control-unit microprogramming

Answer key 

1.8

Data Dependency (2) [top](#) 

#### 1.8.1 Data Dependency: GATE CSE 2015 Set 3 | Question: 47 [top](#)

Consider the following code sequence having five instructions from  $I_1$  to  $I_5$ . Each of these instructions has the following format.

$OP\ R_i, R_j, R_k$

Where operation OP is performed on contents of registers  $R_j$  and  $R_k$  and the result is stored in register  $R_i$ .

$I_1$ : ADD R1, R2, R3

$I_2$ : MUL R7, R1, R3

$I_3$ : SUB R4, R1, R5

$I_4$ : ADD R3, R2, R4

$I_5$ : MUL R7, R8, R9

Consider the following three statements.

S1: There is an anti-dependence between instructions  $I_2$  and  $I_5$

S2: There is an anti-dependence between instructions  $I_2$  and  $I_4$

S3: Within an instruction pipeline an anti-dependence always creates one or more stalls

Which one of the above statements is/are correct?

- A. Only S1 is true
- C. Only S1 and S3 are true

- B. Only S2 is true
- D. Only S2 and S3 are true

gatecse-2015-set3 co-and-architecture pipelining data-dependency normal

Answer key 

#### 1.8.2 Data Dependency: GATE IT 2007 | Question: 39 [top](#)

Data forwarding techniques can be used to speed up the operation in presence of data dependencies. Consider the following replacements of LHS with RHS.

- i.  $R1 \rightarrow Loc, Loc \rightarrow R2 \equiv R1 \rightarrow R2, R1 \rightarrow Loc$
- ii.  $R1 \rightarrow Loc, Loc \rightarrow R2 \equiv R1 \rightarrow R2$
- iii.  $R1 \rightarrow Loc, R2 \rightarrow Loc \equiv R1 \rightarrow Loc$
- iv.  $R1 \rightarrow Loc, R2 \rightarrow Loc \equiv R2 \rightarrow Loc$

In which of the following options, will the result of executing the RHS be the same as executing the LHS irrespective of the instructions that follow ?

- A. i and iii
- C. ii and iii
- B. i and iv
- D. ii and iv

gateit-2007 data-dependency co-and-architecture

Answer key 

1.9

Data Path (6) [top](#)

#### 1.9.1 Data Path: GATE CSE 1990 | Question: 8a [top](#)

A single bus CPU consists of four general purpose register, namely,  $R0, \dots, R3$ , ALU, MAR, MDR, PC, SP and IR (Instruction Register). Assuming suitable microinstructions, write a microroutine for the instruction, ADD  $R0, R1$ .

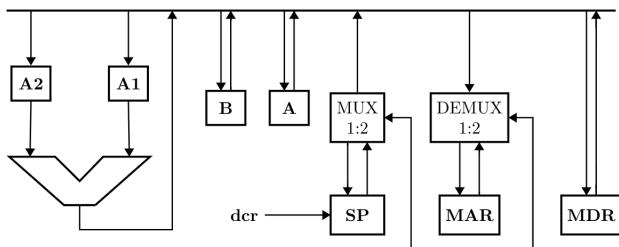
gate1990 descriptive co-and-architecture data-path

Answer key 

### 1.9.2 Data Path: GATE CSE 2001 | Question: 2.13 top



Consider the following data path of a simple non-pipelined CPU. The registers  $A, B, A_1, A_2, \text{MDR}$ , the bus and the ALU are 8-bit wide. SP and MAR are 16-bit registers. The MUX is of size  $8 \times (2 : 1)$  and the DEMUX is of size  $8 \times (1 : 2)$ . Each memory operation takes 2 CPU clock cycles and uses MAR (Memory Address Register) and MDR (Memory Date Register). SP can be decremented locally.



The CPU instruction "push r" where,  $r = A$  or  $B$  has the specification

- $M[\text{SP}] \leftarrow r$
- $\text{SP} \leftarrow \text{SP} - 1$

How many CPU clock cycles are required to execute the "push r" instruction?

- A. 2      B. 3      C. 4      D. 5

gatecse-2001 co-and-architecture data-path machine-instructions normal

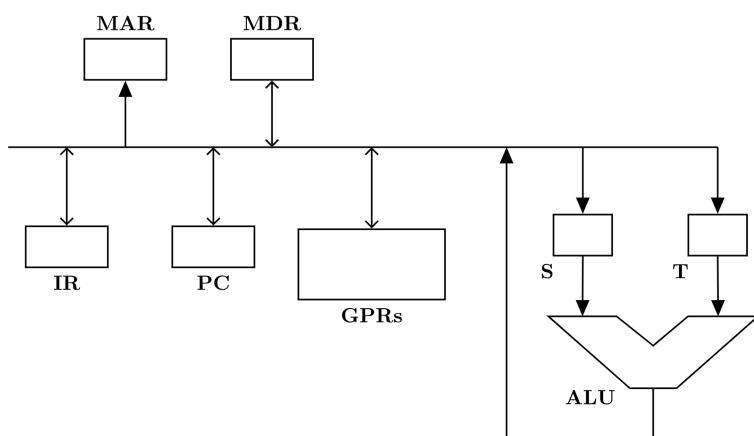
[Answer key](#)



### 1.9.3 Data Path: GATE CSE 2005 | Question: 79 top



Consider the following data path of a CPU.



The ALU, the bus and all the registers in the data path are of identical size. All operations including incrementation of the PC and the GPRs are to be carried out in the ALU. Two clock cycles are needed for memory read operation – the first one for loading address in the MAR and the next one for loading data from the memory bus into the MDR.

The instruction "add R0, R1" has the register transfer interpretation  $R0 \leftarrow R0 + R1$ . The minimum number of clock cycles needed for execution cycle of this instruction is:

- A. 2      B. 3      C. 4      D. 5

gatecse-2005 co-and-architecture machine-instructions data-path normal

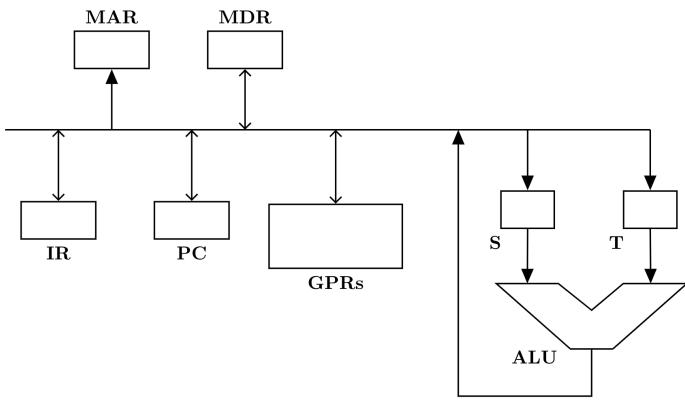
[Answer key](#)



### 1.9.4 Data Path: GATE CSE 2005 | Question: 80 top



Consider the following data path of a CPU.



The ALU, the bus and all the registers in the data path are of identical size. All operations including incrementation of the PC and the GPRs are to be carried out in the ALU. Two clock cycles are needed for memory read operation – the first one for loading address in the MAR and the next one for loading data from the memory bus into the MDR.

The instruction "call Rn, sub" is a two word instruction. Assuming that PC is incremented during the fetch cycle of the first word of the instruction, its register transfer interpretation is

$$Rn \leftarrow PC + 1;$$

$$PC \leftarrow M[PC];$$

The minimum number of **CPU** clock cycles needed during the execution cycle of this instruction is:

A. 2

B. 3

C. 4

D. 5

co-and-architecture normal gatecse-2005 data-path machine-instructions

[Answer key](#)

#### 1.9.5 Data Path: GATE CSE 2016 Set 2 | Question: 30 top ↗

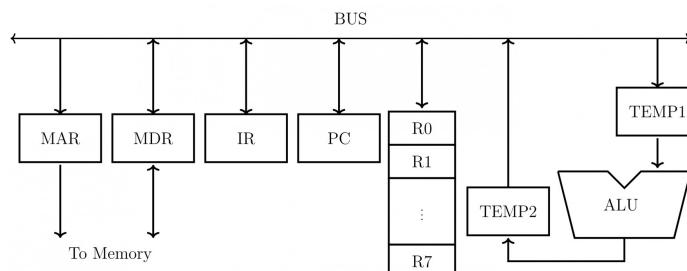
Suppose the functions  $F$  and  $G$  can be computed in 5 and 3 nanoseconds by functional units  $U_F$  and  $U_G$ , respectively. Given two instances of  $U_F$  and two instances of  $U_G$ , it is required to implement the computation  $F(G(X_i))$  for  $1 \leq i \leq 10$ . Ignoring all other delays, the minimum time required to complete this computation is \_\_\_\_\_ nanoseconds.

gatecse-2016-set2 co-and-architecture data-path normal numerical-answers

[Answer key](#)

#### 1.9.6 Data Path: GATE CSE 2020 | Question: 4 top ↗

Consider the following data path diagram.



Consider an instruction:  $R0 \leftarrow R1 + R2$ . The following steps are used to execute it over the given data path. Assume that PC is incremented appropriately. The subscripts  $r$  and  $w$  indicate read and write operations, respectively.

1.  $R2_r$ , TEMP1<sub>r</sub>, ALU<sub>add</sub>, TEMP2<sub>w</sub>
2.  $R1_r$ , TEMP1<sub>w</sub>
3.  $PC_r$ , MAR<sub>w</sub>, MEM<sub>r</sub>
4. TEMP2<sub>r</sub>, R0<sub>w</sub>
5. MDR<sub>r</sub>, IR<sub>w</sub>

Which one of the following is the correct order of execution of the above steps?

- A. 2,1,4,5,3      B. 1,2,4,3,5      C. 3,5,2,1,4      D. 3,5,1,2,4

gatecse-2020 co-and-architecture data-path 1-mark

Answer key 

1.10

Direct Mapping (1) 

1.10.1 Direct Mapping: GATE CSE 2022 | Question: 44 



Consider a system with 2 KB direct mapped data cache with a block size of 64 bytes. The system has a physical address space of 64 KB and a word length of 16 bits. During the execution of a program, four data words P, Q, R, and S are accessed in that order 10 times (i.e., PQRSPQRS...). Hence, there are 40 accesses to data cache altogether. Assume that the data cache is initially empty and no other data words are accessed by the program. The addresses of the first bytes of P, Q, R, and S are 0xA248, 0xC28A, 0xCA8A, and 0xA262, respectively. For the execution of the above program, which of the following statements is/are TRUE with respect to the data cache?

- A. Every access to S is a hit.
- B. Once P is brought to the cache it is never evicted.
- C. At the end of the execution only R and S reside in the cache.
- D. Every access to R evicts Q from the cache.

gatecse-2022 co-and-architecture direct-mapping multiple-selects 2-marks

Answer key 

1.11

Dma (7) 

1.11.1 Dma: GATE CSE 2004 | Question: 68 



A hard disk with a transfer rate of 10 Mbytes/second is constantly transferring data to memory using DMA. The processor runs at 600 MHz, and takes 300 and 900 clock cycles to initiate and complete DMA transfer respectively. If the size of the transfer is 20 Kbytes, what is the percentage of processor time consumed for the transfer operation?

- A. 5.0%
- B. 1.0%
- C. 0.5%
- D. 0.1%

gatecse-2004 dma normal co-and-architecture

Answer key 

1.11.2 Dma: GATE CSE 2005 | Question: 70 



Consider a disk drive with the following specifications:

16 surfaces, 512 tracks/surface, 512 sectors/track, 1 KB/sector, rotation speed 3000 rpm. The disk is operated in cycle stealing mode whereby whenever one 4 byte word is ready it is sent to memory; similarly, for writing, the disk interface reads a 4 byte word from the memory in each DMA cycle. Memory cycle time is 40 nsec. The maximum percentage of time that the CPU gets blocked during DMA operation is:

- A. 10
- B. 25
- C. 40
- D. 50

gatecse-2005 co-and-architecture disk normal dma

Answer key 

1.11.3 Dma: GATE CSE 2011 | Question: 28 



On a non-pipelined sequential processor, a program segment, which is the part of the interrupt service routine, is given to transfer 500 bytes from an I/O device to memory.

Initialize the address register  
Initialize the count to 500  
LOOP: Load a byte from device  
Store in memory at address given by address register  
Increment the address register

Decrement the count  
If count !=0 go to LOOP

Assume that each statement in this program is equivalent to a machine instruction which takes one clock cycle to execute if it is a non-load/store instruction. The load-store instructions take two clock cycles to execute.

The designer of the system also has an alternate approach of using the DMA controller to implement the same transfer. The DMA controller requires 20 clock cycles for initialization and other overheads. Each DMA transfer cycle takes two clock cycles to transfer one byte of data from the device to the memory.

What is the approximate speed up when the DMA controller based design is used in a place of the interrupt driven program based input-output?

- A. 3.4      B. 4.4      C. 5.1      D. 6.7

gatecse-2011 co-and-architecture dma normal

Answer key

#### 1.11.4 Dma: GATE CSE 2016 Set 1 | Question: 31

The size of the data count register of a DMA controller is 16 bits. The processor needs to transfer a file of 29,154 kilobytes from disk to main memory. The memory is byte addressable. The minimum number of times the DMA controller needs to get the control of the system bus from the processor to transfer the file from the disk to main memory is \_\_\_\_\_.

gatecse-2016-set1 co-and-architecture dma normal numerical-answers

Answer key

#### 1.11.5 Dma: GATE CSE 2021 Set 2 | Question: 20

Consider a computer system with DMA support. The DMA module is transferring one 8-bit character in one CPU cycle from a device to memory through *cycle stealing* at regular intervals. Consider a 2 MHz processor. If 0.5% processor cycles are used for DMA, the data transfer rate of the device is \_\_\_\_\_ bits per second.

gatecse-2021-set2 numerical-answers co-and-architecture dma 1-mark

Answer key

#### 1.11.6 Dma: GATE CSE 2022 | Question: 7

Which one of the following facilitates transfer of bulk data from hard disk to main memory with the highest throughput?

- A. DMA based I/O transfer      B. Interrupt driven I/O transfer  
C. Polling based I/O transfer      D. Programmed I/O transfer

gatecse-2022 co-and-architecture dma 1-mark

Answer key

#### 1.11.7 Dma: GATE IT 2004 | Question: 51

The storage area of a disk has the innermost diameter of 10 cm and outermost diameter of 20 cm. The maximum storage density of the disk is 1400 bits/cm. The disk rotates at a speed of 4200 RPM. The main memory of a computer has 64-bit word length and 1 $\mu$ s cycle time. If cycle stealing is used for data transfer from the disk, the percentage of memory cycles stolen for transferring one word is

- A. 0.5%      B. 1%      C. 5%      D. 10%

gateit-2004 co-and-architecture dma normal

Answer key

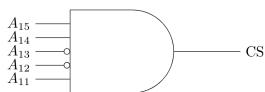
### 1.12

#### Dram (1)

#### 1.12.1 Dram: GATE CSE 2019 | Question: 2

The chip select logic for a certain DRAM chip in a memory system design is shown below. Assume that the

memory system has 16 address lines denoted by  $A_{15}$  to  $A_0$ . What is the range of address (in hexadecimal) of the memory system that can get enabled by the chip select (CS) signal?



- A. C800 to CFFF
- B. CA00 to CAFF
- C. C800 to C8FF
- D. DA00 to DFFF

gatecse-2019 co-and-architecture dram 1-mark

[Answer key](#)

1.13

Ieee Representation (1) [top](#)

#### 1.13.1 Ieee Representation: GATE CSE 2023 | Question: 35 [top](#)



Consider the IEEE-754 single precision floating point numbers  $P = 0xC1800000$  and  $Q = 0x3F5C2EF4$ .

Which one of the following corresponds to the product of these numbers (i.e.,  $P \times Q$ ), represented in the IEEE-754 single precision format?

- A. 0x404C2EF4
- B. 0x405C2EF4
- C. 0xC15C2EF4
- D. 0xC14C2EF4

gatecse-2023 co-and-architecture ieee-representation 2-marks

[Answer key](#)

1.14

Instruction Execution (7) [top](#)

#### 1.14.1 Instruction Execution: GATE CSE 1990 | Question: 4-iii [top](#)



State whether the following statements are TRUE or FALSE with reason:

The flags are affected when conditional CALL or JUMP instructions are executed.

gate1990 true-false co-and-architecture instruction-execution

[Answer key](#)

#### 1.14.2 Instruction Execution: GATE CSE 1992 | Question: 01-iv [top](#)



Many of the advanced microprocessors prefetch instructions and store it in an instruction buffer to speed up processing. This speed up is achieved because \_\_\_\_\_

gate1992 co-and-architecture easy instruction-execution fill-in-the-blanks

[Answer key](#)

#### 1.14.3 Instruction Execution: GATE CSE 1995 | Question: 1.2 [top](#)



Which of the following statements is true?

- A. ROM is a Read/Write memory
- B. PC points to the last instruction that was executed
- C. Stack works on the principle of LIFO
- D. All instructions affect the flags

gate1995 co-and-architecture normal instruction-execution

[Answer key](#)

#### 1.14.4 Instruction Execution: GATE CSE 2002 | Question: 1.13 [top](#)



Which of the following is not a form of memory

- A. instruction cache
- B. instruction register
- C. instruction opcode
- D. translation look-a-side buffer

gatecse-2002 co-and-architecture easy instruction-execution

[Answer key](#)

#### 1.14.5 Instruction Execution: GATE CSE 2006 | Question: 43 top



Consider a new instruction named branch-on-bit-set (mnemonic bbs). The instruction “bbs reg, pos, label” jumps to label if bit in position pos of register operand reg is one. A register is 32 -bits wide and the bits are numbered 0 to 31, bit in position 0 being the least significant. Consider the following emulation of this instruction on a processor that does not have bbs implemented.

$$temp \leftarrow reg \& mask$$

Branch to label if temp is non-zero. The variable temp is a temporary register. For correct emulation, the variable mask must be generated by

- A.  $mask \leftarrow 0x1 << pos$
- B.  $mask \leftarrow 0xffffffff << pos$
- C.  $mask \leftarrow pos$
- D.  $mask \leftarrow 0xf$

gatecse-2006 co-and-architecture normal instruction-execution

[Answer key](#)

#### 1.14.6 Instruction Execution: GATE CSE 2017 Set 1 | Question: 49 top



Consider a RISC machine where each instruction is exactly 4 bytes long. Conditional and unconditional branch instructions use PC-relative addressing mode with Offset specified in bytes to the target location of the branch instruction. Further the Offset is always with respect to the address of the next instruction in the program sequence. Consider the following instruction sequence

Instr. No.	Instruction
i:	add R2, R3, R4
i+1:	sub R5, R6, R7
i+2:	cmp R1, R9, R10
i+3:	beq R1, Offset

If the target of the branch instruction is  $i$ , then the decimal value of the Offset is \_\_\_\_\_.

gatecse-2017-set1 co-and-architecture normal numerical-answers instruction-execution

[Answer key](#)

#### 1.14.7 Instruction Execution: GATE CSE 2021 Set 2 | Question: 53 top



Consider a pipelined processor with 5 stages, Instruction Fetch(IF), Instruction Decode(ID), Execute (EX), Memory Access (MEM), and Write Back (WB). Each stage of the pipeline, except the EX stage, takes one cycle. Assume that the ID stage merely decodes the instruction and the register read is performed in the EX stage. The EX stage takes one cycle for ADD instruction and the register read is performed in the EX stage. The EX stage takes one cycle for ADD instruction and two cycles for MUL instruction. Ignore pipeline register latencies.

Consider the following sequence of 8 instructions:

ADD, MUL, ADD, MUL, ADD, MUL, ADD, MUL

Assume that every MUL instruction is data-dependent on the ADD instruction just before it and every ADD instruction (except the first ADD) is data-dependent on the MUL instruction just before it. The *speedup* defined as follows.

$$Speedup = \frac{\text{Execution time without operand forwarding}}{\text{Execution time with operand forwarding}}$$

The *Speedup* achieved in executing the given instruction sequence on the pipelined processor (rounded to 2 decimal places) is \_\_\_\_\_

gatecse-2021-set2 co-and-architecture pipelining instruction-execution numerical-answers 2-marks

[Answer key](#)

1.15

**Instruction Format (7)****1.15.1 Instruction Format: GATE CSE 1988 | Question: 2-ii**

Using an expanding opcode encoding for instructions, is it possible to encode all of the following in an instruction format shown in the below figure. Justify your answer.

- 14 double address instructions
- 127 single address instructions
- 60 no address (zero address) instructions

← 4 bits →	← 6 bits →	← 6 bits →
Opcode	Operand 1 Address	Operand 2 Address

gate1988 normal co-and-architecture instruction-format descriptive

**Answer key****1.15.2 Instruction Format: GATE CSE 1992 | Question: 01-vi**

In an 11-bit computer instruction format, the size of address field is 4-bits. The computer uses expanding OP code technique and has 5 two-address instructions and 32 one-address instructions. The number of zero-address instructions it can support is \_\_\_\_\_

gate1992 co-and-architecture machine-instructions instruction-format normal numerical-answers

**Answer key****1.15.3 Instruction Format: GATE CSE 1994 | Question: 3.2**

State True or False with one line explanation

Expanding opcode instruction formats are commonly employed in RISC. (Reduced Instruction Set Computers) machines.

gate1994 co-and-architecture machine-instructions instruction-format normal true-false

**Answer key****1.15.4 Instruction Format: GATE CSE 2014 Set 1 | Question: 9**

A machine has a 32-bit architecture, with 1-word long instructions. It has 64 registers, each of which is 32 bits long. It needs to support 45 instructions, which have an immediate operand in addition to two register operands. Assuming that the immediate operand is an unsigned integer, the maximum value of the immediate operand is \_\_\_\_\_

gatecse-2014-set1 co-and-architecture machine-instructions instruction-format numerical-answers normal

**Answer key****1.15.5 Instruction Format: GATE CSE 2016 Set 2 | Question: 31**

Consider a processor with 64 registers and an instruction set of size twelve. Each instruction has five distinct fields, namely, opcode, two source register identifiers, one destination register identifier, and twelve-bit immediate value. Each instruction must be stored in memory in a byte-aligned fashion. If a program has 100 instructions, the amount of memory (in bytes) consumed by the program text is \_\_\_\_\_.

gatecse-2016-set2 instruction-format machine-instructions co-and-architecture normal numerical-answers

**Answer key****1.15.6 Instruction Format: GATE CSE 2018 | Question: 51**

A processor has 16 integer registers ( $R_0, R_1, \dots, R_{15}$ ) and 64 floating point registers ( $F_0, F_1, \dots, F_{63}$ ). It uses a 2-byte instruction format. There are four categories of instructions:

Type-1, Type-2, Type-3, and Type-4. Type-1 category consists of four instructions, each with 3 integer register operands (3Rs). Type-2 category consists of eight instructions, each with 2 floating point register operands (2Fs). Type-3 category consists of fourteen instructions, each with one integer register operand and one floating point register operand (1R+1F). Type-4 category consists of N instructions, each with a floating point register operand (1F).

The maximum value of N is \_\_\_\_\_.

gatecse-2018 co-and-architecture machine-instructions instruction-format numerical-answers 2-marks

[Answer key](#)

#### 1.15.7 Instruction Format: GATE CSE 2020 | Question: 44 [top](#)

A processor has 64 registers and uses 16-bit instruction format. It has two types of instructions: I-type and R-type. Each I-type instruction contains an opcode, a register name, and a 4-bit immediate value. Each R-type instruction contains an opcode and two register names. If there are 8 distinct I-type opcodes, then the maximum number of distinct R-type opcodes is \_\_\_\_\_.

gatecse-2020 co-and-architecture numerical-answers instruction-format machine-instructions 2-marks

[Answer key](#)

### 1.16

#### Interrupts (8) [top](#)

##### 1.16.1 Interrupts: GATE CSE 1987 | Question: 1-viii [top](#)



On receiving an interrupt from a I/O device the CPU:

- A. Halts for a predetermined time.
- B. Hands over control of address bus and data bus to the interrupting device.
- C. Branches off to the interrupt service routine immediately.
- D. Branches off to the interrupt service routine after completion of the current instruction.

gate1987 co-and-architecture interrupts

[Answer key](#)

##### 1.16.2 Interrupts: GATE CSE 1995 | Question: 1.3 [top](#)



In a vectored interrupt:

- A. The branch address is assigned to a fixed location in memory
- B. The interrupting source supplies the branch information to the processor through an interrupt vector
- C. The branch address is obtained from a register in the processor
- D. None of the above

gate1995 co-and-architecture interrupts normal

[Answer key](#)

##### 1.16.3 Interrupts: GATE CSE 1998 | Question: 1.20 [top](#)



Which of the following is true?

- A. Unless enabled, a CPU will not be able to process interrupts.
- B. Loop instructions cannot be interrupted till they complete.
- C. A processor checks for interrupts before executing a new instruction.
- D. Only level triggered interrupts are possible on microprocessors.

gate1998 co-and-architecture interrupts normal

[Answer key](#)

#### 1.16.4 Interrupts: GATE CSE 2002 | Question: 1.9 [top](#)

A device employing INTR line for device interrupt puts the CALL instruction on the data bus while:

- A. *INTA* is active
- B. HOLD is active
- C. READY is inactive
- D. None of the above

gatecse-2002 co-and-architecture interrupts normal

[Answer key](#)



#### 1.16.5 Interrupts: GATE CSE 2005 | Question: 69 [top](#)

A device with data transfer rate 10 KB/sec is connected to a CPU. Data is transferred byte-wise. Let the interrupt overhead be  $4\mu\text{sec}$ . The byte transfer time between the device interface register and CPU or memory is negligible. What is the minimum performance gain of operating the device under interrupt mode over operating it under program-controlled mode?

- A. 15
- B. 25
- C. 35
- D. 45

gatecse-2005 co-and-architecture interrupts

[Answer key](#)



#### 1.16.6 Interrupts: GATE CSE 2009 | Question: 8, UGCNET-June2012-III: 58 [top](#)

A CPU generally handles an interrupt by executing an interrupt service routine:

- A. As soon as an interrupt is raised.
- B. By checking the interrupt register at the end of fetch cycle.
- C. By checking the interrupt register after finishing the execution of the current instruction.
- D. By checking the interrupt register at fixed time intervals.

gatecse-2009 co-and-architecture interrupts normal ugcnetcse-june2012-paper3

[Answer key](#)



#### 1.16.7 Interrupts: GATE CSE 2020 | Question: 3 [top](#)

Consider the following statements.

- I. Daisy chaining is used to assign priorities in attending interrupts.
- II. When a device raises a vectored interrupt, the CPU does polling to identify the source of interrupt.
- III. In polling, the CPU periodically checks the status bits to know if any device needs its attention.
- IV. During DMA, both the CPU and DMA controller can be bus masters at the same time.

Which of the above statements is/are TRUE?

- A. I and II only
- B. I and IV only
- C. I and III only
- D. III only

gatecse-2020 co-and-architecture interrupts 1-mark

[Answer key](#)



#### 1.16.8 Interrupts: GATE CSE 2023 | Question: 24 [top](#)

A keyboard connected to a computer is used at a rate of 1 keystroke per second. The computer system polls the keyboard every 10 ms (milli seconds) to check for a keystroke and consumes 100  $\mu\text{s}$  (micro seconds) for each poll. If it is determined after polling that a key has been pressed, the system consumes an additional 200  $\mu\text{s}$  to process the keystroke. Let  $T_1$  denote the fraction of a second spent in polling and processing a keystroke.



In an alternative implementation, the system uses interrupts instead of polling. An interrupt is raised for every keystroke. It takes a total of 1 ms for servicing an interrupt and processing a keystroke. Let  $T_2$  denote the fraction of a second spent in servicing the interrupt and processing a keystroke.

The ratio  $\frac{T_1}{T_2}$  is \_\_\_\_\_. (Rounded off to one decimal place)

gatecse-2023 co-and-architecture interrupts numerical-answers 1-mark

[Answer key](#)

1.17

Io Handling (7) [top](#)



#### 1.17.1 Io Handling: GATE CSE 1987 | Question: 2a [top](#)

State whether the following statements are TRUE or FALSE

In a microprocessor-based system, if a bus (DMA) request and an interrupt request arrive simultaneously, the microprocessor attends first to the bus request.

gate1987 co-and-architecture interrupts io-handling true-false

[Answer key](#)



#### 1.17.2 Io Handling: GATE CSE 1987 | Question: 2b [top](#)

State whether the following statements are TRUE or FALSE:

Data transfer between a microprocessor and an I/O device is usually faster in memory-mapped-I/O scheme than in I/O-mapped -I/O scheme.

gate1987 co-and-architecture io-handling true-false

[Answer key](#)



#### 1.17.3 Io Handling: GATE CSE 1990 | Question: 4-ii [top](#)

State whether the following statements are TRUE or FALSE with reason:

The data transfer between memory and I/O devices using programmed I/O is faster than interrupt-driven I/O.

gate1990 true-false co-and-architecture io-handling interrupts

[Answer key](#)



#### 1.17.4 Io Handling: GATE CSE 1996 | Question: 1.24 [top](#)

For the daisy chain scheme of connecting I/O devices, which of the following statements is true?

- A. It gives non-uniform priority to various devices
- B. It gives uniform priority to all devices
- C. It is only useful for connecting slow devices to a processor device
- D. It requires a separate interrupt pin on the processor for each device

gate1996 co-and-architecture io-handling normal

[Answer key](#)



#### 1.17.5 Io Handling: GATE CSE 1996 | Question: 25 [top](#)

A hard disk is connected to a 50 MHz processor through a DMA controller. Assume that the initial set-up of a DMA transfer takes 1000 clock cycles for the processor, and assume that the handling of the interrupt at DMA completion requires 500 clock cycles for the processor. The hard disk has a transfer rate of 2000 Kbytes/sec and average block transferred is 4 K bytes. What fraction of the processor time is consumed by the disk, if the disk is actively transferring 100% of the time?

gate1996 co-and-architecture io-handling dma numerical-answers normal

[Answer key](#)

### 1.17.6 I/O Handling: GATE CSE 1997 | Question: 2.4 top



The correct matching for the following pairs is:

- |                             |                    |
|-----------------------------|--------------------|
| (A) DMA I/O                 | (1) High speed RAM |
| (B) Cache                   | (2) Disk           |
| (C) Interrupt I/O           | (3) Printer        |
| (D) Condition Code Register | (4) ALU            |

- A. A - 4 B - 3 C - 1 D - 2  
C. A - 4 B - 3 C - 2 D - 1

- B. A - 2 B - 1 C - 3 D - 4  
D. A - 2 B - 3 C - 4 D - 1

gate1997 co-and-architecture normal io-handling

[Answer key](#)

### 1.17.7 I/O Handling: GATE CSE 2008 | Question: 64, ISRO2009-13 top



Which of the following statements about synchronous and asynchronous I/O is NOT true?

- A. An ISR is invoked on completion of I/O in synchronous I/O but not in asynchronous I/O
- B. In both synchronous and asynchronous I/O, an ISR (Interrupt Service Routine) is invoked after completion of the I/O
- C. A process making a synchronous I/O call waits until I/O is complete, but a process making an asynchronous I/O call does not wait for completion of the I/O
- D. In the case of synchronous I/O, the process waiting for the completion of I/O is woken up by the ISR that is invoked after the completion of I/O

gatecse-2008 operating-system io-handling normal isro2009

[Answer key](#)

## 1.18

### Machine Instructions (19) top



#### 1.18.1 Machine Instructions: GATE CSE 1988 | Question: 9i top

The following program fragment was written in an assembly language for a single address computer with one accumulator register:

```
LOAD B
MULT C
STORE T1
ADD A
STORE T2
MULT T2
ADD T1
STORE Z
```

Give the arithmetic expression implemented by the fragment.

gate1988 normal descriptive co-and-architecture machine-instructions

[Answer key](#)

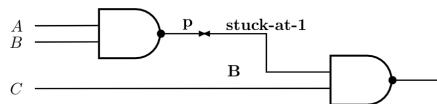
#### 1.18.2 Machine Instructions: GATE CSE 1994 | Question: 12 top



- A. Assume that a CPU has only two registers  $R_1$  and  $R_2$  and that only the following instruction is available  $XOR R_i, R_j; \{R_j \leftarrow R_i \oplus R_j, \text{ for } i, j = 1, 2\}$

Using this XOR instruction, find an instruction sequence in order to exchange the contents of the registers  $R_1$  and  $R_2$ .

- B. The line p of the circuit shown in figure has stuck at 1 fault. Determine an input test to detect the fault.



gate1994 co-and-architecture machine-instructions normal descriptive

**Answer key**

### 1.18.3 Machine Instructions: GATE CSE 1999 | Question: 17 top



Consider the following program fragment in the assembly language of a certain hypothetical processor. The processor has three general purpose registers  $R1$ ,  $R2$  and  $R3$ . The meanings of the instructions are shown by comments (starting with ;) after the instructions.

```
X: CMP R1, 0; Compare R1 and 0, set flags appropriately in status register
JZ Z; Jump if zero to target Z
MOV R2, R1; Copy contents of R1 to R2
SHR R1; Shift right R1 by 1 bit
SHL R1; Shift left R1 by 1 bit
CMP R2, R1; Compare R2 and R1 and set flag in status register
JZ Y; Jump if zero to target Y
INC R3; Increment R3 by 1;
Y: SHR R1; Shift right R1 by 1 bit
JMP X; Jump to target X
Z:...
```

- Initially  $R1$ ,  $R2$  and  $R3$  contain the values 5, 0 and 0 respectively, what are the final values of  $R1$  and  $R3$  when control reaches  $Z$ ?
- In general, if  $R1$ ,  $R2$  and  $R3$  initially contain the values  $n$ , 0, and 0 respectively. What is the final value of  $R3$  when control reaches  $Z$ ?

gate1999 co-and-architecture machine-instructions normal descriptive

**Answer key**

### 1.18.4 Machine Instructions: GATE CSE 2003 | Question: 48 top



Consider the following assembly language program for a hypothetical processor  $A$ ,  $B$ , and  $C$  are 8-bit registers. The meanings of various instructions are shown as comments.

```
MOV B, #0      ; B ← 0
MOV C, #8      ; C ← 8
Z: CMP C, #0    ; compare C with 0
JZ X          ; jump to X if zero flag is set
SUB C, #1      ; C ← C – 1
RRCA, #1       ; right rotate A through carry by one bit. Thus:
                ; If the initial values of A and the carry flag are  $a_7 \dots a_0$  and
                ;  $c_0$  respectively, their values after the execution of this
                ; instruction will be  $c_0 a_7 \dots a_1$  and  $a_0$  respectively.
JC Y          ; jump to Y if carry flag is set
JMP Z          ; jump to Z
Y: ADD B, #1    ; B ← B + 1
JMP Z          ; jump to Z
X:            ;
```

If the initial value of register A is  $A_0$  the value of register B after the program execution will be

- the number of 0 bits in  $A_0$
- the number of 1 bits in  $A_0$
- $A_0$
- 8

gatecse-2003 co-and-architecture machine-instructions normal

Answer key

### 1.18.5 Machine Instructions: GATE CSE 2003 | Question: 49 top



Consider the following assembly language program for a hypothetical processor  $A, B$ , and  $C$  are 8 bit registers. The meanings of various instructions are shown as comments.

```
MOV B, #0 ;B ← 0
MOV C, #8 ;C ← 8
Z: CMP #0 C, ;compare C with 0
JZ X ;jump to X if zero flag is set
SUB C, #1 ;C ← C – 1
RRC A, #1 ;right rotate A through carry by one bit. Thus:
```

; If the initial values of A and the carry flag are  $a_7 \dots a_0$  and  
;  $c_0$  respectively, their values after the execution of this  
; instruction will be  $c_0 a_7 \dots a_1$  and  $a_0$  respectively.

```
JC Y ;jump to Y if carry flag is set
JMP Z ;jump to Z
Y: ADD B, #1 ;B ← B + 1
JMP Z ;jump to Z
```

X:

Which of the following instructions when inserted at location  $X$  will ensure that the value of the register  $A$  after program execution is as same as its initial value?

- A. RRC A, #1
- B. NOP; no operation
- C. LRC A, #1; left rotate  $A$  through carry flag by one bit
- D. ADD A, #1

gatecse-2003 co-and-architecture machine-instructions normal

Answer key

### 1.18.6 Machine Instructions: GATE CSE 2004 | Question: 63 top



Consider the following program segment for a hypothetical CPU having three user registers  $R_1, R_2$  and  $R_3$ .

Instruction	Operation	Instruction size (in words)
MOV $R_1, 5000$	$R_1 \leftarrow \text{Memory}[5000]$	2
MOV $R_2, (R_1)$	$R_2 \leftarrow \text{Memory}[(R_1)]$	1
ADD $R_2, R_3$	$R_2 \leftarrow R_2 + R_3$	1
MOV 6000, $R_2$	$\text{Memory}[6000] \leftarrow R_2$	2
HALT	Machine Halts	1

Consider that the memory is byte addressable with size 32 bits, and the program has been loaded starting from memory location 1000 (decimal). If an interrupt occurs while the CPU has been halted after executing the HALT instruction, the return address (in decimal) saved in the stack will be

- A. 1007
- B. 1020
- C. 1024
- D. 1028

gatecse-2004 co-and-architecture machine-instructions normal

Answer key

### 1.18.7 Machine Instructions: GATE CSE 2004 | Question: 64 top



Consider the following program segment for a hypothetical CPU having three user registers  $R_1, R_2$  and  $R_3$ .

Instruction	Operation	Instruction size (in Words)
MOV $R_1, 5000$	$R_1 \leftarrow \text{Memory}[5000]$	2
MOV $R_2(R_1)$	$R_2 \leftarrow \text{Memory}[(R_1)]$	1
ADD $R_2, R_3$	$R_2 \leftarrow R_2 + R_3$	1
MOV 6000, $R_2$	$\text{Memory}[6000] \leftarrow R_2$	2
Halt	Machine Halts	1

Let the clock cycles required for various operations be as follows:

Register to/from memory transfer	3 clock cycles
ADD with both operands in register	1 clock cycles
Instruction fetch and decode	2 clock cycles

The total number of clock cycles required to execute the program is

- A. 29      B. 24      C. 23      D. 20

gatecse-2004 co-and-architecture machine-instructions normal

[Answer key](#)

### 1.18.8 Machine Instructions: GATE CSE 2006 | Question: 09, ISRO2009-35 top



A CPU has 24-bit instructions. A program starts at address 300 (in decimal). Which one of the following is a legal program counter (all values in decimal)?

- A. 400      B. 500      C. 600      D. 700

gatecse-2006 co-and-architecture machine-instructions easy isro2009

[Answer key](#)

### 1.18.9 Machine Instructions: GATE CSE 2007 | Question: 54 top



In a simplified computer the instructions are:

OP $R_j, R_i$	Perform $R_j \text{ OP } R_i$ and store the result in register $R_j$
OP $m, R_i$	Perform $val \text{ OP } R_i$ and store the result in register $R_i$ $val$ denotes the content of the memory location $m$
MOV $m, R_i$	Moves the content of memory location $m$ to register $R_i$
MOV $R_i, m$	Moves the content of register $R_i$ to memory location $m$

The computer has only two registers, and OP is either ADD or SUB. Consider the following basic block:

- $t_1 = a + b$
- $t_2 = c + d$
- $t_3 = e - t_2$
- $t_4 = t_1 - t_3$

Assume that all operands are initially in memory. The final value of the computation should be in memory. What is the minimum number of MOV instructions in the code generated for this basic block?

- A. 2      B. 3      C. 5      D. 6

gatecse-2007 co-and-architecture machine-instructions normal

[Answer key](#)

### 1.18.10 Machine Instructions: GATE CSE 2007 | Question: 71 top 4



Consider the following program segment. Here R1, R2 and R3 are the general purpose registers.

	Instruction	Operation	Instruction Size (no. of words)
	MOV R1,(3000)	R1 ← M[3000]	2
LOOP:	MOV R2,(R3)	R2 ← M[R3]	1
	ADD R2,R1	R2 ← R1 + R2	1
	MOV (R3),R2	M[R3] ← R2	1
	INC R3	R3 ← R3 + 1	1
	DEC R1	R1 ← R1 - 1	1
	BNZ LOOP	Branch on not zero	2
	HALT	Stop	1

Assume that the content of memory location 3000 is 10 and the content of the register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 1000. All the numbers are in decimal.

Assume that the memory is word addressable. The number of memory references for accessing the data in executing the program completely is

- A. 10      B. 11      C. 20      D. 21

gatecse-2007 co-and-architecture machine-instructions interrupts normal

[Answer key](#)



### 1.18.11 Machine Instructions: GATE CSE 2007 | Question: 72 top 4

Consider the following program segment. Here R1, R2 and R3 are the general purpose registers.

	Instruction	Operation	Instruction Size (no. of words)
	MOV R1,(3000)	R1 ← M[3000]	2
LOOP:	MOV R2,(R3)	R2 ← M[R3]	1
	ADD R2,R1	R2 ← R1 + R2	1
	MOV (R3),R2	M[R3] ← R2	1
	INC R3	R3 ← R3 + 1	1
	DEC R1	R1 ← R1 - 1	1
	BNZ LOOP	Branch on not zero	2
	HALT	Stop	1

Assume that the content of memory location 3000 is 10 and the content of the register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 1000. All the numbers are in decimal.

Assume that the memory is word addressable. After the execution of this program, the content of memory location 2010 is:

- A. 100      B. 101      C. 102      D. 110

gatecse-2007 co-and-architecture machine-instructions interrupts normal

[Answer key](#)



### 1.18.12 Machine Instructions: GATE CSE 2007 | Question: 73 top 4

Consider the following program segment. Here R1, R2 and R3 are the general purpose registers.

	Instruction	Operation	Instruction Size (no. of words)
	MOV R1,(3000)	R1 $\leftarrow$ M[3000]	2
LOOP:	MOV R2,(R3)	R2 $\leftarrow$ M[R3]	1
	ADD R2,R1	R2 $\leftarrow$ R1 + R2	1
	MOV (R3),R2	M[R3] $\leftarrow$ R2	1
	INC R3	R3 $\leftarrow$ R3 + 1	1
	DEC R1	R1 $\leftarrow$ R1 - 1	1
	BNZ LOOP	Branch on not zero	2
	HALT	Stop	1

Assume that the content of memory location 3000 is 10 and the content of the register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 1000. All the numbers are in decimal.

Assume that the memory is byte addressable and the word size is 32 bits. If an interrupt occurs during the execution of the instruction “INC R3”, what return address will be pushed on to the stack?

- A. 1005      B. 1020      C. 1024      D. 1040

gatecse-2007 co-and-architecture machine-instructions interrupts normal

Answer key ↗

#### 1.18.13 Machine Instructions: GATE CSE 2008 | Question: 34 top ↗

Which of the following must be true for the RFE (Return From Exception) instruction on a general purpose processor?

- I. It must be a trap instruction
- II. It must be a privileged instruction
- III. An exception cannot be allowed to occur during execution of an RFE instruction

- A. I only      B. II only      C. I and II only      D. I, II and III only

gatecse-2008 co-and-architecture machine-instructions normal

Answer key ↗

#### 1.18.14 Machine Instructions: GATE CSE 2015 Set 2 | Question: 42 top ↗

Consider a processor with byte-addressable memory. Assume that all registers, including program counter (PC) and Program Status Word (PSW), are size of two bytes. A stack in the main memory is implemented from memory location  $(0100)_{16}$  and it grows upward. The stack pointer (SP) points to the top element of the stack. The current value of SP is  $(016E)_{16}$ . The CALL instruction is of two words, the first word is the op-code and the second word is the starting address of the subroutine (one word = 2 bytes). The CALL instruction is implemented as follows:

- Store the current value of PC in the stack
- Store the value of PSW register in the stack
- Load the starting address of the subroutine in PC

The content of PC just before the fetch of a CALL instruction is  $(5FA0)_{16}$ . After execution of the CALL instruction, the value of the stack pointer is:

- A.  $(016A)_{16}$       B.  $(016C)_{16}$       C.  $(0170)_{16}$       D.  $(0172)_{16}$

gatecse-2015-set2 co-and-architecture machine-instructions easy

Answer key ↗

### 1.18.15 Machine Instructions: GATE CSE 2016 Set 2 | Question: 10 top



A processor has 40 distinct instruction and 24 general purpose registers. A 32-bit instruction word has an opcode, two registers operands and an immediate operand. The number of bits available for the immediate operand field is \_\_\_\_\_.

gatecse-2016-set2 machine-instructions co-and-architecture easy numerical-answers

[Answer key](#)

### 1.18.16 Machine Instructions: GATE CSE 2021 Set 1 | Question: 55 top



Consider the following instruction sequence where registers R1, R2 and R3 are general purpose and MEMORY[X] denotes the content at the memory location X.

Instruction	Semantics	Instruction Size (bytes)
MOV R1, (5000)	$R1 \leftarrow \text{MEMORY}[5000]$	4
MOV R2, (R3)	$R2 \leftarrow \text{MEMORY}[R3]$	4
ADDR2, R1	$R2 \leftarrow R1 + R2$	2
MOV (R3), R2	$\text{MEMORY}[R3] \leftarrow R2$	4
INC R3	$R3 \leftarrow R3 + 1$	2
DEC R1	$R1 \leftarrow R1 - 1$	2
BNZ 1004	Branch if not zero to the given absolute address	2
HALT	Stop	1

Assume that the content of the memory location 5000 is 10, and the content of the register R3 is 3000. The content of each of the memory locations from 3000 to 3020 is 50. The instruction sequence starts from the memory location 1000. All the numbers are in decimal format. Assume that the memory is byte addressable.

After the execution of the program, the content of memory location 3010 is \_\_\_\_\_

gatecse-2021-set1 co-and-architecture machine-instructions numerical-answers 2-marks

[Answer key](#)

### 1.18.17 Machine Instructions: GATE IT 2004 | Question: 46 top



If we use internal data forwarding to speed up the performance of a CPU (R1, R2 and R3 are registers and M[100] is a memory reference), then the sequence of operations

$R1 \rightarrow M[100]$   
 $M[100] \rightarrow R2$   
 $M[100] \rightarrow R3$

can be replaced by

- |   |  |
|---|--|
| A. $R1 \rightarrow R3$<br>$R2 \rightarrow M[100]$ | B. $M[100] \rightarrow R2$<br>$R1 \rightarrow R2$<br>$R1 \rightarrow R3$ |
| C. $R1 \rightarrow M[100]$<br>$R2 \rightarrow R3$ | D. $R1 \rightarrow R2$<br>$R1 \rightarrow R3$<br>$R1 \rightarrow M[100]$ |

gateit-2004 co-and-architecture machine-instructions easy

[Answer key](#)

### 1.18.18 Machine Instructions: GATE IT 2007 | Question: 41 top



Following table indicates the latencies of operations between the instruction producing the result and instruction using the result.

Instruction producing the result	Instruction using the result	Latency
ALU Operation	ALU Operation	2
ALU Operation	Store	2
Load	ALU Operation	1
Load	Store	0

Consider the following code segment:

```

Load R1, Loc 1; Load R1 from memory location Loc1
Load R2, Loc 2; Load R2 from memory location Loc 2
Add R1, R2, R1; Add R1 and R2 and save result in R1
Dec R2; Decrement R2
Dec R1; Decrement R1
Mpy R1, R2, R3; Multiply R1 and R2 and save result in R3
Store R3, Loc 3; Store R3 in memory location Loc 3

```

What is the number of cycles needed to execute the above code segment assuming each instruction takes one cycle to execute?

- A. 7      B. 10      C. 13      D. 14

gateit-2007 co-and-architecture machine-instructions normal

[Answer key](#)

#### 1.18.19 Machine Instructions: GATE IT 2008 | Question: 38

Assume that  $EA = (X) +$  is the effective address equal to the contents of location X, with X incremented by one word length after the effective address is calculated;  $EA = -(X)$  is the effective address equal to the contents of location X, with X decremented by one word length before the effective address is calculated;  $EA = (X) -$  is the effective address equal to the contents of location X, with X decremented by one word length after the effective address is calculated. The format of the instruction is (opcode, source, destination), which means (destination  $\leftarrow$  source op destination). Using X as a stack pointer, which of the following instructions can pop the top two elements from the stack, perform the addition operation and push the result back to the stack.

- A. ADD  $(X) -, (X)$   
 C. ADD  $-(X), (X) +$   
 B. ADD  $(X), (X) -$   
 D. ADD  $-(X), (X)$

gateit-2008 co-and-architecture machine-instructions normal

[Answer key](#)

#### 1.19

#### Memory Interfacing (3)

##### 1.19.1 Memory Interfacing: GATE CSE 2016 Set 1 | Question: 09

A processor can support a maximum memory of 4 GB, where the memory is word-addressable (a word consists of two bytes). The size of address bus of the processor is at least \_\_\_\_\_ bits.

gatecse-2016-set1 co-and-architecture easy numerical-answers memory-interfacing

[Answer key](#)

##### 1.19.2 Memory Interfacing: GATE CSE 2018 | Question: 23

A 32-bit wide main memory unit with a capacity of 1 GB is built using  $256M \times 4$ -bit DRAM chips. The number of rows of memory cells in the DRAM chip is  $2^{14}$ . The time taken to perform one refresh operation is 50 nanoseconds. The refresh period is 2 milliseconds. The percentage (rounded to the closest integer) of the time available for performing the memory read/write operations in the main memory unit is \_\_\_\_\_.

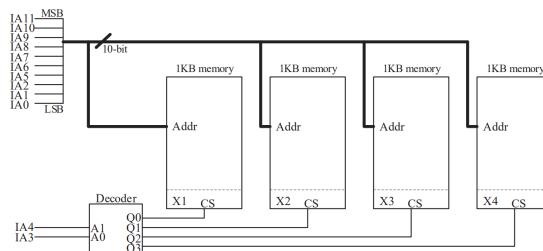
gatecse-2018 co-and-architecture memory-interfacing normal numerical-answers 1-mark

[Answer key](#)

##### 1.19.3 Memory Interfacing: GATE CSE 2023 | Question: 32

A 4 kilobyte (KB) byte-addressable memory is realized using four 1 KB memory blocks. Two input address

lines (IA4 and IA3) are connected to the chip select (CS) port of these memory blocks through a decoder as shown in the figure. The remaining ten input address lines from IA11-IA0 are connected to the address port of these blocks. The chip select (CS) is active high.



The input memory addresses (IA11-IA0), in decimal, for the starting locations (Addr = 0) of each block (indicated as X1, X2, X3, X4 in the figure) are among the options given below. Which one of the following options is CORRECT?

- A. (0,1,2,3)      B. (0,1024,2048,3072)      C. (0,8,16,24)      D. (0,0,0,0)

gatecse-2023 co-and-architecture memory-interfacing 2-marks

[Answer key](#)

1.20

### Memory Interleaving (1) [top](#)

#### 1.20.1 Memory Interleaving: GATE CSE 1990 | Question: 4-iv [top](#)



Transferring data in blocks from the main memory to the cache memory enables an interleaved main memory unit to operate unit at its maximum speed. True/False. Explain.

gate-1990 true-false co-and-architecture cache-memory memory-interleaving

[Answer key](#)

1.21

### Microprogramming (12) [top](#)

#### 1.21.1 Microprogramming: GATE CSE 1987 | Question: 4a [top](#)



Find out the width of the control memory of a horizontal microprogrammed control unit, given the following specifications:

- 16 control lines for the processor consisting of ALU and 7 registers.
- Conditional branching facility by checking 4 status bits.
- Provision to hold 128 words in the control memory.

gate1987 co-and-architecture microprogramming descriptive

[Answer key](#)

#### 1.21.2 Microprogramming: GATE CSE 1996 | Question: 2.25 [top](#)



A micro program control unit is required to generate a total of 25 control signals. Assume that during any micro instruction, at most two control signals are active. Minimum number of bits required in the control word to generate the required control signals will be:

- A. 2      B. 2.5      C. 10      D. 12

gate1996 co-and-architecture microprogramming normal

[Answer key](#)

#### 1.21.3 Microprogramming: GATE CSE 1997 | Question: 5.3 [top](#)



A micro instruction is to be designed to specify:

- none or one of the three micro operations of one kind and
- none or upto six micro operations of another kind

The minimum number of bits in the micro-instruction is:

- A. 9      B. 5      C. 8      D. None of the above

gate1997 co-and-architecture microporogramming normal

[Answer key](#)

#### 1.21.4 Microprogramming: GATE CSE 1999 | Question: 2.19 [top](#)

Arrange the following configuration for CPU in decreasing order of operating speeds:

Hard wired control, Vertical microprogramming, Horizontal microprogramming.

- A. Hard wired control, Vertical microprogramming, Horizontal microprogramming.
- B. Hard wired control, Horizontal microprogramming, Vertical microprogramming.
- C. Horizontal microprogramming, Vertical microprogramming, Hard wired control.
- D. Vertical microprogramming, Horizontal microprogramming, Hard wired control.

gate1999 co-and-architecture microporogramming normal

[Answer key](#)

#### 1.21.5 Microprogramming: GATE CSE 2002 | Question: 2.7 [top](#)

Horizontal microprogramming:

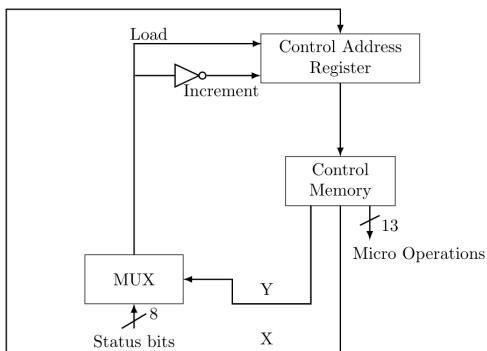
- A. does not require use of signal decoders
- B. results in larger sized microinstructions than vertical microprogramming
- C. uses one bit for each control signal
- D. all of the above

gatecse-2002 co-and-architecture microporogramming

[Answer key](#)

#### 1.21.6 Microprogramming: GATE CSE 2004 | Question: 67 [top](#)

The microinstructions stored in the control memory of a processor have a width of 26 bits. Each microinstruction is divided into three fields: a micro-operation field of 13 bits, a next address field ( $X$ ), and a MUX select field ( $Y$ ). There are 8 status bits in the input of the MUX.



How many bits are there in the  $X$  and  $Y$  fields, and what is the size of the control memory in number of words?

- A. 10,3,1024      B. 8,5,256      C. 5,8,2048      D. 10,3,512

gatecse-2004 co-and-architecture microporogramming normal

[Answer key](#)

#### 1.21.7 Microprogramming: GATE CSE 2013 | Question: 28 [top](#)

Consider the following sequence of micro-operations.

MBR  $\leftarrow$  PC

MAR  $\leftarrow$  X PC  $\leftarrow$  Y  
 Memory  $\leftarrow$  MBR

Which one of the following is a possible operation performed by this sequence?

- A. Instruction fetch
- B. Operand fetch
- C. Conditional branch
- D. Initiation of interrupt service

gatecse-2013 co-and-architecture microprogramming normal

[Answer key](#)

### 1.21.8 Microprogramming: GATE IT 2004 | Question: 49 [top](#)

A CPU has only three instructions  $I_1$ ,  $I_2$  and  $I_3$ , which use the following signals in time steps  $T_1 - T_5$ :

$I_1 : T_1 : \text{Ain, Bout, Cin}$

$T_2 : \text{PCout, Bin}$

$T_3 : \text{Zout, Ain}$

$T_4 : \text{Bin, Cout}$

$T_5 : \text{End}$

$I_2 : T_1 : \text{Cin, Bout, Din}$

$T_2 : \text{Aout, Bin}$

$T_3 : \text{Zout, Ain}$

$T_4 : \text{Bin, Cout}$

$T_5 : \text{End}$

$I_3 : T_1 : \text{Din, Aout}$

$T_2 : \text{Ain, Bout}$

$T_3 : \text{Zout, Ain}$

$T_4 : \text{Dout, Ain}$

$T_5 : \text{End}$

Which of the following logic functions will generate the hardwired control for the signal Ain ?

- A.  $T_1.I_1 + T_2.I_3 + T_4.I_3 + T_3$
- B.  $(T_1 + T_2 + T_3).I_3 + T_1.I_1$
- C.  $(T_1 + T_2).I_1 + (T_2 + T_4).I_3 + T_3$
- D.  $(T_1 + T_2).I_2 + (T_1 + T_3).I_1 + T_3$

gateit-2004 co-and-architecture microprogramming normal

[Answer key](#)

### 1.21.9 Microprogramming: GATE IT 2005 | Question: 45 [top](#)

A hardwired CPU uses 10 control signals  $S_1$  to  $S_{10}$ , in various time steps  $T_1$  to  $T_5$ , to implement 4 instructions  $I_1$  to  $I_4$  as shown below:

	<b>T<sub>1</sub></b>	<b>T<sub>2</sub></b>	<b>T<sub>3</sub></b>	<b>T<sub>4</sub></b>	<b>T<sub>5</sub></b>
<b>I<sub>1</sub></b>	$S_1, S_3, S_5$	$S_2, S_4, S_6$	$S_1, S_7$	$S_{10}$	$S_3, S_8$
<b>I<sub>2</sub></b>	$S_1, S_3, S_5$	$S_8, S_9, S_{10}$	$S_5, S_6, S_7$	$S_6$	$S_{10}$
<b>I<sub>3</sub></b>	$S_1, S_3, S_5$	$S_7, S_8, S_{10}$	$S_2, S_6, S_9$	$S_{10}$	$S_1, S_3$
<b>I<sub>4</sub></b>	$S_1, S_3, S_5$	$S_2, S_6, S_7$	$S_5, S_{10}$	$S_6, S_9$	$S_{10}$

Which of the following pairs of expressions represent the circuit for generating control signals  $S_5$  and  $S_{10}$  respectively?

$((I_j + I_k)T_n$  indicates that the control signal should be generated in time step  $T_n$  if the instruction being executed is  $I_j$  or  $I_k$ )

- A.  $S_5 = T_1 + I_2 \cdot T_3$  and  
 $S_{10} = (I_1 + I_3) \cdot T_4 + (I_2 + I_4) \cdot T_5$
- B.  $S_5 = T_1 + (I_2 + I_4) \cdot T_3$  and  
 $S_{10} = (I_1 + I_3) \cdot T_4 + (I_2 + I_4) \cdot T_5$
- C.  $S_5 = T_1 + (I_2 + I_4) \cdot T_3$  and  
 $S_{10} = (I_2 + I_3 + I_4) \cdot T_2 + (I_1 + I_3) \cdot T_4 + (I_2 + I_4) \cdot T_5$

D.  $S_5 = T_1 + (I_2 + I_4) \cdot T_3$  and

$$S_{10} = (I_2 + I_3) \cdot T_2 + I_4 \cdot T_3 + (I_1 + I_3) \cdot T_4 + (I_2 + I_4) \cdot T_5$$

gateit-2005 co-and-architecture microprogramming normal

**Answer key**

### 1.21.10 Microprogramming: GATE IT 2005 | Question: 49 top ↗

An instruction set of a processor has 125 signals which can be divided into 5 groups of mutually exclusive signals as follows:

Group 1 : 20 signals, Group 2 : 70 signals, Group 3 : 2 signals, Group 4 : 10 signals, Group 5 : 23 signals.

How many bits of the control words can be saved by using vertical microprogramming over horizontal microprogramming?

- A. 0      B. 103      C. 22      D. 55

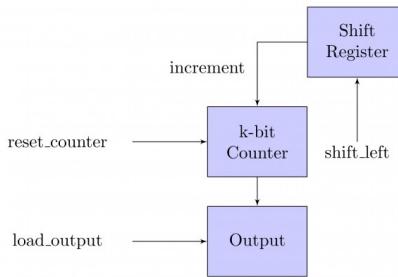
gateit-2005 co-and-architecture microprogramming normal

**Answer key**

### 1.21.11 Microprogramming: GATE IT 2006 | Question: 41 top ↗

The data path shown in the figure computes the number of 1s in the 32 – bit input word corresponding to an unsigned even integer stored in the shift register.

The unsigned counter, initially zero, is incremented if the most significant bit of the shift register is 1.



The microprogram for the control is shown in the table below with missing control words for microinstructions  $I_1, I_2, \dots, I_n$ .

Microinstruction	Reset_Counter	Shift_left	Load_output
BEGIN	1	0	0
I1	?	?	?
:	:	:	:
In	?	?	?
END	0	0	1

The counter width (k), the number of missing microinstructions (n), and the control word for microinstructions  $I_1, I_2, \dots, I_n$  are, respectively,

- A. 32,5,010      B. 5,32,010      C. 5,31,011      D. 5,31,010

gateit-2006 co-and-architecture microprogramming normal

**Answer key**

### 1.21.12 Microprogramming: GATE IT 2008 | Question: 39 top ↗

Consider a CPU where all the instructions require 7 clock cycles to complete execution. There are 140 instructions in the instruction set. It is found that 125 control signals are needed to be generated by the control unit. While designing the horizontal microprogrammed control unit, single address field format is used for branch control logic. What is the minimum size of the control word and control address register?

A. 125,7

B. 125,10

C. 135,9

D. 135,10

gateit-2008 co-and-architecture microprogramming normal

Answer key 

1.22

## Pipelining (37)

### 1.22.1 Pipelining: GATE CSE 1999 | Question: 13



An instruction pipeline consists of 4 stages – Fetch ( $F$ ), Decode field ( $D$ ), Execute ( $E$ ) and Result Write ( $W$ ). The 5 instructions in a certain instruction sequence need these stages for the different number of clock cycles as shown by the table below

Instruction	F	D	E	W
1	1	2	1	1
2	1	2	2	1
3	2	1	3	2
4	1	3	2	1
5	1	2	1	2

Find the number of clock cycles needed to perform the 5 instructions.

gate1999 co-and-architecture pipelining normal numerical-answers

Answer key 

### 1.22.2 Pipelining: GATE CSE 2000 | Question: 1.8



Comparing the time  $T_1$  taken for a single instruction on a pipelined CPU with time  $T_2$  taken on a non-pipelined but identical CPU, we can say that

A.  $T_1 \leq T_2$   
C.  $T_1 < T_2$

B.  $T_1 \geq T_2$   
D.  $T_1$  and  $T_2$  plus the time taken for one instruction fetch cycle

gatecse-2000 pipelining co-and-architecture easy

Answer key 

### 1.22.3 Pipelining: GATE CSE 2000 | Question: 12



An instruction pipeline has five stages where each stage take 2 nanoseconds and all instruction use all five stages. Branch instructions are not overlapped. i.e., the instruction after the branch is not fetched till the branch instruction is completed. Under ideal conditions,

- Calculate the average instruction execution time assuming that 20% of all instructions executed are branch instruction. Ignore the fact that some branch instructions may be conditional.
- If a branch instruction is a conditional branch instruction, the branch need not be taken. If the branch is not taken, the following instructions can be overlapped. When 80% of all branch instructions are conditional branch instructions, and 50% of the conditional branch instructions are such that the branch is taken, calculate the average instruction execution time.

gatecse-2000 co-and-architecture pipelining normal descriptive

Answer key 

### 1.22.4 Pipelining: GATE CSE 2001 | Question: 12



Consider a 5-stage pipeline - IF (Instruction Fetch), ID (Instruction Decode and register read), EX (Execute), MEM (memory), and WB (Write Back). All (memory or register) reads take place in the second phase of a clock cycle and all writes occur in the first phase. Consider the execution of the following instruction sequence:

I1:	sub $r2, r3, r4$	$/*\ r2 \leftarrow r3 - r4 */$
I2:	sub $r4, r2, r3$	$/*\ r4 \leftarrow r2 - r3 */$
I3:	sw $r2, 100(r1)$	$/*\ M[r1 + 100] \leftarrow r2 */$
I4:	sub $r3, r4, r2$	$/*\ r3 \leftarrow r4 - r2 */$

- A. Show all data dependencies between the four instructions.  
 B. Identify the data hazards.  
 C. Can all hazards be avoided by forwarding in this case.

gatecse-2001 co-and-architecture pipelining normal descriptive

[Answer key](#)

#### 1.22.5 Pipelining: GATE CSE 2002 | Question: 2.6, ISRO2008-19 [top](#)



The performance of a pipelined processor suffers if:

- A. the pipeline stages have different delays  
 B. consecutive instructions are dependent on each other  
 C. the pipeline stages share hardware resources  
 D. All of the above

gatecse-2002 co-and-architecture pipelining easy isro2008

[Answer key](#)

#### 1.22.6 Pipelining: GATE CSE 2003 | Question: 10, ISRO-DEC2017-41 [top](#)



For a pipelined CPU with a single ALU, consider the following situations

- I. The  $j + 1^{st}$  instruction uses the result of the  $j^{th}$  instruction as an operand  
 II. The execution of a conditional jump instruction  
 III. The  $j^{th}$  and  $j + 1^{st}$  instructions require the ALU at the same time.

Which of the above can cause a hazard

- A. I and II only      B. II and III only      C. III only      D. All the three

gatecse-2003 co-and-architecture pipelining normal isrodec2017

[Answer key](#)

#### 1.22.7 Pipelining: GATE CSE 2004 | Question: 69 [top](#)



A 4-stage pipeline has the stage delays as 150, 120, 160 and 140 nanoseconds, respectively. Registers that are used between the stages have a delay of 5 nanoseconds each. Assuming constant clocking rate, the total time taken to process 1000 data items on this pipeline will be:

- A. 120.4 microseconds      B. 160.5 microseconds  
 C. 165.5 microseconds      D. 590.0 microseconds

gatecse-2004 co-and-architecture pipelining normal

[Answer key](#)

#### 1.22.8 Pipelining: GATE CSE 2005 | Question: 68 [top](#)



A 5 stage pipelined CPU has the following sequence of stages:

- IF – instruction fetch from instruction memory
- RD – Instruction decode and register read
- EX – Execute: ALU operation for data and address computation
- MA – Data memory access – for write access, the register read at RD state is used.
- WB – Register write back

Consider the following sequence of instructions:

- $I_1: L R0, loc\ 1; R0 \leftarrow M[loc1]$
- $I_2: A R0, R0; R0 \leftarrow R0 + R0$
- $I_3: S R2, R0; R2 \leftarrow R2 - R0$

Let each stage take one clock cycle.

What is the number of clock cycles taken to complete the above sequence of instructions starting from the fetch of  $I_1$ ?

- A. 8      B. 10      C. 12      D. 15

gatecse-2005 co-and-architecture pipelining normal

Answer key 

#### 1.22.9 Pipelining: GATE CSE 2006 | Question: 42

A CPU has a five-stage pipeline and runs at 1 GHz frequency. Instruction fetch happens in the first stage of the pipeline. A conditional branch instruction computes the target address and evaluates the condition in the third stage of the pipeline. The processor stops fetching new instructions following a conditional branch until the branch outcome is known. A program executes  $10^9$  instructions out of which 20% are conditional branches. If each instruction takes one cycle to complete on average, the total execution time of the program is:

- A. 1.0 second      B. 1.2 seconds      C. 1.4 seconds      D. 1.6 seconds

gatecse-2006 co-and-architecture pipelining normal

Answer key 

#### 1.22.10 Pipelining: GATE CSE 2007 | Question: 37, ISRO2009-37

Consider a pipelined processor with the following four stages:

- IF: Instruction Fetch
- ID: Instruction Decode and Operand Fetch
- EX: Execute
- WB: Write Back

The IF, ID and WB stages take one clock cycle each to complete the operation. The number of clock cycles for the EX stage depends on the instruction. The ADD and SUB instructions need 1 clock cycle and the MUL instruction needs 3 clock cycles in the EX stage. Operand forwarding is used in the pipelined processor. What is the number of clock cycles taken to complete the following sequence of instructions?

<b>ADD</b>	R2, R1, R0	$R2 \leftarrow R1 + R0$
<b>MUL</b>	R4, R3, R2	$R4 \leftarrow R3 * R2$
<b>SUB</b>	R6, R5, R4	$R6 \leftarrow R5 - R4$

- A. 7      B. 8      C. 10      D. 14

gatecse-2007 co-and-architecture pipelining normal isro2009

Answer key 

#### 1.22.11 Pipelining: GATE CSE 2008 | Question: 36

Which of the following are NOT true in a pipelined processor?

- Bypassing can handle all RAW hazards
- Register renaming can eliminate all register carried WAR hazards
- Control hazard penalties can be eliminated by dynamic branch prediction

- A. I and II only      B. I and III only      C. II and III only      D. I, II and III

gatecse-2008 pipelining co-and-architecture normal

Answer key 

### 1.22.12 Pipelining: GATE CSE 2008 | Question: 76 top



Delayed branching can help in the handling of control hazards

For all delayed conditional branch instructions, irrespective of whether the condition evaluates to true or false,

- A. The instruction following the conditional branch instruction in memory is executed
- B. The first instruction in the fall through path is executed
- C. The first instruction in the taken path is executed
- D. The branch takes longer to execute than any other instruction

gatecse-2008 co-and-architecture pipelining normal

[Answer key](#)

### 1.22.13 Pipelining: GATE CSE 2008 | Question: 77 top



Delayed branching can help in the handling of control hazards

The following code is to run on a pipelined processor with one branch delay slot:

- I1: ADD  $R2 \leftarrow R7 + R8$
- I2: Sub  $R4 \leftarrow R5 - R6$
- I3: ADD  $R1 \leftarrow R2 + R3$
- I4: STORE Memory  $[R4] \leftarrow R1$

BRANCH to Label if  $R1 == 0$

Which of the instructions I1, I2, I3 or I4 can legitimately occupy the delay slot without any program modification?

- A. I1
- B. I2
- C. I3
- D. I4

gatecse-2008 co-and-architecture pipelining normal

[Answer key](#)

### 1.22.14 Pipelining: GATE CSE 2009 | Question: 28 top



Consider a 4 stage pipeline processor. The number of cycles needed by the four instructions  $I1, I2, I3, I4$  in stages  $S1, S2, S3, S4$  is shown below:

	<b>S1</b>	<b>S2</b>	<b>S3</b>	<b>S4</b>
<b>I1</b>	2	1	1	1
<b>I2</b>	1	3	2	2
<b>I3</b>	2	1	1	3
<b>I4</b>	1	2	2	2

What is the number of cycles needed to execute the following loop?

For (i=1 to 2) {I1; I2; I3; I4;}

- A. 16
- B. 23
- C. 28
- D. 30

gatecse-2009 co-and-architecture pipelining normal

[Answer key](#)

### 1.22.15 Pipelining: GATE CSE 2010 | Question: 33 top



A 5-stage pipelined processor has Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Perform Operation (PO) and Write Operand (WO) stages. The IF, ID, OF and WO stages take 1 clock cycle each for any instruction. The PO stage takes 1 clock cycle for ADD and SUB instructions, 3 clock cycles for MUL instruction and 6 clock cycles for DIV instruction respectively. Operand forwarding is used in the pipeline. What is the number of clock cycles needed to execute the following sequence of instructions?

Instruction	Meaning of instruction
$t_0: MUL R_2, R_0, R_1$	$R_2 \leftarrow R_0 * R_1$
$t_1: DIV R_5, R_3, R_4$	$R_5 \leftarrow R_3 / R_4$
$t_2: ADD R_2, R_5, R_2$	$R_2 \leftarrow R_5 + R_2$
$t_3 : SUB R_5, R_2, R_6$	$R_5 \leftarrow R_2 - R_6$

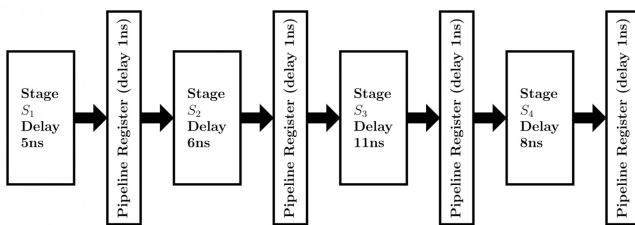
- A. 13      B. 15      C. 17      D. 19

gatecse-2010 co-and-architecture pipelining normal

Answer key 

#### 1.22.16 Pipelining: GATE CSE 2011 | Question: 41 top

Consider an instruction pipeline with four stages ( $S_1, S_2, S_3$  and  $S_4$ ) each with combinational circuit only. The pipeline registers are required between each stage and at the end of the last stage. Delays for the stages and for the pipeline registers are as given in the figure.



What is the approximate speed up of the pipeline in steady state under ideal conditions when compared to the corresponding non-pipeline implementation?

- A. 4.0      B. 2.5      C. 1.1      D. 3.0

gatecse-2011 co-and-architecture pipelining normal

Answer key 

#### 1.22.17 Pipelining: GATE CSE 2012 | Question: 20, ISRO2016-23 top

Register renaming is done in pipelined processors:

- A. as an alternative to register allocation at compile time
- B. for efficient access to function parameters and local variables
- C. to handle certain kinds of hazards
- D. as part of address translation

gatecse-2012 co-and-architecture pipelining easy isro2016

Answer key 

#### 1.22.18 Pipelining: GATE CSE 2013 | Question: 45 top

Consider an instruction pipeline with five stages without any branch prediction:

Fetch Instruction (FI), Decode Instruction (DI), Fetch Operand (FO), Execute Instruction (EI) and Write Operand (WO). The stage delays for FI, DI, FO, EI and WO are 5 ns, 7 ns, 10 ns, 8 ns and 6 ns, respectively. There are intermediate storage buffers after each stage and the delay of each buffer is 1 ns. A program consisting of 12 instructions  $I_1, I_2, I_3, \dots, I_{12}$  is executed in this pipelined processor. Instruction  $I_4$  is the only branch instruction and its branch target is  $I_9$ . If the branch is taken during the execution of this program, the time (in ns) needed to complete the program is

- A. 132      B. 165  
C. 176      D. 328

gatecse-2013 normal co-and-architecture pipelining

Answer key 

### 1.22.19 Pipelining: GATE CSE 2014 Set 1 | Question: 43 top



Consider a 6-stage instruction pipeline, where all stages are perfectly balanced. Assume that there is no cycle-time overhead of pipelining. When an application is executing on this 6-stage pipeline, the speedup achieved with respect to non-pipelined execution if 25% of the instructions incur 2 pipeline stall cycles is \_\_\_\_\_.

gatecse-2014-set1 co-and-architecture pipelining numerical-answers normal

Answer key

### 1.22.20 Pipelining: GATE CSE 2014 Set 3 | Question: 43 top



An instruction pipeline has five stages, namely, instruction fetch (IF), instruction decode and register fetch (ID/RF), instruction execution (EX), memory access (MEM), and register writeback (WB) with stage latencies 1 ns, 2.2 ns, 2 ns, 1 ns, and 0.75 ns, respectively (ns stands for nanoseconds). To gain in terms of frequency, the designers have decided to split the ID/RF stage into three stages (ID, RF1, RF2) each of latency  $2.2/3$  ns. Also, the EX stage is split into two stages (EX1, EX2) each of latency 1 ns. The new design has a total of eight pipeline stages. A program has 20% branch instructions which execute in the EX stage and produce the next instruction pointer at the end of the EX stage in the old design and at the end of the EX2 stage in the new design. The IF stage stalls after fetching a branch instruction until the next instruction pointer is computed. All instructions other than the branch instruction have an average CPI of one in both the designs. The execution times of this program on the old and the new design are  $P$  and  $Q$  nanoseconds, respectively. The value of  $P/Q$  is \_\_\_\_\_.

gatecse-2014-set3 co-and-architecture pipelining numerical-answers normal

Answer key

### 1.22.21 Pipelining: GATE CSE 2014 Set 3 | Question: 9 top



Consider the following processors (ns stands for nanoseconds). Assume that the pipeline registers have zero latency.

- P1: Four-stage pipeline with stage latencies 1 ns, 2 ns, 2 ns, 1 ns.
- P2: Four-stage pipeline with stage latencies 1 ns, 1.5 ns, 1.5 ns, 1.5 ns.
- P3: Five-stage pipeline with stage latencies 0.5 ns, 1 ns, 1 ns, 0.6 ns, 1 ns.
- P4: Five-stage pipeline with stage latencies 0.5 ns, 0.5 ns, 1 ns, 1 ns, 1.1 ns.

Which processor has the highest peak clock frequency?

- A. P1      B. P2      C. P3      D. P4

gatecse-2014-set3 co-and-architecture pipelining normal

Answer key

### 1.22.22 Pipelining: GATE CSE 2015 Set 1 | Question: 38 top



Consider a non-pipelined processor with a clock rate of 2.5 gigahertz and average cycles per instruction of four. The same processor is upgraded to a pipelined processor with five stages; but due to the internal pipeline delay, the clock speed is reduced to 2 gigahertz. Assume that there are no stalls in the pipeline. The speedup achieved in this pipelined processor is \_\_\_\_\_.

gatecse-2015-set1 co-and-architecture pipelining normal numerical-answers

Answer key

### 1.22.23 Pipelining: GATE CSE 2015 Set 2 | Question: 44 top



Consider the sequence of machine instruction given below:

MUL	R5, R0, R1
DIV	R6, R2, R3
ADD	R7, R5, R6
SUB	R8, R7, R4

In the above sequence,  $R0$  to  $R8$  are general purpose registers. In the instructions shown, the first register shows the result of the operation performed on the second and the third registers. This sequence of instructions is to be executed in a pipelined instruction processor with the following 4 stages: (1) Instruction Fetch and Decode (*IF*), (2) Operand Fetch (*OF*), (3) Perform Operation (*PO*) and (4) Write back the result (*WB*). The *IF*, *OF* and *WB* stages take 1 clock cycle each for any instruction. The *PO* stage takes 1 clock cycle for ADD and SUB instruction, 3 clock cycles for MUL instruction and 5 clock cycles for DIV instruction. The pipelined processor uses operand forwarding from the *PO* stage to the *OF* stage. The number of clock cycles taken for the execution of the above sequence of instruction is \_\_\_\_\_.

gatecse-2015-set2 co-and-architecture pipelining normal numerical-answers

[Answer key](#)

#### 1.22.24 Pipelining: GATE CSE 2015 Set 3 | Question: 51 [top](#)

Consider the following reservation table for a pipeline having three stages  $S_1$ ,  $S_2$  and  $S_3$ .

Time →	1	2	3	4	5
$S_1$	$X$			$X$	
$S_2$		$X$		$X$	
$S_3$			$X$		

The minimum average latency (MAL) is \_\_\_\_\_

gatecse-2015-set3 co-and-architecture pipelining difficult numerical-answers

[Answer key](#)

#### 1.22.25 Pipelining: GATE CSE 2016 Set 1 | Question: 32 [top](#)

The stage delays in a 4-stage pipeline are 800, 500, 400 and 300 picoseconds. The first stage (with delay 800 picoseconds) is replaced with a functionality equivalent design involving two stages with respective delays 600 and 350 picoseconds. The throughput increase of the pipeline is \_\_\_\_\_ percent.

gatecse-2016-set1 co-and-architecture pipelining normal numerical-answers

[Answer key](#)

#### 1.22.26 Pipelining: GATE CSE 2016 Set 2 | Question: 33 [top](#)

Consider a 3 GHz (gigahertz) processor with a three stage pipeline and stage latencies  $\tau_1$ ,  $\tau_2$  and  $\tau_3$  such that  $\tau_1 = \frac{3\tau_2}{4} = 2\tau_3$ . If the longest pipeline stage is split into two pipeline stages of equal latency , the new frequency is \_\_\_\_\_ GHz, ignoring delays in the pipeline registers.

gatecse-2016-set2 co-and-architecture pipelining normal numerical-answers

[Answer key](#)

#### 1.22.27 Pipelining: GATE CSE 2017 Set 1 | Question: 50 [top](#)

Instruction execution in a processor is divided into 5 stages, *Instruction Fetch* (*IF*), *Instruction Decode* (*ID*), *Operand fetch* (*OF*), *Execute* (*EX*), and *Write Back* (*WB*). These stages take 5, 4, 20, 10 and 3 nanoseconds (**ns**) respectively. A pipelined implementation of the processor requires buffering between each pair of consecutive stages with a delay of 2 ns. Two pipelined implementation of the processor are contemplated:

- i. a naive pipeline implementation (NP) with 5 stages and
- ii. an efficient pipeline (EP) where the *OF* stage is divided into stages *OF1* and *OF2* with execution times of 12 ns and 8 ns respectively.

The speedup (correct to two decimal places) achieved by EP over NP in executing 20 independent instructions with no hazards is \_\_\_\_\_ .

**Answer key****1.22.28 Pipelining: GATE CSE 2018 | Question: 50**

The instruction pipeline of a RISC processor has the following stages: Instruction Fetch (*IF*), Instruction Decode (*ID*), Operand Fetch (*OF*), Perform Operation (*PO*) and Writeback (*WB*). The *IF*, *ID*, *OF* and *WB* stages take 1 clock cycle each for every instruction. Consider a sequence of 100 instructions. In the *PO* stage, 40 instructions take 3 clock cycles each, 35 instructions take 2 clock cycles each, and the remaining 25 instructions take 1 clock cycle each. Assume that there are no data hazards and no control hazards.

The number of clock cycles required for completion of execution of the sequence of instruction is \_\_\_\_\_.

**Answer key****1.22.29 Pipelining: GATE CSE 2020 | Question: 43**

Consider a non-pipelined processor operating at 2.5 GHz. It takes 5 clock cycles to complete an instruction. You are going to make a 5-stage pipeline out of this processor. Overheads associated with pipelining force you to operate the pipelined processor at 2 GHz. In a given program, assume that 30% are memory instructions, 60% are ALU instructions and the rest are branch instructions. 5% of the memory instructions cause stalls of 50 clock cycles each due to cache misses and 50% of the branch instructions cause stalls of 2 cycles each. Assume that there are no stalls associated with the execution of ALU instructions. For this program, the speedup achieved by the pipelined processor over the non-pipelined processor (round off to 2 decimal places) is\_\_\_\_\_.

**Answer key****1.22.30 Pipelining: GATE CSE 2021 Set 1 | Question: 53**

A five-stage pipeline has stage delays of 150, 120, 150, 160 and 140 nanoseconds. The registers that are used between the pipeline stages have a delay of 5 nanoseconds each.

The total time to execute 100 independent instructions on this pipeline, assuming there are no pipeline stalls, is \_\_\_\_\_ nanoseconds.

**Answer key****1.22.31 Pipelining: GATE CSE 2023 | Question: 23**

Consider a 3-stage pipelined processor having a delay of 10 ns (nanoseconds), 20 ns, and 14 ns, for the first, second, and the third stages, respectively. Assume that there is no other delay and the processor does not suffer from any pipeline hazards. Also assume that one instruction is fetched every cycle.

The total execution time for executing 100 instructions on this processor is \_\_\_\_\_ ns.

**Answer key****1.22.32 Pipelining: GATE IT 2004 | Question: 47**

Consider a pipeline processor with 4 stages *S*<sub>1</sub> to *S*<sub>4</sub>. We want to execute the following loop:

```
for (i = 1; i <= 1000; i++)
{I1, I2, I3, I4}
```

where the time taken (in ns) by instructions *I*<sub>1</sub> to *I*<sub>4</sub> for stages *S*<sub>1</sub> to *S*<sub>4</sub> are given below:

	$S_1$	$S_2$	$S_3$	$S_4$
<b>I1</b>	1	2	1	2
<b>I2</b>	2	1	2	1
<b>I3</b>	1	1	2	1
<b>I4</b>	2	1	2	1

The output of  $I_1$  for  $i = 2$  will be available after

- A. 11 ns      B. 12 ns      C. 13 ns      D. 28 ns

gateit-2004 co-and-architecture pipelining normal

[Answer key](#) 

#### 1.22.33 Pipelining: GATE IT 2005 | Question: 44

We have two designs  $D_1$  and  $D_2$  for a synchronous pipeline processor.  $D_1$  has 5 pipeline stages with execution times of 3 nsec, 2 nsec, 4 nsec, 2 nsec and 3 nsec while the design  $D_2$  has 8 pipeline stages each with 2 nsec execution time. How much time can be saved using design  $D_2$  over design  $D_1$  for executing 100 instructions?

- A. 214 nsec      B. 202 nsec  
C. 86 nsec      D. -200 nsec

gateit-2005 co-and-architecture pipelining normal

[Answer key](#) 

#### 1.22.34 Pipelining: GATE IT 2006 | Question: 78

A pipelined processor uses a 4-stage instruction pipeline with the following stages: Instruction fetch (IF), Instruction decode (ID), Execute (EX) and Writeback (WB). The arithmetic operations as well as the load and store operations are carried out in the EX stage. The sequence of instructions corresponding to the statement  $X = (S - R * (P + Q)) / T$  is given below. The values of variables  $P, Q, R, S$  and  $T$  are available in the registers  $R_0, R_1, R_2, R_3$  and  $R_4$  respectively, before the execution of the instruction sequence.

ADD	$R_5, R_0, R_1$	$; R_5 \leftarrow R_0 + R_1$
MUL	$R_6, R_2, R_5$	$; R_6 \leftarrow R_2 * R_5$
SUB	$R_5, R_3, R_6$	$; R_5 \leftarrow R_3 - R_6$
DIV	$R_6, R_5, R_4$	$; R_6 \leftarrow R_5 / R_4$
STORE	$R_6, X$	$; X \leftarrow R_6$

The number of Read-After-Write (RAW) dependencies, Write-After-Read (WAR) dependencies, and Write-After-Write (WAW) dependencies in the sequence of instructions are, respectively,

- A. 2,2,4      B. 3,2,3      C. 4,2,2      D. 3,3,2

gateit-2006 co-and-architecture pipelining normal

[Answer key](#) 

#### 1.22.35 Pipelining: GATE IT 2006 | Question: 79

A pipelined processor uses a 4-stage instruction pipeline with the following stages: Instruction fetch (IF), Instruction decode (ID), Execute (EX) and Writeback (WB). The arithmetic operations as well as the load and store operations are carried out in the EX stage. The sequence of instructions corresponding to the statement  $X = (S - R * (P + Q)) / T$  is given below. The values of variables  $P, Q, R, S$  and  $T$  are available in the registers  $R_0, R_1, R_2, R_3$  and  $R_4$  respectively, before the execution of the instruction sequence.

ADD	$R5, R0, R1$	$; R5 \leftarrow R0 + R1$
MUL	$R6, R2, R5$	$; R6 \leftarrow R2 * R5$
SUB	$R5, R3, R6$	$; R5 \leftarrow R3 - R6$
DIV	$R6, R5, R4$	$; R6 \leftarrow R5/R4$
STORE	$R6, X$	$; X \leftarrow R6$

The IF, ID and WB stages take 1 clock cycle each. The EX stage takes 1 clock cycle each for the ADD, SUB and STORE operations, and 3 clock cycles each for MUL and DIV operations. Operand forwarding from the EX stage to the ID stage is used. The number of clock cycles required to complete the sequence of instructions is

- A. 10      B. 12      C. 14      D. 16

gateit-2006 co-and-architecture pipelining normal

[Answer key](#) 

#### 1.22.36 Pipelining: GATE IT 2007 | Question: 6, ISRO2011-25

A processor takes 12 cycles to complete an instruction I. The corresponding pipelined processor uses 6 stages with the execution times of 3, 2, 5, 4, 6 and 2 cycles respectively. What is the asymptotic speedup assuming that a very large number of instructions are to be executed?

- A. 1.83      B. 2      C. 3      D. 6

gateit-2007 co-and-architecture pipelining normal isro2011

[Answer key](#) 

#### 1.22.37 Pipelining: GATE IT 2008 | Question: 40

A non pipelined single cycle processor operating at 100 MHz is converted into a synchronous pipelined processor with five stages requiring 2.5 nsec, 1.5 nsec, 2 nsec, 1.5 nsec and 2.5 nsec, respectively. The delay of the latches is 0.5 nsec. The speedup of the pipeline processor for a large number of instructions is:

- A. 4.5      B. 4.0      C. 3.33      D. 3.0

gateit-2008 co-and-architecture pipelining normal

[Answer key](#) 

### 1.23

#### Runtime Environment (2)

#### 1.23.1 Runtime Environment: GATE CSE 2001 | Question: 1.10, UGCNET-Dec2012-III: 36

Suppose a processor does not have any stack pointer registers, which of the following statements is true?

- A. It cannot have subroutine call instruction
- B. It cannot have nested subroutines call
- C. Interrupts are not possible
- D. All subroutine calls and interrupts are possible

gatecse-2001 co-and-architecture normal ugcnetcse-dec2012-paper3 runtime-environment

[Answer key](#) 

#### 1.23.2 Runtime Environment: GATE CSE 2008 | Question: 37, ISRO2009-38

The use of multiple register windows with overlap causes a reduction in the number of memory accesses for:

- I. Function locals and parameters
  - II. Register saves and restores
  - III. Instruction fetches
- A. I only      B. II only      C. III only      D. I, II and III

gatecse-2008 co-and-architecture normal isro2009 runtime-environment

Answer key

1.24

Speedup (2) top

1.24.1 Speedup: GATE CSE 2014 Set 1 | Question: 55 top



Consider two processors  $P_1$  and  $P_2$  executing the same instruction set. Assume that under identical conditions, for the same input, a program running on  $P_2$  takes 25% less time but incurs 20% more CPI (clock cycles per instruction) as compared to the program running on  $P_1$ . If the clock frequency of  $P_1$  is 1GHz, then the clock frequency of  $P_2$  (in GHz) is \_\_\_\_\_.

gatecse-2014-set1 co-and-architecture numerical-answers normal speedup

Answer key

1.24.2 Speedup: GATE IT 2004 | Question: 50 top



In an enhancement of a design of a CPU, the speed of a floating point unit has been increased by 20% and the speed of a fixed point unit has been increased by 10%. What is the overall speedup achieved if the ratio of the number of floating point operations to the number of fixed point operations is 2 : 3 and the floating point operation used to take twice the time taken by the fixed point operation in the original design?

- A. 1.155      B. 1.185      C. 1.255      D. 1.285

gateit-2004 normal co-and-architecture speedup

Answer key

1.25

Stall (1) top

1.25.1 Stall: GATE CSE 2022 | Question: 51 top



A processor  $X_1$  operating at 2 GHz has a standard 5-stage RISC instruction pipeline having a base CPI (cycles per instruction) of one without any pipeline hazards. For a given program  $P$  that has 30% branch instructions, control hazards incur 2 cycles stall for every branch. A new version of the processor  $X_2$  operating at same clock frequency has an additional branch predictor unit (BPU) that completely eliminates stalls for correctly predicted branches. There is neither any savings nor any additional stalls for wrong predictions. There are no structural hazards and data hazards for  $X_1$  and  $X_2$ . If the BPU has a prediction accuracy of 80%, the speed up (*rounded off to two decimal places*) obtained by  $X_2$  over  $X_1$  in executing  $P$  is \_\_\_\_\_.

gatecse-2022 numerical-answers co-and-architecture pipelining stall 2-marks

Answer key

1.26

Virtual Memory (3) top

1.26.1 Virtual Memory: GATE CSE 1991 | Question: 03,iii top



The total size of address space in a virtual memory system is limited by:

- A. the length of MAR  
C. the available main memory  
E. none of the above
- B. the available secondary storage  
D. all of the above

gate1991 co-and-architecture virtual-memory normal multiple-selects

Answer key

1.26.2 Virtual Memory: GATE CSE 2004 | Question: 47 top



Consider a system with a two-level paging scheme in which a regular memory access takes 150 nanoseconds, and servicing a page fault takes 8 milliseconds. An average instruction takes 100 nanoseconds of CPU time, and two memory accesses. The TLB hit ratio is 90%, and the page fault rate is one in every 10,000 instructions. What is the effective average instruction execution time?

- A. 645 nanoseconds  
C. 1215 nanoseconds
- B. 1050 nanoseconds  
D. 1230 nanoseconds

gatecse-2004 co-and-architecture virtual-memory normal

[Answer key](#)

### 1.26.3 Virtual Memory: GATE CSE 2008 | Question: 38 top



In an instruction execution pipeline, the earliest that the data TLB (Translation Lookaside Buffer) can be accessed is:

- A. before effective address calculation has started
- B. during effective address calculation
- C. after effective address calculation has completed
- D. after data cache lookup has completed

gatecse-2008 co-and-architecture virtual-memory normal

[Answer key](#)

## Answer Keys

1.1.1	C	1.1.2	N/A	1.1.3	N/A	1.1.4	N/A	1.1.5	B
1.1.6	D	1.1.7	A;B;C;D	1.1.8	C	1.1.9	A	1.1.10	B
1.1.11	C	1.1.12	B	1.1.13	C	1.1.14	C	1.1.16	D
1.1.17	D	1.2.1	B	1.3.1	N/A	1.3.2	N/A	1.3.3	22
1.3.4	180	1.3.6	D	1.3.7	D	1.3.8	61.25	1.3.9	N/A
1.3.10	B	1.3.11	B	1.3.12	N/A	1.3.13	N/A	1.3.14	C
1.3.15	A	1.3.16	A	1.3.17	D	1.3.18	C	1.3.20	D
1.3.22	A	1.3.23	A	1.3.24	D	1.3.25	B	1.3.26	C
1.3.27	D	1.3.28	C	1.3.29	C	1.3.30	D	1.3.31	C
1.3.32	A	1.3.33	A	1.3.34	A	1.3.35	D	1.3.36	D
1.3.37	20	1.3.39	14	1.3.40	A	1.3.42	30	1.3.43	0.05
1.3.44	14	1.3.45	A	1.3.46	4.7 : 4.8	1.3.47	18	1.3.48	B
1.3.49	D	1.3.51	13.3:13.3;13.5:13.5	1.3.52	B	1.3.53	17 : 17	1.3.54	2 : 2
1.3.55	A	1.3.56	A;B;D	1.3.57	0.85	1.3.58	19	1.3.59	C
1.3.60	B	1.3.61	C	1.3.62	C	1.3.63	A	1.3.64	B
1.3.65	D	1.3.66	A	1.4.1	A;B;C;D	1.4.2	D	1.5.1	N/A
1.5.2	B	1.6.1	76	1.7.1	B	1.8.1	B	1.8.2	B
1.9.1	N/A	1.9.2	D	1.9.3	B	1.9.4	B	1.9.5	28
1.9.6	C	1.10.1	A;B;D	1.11.1	D	1.11.2	B	1.11.3	A
1.11.4	456	1.11.5	80000 : 80000	1.11.6	A	1.11.7	C	1.13.1	C
1.14.1	False	1.14.2	N/A	1.14.3	C	1.14.4	C	1.14.5	A
1.14.6	-16.0	1.14.7	1.87 : 1.88	1.15.1	N/A	1.15.2	256	1.15.3	True
1.15.4	16383	1.15.5	500	1.15.7	14	1.16.1	D	1.16.2	B
1.16.3	A	1.16.4	A	1.16.5	B	1.16.6	C	1.16.7	C
1.16.8	10.2	1.17.1	True	1.17.2	True	1.17.3	False	1.17.4	A
1.17.5	1.4 : 1.5	1.17.6	B	1.17.7	B	1.18.1	N/A	1.18.2	N/A
1.18.3	N/A	1.18.4	B	1.18.5	A	1.18.6	D	1.18.7	B

1.18.8	C	1.18.9	B	1.18.10	D	1.18.11	A	1.18.12	C
1.18.13	D	1.18.14	D	1.18.15	16	1.18.16	50 : 50	1.18.17	D
1.18.18	C	1.18.19	A	1.19.1	31	1.19.2	59 : 60	1.19.3	C
1.20.1	Q-Q	1.21.1	N/A	1.21.2	C	1.21.3	C	1.21.4	B
1.21.5	D	1.21.6	A	1.21.7	D	1.21.8	A	1.21.9	D
1.21.10	B	1.21.11	D	1.21.12	D	1.22.1	15	1.22.4	N/A
1.22.5	D	1.22.6	D	1.22.7	C	1.22.8	A	1.22.9	C
1.22.10	B	1.22.11	B	1.22.12	A	1.22.13	D	1.22.14	B
1.22.15	B	1.22.16	B	1.22.17	C	1.22.18	B	1.22.19	4
1.22.20	1.50 : 1.60	1.22.21	C	1.22.23	13	1.22.24	3	1.22.26	4
1.22.27	1.50 : 1.51	1.22.28	219	1.22.29	2.15:2.18	1.22.30	17160 : 17160	1.22.31	2040
1.22.32	C	1.22.33	B	1.22.34	C	1.22.35	B	1.22.36	B
1.22.37	C	1.23.1	X	1.23.2	A	1.24.2	A	1.25.1	1.42:1.45
1.26.1	A;B	1.26.2	D	1.26.3	C				



### 2.0.1 GATE CSE 2022 | Question: 25 top ↗



Consider the resolution of the domain name `www.gate.org.in` by a DNS resolver. Assume that no resource records are cached anywhere across the DNS servers and that iterative query mechanism is used in the resolution. The number of DNS query-response pairs involved in completely resolving the domain name is \_\_\_\_\_.

gatecse-2022 numerical-answers computer-networks 1-mark

**Answer key ↗**

### 2.0.2 GATE CSE 2022 | Question: 49 top ↗



Consider a 100 Mbps link between an earth station (sender) and a satellite (receiver) at an altitude of 2100 km. The signal propagates at a speed of  $3 \times 10^8$  m/s. The time taken (in milliseconds, rounded off to two decimal places) for the receiver to completely receive a packet of 1000 bytes transmitted by the sender is \_\_\_\_\_.

gatecse-2022 numerical-answers computer-networks 2-marks

**Answer key ↗**

## 2.1

### Application Layer Protocols (10) top ↗



#### 2.1.1 Application Layer Protocols: GATE CSE 2008 | Question: 14, ISRO2016-74 top ↗

What is the maximum size of data that the application layer can pass on to the TCP layer below?

- A. Any size
- B.  $2^{16}$  bytes - size of TCP header
- C.  $2^{16}$  bytes
- D. 1500 bytes

gatecse-2008 easy computer-networks application-layer-protocols isro2016

**Answer key ↗**

#### 2.1.2 Application Layer Protocols: GATE CSE 2011 | Question: 4 top ↗



Consider the different activities related to email.

- m1 : Send an email from mail client to mail server
- m2 : Download an email from mailbox server to a mail client
- m3 : Checking email in a web browser

Which is the application level protocol used in each activity?

- A. m1 : HTTP m2 : SMTP m3 : POP
- B. m1 : SMTP m2 : FTP m3 : HTTP
- C. m1 : SMTP m2 : POP m3 : HTTP
- D. m1 : POP m2 : SMTP m3 : IMAP

gatecse-2011 computer-networks application-layer-protocols easy

**Answer key ↗**

#### 2.1.3 Application Layer Protocols: GATE CSE 2012 | Question: 10 top ↗



The protocol data unit (PDU) for the application layer in the Internet stack is:

- A. Segment
- B. Datagram
- C. Message
- D. Frame

gatecse-2012 computer-networks application-layer-protocols easy

**Answer key ↗**

#### 2.1.4 Application Layer Protocols: GATE CSE 2016 Set 1 | Question: 25 top



Which of the following is/are example(s) of stateful application layer protocol?

- i. HTTP
  - ii. FTP
  - iii. TCP
  - iv. POP3
- A. (i) and (ii) only    B. (ii) and (iii) only    C. (ii) and (iv) only    D. (iv) only

gatecse-2016-set1 computer-networks application-layer-protocols normal

[Answer key](#)

#### 2.1.5 Application Layer Protocols: GATE CSE 2019 | Question: 16 top



Which of the following protocol pairs can be used to send and retrieve e-mails (in that order)?

- A. IMAP, POP3    B. SMTP, POP3    C. SMTP, MIME    D. IMAP, SMTP

gatecse-2019 computer-networks application-layer-protocols 1-mark

[Answer key](#)

#### 2.1.6 Application Layer Protocols: GATE CSE 2020 | Question: 25 top



Assume that you have made a request for a web page through your web browser to a web server. Initially the browser cache is empty. Further, the browser is configured to send HTTP requests in non-persistent mode. The web page contains text and five very small images. The minimum number of TCP connections required to display the web page completely in your browser is \_\_\_\_\_.

gatecse-2020 numerical-answers computer-networks application-layer-protocols 1-mark

[Answer key](#)

#### 2.1.7 Application Layer Protocols: GATE IT 2005 | Question: 25 top



Consider the three commands : PROMPT, HEAD and RCPT.

Which of the following options indicate a correct association of these commands with protocols where these are used?

- |                    |                    |
|--------------------|--------------------|
| A. HTTP, SMTP, FTP | B. FTP, HTTP, SMTP |
| C. HTTP, FTP, SMTP | D. SMTP, HTTP, FTP |

gateit-2005 computer-networks application-layer-protocols normal

[Answer key](#)

#### 2.1.8 Application Layer Protocols: GATE IT 2005 | Question: 77 top



Assume that "host1.mydomain.dom" has an IP address of 145.128.16.8. Which of the following options would be most appropriate as a subsequence of steps in performing the reverse lookup of 145.128.16.8 ? In the following options "NS" is an abbreviation of "nameserver".

- A. Query a NS for the root domain and then NS for the "dom" domains
- B. Directly query a NS for "dom" and then a NS for "mydomain.dom" domains
- C. Query a NS for in-addr.arpa and then a NS for 128.145.in-addr.arpa domains
- D. Directly query a NS for 145.in-addr.arpa and then a NS for 128.145.in-addr.arpa domains

gateit-2005 computer-networks normal application-layer-protocols

[Answer key](#)

#### 2.1.9 Application Layer Protocols: GATE IT 2006 | Question: 18 top



HELO and PORT, respectively, are commands from the protocols:

- |                    |                    |
|--------------------|--------------------|
| A. FTP and HTTP    | B. TELNET and POP3 |
| C. HTTP and TELNET | D. SMTP and FTP    |

**Answer key****2.1.10 Application Layer Protocols: GATE IT 2008 | Question: 20**

Provide the best matching between the entries in the two columns given in the table below:

I.	Proxy Server	a.	Firewall
II.	Kazaa, DC++	b.	Caching
III.	Slip	c.	P2P
IV.	DNS	d.	PPP

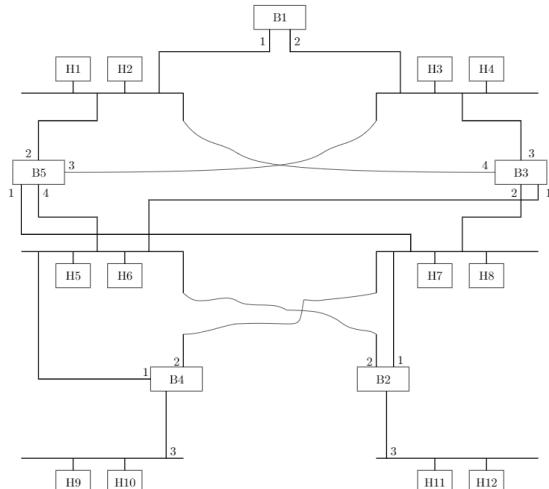
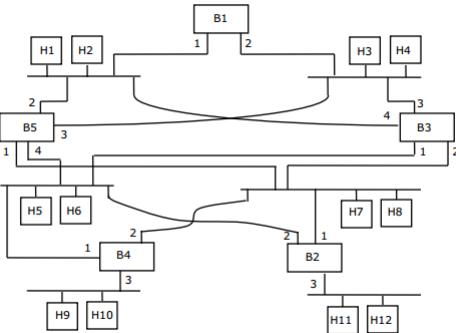
- A. I-a, II-d, III-c, IV-b  
 C. I-a, II-c, III-d, IV-b

- B. I-b, II-d, III-c, IV-a  
 D. I-b, II-c, III-d, IV-a

**Answer key****2.2****Bridges (2)****2.2.1 Bridges: GATE CSE 2006 | Question: 82**

Consider the diagram shown below where a number of LANs are connected by (transparent) bridges. In order to avoid packets looping through circuits in the graph, the bridges organize themselves in a spanning tree. First, the root bridge is identified as the bridge with the least serial number. Next, the root sends out (one or more) data units to enable the setting up of the spanning tree of shortest paths from the root bridge to each bridge.

Each bridge identifies a port (the root port) through which it will forward frames to the root bridge. Port conflicts are always resolved in favour of the port with the lower index value. When there is a possibility of multiple bridges forwarding to the same LAN (but not through the root port), ties are broken as follows: bridges closest to the root get preference and between such bridges, the one with the lowest serial number is preferred.



For the given connection of LANs by bridges, which one of the following choices represents the depth first traversal of the spanning tree of bridges?

- A. B1, B5, B3, B4, B2  
 C. B1, B5, B2, B3, B4

- B. B1, B3, B5, B2, B4  
 D. B1, B3, B4, B5, B2

gatecse-2006 computer-networks bridges normal

[Answer key](#)

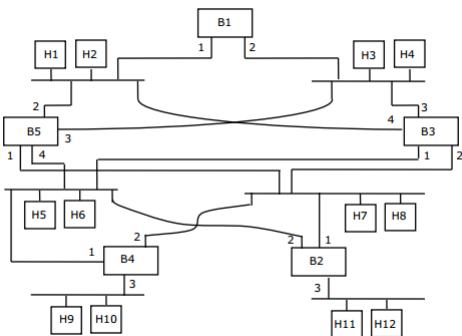


### 2.2.2 Bridges: GATE CSE 2006 | Question: 83 top ↗

Consider the diagram shown below where a number of LANs are connected by (transparent) bridges. In order to avoid packets looping through circuits in the graph, the bridges organize themselves in a spanning tree. First, the root bridge is identified as the bridge with the least serial number. Next, the root sends out (one or more) data

units to enable the setting up of the spanning tree of shortest paths from the root bridge to each bridge.

Each bridge identifies a port (the root port) through which it will forward frames to the root bridge. Port conflicts are always resolved in favour of the port with the lower index value. When there is a possibility of multiple bridges forwarding to the same LAN (but not through the root port), ties are broken as follows: bridges closest to the root get preference and between such bridges, the one with the lowest serial number is preferred.



Consider the spanning tree  $B1, B5, B3, B4, B2$  for the given connection of LANs by bridges, that represents the depth first traversal of the spanning tree of bridges. Let host  $H1$  send out a broadcast ping packet. Which of the following options represents the correct forwarding table on  $B3$ ?

Hosts	Port
H1, H2, H3, H4	3
H5, H6, H9, H10	1
H7, H8, H11, H12	2

Hosts	Port
H1, H2	4
H3, H4	3
H5, H6	1
H7, H8, H9, H10, H11, H12	2

Hosts	Port
H3, H4	3
H5, H6, H9, H10	1
H1, H2	4
H7, H8, H11, H12	2

Hosts	Port
H1, H2, H3, H4	3
H5, H7, H9, H10	1
H7, H8, H11, H12	4

gatecse-2006 computer-networks bridges normal

[Answer key](#)

2.3

Communication (3) top ↗



### 2.3.1 Communication: GATE CSE 2012 | Question: 44 top ↗

Consider a source computer ( $S$ ) transmitting a file of size  $10^6$  bits to a destination computer ( $D$ ) over a network of two routers ( $R_1$  and  $R_2$ ) and three links ( $L_1, L_2$ , and  $L_3$ ).  $L_1$  connects  $S$  to  $R_1$ ;  $L_2$  connects  $R_1$  to  $R_2$ ; and  $L_3$  connects  $R_2$  to  $D$ . Let each link be of length 100 km. Assume signals travel over each link at a speed of  $10^8$  meters per second. Assume that the link bandwidth on each link is 1 Mbps. Let the file be broken down into 1000 packets each of size 1000 bits. Find the total sum of transmission and propagation delays in transmitting the file from  $S$  to  $D$ ?

- A. 1005 ms      B. 1010 ms      C. 3000 ms      D. 3003 ms

**Answer key****2.3.2 Communication: GATE IT 2007 | Question: 62** 

Let us consider a statistical time division multiplexing of packets. The number of sources is 10. In a time unit, a source transmits a packet of 1000 bits. The number of sources sending data for the first 20 time units is 6, 9, 3, 7, 2, 2, 2, 3, 4, 6, 1, 10, 7, 5, 8, 3, 6, 2, 9, 5 respectively. The output capacity of multiplexer is 5000 bits per time unit. Then the average number of backlogged of packets per time unit during the given period is

- A. 5      B. 4.45      C. 3.45      D. 0

**Answer key****2.3.3 Communication: GATE IT 2007 | Question: 64** 

A broadcast channel has 10 nodes and total capacity of 10 Mbps. It uses polling for medium access. Once a node finishes transmission, there is a polling delay of 80  $\mu$ s to poll the next node. Whenever a node is polled, it is allowed to transmit a maximum of 1000 bytes. The maximum throughput of the broadcast channel is:

- A. 1 Mbps      B. 100/11 Mbps      C. 10 Mbps      D. 100 Mbps

**Answer key****2.4****Congestion Control (7)** **2.4.1 Congestion Control: GATE CSE 2008 | Question: 56** 

In the slow start phase of the TCP congestion algorithm, the size of the congestion window:

- A. does not increase      B. increase linearly  
C. increases quadratically      D. increases exponentially

**Answer key****2.4.2 Congestion Control: GATE CSE 2012 | Question: 45** 

Consider an instance of TCP's Additive Increase Multiplicative Decrease (AIMD) algorithm where the window size at the start of the slow start phase is 2 MSS and the threshold at the start of the first transmission is 8 MSS. Assume that a timeout occurs during the fifth transmission. Find the congestion window size at the end of the tenth transmission.

- A. 8 MSS      B. 14 MSS      C. 7 MSS      D. 12 MSS

**Answer key****2.4.3 Congestion Control: GATE CSE 2014 Set 1 | Question: 27** 

Let the size of congestion window of a TCP connection be 32 KB when a timeout occurs. The round trip time of the connection is 100 msec and the maximum segment size used is 2 KB. The time taken (in msec) by the TCP connection to get back to 32 KB congestion window is \_\_\_\_\_.

**Answer key****2.4.4 Congestion Control: GATE CSE 2015 Set 1 | Question: 29** 

Consider a LAN with four nodes  $S_1, S_2, S_3$ , and  $S_4$ . Time is divided into fixed-size slots, and a node can begin its transmission only at the beginning of a slot. A collision is said to have occurred if more than one node transmits in the same slot. The probabilities of generation of a frame in a time slot by  $S_1, S_2, S_3$ , and  $S_4$  are

0.1, 0.2, 0.3 and 0.4 respectively. The probability of sending a frame in the first slot without any collision by any of these four stations is \_\_\_\_\_.

gatecse-2015-set1 computer-networks normal numerical-answers congestion-control

Answer key 

#### 2.4.5 Congestion Control: GATE CSE 2018 | Question: 14

Consider the following statements regarding the slow start phase of the TCP congestion control algorithm. Note that  $cwnd$  stands for the TCP congestion window and MSS window denotes the Maximum Segments Size:

- i. The  $cwnd$  increases by 2 MSS on every successful acknowledgment
- ii. The  $cwnd$  approximately doubles on every successful acknowledgment
- iii. The  $cwnd$  increases by 1 MSS every round trip time
- iv. The  $cwnd$  approximately doubles every round trip time

Which one of the following is correct?

- |                                 |                                |
|---------------------------------|--------------------------------|
| A. Only (ii) and (iii) are true | B. Only (i) and (iii) are true |
| C. Only (iv) is true            | D. Only (i) and (iv) are true  |

gatecse-2018 computer-networks tcp congestion-control normal 1-mark

Answer key 

#### 2.4.6 Congestion Control: GATE CSE 2018 | Question: 55

Consider a simple communication system where multiple nodes are connected by a shared broadcast medium (like Ethernet or wireless). The nodes in the system use the following carrier-sense based medium access protocol. A node that receives a packet to transmit will carrier-sense the medium for 5 units of time. If the node does not detect any other transmission, it starts transmitting its packet in the next time unit. If the node detects another transmission, it waits until this other transmission finishes, and then begins to carrier-sense for 5 time units again. Once they start to transmit, nodes do not perform any collision detection and continue transmission even if a collision occurs. All transmissions last for 20 units of time. Assume that the transmission signal travels at the speed of 10 meters per unit time in the medium.

Assume that the system has two nodes  $P$  and  $Q$ , located at a distance  $d$  meters from each other.  $P$  starts transmitting a packet at time  $t = 0$  after successfully completing its carrier-sense phase. Node  $Q$  has a packet to transmit at time  $t = 0$  and begins to carrier-sense the medium.

The maximum distance  $d$  (in meters, rounded to the closest integer) that allows  $Q$  to successfully avoid a collision between its proposed transmission and  $P$ 's ongoing transmission is \_\_\_\_\_.

gatecse-2018 computer-networks congestion-control numerical-answers 2-marks

Answer key 

#### 2.4.7 Congestion Control: GATE IT 2005 | Question: 73

On a TCP connection, current congestion window size is Congestion Window = 4 KB. The window size advertised by the receiver is Advertise Window = 6 KB. The last byte sent by the sender is LastByteSent = 10240 and the last byte acknowledged by the receiver is LastByteAcked = 8192. The current window size at the sender is:

- A. 2048 bytes
- B. 4096 bytes
- C. 6144 bytes
- D. 8192 bytes

gateit-2005 computer-networks congestion-control normal

Answer key 

## 2.5

#### Crc Polynomial (4)

##### 2.5.1 Crc Polynomial: GATE CSE 2007 | Question: 68, ISRO2016-73

The message 11001001 is to be transmitted using the CRC polynomial  $x^3 + 1$  to protect it from errors. The message that should be transmitted is:



- A. 11001001000      B. 11001001011      C. 11001010      D. 110010010011

gatecse-2007 computer-networks error-detection crc-polynomial normal isro2016

[Answer key](#)

#### 2.5.2 Crc Polynomial: GATE CSE 2017 Set 1 | Question: 32 top

A computer network uses polynomials over  $GF(2)$  for error checking with 8 bits as information bits and uses  $x^3 + x + 1$  as the generator polynomial to generate the check bits. In this network, the message 01011011 is transmitted as:

- A. 01011011010      B. 01011011011      C. 01011011101      D. 01011011100

gatecse-2017-set1 computer-networks crc-polynomial normal

[Answer key](#)

#### 2.5.3 Crc Polynomial: GATE CSE 2021 Set 2 | Question: 34 top

Consider the cyclic redundancy check (CRC) based error detecting scheme having the generator polynomial  $X^3 + X + 1$ . Suppose the message  $m_4m_3m_2m_1m_0 = 11000$  is to be transmitted. Check bits  $c_2c_1c_0$  are appended at the end of the message by the transmitter using the above CRC scheme. The transmitted bit string is denoted by  $m_4m_3m_2m_1m_0c_2c_1c_0$ . The value of the checkbit sequence  $c_2c_1c_0$  is

- A. 101      B. 110      C. 100      D. 111

gatecse-2021-set2 computer-networks crc-polynomial 2-marks

[Answer key](#)

#### 2.5.4 Crc Polynomial: GATE IT 2005 | Question: 78 top

Consider the following message  $M = 1010001101$ . The cyclic redundancy check (CRC) for this message using the divisor polynomial  $x^5 + x^4 + x^2 + 1$  is :

- A. 01110      B. 01011      C. 10101      D. 10110

gateit-2005 computer-networks crc-polynomial normal

[Answer key](#)

2.6

Csma Cd (5) top

#### 2.6.1 Csma Cd: GATE CSE 2015 Set 3 | Question: 6 top

Consider a CSMA/CD network that transmits data at a rate of 100 Mbps ( $10^8$  bits per second) over a 1 km (kilometre) cable with no repeaters. If the minimum frame size required for this network is 1250 bytes, What is the signal speed (km/sec) in the cable?

- A. 8000      B. 10000      C. 16000      D. 20000

gatecse-2015-set3 computer-networks congestion-control csma-cd normal

[Answer key](#)

#### 2.6.2 Csma Cd: GATE CSE 2016 Set 2 | Question: 53 top

A network has a data transmission bandwidth of  $20 \times 10^6$  bits per second. It uses CSMA/CD in the MAC layer. The maximum signal propagation time from one node to another node is 40 microseconds. The minimum size of a frame in the network is \_\_\_\_\_ bytes.

gatecse-2016-set2 computer-networks csma-cd numerical-answers normal

[Answer key](#)

### 2.6.3 Csma Cd: GATE IT 2005 | Question: 27 top



Which of the following statements is TRUE about CSMA/CD:

- A. IEEE 802.11 wireless LAN runs CSMA/CD protocol
- B. Ethernet is not based on CSMA/CD protocol
- C. CSMA/CD is not suitable for a high propagation delay network like satellite network
- D. There is no contention in a CSMA/CD network

gateit-2005 computer-networks congestion-control csma-cd normal

[Answer key](#)

### 2.6.4 Csma Cd: GATE IT 2005 | Question: 71 top



A network with CSMA/CD protocol in the MAC layer is running at 1Gbps over a 1km cable with no repeaters. The signal speed in the cable is  $2 \times 10^8$  m/sec. The minimum frame size for this network should be:

- A. 10000bits
- B. 10000bytes
- C. 5000 bits
- D. 5000bytes

gateit-2005 computer-networks congestion-control csma-cd normal

[Answer key](#)

### 2.6.5 Csma Cd: GATE IT 2008 | Question: 65 top



The minimum frame size required for a CSMA/CD based computer network running at 1Gbps on a 200m cable with a link speed of  $2 \times 10^8$  m/sec is:

- A. 125bytes
- B. 250bytes
- C. 500bytes
- D. None of the above

gateit-2008 computer-networks csma-cd normal

[Answer key](#)

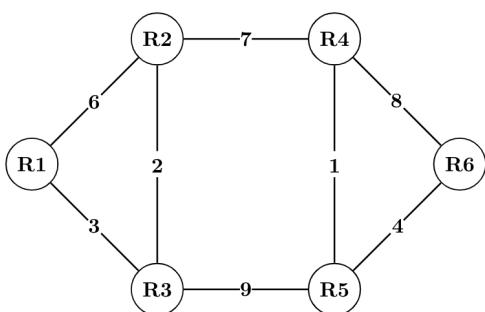
## 2.7

### Distance Vector Routing (8) top

#### 2.7.1 Distance Vector Routing: GATE CSE 2010 | Question: 54 top



Consider a network with 6 routers R1 to R6 connected with links having weights as shown in the following diagram.



All the routers use the distance vector based routing algorithm to update their routing tables. Each router starts with its routing table initialized to contain an entry for each neighbor with the weight of the respective connecting link. After all the routing tables stabilize, how many links in the network will never be used for carrying any data?

- A. 4
- B. 3
- C. 2
- D. 1

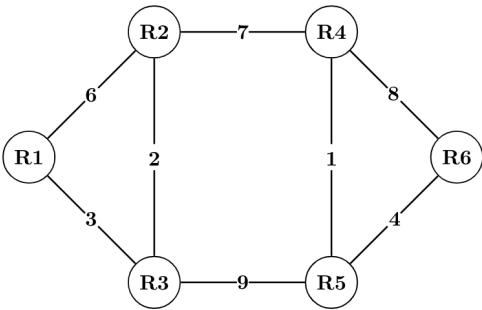
gatecse-2010 computer-networks routing distance-vector-routing normal

[Answer key](#)

#### 2.7.2 Distance Vector Routing: GATE CSE 2010 | Question: 55 top



Consider a network with 6 routers R1 to R6 connected with links having weights as shown in the following diagram.



Suppose the weights of all unused links are changed to 2 and the distance vector algorithm is used again until all routing tables stabilize. How many links will now remain unused?

- A. 0      B. 1      C. 2      D. 3

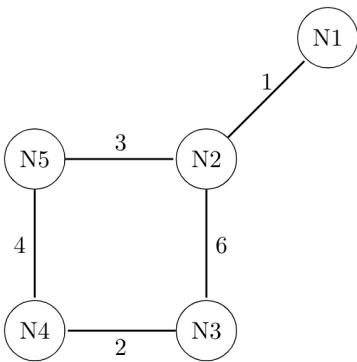
gatecse-2010 computer-networks routing distance-vector-routing normal

[Answer key](#)



### 2.7.3 Distance Vector Routing: GATE CSE 2011 | Question: 52 top

Consider a network with five nodes,  $N_1$  to  $N_5$ , as shown as below.



The network uses a Distance Vector Routing protocol. Once the routes have been stabilized, the distance vectors at different nodes are as follows.

- N1:** (0, 1, 7, 8, 4)
- N2:** (1, 0, 6, 7, 3)
- N3:** (7, 6, 0, 2, 6)
- N4:** (8, 7, 2, 0, 4)
- N5:** (4, 3, 6, 4, 0)

Each distance vector is the distance of the best known path at that instance to nodes,  $N_1$  to  $N_5$ , where the distance to itself is 0. Also, all links are symmetric and the cost is identical in both directions. In each round, all nodes exchange their distance vectors with their respective neighbors. Then all nodes update their distance vectors. In between two rounds, any change in cost of a link will cause the two incident nodes to change only that entry in their distance vectors.

The cost of link  $N_2 - N_3$  reduces to 2 (in both directions). After the next round of updates, what will be the new distance vector at node,  $N_3$ ?

- A. (3, 2, 0, 2, 5)      B. (3, 2, 0, 2, 6)  
 C. (7, 2, 0, 2, 5)      D. (7, 2, 0, 2, 6)

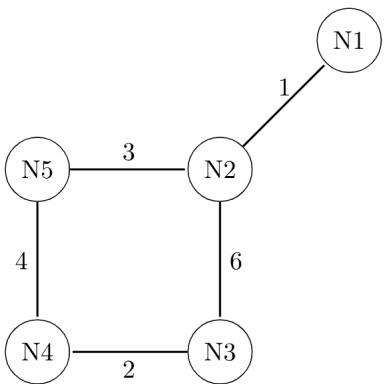
gatecse-2011 computer-networks routing distance-vector-routing normal

[Answer key](#)



### 2.7.4 Distance Vector Routing: GATE CSE 2011 | Question: 53 top

Consider a network with five nodes,  $N_1$  to  $N_5$ , as shown as below.



The network uses a Distance Vector Routing protocol. Once the routes have been stabilized, the distance vectors at different nodes are as follows.

- **N1:** (0, 1, 7, 8, 4)
- **N2:** (1, 0, 6, 7, 3)
- **N3:** (7, 6, 0, 2, 6)
- **N4:** (8, 7, 2, 0, 4)
- **N5:** (4, 3, 6, 4, 0)

Each distance vector is the distance of the best known path at that instance to nodes,  $N_1$  to  $N_5$ , where the distance to itself is 0. Also, all links are symmetric and the cost is identical in both directions. In each round, all nodes exchange their distance vectors with their respective neighbors. Then all nodes update their distance vectors. In between two rounds, any change in cost of a link will cause the two incident nodes to change only that entry in their distance vectors.

The cost of link  $N_2 - N_3$  reduces to 2 (in both directions). After the next round of updates, the link  $N_1 - N_2$  goes down.  $N_2$  will reflect this change immediately in its distance vector as cost,  $\infty$ . After the **NEXT ROUND** of update, what will be the cost to  $N_1$  in the distance vector of  $N_3$ ?

- A. 3      B. 9      C. 10      D.  $\infty$

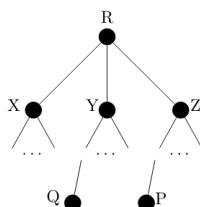
gatecse-2011 computer-networks routing distance-vector-routing normal

**Answer key**

### 2.7.5 Distance Vector Routing: GATE CSE 2021 Set 2 | Question: 45 top



Consider a computer network using the distance vector routing algorithm in its network layer. The partial topology of the network is shown below.

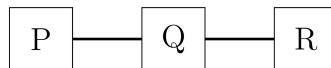


The objective is to find the shortest-cost path from the router  $R$  to routers  $P$  and  $Q$ . Assume that  $R$  does not initially know the shortest routes to  $P$  and  $Q$ . Assume that  $R$  has three neighbouring routers denoted as  $X$ ,  $Y$  and  $Z$ . During one iteration,  $R$  measures its distance to its neighbours  $X$ ,  $Y$ , and  $Z$  as 3, 2 and 5, respectively. Router  $R$  gets routing vectors from its neighbours that indicate that the distance to router  $P$  from routers  $X$ ,  $Y$  and  $Z$  are 7, 6 and 5, respectively. The routing vector also indicates that the distance to router  $Q$  from routers  $X$ ,  $Y$  and  $Z$  are 4, 6 and 8 respectively. Which of the following statement(s) is/are correct with respect to the new routing table of  $R$ , after updation during this iteration?

- A. The distance from  $R$  to  $P$  will be stored as 10
- B. The distance from  $R$  to  $Q$  will be stored as 7
- C. The next hop router for a packet from  $R$  to  $P$  is  $Y$
- D. The next hop router for a packet from  $R$  to  $Q$  is  $Z$

**Answer key****2.7.6 Distance Vector Routing: GATE CSE 2022 | Question: 47**

Consider a network with three routers P, Q, R shown in the figure below. All the links have cost of unity.



The routers exchange distance vector routing information and have converged on the routing tables, after which the link Q-R fails. Assume that P and Q send out routing updates at random times, each at the same average rate. The probability of a routing loop formation (*rounded off to one decimal place*) between P and Q, leading to count-to-infinity problem, is \_\_\_\_\_.

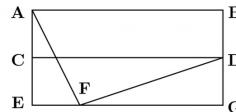
**Answer key****2.7.7 Distance Vector Routing: GATE IT 2005 | Question: 29**

Count to infinity is a problem associated with:

- A. link state routing protocol.
- B. distance vector routing protocol
- C. DNS while resolving host name
- D. TCP for congestion control

**Answer key****2.7.8 Distance Vector Routing: GATE IT 2007 | Question: 60**

For the network given in the figure below, the routing tables of the four nodes A, E, D and G are shown. Suppose that F has estimated its delay to its neighbors, A, E, D and G as 8, 10, 12 and 6 msec respectively and updates its routing table using distance vector routing technique.

**Routing Table of A**

A	0
B	40
C	14
D	17
E	21
F	9
G	24

**Routing Table of D**

A	20
B	8
C	30
D	0
E	14
F	7
G	22

**Routing Table of E**

A	24
B	27
C	7
D	20
E	0
F	11
G	22

**Routing Table of G**

A	21
B	24
C	22
D	19
E	22
F	10
G	0

A.

A	8
B	20
C	17
D	12
E	10
F	0
G	6

B.

A	21
B	8
C	7
D	19
E	14
F	0
G	22

C.

A	8
B	20
C	17
D	12
E	10
F	16
G	6

D.

A	8
B	8
C	7
D	12
E	10
F	0
G	6

[Answer key](#)

2.8

Error Detection (8) [top](#)

**2.8.1 Error Detection: GATE CSE 1992 | Question: 01,ii** [top](#)



Consider a 3-bit error detection and 1-bit error correction hamming code for 4-bit data. The extra parity bits required would be \_\_\_\_\_ and the 3-bit error detection is possible because the code has a minimum distance of \_\_\_\_\_.

gate1992 computer-networks error-detection normal fill-in-the-blanks

[Answer key](#)

**2.8.2 Error Detection: GATE CSE 1995 | Question: 1.12** [top](#)



What is the distance of the following code 000000, 010101, 000111, 011001, 111111?

- A. 2
- B. 3
- C. 4
- D. 1

gate1995 computer-networks error-detection normal

[Answer key](#)

**2.8.3 Error Detection: GATE CSE 2009 | Question: 48** [top](#)



Let  $G(x)$  be the generator polynomial used for CRC checking. What is the condition that should be satisfied by  $G(x)$  to detect odd number of bits in error?

- A.  $G(x)$  contains more than two terms
- B.  $G(x)$  does not divide  $1 + x^k$ , for any  $k$  not exceeding the frame length
- C.  $1 + x$  is a factor of  $G(x)$
- D.  $G(x)$  has an odd number of terms.

gatecse-2009 computer-networks error-detection normal

[Answer key](#)

**2.8.4 Error Detection: GATE CSE 2014 Set 3 | Question: 24** [top](#)



A bit-stuffing based framing protocol uses an 8-bit delimiter pattern of 01111110. If the output bit-string after stuffing is 01111100101, then the input bit-string is:

- A. 0111110100
- B. 0111110101
- C. 0111111101
- D. 0111111111

gatecse-2014-set3 computer-networks error-detection

[Answer key](#)

**2.8.5 Error Detection: GATE IT 2005 | Question: 74** [top](#)



In a communication network, a packet of length  $L$  bits takes link  $L_1$  with a probability of  $p_1$  or link  $L_2$  with a probability of  $p_2$ . Link  $L_1$  and  $L_2$  have bit error probability of  $b_1$  and  $b_2$  respectively. The probability that the packet will be received without error via either  $L_1$  or  $L_2$  is

- A.  $(1 - b_1)^L p_1 + (1 - b_2)^L p_2$
- B.  $[1 - (b_1 + b_2)^L] p_1 p_2$
- C.  $(1 - b_1)^L (1 - b_2)^L p_1 p_2$
- D.  $1 - (b_1^L p_1 + b_2^L p_2)$

gateit-2005 computer-networks error-detection probability normal

[Answer key](#)

**2.8.6 Error Detection: GATE IT 2007 | Question: 43** [top](#)



An error correcting code has the following code words: 00000000, 00001111, 01010101, 10101010, 11110000. What is the maximum number of bit errors that can be corrected?

- A. 0
- B. 1
- C. 2
- D. 3

**Answer key****2.8.7 Error Detection: GATE IT 2008 | Question: 66**

Data transmitted on a link uses the following  $2D$  parity scheme for error detection:

Each sequence of 28 bits is arranged in a  $4 \times 7$  matrix (rows  $r_0$  through  $r_3$ , and columns  $d_7$  through  $d_0$ ) and is padded with a column  $d_0$  and row  $r_4$  of parity bits computed using the Even parity scheme. Each bit of column  $d_0$  (respectively, row  $r_4$ ) gives the parity of the corresponding row (respectively, column). These 40 bits are transmitted over the data link.

	$d_7$	$d_6$	$d_5$	$d_4$	$d_3$	$d_2$	$d_1$	$d_0$
$r_0$	0	1	0	1	0	0	1	1
$r_1$	1	1	0	0	1	1	1	0
$r_2$	0	0	0	1	0	1	0	0
$r_3$	0	1	1	0	1	0	1	0
$r_4$	1	1	0	0	0	1	1	0

The table shows data received by a receiver and has  $n$  corrupted bits. What is the minimum possible value of  $n$ ?

- A. 1      B. 2      C. 3      D. 4

**Answer key****2.8.8 Error Detection: GATE1987-2-i**

Match the pairs in the following questions:

(A) Cyclic Redundancy Code	(p) Error Correction
(B) Serial Communication	(q) Wired-OR
(C) Open Collector	(r) Error detection
(D) Hamming Code	(s) RS-232-C

**Answer key****2.9****Ethernet (5)****2.9.1 Ethernet: GATE CSE 2004 | Question: 54**

$A$  and  $B$  are the only two stations on an Ethernet. Each has a steady queue of frames to send. Both  $A$  and  $B$  attempt to transmit a frame, collide, and  $A$  wins the first backoff race. At the end of this successful transmission by  $A$ , both  $A$  and  $B$  attempt to transmit and collide. The probability that  $A$  wins the second backoff race is:

- A. 0.5      B. 0.625      C. 0.75      D. 1.0

**Answer key****2.9.2 Ethernet: GATE CSE 2013 | Question: 36**

Determine the maximum length of the cable (in km) for transmitting data at a rate of 500 Mbps in an Ethernet LAN with frames of size 10,000 bits. Assume the signal speed in the cable to be 2,00,000 km/s.

- A. 1      B. 2  
C. 2.5      D. 5

[Answer key](#)

### 2.9.3 Ethernet: GATE CSE 2016 Set 2 | Question: 24 [top](#)

In an Ethernet local area network, which one of the following statements is **TRUE**?

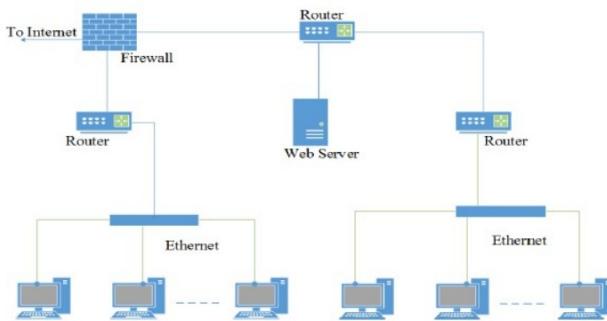
- A. A station stops to sense the channel once it starts transmitting a frame.
- B. The purpose of the jamming signal is to pad the frames that are smaller than the minimum frame size.
- C. A station continues to transmit the packet even after the collision is detected.
- D. The exponential back off mechanism reduces the probability of collision on retransmissions.

gatecse-2016-set2 computer-networks ethernet normal

[Answer key](#)

### 2.9.4 Ethernet: GATE CSE 2022 | Question: 12 [top](#)

Consider an enterprise network with two Ethernet segments, a web server and a firewall, connected via three routers as shown below.



What is the number of subnets inside the enterprise network?

- A. 3
- B. 12
- C. 6
- D. 8

gatecse-2022 computer-networks ethernet 1-mark

[Answer key](#)

### 2.9.5 Ethernet: GATE IT 2006 | Question: 19 [top](#)

Which of the following statements is **TRUE**?

- A. Both Ethernet frame and IP packet include checksum fields
- B. Ethernet frame includes a checksum field and IP packet includes a CRC field
- C. Ethernet frame includes a CRC field and IP packet includes a checksum field
- D. Both Ethernet frame and IP packet include CRC fields

gateit-2006 computer-networks normal ethernet

[Answer key](#)

2.10

[Go Back N \(1\)](#) [top](#)

### 2.10.1 Go Back N: GATE CS Applied Course Test Series [top](#)

In the GO back N ARQ sender is sending the 15 packets to the destination with a window size of 5. Assume every sixth packet while transmission is lost. How many transmissions will there be?

computer-networks applied-gate-test-series go-back-n

[Answer key](#)

2.11

[Hamming Code \(2\)](#) [top](#)

### 2.11.1 Hamming Code: GATE CSE 1994 | Question: 9 top



Following 7 bit single error correcting hamming coded message is received.

7	6	5	4	3	2	1	bit No.
1	0	0	0	1	1	0	<input type="text" value="X"/>

Determine if the message is correct (assuming that at most 1 bit could be corrupted). If the message contains an error find the bit which is erroneous and gives correct message.

gate1994 computer-networks error-detection hamming-code normal descriptive

**Answer key** [a]

### 2.11.2 Hamming Code: GATE CSE 2021 Set 1 | Question: 29 top



Assume that a 12-bit Hamming codeword consisting of 8-bit data and 4 check bits is  $d_8d_7d_6d_5c_8d_4d_3d_2c_4d_1c_2c_1$ , where the data bits and the check bits are given in the following tables:

Data bits								Check bits			
$d_8 \quad d_7 \quad d_6 \quad d_5 \quad d_4 \quad d_3 \quad d_2 \quad d_1$								$c_8$	$c_4$	$c_2$	$c_1$
1	1	0	$x$	0	1	0	1	$y$	0	1	0

Which one of the following choices gives the correct values of  $x$  and  $y$ ?

- A.  $x$  is 0 and  $y$  is 0    B.  $x$  is 0 and  $y$  is 1    C.  $x$  is 1 and  $y$  is 0    D.  $x$  is 1 and  $y$  is 1

gatecse-2021-set1 computer-networks hamming-code 2-marks

**Answer key** [a]

## 2.12

### Icmp (1) top



### 2.12.1 Icmp: GATE IT 2005 | Question: 26 top

Traceroute reports a possible route that is taken by packets moving from some host  $A$  to some other host  $B$ . Which of the following options represents the technique used by traceroute to identify these hosts:

- A. By progressively querying routers about the next router on the path to  $B$  using ICMP packets, starting with the first router
- B. By requiring each router to append the address to the ICMP packet as it is forwarded to  $B$ . The list of all routers en-route to  $B$  is returned by  $B$  in an ICMP reply packet
- C. By ensuring that an ICMP reply packet is returned to  $A$  by each router en-route to  $B$ , in the ascending order of their hop distance from  $A$
- D. By locally computing the shortest path from  $A$  to  $B$

gateit-2005 computer-networks icmp application-layer-protocols normal

**Answer key** [a]

## 2.13

### Ip Address (1) top



### 2.13.1 Ip Address: GATE CSE 2023 | Question: 42 top

Suppose in a web browser, you click on the [www.gate-2023.in](http://www.gate-2023.in) URL. The browser cache is empty. The IP address for this URL is not cached in your local host, so a DNS lookup is triggered (by the local DNS server deployed on your local host) over the 3-tier DNS hierarchy in an iterative mode. No resource records are cached anywhere across all DNS servers.

Let RTT denote the round trip time between your local host and DNS servers in the DNS hierarchy. The round trip time between the local host and the web server hosting [www.gate-2023.in](http://www.gate-2023.in) is also equal to RTT. The HTML file associated with the URL is small enough to have negligible transmission time and negligible rendering time by your web browser, which references 10 equally small objects on the same web server.

Which of the following statements is/are CORRECT about the minimum elapsed time between clicking on the URL and your browser fully rendering it?

- A. 7 RTTs, in case of non-persistent HTTP with 5 parallel TCP connections.
- B. 5 RTTs, in case of persistent HTTP with pipelining.
- C. 9 RTTs, in case of non-persistent HTTP with 5 parallel TCP connections.
- D. 6 RTTs, in case of persistent HTTP with pipelining.

gatecse-2023 computer-networks ip-address multiple-selects 2-marks

[Answer key](#)

2.14

Ip Addressing (8) [top](#)

#### 2.14.1 Ip Addressing: GATE CSE 2003 | Question: 27 [top](#)



Which of the following assertions is FALSE about the Internet Protocol (IP)?

- A. It is possible for a computer to have multiple IP addresses
- B. IP packets from the same source to the same destination can take different routes in the network
- C. IP ensures that a packet is discarded if it is unable to reach its destination within a given number of hops
- D. The packet source cannot set the route of an outgoing packets; the route is determined only by the routing tables in the routers on the way

gatecse-2003 computer-networks ip-addressing normal

[Answer key](#)

#### 2.14.2 Ip Addressing: GATE CSE 2004 | Question: 56 [top](#)



Consider three IP networks  $A$ ,  $B$  and  $C$ . Host  $H_A$  in network  $A$  sends messages each containing 180 bytes of application data to a host  $H_C$  in network  $C$ . The TCP layer prefixes 20 byte header to the message.

This passes through an intermediate network  $B$ . The maximum packet size, including 20 byte IP header, in each network is:

- A: 1000 bytes
- B: 100 bytes
- C: 1000 bytes

The network  $A$  and  $B$  are connected through a 1 Mbps link, while  $B$  and  $C$  are connected by a 512 Kbps link (bps = bits per second).



Assuming that the packets are correctly delivered, how many bytes, including headers, are delivered to the IP layer at the destination for one application message, in the best case? Consider only data packets.

- A. 200
- B. 220
- C. 240
- D. 260

gatecse-2004 computer-networks ip-addressing tcp normal

[Answer key](#)

#### 2.14.3 Ip Addressing: GATE CSE 2004 | Question: 57 [top](#)



Consider three IP networks  $A$ ,  $B$  and  $C$ . Host  $H_A$  in network  $A$  sends messages each containing 180 bytes of application data to a host  $H_C$  in network  $C$ . The TCP layer prefixes 20 byte header to the message. This passes through an intermediate network  $B$ . The maximum packet size, including 20 byte IP header, in each network, is:

- A : 1000 bytes
- B : 100 bytes
- C : 1000 bytes

The network  $A$  and  $B$  are connected through a  $1 \text{ Mbps}$  link, while  $B$  and  $C$  are connected by a  $512 \text{ Kbps}$  link ( $\text{bps} = \text{bits per second}$ ).



What is the rate at which application data is transferred to host  $H_C$ ? Ignore errors, acknowledgments, and other overheads.

- A.  $325.5 \text{ Kbps}$
- B.  $354.5 \text{ Kbps}$
- C.  $409.6 \text{ Kbps}$
- D.  $512.0 \text{ Kbps}$

gatecse-2004 computer-networks ip-addressing tcp normal

[Answer key](#)

#### 2.14.4 Ip Addressing: GATE CSE 2012 | Question: 23 [top](#)

In the IPv4 addressing format, the number of networks allowed under Class  $C$  addresses is:

- A.  $2^{14}$
- B.  $2^7$
- C.  $2^{21}$
- D.  $2^{24}$

gatecse-2012 computer-networks ip-addressing easy

[Answer key](#)

#### 2.14.5 Ip Addressing: GATE CSE 2013 | Question: 37 [top](#)

In an IPv4 datagram, the  $M$  bit is 0, the value of  $HLEN$  is 10, the value of total length is 400 and the fragment offset value is 300. The position of the datagram, the sequence numbers of the first and the last bytes of the payload, respectively are:

- A. Last fragment, 2400 and 2789
- B. First fragment, 2400 and 2759
- C. Last fragment, 2400 and 2759
- D. Middle fragment, 300 and 689

gatecse-2013 computer-networks ip-addressing normal

[Answer key](#)

#### 2.14.6 Ip Addressing: GATE CSE 2014 Set 3 | Question: 27 [top](#)

Every host in an IPv4 network has a 1-second resolution real-time clock with battery backup. Each host needs to generate up to 1000 unique identifiers per second. Assume that each host has a globally unique IPv4 address. Design a 50-bit globally unique ID for this purpose. After what period (in seconds) will the identifiers generated by a host wrap around?

gatecse-2014-set3 computer-networks ip-addressing numerical-answers normal

[Answer key](#)

#### 2.14.7 Ip Addressing: GATE CSE 2017 Set 2 | Question: 20 [top](#)

The maximum number of IPv4 router addresses that can be listed in the record route (RR) option field of an IPv4 header is \_\_\_\_\_.

gatecse-2017-set2 computer-networks ip-addressing numerical-answers

[Answer key](#)

#### 2.14.8 Ip Addressing: GATE CSE 2018 | Question: 54 [top](#)

Consider an IP packet with a length of 4,500 bytes that includes a 20-byte IPv4 header and 40-byte TCP header. The packet is forwarded to an IPv4 router that supports a Maximum Transmission Unit (MTU) of 600 bytes. Assume that the length of the IP header in all the outgoing fragments of this packet is 20 bytes. Assume that the fragmentation offset value stored in the first fragment is 0.

The fragmentation offset value stored in the third fragment is \_\_\_\_\_.

gatecse-2018 computer-networks ip-addressing numerical-answers 2-marks

[Answer key](#)

2.15

Ip Packet (8) [top](#)

2.15.1 Ip Packet: GATE CSE 2006 | Question: 5 [top](#)



For which one of the following reasons does internet protocol(IP) use the time-to-live(TTL) field in IP datagram header?

- A. Ensure packets reach destination within that time
- B. Discard packets that reach later than that time
- C. Prevent packets from looping indefinitely
- D. Limit the time for which a packet gets queued in intermediate routers

gatecse-2006 computer-networks ip-addressing ip-packet easy

[Answer key](#)

2.15.2 Ip Packet: GATE CSE 2010 | Question: 15. PGEE 2018 [top](#)



One of the header fields in an IP datagram is the Time-to-Live (TTL) field. Which of the following statements best explains the need for this field?

- A. It can be used to prioritize packets.
- B. It can be used to reduce delays.
- C. It can be used to optimize throughput.
- D. It can be used to prevent packet looping.

gatecse-2010 computer-networks ip-packet easy

[Answer key](#)

2.15.3 Ip Packet: GATE CSE 2014 Set 3 | Question: 25 [top](#)



Host A (on TCP/IP v4 network A) sends an IP datagram D to host B (also on TCP/IP v4 network B). Assume that no error occurred during the transmission of D. When D reaches B, which of the following IP header field(s) may be different from that of the original datagram D?

- i. TTL
  - ii. Checksum
  - iii. Fragment Offset
- 
- A. i only
  - B. i and ii only
  - C. ii and iii only
  - D. i, ii and iii

gatecse-2014-set3 computer-networks ip-packet normal

[Answer key](#)

2.15.4 Ip Packet: GATE CSE 2014 Set 3 | Question: 28 [top](#)



An *IP* router with a Maximum Transmission Unit (MTU) of 1500 bytes has received an *IP* packet of size 4404 bytes with an *IP* header of length 20 bytes. The values of the relevant fields in the header of the third *IP* fragment generated by the router for this packet are:

- A. MF bit: 0, Datagram Length:1444; Offset: 370
- B. MF bit: 1, Datagram Length: 1424; Offset: 185
- C. MF bit: 1, Datagram Length: 1500; Offset: 370
- D. MF bit: 0, Datagram Length: 1424; Offset: 2960

gatecse-2014-set3 computer-networks ip-packet normal

[Answer key](#)

2.15.5 Ip Packet: GATE CSE 2015 Set 1 | Question: 22 [top](#)



Which of the following fields of an IP header is NOT modified by a typical IP router?

- A. Check sum
- B. Source address
- C. Time to Live (TTL)
- D. Length

gatecse-2015-set1 computer-networks ip-packet easy

[Answer key](#)

### 2.15.6 Ip Packet: GATE CSE 2015 Set 2 | Question: 52 [top](#)



Host A sends a UDP datagram containing 8880 bytes of user data to host B over an Ethernet LAN. Ethernet frames may carry data up to 1500 bytes (i.e. MTU = 1500 bytes). Size of UDP header is 8 bytes and size of IP header is 20 bytes. There is no option field in IP header. How many total number of IP fragments will be transmitted and what will be the contents of offset field in the last fragment?

- A. 6 and 925      B. 6 and 7400      C. 7 and 1110      D. 7 and 8880

gatecse-2015-set2 computer-networks ip-packet normal

[Answer key](#)

### 2.15.7 Ip Packet: GATE CSE 2016 Set 1 | Question: 53 [top](#)



An IP datagram of size 1000 bytes arrives at a router. The router has to forward this packet on a link whose MTU (maximum transmission unit) is 100 bytes. Assume that the size of the IP header is 20 bytes.

The number of fragments that the IP datagram will be divided into for transmission is \_\_\_\_\_.

gatecse-2016-set1 computer-networks ip-packet normal numerical-answers

[Answer key](#)

### 2.15.8 Ip Packet: GATE IT 2004 | Question: 86 [top](#)



In the TCP/IP protocol suite, which one of the following is NOT part of the IP header?

- A. Fragment Offset      B. Source IP address  
C. Destination IP address      D. Destination port number

gateit-2004 computer-networks ip-packet normal

[Answer key](#)

## 2.16

### Lan Technologies (6) [top](#)



#### 2.16.1 Lan Technologies: GATE CSE 2003 | Question: 83 [top](#)

A  $2 \text{ km}$  long broadcast LAN has  $10^7$  bps bandwidth and uses CSMA/CD. The signal travels along the wire at  $2 \times 10^8 \text{ m/s}$ . What is the minimum packet size that can be used on this network?

- A. 50 bytes      B. 100 bytes      C. 200 bytes      D. None of the above

gatecse-2003 computer-networks lan-technologies normal

[Answer key](#)

#### 2.16.2 Lan Technologies: GATE CSE 2007 | Question: 65 [top](#)



There are  $n$  stations in slotted LAN. Each station attempts to transmit with a probability  $p$  in each time slot. What is the probability that **ONLY** one station transmits in a given time slot?

- A.  $np(1 - p)^{n-1}$       B.  $(1 - p)^{n-1}$       C.  $p(1 - p)^{n-1}$       D.  $1 - (1 - p)^{n-1}$

gatecse-2007 computer-networks lan-technologies probability normal

[Answer key](#)

#### 2.16.3 Lan Technologies: GATE CSE 2019 | Question: 49 [top](#)



Consider that 15 machines need to be connected in a LAN using 8-port Ethernet switches. Assume that these switches do not have any separate uplink ports. The minimum number of switches needed is \_\_\_\_\_

gatecse-2019 numerical-answers computer-networks lan-technologies 2-marks

[Answer key](#)

#### 2.16.4 Lan Technologies: GATE IT 2004 | Question: 27 top

A host is connected to a Department network which is part of a University network. The University network, in turn, is part of the Internet. The largest network in which the Ethernet address of the host is unique is

- A. the subnet to which the host belongs
- B. the Department network
- C. the University network
- D. the Internet

gateit-2004 computer-networks lan-technologies ethernet normal

[Answer key](#) 

#### 2.16.5 Lan Technologies: GATE IT 2005 | Question: 28 top

Which of the following statements is FALSE regarding a bridge?

- A. Bridge is a layer 2 device
- B. Bridge reduces collision domain
- C. Bridge is used to connect two or more LAN segments
- D. Bridge reduces broadcast domain

gateit-2005 computer-networks lan-technologies ethernet normal

[Answer key](#) 

#### 2.16.6 Lan Technologies: GATE IT 2006 | Question: 66 top

A router has two full-duplex Ethernet interfaces each operating at  $100 \text{ Mb/s}$ . Ethernet frames are at least 84 bytes long (including the Preamble and the Inter-Packet-Gap). The maximum packet processing time at the router for wirespeed forwarding to be possible is (in microseconds)

- A. 0.01
- B. 3.36
- C. 6.72
- D. 8

gateit-2006 computer-networks lan-technologies ethernet normal

[Answer key](#) 

### 2.17

#### Link State Routing (1) top

#### 2.17.1 Link State Routing: GATE CSE 2014 Set 1 | Question: 23 top

Consider the following three statements about link state and distance vector routing protocols, for a large network with 500 network nodes and 4000 links.

- [S1]: The computational overhead in link state protocols is higher than in distance vector protocols.
- [S2]: A distance vector protocol (with split horizon) avoids persistent routing loops, but not a link state protocol.
- [S3]: After a topology change, a link state protocol will converge faster than a distance vector protocol.

Which one of the following is correct about  $S_1$ ,  $S_2$ , and  $S_3$ ?

- A.  $S_1$ ,  $S_2$ , and  $S_3$  are all true.
- B.  $S_1$ ,  $S_2$ , and  $S_3$  are all false.
- C.  $S_1$  and  $S_2$  are true, but  $S_3$  is false.
- D.  $S_1$  and  $S_3$  are true, but  $S_2$  is false.

gatecse-2014-set1 computer-networks routing distance-vector-routing link-state-routing normal

[Answer key](#) 

### 2.18

#### Mac Protocol (4) top

#### 2.18.1 Mac Protocol: GATE CSE 2005 | Question: 74 top

Suppose the round trip propagation delay for a  $10 \text{ Mbps}$  Ethernet having 48-bit jamming signal is  $46.4 \mu\text{s}$ . The minimum frame size is:

- A. 94
- B. 416
- C. 464
- D. 512

gatecse-2005 computer-networks mac-protocol ethernet

[Answer key](#) 

#### 2.18.2 Mac Protocol: GATE CSE 2015 Set 2 | Question: 8 top

A link has transmission speed of  $10^6$  bits/sec. It uses data packets of size 1000 bytes each. Assume that

the acknowledgment has negligible transmission delay and that its propagation delay is the same as the data propagation delay. Also, assume that the processing delays at nodes are negligible. The efficiency of the stop-and-wait protocol in this setup is exactly 25%. The value of the one way propagation delay (in milliseconds) is\_\_\_\_\_.

gatecse-2015-set2 computer-networks mac-protocol stop-and-wait normal numerical-answers

Answer key 

### 2.18.3 Mac Protocol: GATE IT 2004 | Question: 85

Consider a simplified time slotted MAC protocol, where each host always has data to send and transmits with probability  $p = 0.2$  in every slot. There is no backoff and one frame can be transmitted in one slot. If more than one host transmits in the same slot, then the transmissions are unsuccessful due to collision. What is the maximum number of hosts which this protocol can support if each host has to be provided a minimum throughput of 0.16 frames per time slot?

- A. 1      B. 2      C. 3      D. 4

gateit-2004 computer-networks congestion-control mac-protocol normal

Answer key 

### 2.18.4 Mac Protocol: GATE IT 2005 | Question: 75

In a TDM medium access control bus LAN, each station is assigned one time slot per cycle for transmission. Assume that the length of each time slot is the time to transmit 100 bits plus the end-to-end propagation delay. Assume a propagation speed of  $2 \times 10^8 \text{ m/sec}$ . The length of the LAN is 1 km with a bandwidth of 10 Mbps. The maximum number of stations that can be allowed in the LAN so that the throughput of each station can be  $2/3$  Mbps is

- A. 3      B. 5      C. 10      D. 20

gateit-2005 computer-networks mac-protocol normal

Answer key 

## 2.19

### Network Flow (5)

#### 2.19.1 Network Flow: GATE CSE 1992 | Question: 01,V

A simple and reliable data transfer can be accomplished by using the 'handshake protocol'. It accomplishes reliable data transfer because for every data item sent by the transmitter \_\_\_\_\_.

gate1992 computer-networks network-flow easy fill-in-the-blanks

Answer key 

#### 2.19.2 Network Flow: GATE CSE 2017 Set 2 | Question: 35

Consider two hosts  $X$  and  $Y$ , connected by a single direct link of rate  $10^6$  bits/sec. The distance between the two hosts is 10,000 km and the propagation speed along the link is  $2 \times 10^8$  m/sec. Host  $X$  sends a file of 50,000 bytes as one large message to host  $Y$  continuously. Let the transmission and propagation delays be  $p$  milliseconds and  $q$  milliseconds respectively. Then the value of  $p$  and  $q$  are

- A.  $p = 50$  and  $q = 100$  B.  $p = 50$  and  $q = 400$  C.  $p = 100$  and  $q = 50$  D.  $p = 400$  and  $q = 50$

gatecse-2017-set2 computer-networks network-flow

Answer key 

#### 2.19.3 Network Flow: GATE IT 2004 | Question: 80

In a data link protocol, the frame delimiter flag is given by 0111. Assuming that bit stuffing is employed, the transmitter sends the data sequence 01110110 as

- A. 01101011 B. 011010110 C. 011101100 D. 0110101100

**Answer key****2.19.4 Network Flow: GATE IT 2004 | Question: 87**

A TCP message consisting of 2100 *bytes* is passed to IP for delivery across two networks. The first network can carry a maximum payload of 1200 *bytes* per frame and the second network can carry a maximum payload of 400 *bytes* per frame, excluding network overhead. Assume that IP overhead per packet is 20 *bytes*. What is the total IP overhead in the second network for this transmission?

- A. 40 bytes      B. 80 bytes      C. 120 bytes      D. 160 bytes

**Answer key****2.19.5 Network Flow: GATE IT 2006 | Question: 67**

A link of capacity 100 Mbps is carrying traffic from a number of sources. Each source generates an on-off traffic stream; when the source is on, the rate of traffic is 10 Mbps, and when the source is off, the rate of traffic is zero. The duty cycle, which is the ratio of on-time to off-time, is 1 : 2. When there is no buffer at the link, the minimum number of sources that can be multiplexed on the link so that link capacity is not wasted and no data loss occurs is  $S_1$ . Assuming that all sources are synchronized and that the link is provided with a large buffer, the maximum number of sources that can be multiplexed so that no data loss occurs is  $S_2$ . The values of  $S_1$  and  $S_2$  are, respectively,

- A. 10 and 30      B. 12 and 25      C. 5 and 33      D. 15 and 22

**Answer key****2.20****Network Layering (6)****2.20.1 Network Layering: GATE CSE 2003 | Question: 28**

Which of the following functionality *must* be implemented by a transport protocol over and above the network protocol?

- A. Recovery from packet losses  
C. Packet delivery in the correct order
- B. Detection of duplicate packets  
D. End to end connectivity

**Answer key****2.20.2 Network Layering: GATE CSE 2004 | Question: 15**

Choose the best matching between Group 1 and Group 2

<b>Group-1</b>	<b>Group-2</b>
P. Data link layer	1. Ensures reliable transport of data over a physical point-to-point link
Q. Network layer	2. Encodes/decodes data for physical transmission
R. Transport layer	3. Allows end-to-end communication between two processes
	4. Routes data from one network node to the next

- A. P-1, Q-4, R-3      B. P-2, Q-4, R-1      C. P-2, Q-3, R-1      D. P-1, Q-3, R-2

**Answer key**

### 2.20.3 Network Layering: GATE CSE 2007 | Question: 70 top



Match the following:

- |     |      |     |                   |
|-----|------|-----|-------------------|
| (P) | SMTP | (1) | Application layer |
| (Q) | BGP  | (2) | Transport layer   |
| (R) | TCP  | (3) | Data link layer   |
| (S) | PPP  | (4) | Network layer     |
|     |      | (5) | Physical layer    |

A. P - 2, Q - 1, R - 3, S - 5  
C. P - 1, Q - 4, R - 2, S - 5

B. P - 1, Q - 4, R - 2, S - 3  
D. P - 2, Q - 4, R - 1, S - 3

gatecse-2007 computer-networks network-layering network-protocols easy

[Answer key](#)



### 2.20.4 Network Layering: GATE CSE 2013 | Question: 14 top



Assume that source S and destination D are connected through two intermediate routers labeled R. Determine how many times each packet has to visit the network layer and the data link layer during a transmission from S to D.

- A. Network layer – 4 times and Data link layer – 4 times
- B. Network layer – 4 times and Data link layer – 3 times
- C. Network layer – 4 times and Data link layer – 6 times
- D. Network layer – 2 times and Data link layer – 6 times

gatecse-2013 computer-networks network-layering normal

[Answer key](#)



### 2.20.5 Network Layering: GATE CSE 2014 Set 3 | Question: 23 top



In the following pairs of OSI protocol layer/sub-layer and its functionality, the **INCORRECT** pair is

- |   |  |
|---|--|
| A. Network layer and Routing                            | B. Data Link Layer and Bit synchronization             |
| C. Transport layer and End-to-end process communication | D. Medium Access Control sub-layer and Channel sharing |

gatecse-2014-set3 computer-networks network-layering easy

[Answer key](#)



### 2.20.6 Network Layering: GATE CSE 2018 | Question: 13 top



Match the following:

Field	Length in bits
P. UDP Header's Port Number	I. 48
Q. Ethernet MAC Address	II. 8
R. IPv6 Next Header	III. 32
S. TCP Header's Sequence Number	IV. 16

- A. P-III, Q-IV, R-II, S-I
- C. P-IV, Q-I, R-II, S-III
- B. P-II, Q-I, R-IV, S-III
- D. P-IV, Q-I, R-III, S-II

gatecse-2018 computer-networks network-layering normal 1-mark

[Answer key](#)

## 2.21.1 Network Protocols: GATE CSE 2005 | Question: 24 top



The address resolution protocol (ARP) is used for:

- A. Finding the IP address from the DNS
- B. Finding the IP address of the default gateway
- C. Finding the IP address that corresponds to a MAC address
- D. Finding the MAC address that corresponds to an IP address

gatecse-2005 computer-networks normal network-protocols

[Answer key](#)

## 2.21.2 Network Protocols: GATE CSE 2007 | Question: 20 top



Which one of the following uses UDP as the transport protocol?

- A. HTTP
- B. Telnet
- C. DNS
- D. SMTP

gatecse-2007 computer-networks network-protocols application-layer-protocols easy

[Answer key](#)

## 2.21.3 Network Protocols: GATE CSE 2015 Set 1 | Question: 17 top



In one of the pairs of protocols given below , both the protocols can use multiple TCP connections between the same client and the server. Which one is that?

- A. HTTP, FTP
- B. HTTP, TELNET
- C. FTP, SMTP
- D. HTTP, SMTP

gatecse-2015-set1 computer-networks network-protocols normal

[Answer key](#)

## 2.21.4 Network Protocols: GATE CSE 2016 Set 1 | Question: 24 top



Which one of the following protocols is **NOT** used to resolve one form of address to another one?

- A. DNS
- B. ARP
- C. DHCP
- D. RARP

gatecse-2016-set1 computer-networks network-protocols normal

[Answer key](#)

## 2.21.5 Network Protocols: GATE CSE 2019 | Question: 29 top



Suppose that in an IP-over-Ethernet network, a machine X wishes to find the MAC address of another machine Y in its subnet. Which one of the following techniques can be used for this?

- A. X sends an ARP request packet to the local gateway's IP address which then finds the MAC address of Y and sends to X
- B. X sends an ARP request packet to the local gateway's MAC address which then finds the MAC address of Y and sends to X
- C. X sends an ARP request packet with broadcast MAC address in its local subnet
- D. X sends an ARP request packet with broadcast IP address in its local subnet

gatecse-2019 computer-networks network-protocols 2-marks

[Answer key](#)

## 2.21.6 Network Protocols: GATE CSE 2021 Set 1 | Question: 49 top



Consider the sliding window flow-control protocol operating between a sender and a receiver over a full-duplex error-free link. Assume the following:

- The time taken for processing the data frame by the receiver is negligible.
- The time taken for processing the acknowledgement frame by the sender is negligible.
- The sender has infinite number of frames available for transmission.
- The size of the data frame is 2,000 bits and the size of the acknowledgement frame is 10 bits.

- The link data rate in each direction is 1 Mbps ( $= 10^6$  bits per second).
- One way propagation delay of the link is 100 milliseconds.

The minimum value of the sender's window size in terms of the number of frames, (rounded to the nearest integer) needed to achieve a link utilization of 50% is \_\_\_\_\_.

gatecse-2021-set1 computer-networks network-protocols sliding-window numerical-answers 2-marks

[Answer key](#)



### 2.21.7 Network Protocols: GATE CSE 2021 Set 1 | Question: 8 [top](#)

Consider the following two statements.

- $S_1$ : Destination MAC address of an ARP reply is a broadcast address.
- $S_2$ : Destination MAC address of an ARP request is a broadcast address.

Which one of the following choices is correct?

- |                                     |                                     |
|-------------------------------------|-------------------------------------|
| A. Both $S_1$ and $S_2$ are true    | B. $S_1$ is true and $S_2$ is false |
| C. $S_1$ is false and $S_2$ is true | D. Both $S_1$ and $S_2$ are false   |

gatecse-2021-set1 computer-networks network-protocols 1-mark

[Answer key](#)



### 2.21.8 Network Protocols: GATE IT 2007 | Question: 69 [top](#)

Consider the following clauses:

- Not inherently suitable for client authentication.
- Not a state sensitive protocol.
- Must be operated with more than one server.
- Suitable for structured message organization.
- May need two ports on the serve side for proper operation.

The option that has the maximum number of correct matches is

- A. IMAP-i; FTP-ii; HTTP-iii; DNS-iv; POP3-v
- B. FTP-i; POP3-ii; SMTP-iii; HTTP-iv; IMAP-v
- C. POP3-i; SMTP-ii; DNS-iii; IMAP-iv; HTTP-v
- D. SMTP-i; HTTP-ii; IMAP-iii; DNS-iv; FTP-v

gateit-2007 computer-networks network-protocols normal

[Answer key](#)



### 2.21.9 Network Protocols: GATE IT 2008 | Question: 68 [top](#)

Which of the following statements are TRUE?

- **S1**: TCP handles both congestion and flow control
- **S2**: UDP handles congestion but not flow control
- **S3**: Fast retransmit deals with congestion but not flow control
- **S4**: Slow start mechanism deals with both congestion and flow control

- |                                 |                                 |
|---------------------------------|---------------------------------|
| A. $S_1$ , $S_2$ and $S_3$ only | B. $S_1$ and $S_3$ only         |
| C. $S_3$ and $S_4$ only         | D. $S_1$ , $S_3$ and $S_4$ only |

gateit-2008 computer-networks network-protocols normal

[Answer key](#)

2.22

## Network Switching (4) [top](#)



### 2.22.1 Network Switching: GATE CSE 2005 | Question: 73 [top](#)

In a packet switching network, packets are routed from source to destination along a single path having two intermediate nodes. If the message size is 24 bytes and each packet contains a header of 3 bytes, then the

optimum packet size is:

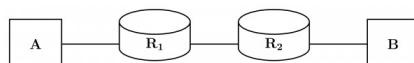
- A. 4      B. 6      C. 7      D. 9

gatecse-2005 computer-networks network-switching normal

[Answer key](#)

### 2.22.2 Network Switching: GATE CSE 2014 Set 2 | Question: 26 [top](#)

Consider the store and forward packet switched network given below. Assume that the bandwidth of each link is  $10^6$  bytes / sec. A user on host *A* sends a file of size  $10^3$  bytes to host *B* through routers *R<sub>1</sub>* and *R<sub>2</sub>* in three different ways. In the first case a single packet containing the complete file is transmitted from *A* to *B*. In the second case, the file is split into 10 equal parts, and these packets are transmitted from *A* to *B*. In the third case, the file is split into 20 equal parts and these packets are sent from *A* to *B*. Each packet contains 100 bytes of header information along with the user data. Consider only transmission time and ignore processing, queuing and propagation delays. Also assume that there are no errors during transmission. Let *T<sub>1</sub>*, *T<sub>2</sub>* and *T<sub>3</sub>* be the times taken to transmit the file in the first, second and third case respectively. Which one of the following is CORRECT?



- A.  $T_1 < T_2 < T_3$   
C.  $T_2 = T_3, T_3 < T_1$   
B.  $T_1 > T_2 > T_3$   
D.  $T_1 = T_3, T_3 > T_2$

gatecse-2014-set2 computer-networks network-switching normal

[Answer key](#)

### 2.22.3 Network Switching: GATE CSE 2015 Set 3 | Question: 36 [top](#)

Two hosts are connected via a packet switch with  $10^7$  bits per second links. Each link has a propagation delay of 20 microseconds. The switch begins forwarding a packet 35 microseconds after it receives the same. If 10000 bits of data are to be transmitted between the two hosts using a packet size of 5000 bits, the time elapsed between the transmission of the first bit of data and the reception of the last bit of the data in microseconds is \_\_\_\_\_.

gatecse-2015-set3 computer-networks normal numerical-answers network-switching

[Answer key](#)

### 2.22.4 Network Switching: GATE IT 2004 | Question: 22 [top](#)

Which one of the following statements is FALSE?

- A. Packet switching leads to better utilization of bandwidth resources than circuit switching  
B. Packet switching results in less variation in delay than circuit switching  
C. Packet switching requires more per-packet processing than circuit switching  
D. Packet switching can lead to reordering unlike in circuit switching

gateit-2004 computer-networks network-switching normal

[Answer key](#)

## 2.23

### Pure Aloha (1) [top](#)

#### 2.23.1 Pure Aloha: GATE CSE 2021 Set 2 | Question: 54 [top](#)

Consider a network using the pure ALOHA medium access control protocol, where each frame is of length 1,000 bits. The channel transmission rate is 1 Mbps ( $= 10^6$  bits per second). The aggregate number of transmissions across all the nodes (including new frame transmissions and retransmitted frames due to collisions) is modelled as a Poisson process with a rate of 1,000 frames per second. Throughput is defined as the average number of frames successfully transmitted per second. The throughput of the network (rounded to the nearest integer) is \_\_\_\_\_

gatecse-2021-set2 computer-networks mac-protocol pure-aloha numerical-answers 2-marks

[Answer key](#)

2.24

**Routers Bridge Hubs Switches (1)** top ↗**2.24.1 Routers Bridge Hubs Switches: GATE CSE 2004 | Question: 16** top ↗

Which of the following is NOT true with respect to a transparent bridge and a router?

- A. Both bridge and router selectively forward data packets
- B. A bridge uses IP addresses while a router uses MAC addresses
- C. A bridge builds up its routing table by inspecting incoming packets
- D. A router can connect between a LAN and a WAN

gatecse-2004 computer-networks routers-bridge-hubs-switches normal
**Answer key ↗**

2.25

**Routing (10)** top ↗**2.25.1 Routing: GATE CSE 2005 | Question: 26** top ↗

In a network of LANs connected by bridges, packets are sent from one LAN to another through intermediate bridges. Since more than one path may exist between two LANs, packets may have to be routed through multiple bridges. Why is the *spanning tree algorithm* used for bridge-routing?

- A. For shortest path routing between LANs
- B. For avoiding loops in the routing paths
- C. For fault tolerance
- D. For minimizing collisions

gatecse-2005 computer-networks routing normal
**Answer key ↗****2.25.2 Routing: GATE CSE 2014 Set 2 | Question: 23** top ↗

Which of the following is TRUE about the interior gateway routing protocols — Routing Information Protocol (*RIP*) and Open Shortest Path First (*OSPF*)

- A. RIP uses distance vector routing and OSPF uses link state routing
- B. OSPF uses distance vector routing and RIP uses link state routing
- C. Both RIP and OSPF use link state routing
- D. Both RIP and OSPF use distance vector routing

gatecse-2014-set2 computer-networks routing normal
**Answer key ↗****2.25.3 Routing: GATE CSE 2014 Set 3 | Question: 26** top ↗

An IP router implementing Classless Inter-domain Routing (CIDR) receives a packet with address 131.23.151.76. The router's routing table has the following entries:

<b>Prefix</b>	<b>Outer Interface Identifier</b>
131.16.0.0/12	3
131.28.0.0/14	5
131.19.0.0/16	2
131.22.0.0/15	1

The identifier of the output interface on which this packet will be forwarded is \_\_\_\_\_.

gatecse-2014-set3 computer-networks routing normal numerical-answers
**Answer key ↗**

#### 2.25.4 Routing: GATE CSE 2017 Set 2 | Question: 09 top



Consider the following statements about the routing protocols. Routing Information Protocol (RIP) and Open Shortest Path First (OSPF) in an IPv4 network.

- I. RIP uses distance vector routing
- II. RIP packets are sent using UDP
- III. OSPF packets are sent using TCP
- IV. OSPF operation is based on link-state routing

Which of the above statements are CORRECT?

- A. I and IV only
- B. I, II and III only
- C. I, II and IV only
- D. II, III and IV only

gatecse-2017-set2 computer-networks routing

[Answer key](#)

#### 2.25.5 Routing: GATE CSE 2020 | Question: 15 top



Consider the following statements about the functionality of an IP based router.

- I. A router does not modify the IP packets during forwarding.
- II. It is not necessary for a router to implement any routing protocol.
- III. A router should reassemble IP fragments if the MTU of the outgoing link is larger than the size of the incoming IP packet.

Which of the above statements is/are TRUE?

- |                    |            |
|--------------------|------------|
| A. I and II only   | B. I only  |
| C. II and III only | D. II only |

gatecse-2020 computer-networks routing 1-mark

[Answer key](#)

#### 2.25.6 Routing: GATE CSE 2023 | Question: 15 top



Which of the following statements is/are INCORRECT about the OSPF (Open Shortest Path First) routing protocol used in the Internet?

- A. OSPF implements Bellman-Ford algorithm to find shortest paths.
- B. OSPF uses Dijkstra's shortest path algorithm to implement least-cost path routing.
- C. OSPF is used as an inter-domain routing protocol.
- D. OSPF implements hierarchical routing.

gatecse-2023 computer-networks routing multiple-selects 1-mark

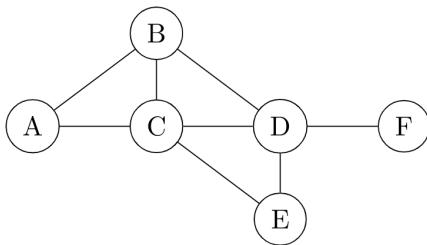
[Answer key](#)

#### 2.25.7 Routing: GATE IT 2005 | Question: 85a top



Consider a simple graph with unit edge costs. Each node in the graph represents a router. Each node maintains a routing table indicating the next hop router to be used to relay a packet to its destination and the cost of the path to the destination through that router. Initially, the routing table is empty. The routing table is synchronously updated as follows. In each updated interval, three tasks are performed.

- i. A node determines whether its neighbours in the graph are accessible. If so, it sets the tentative cost to each accessible neighbour as 1. Otherwise, the cost is set to  $\infty$ .
- ii. From each accessible neighbour, it gets the costs to relay to other nodes via that neighbour (as the next hop).
- iii. Each node updates its routing table based on the information received in the previous two steps by choosing the minimum cost.



For the graph given above, possible routing tables for various nodes after they have stabilized, are shown in the following options. Identify the correct table.

Table for node A		
A	B	C
-	-	-
B	B	1
C	C	1
D	B	3
E	C	3
F	C	4

gateit-2005 computer-networks routing normal

Table for node C		
A	B	C
A	A	1
B	B	1
C	-	-
D	D	1
E	E	1
F	E	3

B.

Table for node B		
A	B	C
A	A	1
B	-	-
C	C	1
D	D	1
E	C	2
F	D	2

C.

Table for node D		
A	B	C
A	B	3
B	B	1
C	C	1
D	-	-
E	E	1
F	F	1

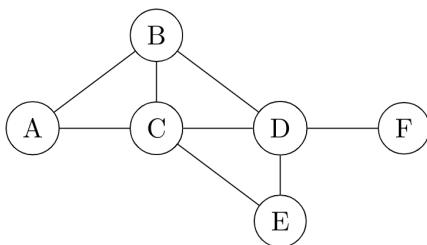
D.

Answer key

#### 2.25.8 Routing: GATE IT 2005 | Question: 85b

Consider a simple graph with unit edge costs. Each node in the graph represents a router. Each node maintains a routing table indicating the next hop router to be used to relay a packet to its destination and the cost of the path to the destination through that router. Initially, the routing table is empty. The routing table is synchronously updated as follows. In each updated interval, three tasks are performed.

- A node determines whether its neighbors in the graph are accessible. If so, it sets the tentative cost to each accessible neighbor as 1. Otherwise, the cost is set to  $\infty$ .
- From each accessible neighbor, it gets the costs to relay to other nodes via that neighbor (as the next hop).
- Each node updates its routing table based on the information received in the previous two steps by choosing the minimum cost.



Continuing from the earlier problem, suppose at some time  $t$ , when the costs have stabilized, node  $A$  goes down. The cost from node  $F$  to node  $A$  at time  $(t + 100)$  is :

- A.  $> 100$  but finite    B.  $\infty$     C. 3    D.  $> 3$  and  $\leq 100$

gateit-2005 computer-networks routing normal

Answer key

#### 2.25.9 Routing: GATE IT 2007 | Question: 63

A group of 15 routers is interconnected in a centralized complete binary tree with a router at each tree node. Router  $i$  communicates with router  $j$  by sending a message to the root of the tree. The root then sends the message back down to router  $j$ . The mean number of hops per message, assuming all possible router pairs are equally likely is

- A. 3    B. 4.26    C. 4.53    D. 5.26

gateit-2007 computer-networks routing binary-tree normal

Answer key 

#### 2.25.10 Routing: GATE IT 2008 | Question: 67



Two popular routing algorithms are Distance Vector(DV) and Link State (LS) routing. Which of the following are true?

- (S1): Count to infinity is a problem only with DV and not LS routing
- (S2): In LS, the shortest path algorithm is run only at one node
- (S3): In DV, the shortest path algorithm is run only at one node
- (S4): DV requires lesser number of network messages than LS

- A. S1, S2 and S4 only   B. S1, S3 and S4 only   C. S2 and S3 only   D. S1 and S4 only

gateit-2008 computer-networks routing normal

Answer key 

#### 2.26

#### Serial Communication (1)



#### 2.26.1 Serial Communication: GATE CSE 1992 | Question: 02,V

Start and stop bits do not contain any 'information' but are used in serial communication

- a. Error detection
- b. Error correction
- c. Synchronization
- d. Slowing down the communications

gate1992 easy computer-networks serial-communication multiple-selects

Answer key 

#### 2.27

#### Sliding Window (15)



#### 2.27.1 Sliding Window: GATE CSE 2003 | Question: 84

Host  $A$  is sending data to host  $B$  over a full duplex link.  $A$  and  $B$  are using the sliding window protocol for flow control. The send and receive window sizes are 5 packets each. Data packets (sent only from  $A$  to  $B$ ) are all 1000 bytes long and the transmission time for such a packet is  $50 \mu s$ . Acknowledgment packets (sent only from  $B$  to  $A$ ) are very small and require negligible transmission time. The propagation delay over the link is  $200 \mu s$ . What is the maximum achievable throughput in this communication?

- A.  $7.69 \times 10^6$  Bps
- B.  $11.11 \times 10^6$  Bps
- C.  $12.33 \times 10^6$  Bps
- D.  $15.00 \times 10^6$  Bps

gatecse-2003 computer-networks sliding-window normal

Answer key 

#### 2.27.2 Sliding Window: GATE CSE 2005 | Question: 25



The maximum window size for data transmission using the selective reject protocol with  $n$ -bit frame sequence numbers is:

- A.  $2^n$
- B.  $2^{n-1}$
- C.  $2^n - 1$
- D.  $2^{n-2}$

gatecse-2005 computer-networks sliding-window easy

Answer key 

#### 2.27.3 Sliding Window: GATE CSE 2006 | Question: 44



Station  $A$  uses 32 byte packets to transmit messages to Station  $B$  using a sliding window protocol. The round trip delay between  $A$  and  $B$  is 80 milliseconds and the bottleneck bandwidth on the path between  $A$  and  $B$  is 128 kbps. What is the optimal window size that  $A$  should use?

- A. 20
- B. 40
- C. 160
- D. 320

gatecse-2006 computer-networks sliding-window normal

Answer key 

#### 2.27.4 Sliding Window: GATE CSE 2006 | Question: 46 [top](#)



Station  $A$  needs to send a message consisting of 9 packets to Station  $B$  using a sliding window (window size 3) and go-back- $n$  error control strategy. All packets are ready and immediately available for transmission. If every 5th packet that  $A$  transmits gets lost (but no acks from  $B$  ever get lost), then what is the number of packets that  $A$  will transmit for sending the message to  $B$ ?

- A. 12      B. 14      C. 16      D. 18

gatecse-2006 computer-networks sliding-window normal

[Answer key](#)

#### 2.27.5 Sliding Window: GATE CSE 2007 | Question: 69 [top](#)



The distance between two stations  $M$  and  $N$  is  $L$  kilometers. All frames are  $K$  bits long. The propagation delay per kilometer is  $t$  seconds. Let  $R$  bits/second be the channel capacity. Assuming that the processing delay is negligible, the minimum number of bits for the sequence number field in a frame for maximum utilization, when the sliding window protocol is used, is:

- A.  $\lceil \log_2 \frac{2LtR+2K}{K} \rceil$   
B.  $\lceil \log_2 \frac{2LtR}{K} \rceil$   
C.  $\lceil \log_2 \frac{2LtR+K}{K} \rceil$   
D.  $\lceil \log_2 \frac{2LtR+2K}{2K} \rceil$

gatecse-2007 computer-networks sliding-window normal

[Answer key](#)

#### 2.27.6 Sliding Window: GATE CSE 2009 | Question: 57, ISRO2016-75 [top](#)



Frames of 1000 bits are sent over a  $10^6$  bps duplex link between two hosts. The propagation time is 25 ms. Frames are to be transmitted into this link to maximally pack them in transit (within the link).

What is the minimum number of bits ( $I$ ) that will be required to represent the sequence numbers distinctly? Assume that no time gap needs to be given between transmission of two frames.

- A.  $I = 2$       B.  $I = 3$       C.  $I = 4$       D.  $I = 5$

gatecse-2009 computer-networks sliding-window normal isro2016

[Answer key](#)

#### 2.27.7 Sliding Window: GATE CSE 2009 | Question: 58 [top](#)



Frames of 1000 bits are sent over a  $10^6$  bps duplex link between two hosts. The propagation time is 25ms. Frames are to be transmitted into this link to maximally pack them in transit (within the link).

Let  $I$  be the minimum number of bits ( $I$ ) that will be required to represent the sequence numbers distinctly assuming that no time gap needs to be given between transmission of two frames.

Suppose that the sliding window protocol is used with the sender window size of  $2^I$ , where  $I$  is the numbers of bits as mentioned earlier and acknowledgements are always piggy backed. After sending  $2^I$  frames, what is the minimum time the sender will have to wait before starting transmission of the next frame? (Identify the closest choice ignoring the frame processing time)

- A. 16ms      B. 18ms      C. 20ms      D. 22ms

gatecse-2009 computer-networks sliding-window normal

[Answer key](#)

#### 2.27.8 Sliding Window: GATE CSE 2014 Set 1 | Question: 28 [top](#)



Consider a selective repeat sliding window protocol that uses a frame size of 1 KB to send data on a 1.5 Mbps link with a one-way latency of 50 msec. To achieve a link utilization of 60%, the minimum number of bits required to represent the sequence number field is \_\_\_\_\_.

gatecse-2014-set1 computer-networks sliding-window numerical-answers normal

[Answer key](#)

### 2.27.9 Sliding Window: GATE CSE 2015 Set 3 | Question: 28 top



Consider a network connecting two systems located 8000 Km apart. The bandwidth of the network is  $500 \times 10^6$  bits per second. The propagation speed of the media is  $4 \times 10^8$  meters per second. It needs to design a Go-Back- $N$  sliding window protocol for this network. The average packet size is  $10^7$  bits. The network is to be used to its full capacity. Assume that processing delays at nodes are negligible. Then, the minimum size in bits of the sequence number field has to be \_\_\_\_\_.

gatecse-2015-set3 computer-networks sliding-window normal numerical-answers

[Answer key](#)

### 2.27.10 Sliding Window: GATE CSE 2016 Set 2 | Question: 55 top



Consider a  $128 \times 10^3$  bits/second satellite communication link with one way propagation delay of 150 milliseconds. Selective retransmission (repeat) protocol is used on this link to send data with a frame size of 1 kilobyte. Neglect the transmission time of acknowledgement. The minimum number of bits required for the sequence number field to achieve 100% utilization is \_\_\_\_\_.

gatecse-2016-set2 computer-networks sliding-window normal numerical-answers

[Answer key](#)

### 2.27.11 Sliding Window: GATE IT 2004 | Question: 81 top



In a sliding window ARQ scheme, the transmitter's window size is  $N$  and the receiver's window size is  $M$ . The minimum number of distinct sequence numbers required to ensure correct operation of the ARQ scheme is

- A.  $\min(M, N)$
- B.  $\max(M, N)$
- C.  $M + N$
- D.  $MN$

gateit-2004 computer-networks sliding-window normal

[Answer key](#)

### 2.27.12 Sliding Window: GATE IT 2004 | Question: 83 top



A 20 Kbps satellite link has a propagation delay of 400 ms. The transmitter employs the "go back  $n$  ARQ" scheme with  $n$  set to 10. Assuming that each frame is 100 byte long, what is the maximum data rate possible?

- A. 5 Kbps
- B. 10 Kbps
- C. 15 Kbps
- D. 20 Kbps

gateit-2004 computer-networks sliding-window normal

[Answer key](#)

### 2.27.13 Sliding Window: GATE IT 2004 | Question: 88 top



Suppose that the maximum transmit window size for a TCP connection is 12000 bytes. Each packet consists of 2000 bytes. At some point in time, the connection is in slow-start phase with a current transmit window of 4000 bytes. Subsequently, the transmitter receives two acknowledgments. Assume that no packets are lost and there are no time-outs. What is the maximum possible value of the current transmit window?

- A. 4000 bytes
- B. 8000 bytes
- C. 10000 bytes
- D. 12000 bytes

gateit-2004 computer-networks sliding-window normal

[Answer key](#)

### 2.27.14 Sliding Window: GATE IT 2006 | Question: 64 top



Suppose that it takes 1 unit of time to transmit a packet (of fixed size) on a communication link. The link layer uses a window flow control protocol with a window size of  $N$  packets. Each packet causes an ack or a nak to be generated by the receiver, and ack/nak transmission times are negligible. Further, the round trip time on the link is equal to  $N$  units. Consider time  $i > N$ . If only acks have been received till time  $i$  (no naks), then the goodput evaluated at the transmitter at time  $i$  (in packets per unit time) is

A.  $1 - \frac{N}{i}$

B.  $\frac{i}{(N+i)}$

C. 1

D.  $1 - e^{(\frac{i}{N})}$

gateit-2006 computer-networks sliding-window normal

Answer key 

#### 2.27.15 Sliding Window: GATE IT 2008 | Question: 64

A 1 Mbps satellite link connects two ground stations. The altitude of the satellite is 36,504 km and speed of the signal is  $3 \times 10^8$  m/s. What should be the packet size for a channel utilization of 25% for a satellite link using go-back-127 sliding window protocol? Assume that the acknowledgment packets are negligible in size and that there are no errors during communication.

- A. 120 bytes      B. 60 bytes      C. 240 bytes      D. 90 bytes

gateit-2008 computer-networks sliding-window normal

Answer key 

#### 2.28

#### Sockets (4)

#### 2.28.1 Sockets: GATE CSE 2008 | Question: 17

Which of the following system calls results in the sending of SYN packets?

- A. socket      B. bind      C. listen      D. connect

gatecse-2008 normal computer-networks sockets

Answer key 

#### 2.28.2 Sockets: GATE CSE 2008 | Question: 59

A client process P needs to make a TCP connection to a server process S. Consider the following situation: the server process S executes a `socket()`, a `bind()` and a `listen()` system call in that order, following which it is preempted. Subsequently, the client process P executes a `socket()` system call followed by `connect()` system call to connect to the server process S. The server process has not executed any `accept()` system call. Which one of the following events could take place?

- A. `connect()` system call returns successfully  
B. `connect()` system call blocks  
C. `connect()` system call returns an error  
D. `connect()` system call results in a core dump

gatecse-2008 computer-networks sockets normal

Answer key 

#### 2.28.3 Sockets: GATE CSE 2014 Set 2 | Question: 24

Which of the following socket API functions converts an unconnected active TCP socket into a passive socket?

- A. connect      B. bind      C. listen      D. accept

gatecse-2014-set2 computer-networks sockets easy

Answer key 

#### 2.28.4 Sockets: GATE CSE 2015 Set 2 | Question: 20

Identify the correct order in which a server process must invoke the function calls `accept`, `bind`, `listen`, and `recv` according to UNIX socket API.

- A. listen, accept, bind, recv
- C. bind, accept, listen, recv

- B. bind, listen, accept, recv
- D. accept, listen, bind, recv

gatecse-2015-set2 computer-networks sockets easy

[Answer key](#)

2.29

### Stop And Wait (6) top ↗

#### 2.29.1 Stop And Wait: GATE CSE 2015 Set 1 | Question: 53 top ↗



Suppose that the stop-and-wait protocol is used on a link with a bit rate of 64 kilobits per second and 20 milliseconds propagation delay. Assume that the transmission time for the acknowledgment and the processing time at nodes are negligible. Then the minimum frame size in bytes to achieve a link utilization of at least 50 % is \_\_\_\_\_.

gatecse-2015-set1 computer-networks stop-and-wait normal numerical-answers

[Answer key](#)

#### 2.29.2 Stop And Wait: GATE CSE 2016 Set 1 | Question: 55 top ↗



A sender uses the Stop-and-Wait ARQ protocol for reliable transmission of frames. Frames are of size 1000 bytes and the transmission rate at the sender is 80 Kbps ( $1\text{Kbps} = 1000 \text{ bits/second}$ ). Size of an acknowledgment is 100 bytes and the transmission rate at the receiver is 8 Kbps. The one-way propagation delay is 100 milliseconds.

Assuming no frame is lost, the sender throughput is \_\_\_\_\_ bytes/ second.

gatecse-2016-set1 computer-networks stop-and-wait normal numerical-answers

[Answer key](#)

#### 2.29.3 Stop And Wait: GATE CSE 2017 Set 1 | Question: 45 top ↗



The values of parameters for the Stop-and-Wait ARQ protocol are as given below:

- Bit rate of the transmission channel = 1 Mbps.
- Propagation delay from sender to receiver = 0.75 ms.
- Time to process a frame = 0.25 ms.
- Number of bytes in the information frame = 1980.
- Number of bytes in the acknowledge frame = 20.
- Number of overhead bytes in the information frame = 20.

Assume there are no transmission errors. Then, the transmission efficiency (expressed in percentage) of the Stop-and-Wait ARQ protocol for the above parameters is \_\_\_\_\_ (correct to 2 decimal places).

gatecse-2017-set1 computer-networks stop-and-wait numerical-answers normal

[Answer key](#)

#### 2.29.4 Stop And Wait: GATE CSE 2023 | Question: 7 top ↗



Suppose two hosts are connected by a point-to-point link and they are configured to use Stop-and-Wait protocol for reliable data transfer. Identify in which one of the following scenarios, the utilization of the link is the lowest.

- A. Longer link length and lower transmission rate
- B. Longer link length and higher transmission rate
- C. Shorter link length and lower transmission rate
- D. Shorter link length and higher transmission rate

gatecse-2023 computer-networks stop-and-wait 1-mark

[Answer key](#)

### 2.29.5 Stop And Wait: GATE IT 2005 | Question: 72 top



A channel has a bit rate of  $4 \text{ kbps}$  and one-way propagation delay of  $20 \text{ ms}$ . The channel uses stop and wait protocol. The transmission time of the acknowledgment frame is negligible. To get a channel efficiency of at least 50%, the minimum frame size should be

- A. 80 bytes      B. 80 bits      C. 160 bytes      D. 160 bits

gateit-2005 computer-networks stop-and-wait normal

[Answer key](#)

### 2.29.6 Stop And Wait: GATE IT 2006 | Question: 68 top



On a wireless link, the probability of packet error is 0.2. A stop-and-wait protocol is used to transfer data across the link. The channel condition is assumed to be independent of transmission to transmission. What is the average number of transmission attempts required to transfer 100 packets?

- A. 100      B. 125      C. 150      D. 200

gateit-2006 computer-networks sliding-window stop-and-wait normal

[Answer key](#)

## 2.30

### Subnetting (20) top



#### 2.30.1 Subnetting: GATE CSE 2003 | Question: 82, ISRO2009-1 top



The subnet mask for a particular network is 255.255.31.0. Which of the following pairs of IP addresses could belong to this network?

- A. 172.57.88.62 and 172.56.87.23      B. 10.35.28.2 and 10.35.29.4  
C. 191.203.31.87 and 191.234.31.88      D. 128.8.129.43 and 128.8.161.55

gatecse-2003 computer-networks subnetting normal isro2009

[Answer key](#)

#### 2.30.2 Subnetting: GATE CSE 2004 | Question: 55 top



The routing table of a router is shown below:

Destination	Subnet Mask	Interface
128.75.43.0	255.255.255.0	Eth0
128.75.43.0	255.255.255.128	Eth1
192.12.17.5	255.255.255.255	Eth3
Default		Eth2

On which interface will the router forward packets addressed to destinations 128.75.43.16 and 192.12.17.10 respectively?

- A. Eth1 and Eth2      B. Eth0 and Eth2      C. Eth0 and Eth3      D. Eth1 and Eth3

gatecse-2004 computer-networks subnetting normal

[Answer key](#)

#### 2.30.3 Subnetting: GATE CSE 2005 | Question: 27 top



An organization has a class *B* network and wishes to form subnets for 64 departments. The subnet mask would be:

- A. 255.255.0.0      B. 255.255.64.0      C. 255.255.128.0      D. 255.255.252.0

gatecse-2005 computer-networks subnetting normal

[Answer key](#)

#### 2.30.4 Subnetting: GATE CSE 2006 | Question: 45 top ↗

Two computers  $C_1$  and  $C_2$  are configured as follows.  $C_1$  has IP address 203.197.2.53 and netmask 255.255.128.0.  $C_2$  has IP address 203.197.75.201 and netmask 255.255.192.0. Which one of the following statements is true?

- A.  $C_1$  and  $C_2$  both assume they are on the same network
- B.  $C_2$  assumes  $C_1$  is on same network, but  $C_1$  assumes  $C_2$  is on a different network
- C.  $C_1$  assumes  $C_2$  is on same network, but  $C_2$  assumes  $C_1$  is on a different network
- D.  $C_1$  and  $C_2$  both assume they are on different networks.

gatecse-2006 computer-networks subnetting normal

[Answer key](#)

#### 2.30.5 Subnetting: GATE CSE 2007 | Question: 67, ISRO2016-72 top ↗

The address of a class B host is to be split into subnets with a 6-bit subnet number. What is the maximum number of subnets and the maximum number of hosts in each subnet?

- A. 62 subnets and 262142 hosts.
- B. 64 subnets and 262142 hosts.
- C. 62 subnets and 1022 hosts.
- D. 64 subnets and 1024 hosts.

gatecse-2007 computer-networks subnetting easy isro2016

[Answer key](#)

#### 2.30.6 Subnetting: GATE CSE 2008 | Question: 57 top ↗

If a class B network on the Internet has a subnet mask of 255.255.248.0, what is the maximum number of hosts per subnet?

- A. 1022
- B. 1023
- C. 2046
- D. 2047

gatecse-2008 computer-networks subnetting easy

[Answer key](#)

#### 2.30.7 Subnetting: GATE CSE 2010 | Question: 47 top ↗

Suppose computers  $A$  and  $B$  have IP addresses 10.105.1.113 and 10.105.1.91 respectively and they both use same netmask  $N$ . Which of the values of  $N$  given below should not be used if  $A$  and  $B$  should belong to the same network?

- A. 255.255.255.0
- B. 255.255.255.128
- C. 255.255.255.192
- D. 255.255.255.224

gatecse-2010 computer-networks subnetting easy

[Answer key](#)

#### 2.30.8 Subnetting: GATE CSE 2012 | Question: 34, ISRO-DEC2017-32 top ↗

An Internet Service Provider (ISP) has the following chunk of CIDR-based IP addresses available with it: 245.248.128.0/20. The ISP wants to give half of this chunk of addresses to Organization  $A$ , and a quarter to Organization  $B$ , while retaining the remaining with itself. Which of the following is a valid allocation of addresses to  $A$  and  $B$ ?

- A. 245.248.136.0/21 and 245.248.128.0/22
- B. 245.248.128.0/21 and 245.248.128.0/22
- C. 245.248.132.0/22 and 245.248.132.0/21
- D. 245.248.136.0/24 and 245.248.132.0/21

gatecse-2012 computer-networks subnetting normal isrodec2017

[Answer key](#)

### 2.30.9 Subnetting: GATE CSE 2015 Set 2 | Question: 41 top



Consider the following routing table at an IP router:

Network No	Net Mask	Next Hop
128.96.170.0	255.255.254.0	Interface 0
128.96.168.0	255.255.254.0	Interface 1
128.96.166.0	255.255.254.0	R2
128.96.164.0	255.255.252.0	R3
0.0.0.0	Default	R4

For each IP address in Group I Identify the correct choice of the next hop from Group II using the entries from the routing table above.

Group I	Group II
i) 128.96.171.92	a) Interface 0
ii) 128.96.167.151	b) Interface 1
iii) 128.96.163.151	c) R2
iv) 128.96.164.121	d) R3
	e) R4

- A. i-a, ii-c, iii-e, iv-d  
C. i-b, ii-c, iii-d, iv-e

- B. i-a, ii-d, iii-b, iv-e  
D. i-b, ii-c, iii-e, iv-d

gatecse-2015-set2 computer-networks subnetting easy

[Answer key](#)

### 2.30.10 Subnetting: GATE CSE 2015 Set 3 | Question: 38 top



In the network 200.10.11.144/27, the fourth octet (in decimal) of the last IP address of the network which can be assigned to a host is \_\_\_\_\_.

gatecse-2015-set3 computer-networks subnetting normal numerical-answers

[Answer key](#)

### 2.30.11 Subnetting: GATE CSE 2019 | Question: 28 top



Consider three machines M, N, and P with IP addresses 100.10.5.2, 100.10.5.5, and 100.10.5.6 respectively. The subnet mask is set to 255.255.255.252 for all the three machines. Which one of the following is true?

- A. M, N, and P all belong to the same subnet  
C. Only N and P belong to the same subnet
- B. Only M and N belong to the same subnet  
D. M, N, and P belong to three different subnets

gatecse-2019 computer-networks subnetting 2-marks

[Answer key](#)

### 2.30.12 Subnetting: GATE CSE 2020 | Question: 38 top



An organization requires a range of IP address to assign one to each of its 1500 computers. The organization has approached an Internet Service Provider (ISP) for this task. The ISP uses CIDR and serves the requests from the available IP address space 202.61.0.0/17. The ISP wants to assign an address space to the organization which will minimize the number of routing entries in the ISP's router using route aggregation. Which of the following address spaces are potential candidates from which the ISP can allot any one of the organization?

- I. 202.61.84.0/21

- II. 202.61.104.0/21
- III. 202.61.64.0/21
- IV. 202.61.144.0/21

- A. I and II only      B. II and III only      C. III and IV only      D. I and IV only

gatecse-2020 computer-networks subnetting 2-marks

[Answer key](#)



#### 2.30.13 Subnetting: GATE CSE 2022 | Question: 45 top

Consider routing table of an organization's router shown below:

Subnet Number	Subnet Mask	Next Hop
12.20.164.0	255.255.252.0	R1
12.20.170.0	255.255.254.0	R2
12.20.168.0	255.255.254.0	Interface 0
12.20.166.0	255.255.254.0	Interface 1
default		R3

Which of the following prefixes in CIDR notation can be collectively used to correctly aggregate all of the subnets in the routing table?

- A. 12.20.164.0/20      B. 12.20.164.0/22  
 C. 12.20.164.0/21      D. 12.20.168.0/22

gatecse-2022 computer-networks subnetting multiple-selects 2-marks

[Answer key](#)



#### 2.30.14 Subnetting: GATE CSE 2023 | Question: 55 top

The forwarding table of a router is shown below.

Subnet Number	Subnet Mask	Interface ID
200.150.0.0	255.255.0.0	1
200.150.64.0	255.255.224.0	2
200.150.68.0	255.255.255.0	3
200.150.68.64	255.255.255.224	4
Default		0

A packet addressed to a destination address 200.150.68.118 arrives at the router. It will be forwarded to the interface with ID \_\_\_\_\_.

gatecse-2023 computer-networks subnetting numerical-answers 2-marks

[Answer key](#)



#### 2.30.15 Subnetting: GATE IT 2004 | Question: 26 top

A subnet has been assigned a subnet mask of 255.255.255.192. What is the maximum number of hosts that can belong to this subnet?

- A. 14      B. 30      C. 62      D. 126

gateit-2004 computer-networks subnetting normal

[Answer key](#)



#### 2.30.16 Subnetting: GATE IT 2005 | Question: 76 top

A company has a class C network address of 204.204.204.0. It wishes to have three subnets, one with

100 hosts and two with 50 hosts each. Which one of the following options represents a feasible set of subnet address/subnet mask pairs?

- A. 204.204.204.128/255.255.255.192  
204.204.204.0/255.255.255.128  
204.204.204.64/255.255.255.128
- B. 204.204.204.0/255.255.255.192  
204.204.204.192/255.255.255.128  
204.204.204.64/255.255.255.128
- C. 204.204.204.128/255.255.255.128  
204.204.204.192/255.255.255.192  
204.204.204.224/255.255.255.192
- D. 204.204.204.128/255.255.255.128  
204.204.204.64/255.255.255.192  
204.204.204.0/255.255.255.192

gateit-2005 computer-networks subnetting normal

[Answer key](#)

#### 2.30.17 Subnetting: GATE IT 2006 | Question: 63, ISRO2015-57 [top](#)

A router uses the following routing table:

Destination	Mask	Interface
144.16.0.0	255.255.0.0	eth0
144.16.64.0	255.255.224.0	eth1
144.16.68.0	255.255.255.0	eth2
144.16.68.64	255.255.255.224	eth3

Packet bearing a destination address 144.16.68.117 arrives at the router. On which interface will it be forwarded?

- A. eth0
- B. eth1
- C. eth2
- D. eth3

gateit-2006 computer-networks subnetting normal isro2015

[Answer key](#)

#### 2.30.18 Subnetting: GATE IT 2006 | Question: 70 [top](#)

A subnetted Class B network has the following broadcast address: 144.16.95.255

Its subnet mask

- A. is necessarily 255.255.224.0
- B. is necessarily 255.255.240.0
- C. is necessarily 255.255.248.0
- D. could be any one of 255.255.224.0, 255.255.240.0, 255.255.248.0

gateit-2006 computer-networks subnetting normal

[Answer key](#)

#### 2.30.19 Subnetting: GATE IT 2008 | Question: 84 [top](#)

Host X has IP address 192.168.1.97 and is connected through two routers R1 and R2 to another host Y with IP address 192.168.1.80. Router R1 has IP addresses 192.168.1.135 and 192.168.1.110. R2 has IP addresses 192.168.1.67 and 192.168.1.155. The netmask used in the network is 255.255.255.224.

Given the information above, how many distinct subnets are guaranteed to already exist in the network?

- A. 1
- B. 2
- C. 3
- D. 6

gateit-2008 computer-networks subnetting normal

[Answer key](#)

### 2.30.20 Subnetting: GATE IT 2008 | Question: 85 [top](#)



Host  $X$  has  $IP$  address 192.168.1.97 and is connected through two routers  $R1$  and  $R2$  to another host  $Y$  with  $IP$  address 192.168.1.80. Router  $R1$  has  $IP$  addresses 192.168.1.135 and 192.168.1.110.  $R2$  has  $IP$  addresses 192.168.1.67 and 192.168.1.155. The netmask used in the network is 255.255.255.224.

Which  $IP$  address should  $X$  configure its gateway as?

- A. 192.168.1.67      B. 192.168.1.110  
 C. 192.168.1.135      D. 192.168.1.155

gateit-2008 computer-networks subnetting normal

[Answer key](#)

2.31

Tcp (19) [top](#)



### 2.31.1 Tcp: GATE CSE 2009 | Question: 47 [top](#)

While opening a  $TCP$  connection, the initial sequence number is to be derived using a time-of-day (ToD) clock that keeps running even when the host is down. The low order 32 bits of the counter of the ToD clock is to be used for the initial sequence numbers. The clock counter increments once per milliseconds. The maximum packet lifetime is given to be 64s.

Which one of the choices given below is closest to the minimum permissible rate at which sequence numbers used for packets of a connection can increase?

- A. 0.015/s      B. 0.064/s      C. 0.135/s      D. 0.327/s

gatecse-2009 computer-networks tcp difficult ambiguous

[Answer key](#)

### 2.31.2 Tcp: GATE CSE 2012 | Question: 22 [top](#)



Which of the following transport layer protocols is used to support electronic mail?

- A. SMTP      B. IP      C. TCP      D. UDP

gatecse-2012 computer-networks tcp easy

[Answer key](#)

### 2.31.3 Tcp: GATE CSE 2015 Set 1 | Question: 19 [top](#)



Suppose two hosts use a  $TCP$  connection to transfer a large file. Which of the following statements is/are FALSE with respect to the  $TCP$  connection?

- If the sequence number of a segment is  $m$ , then the sequence number of the subsequent segment is always  $m + 1$ .
- If the estimated round trip time at any given point of time is  $t$  sec, the value of the retransmission timeout is always set to greater than or equal to  $t$  sec.
- The size of the advertised window never changes during the course of the  $TCP$  connection.
- The number of unacknowledged bytes at the sender is always less than or equal to the advertised window.

- A. III only      B. I and III only      C. I and IV only      D. II and IV only

gatecse-2015-set1 computer-networks tcp normal

[Answer key](#)

### 2.31.4 Tcp: GATE CSE 2015 Set 2 | Question: 34 [top](#)



Assume that the bandwidth for a  $TCP$  connection is 1048560 bits/sec. Let  $\alpha$  be the value of RTT in milliseconds (rounded off to the nearest integer) after which the  $TCP$  window scale option is needed. Let  $\beta$  be the maximum possible window size with window scale option. Then the values of  $\alpha$  and  $\beta$  are

- A. 63 milliseconds,  $65535 \times 2^{14}$       B. 63 milliseconds,  $65535 \times 2^{16}$

C. 500 milliseconds,  $65535 \times 2^{14}$

D. 500 milliseconds,  $65535 \times 2^{16}$

gatecse-2015-set2 computer-networks difficult tcp

Answer key 

### 2.31.5 Tcp: GATE CSE 2015 Set 3 | Question: 22

Consider the following statements.

- I. TCP connections are full duplex
- II. TCP has no option for selective acknowledgement
- III. TCP connections are message streams

- A. Only I is correct
- C. Only II and III are correct

- B. Only I and III are correct
- D. All of I, II and III are correct

gatecse-2015-set3 computer-networks tcp normal

Answer key 

### 2.31.6 Tcp: GATE CSE 2016 Set 2 | Question: 25

Identify the correct sequence in which the following packets are transmitted on the network by a host when a browser requests a webpage from a remote server, assuming that the host has just been restarted.

- A. HTTP GET request, DNS query, TCP SYN
- C. DNS query, TCP SYN, HTTP GET request.
- B. DNS query, HTTP GET request, TCP SYN
- D. TCP SYN, DNS query, HTTP GET request.

gatecse-2016-set2 computer-networks normal tcp

Answer key 

### 2.31.7 Tcp: GATE CSE 2017 Set 1 | Question: 14

Consider a TCP client and a TCP server running on two different machines. After completing data transfer, the TCP client calls close to terminate the connection and a FIN segment is sent to the TCP server. Server-side TCP responds by sending an ACK, which is received by the client-side TCP. As per the TCP connection state diagram (RFC 793), in which state does the client-side TCP connection wait for the FIN from the server-side TCP?

- A. LAST-ACK
- B. TIME-WAIT
- C. FIN-WAIT-1
- D. FIN-WAIT-2

gatecse-2017-set1 computer-networks tcp

Answer key 

### 2.31.8 Tcp: GATE CSE 2018 | Question: 25

Consider a long-lived TCP session with an end-to-end bandwidth of 1 Gbps ( $= 10^9$  bits-per-second). The session starts with a sequence number of 1234. The minimum time (in seconds, rounded to the closest integer) before this sequence number can be used again is \_\_\_\_\_.

gatecse-2018 computer-networks tcp normal numerical-answers 1-mark

Answer key 

### 2.31.9 Tcp: GATE CSE 2020 | Question: 55

Consider a TCP connection between a client and a server with the following specifications; the round trip time is 6 ms, the size of the receiver advertised window is 50 KB, slow-start threshold at the client is 32 KB, and the maximum segment size is 2 KB. The connection is established at time  $t = 0$ . Assume that there are no timeouts and errors during transmission. Then the size of the congestion window (in KB) at time  $t + 60$  ms after all acknowledgements are processed is \_\_\_\_\_

gatecse-2020 numerical-answers computer-networks tcp 2-marks

Answer key 

### 2.31.10 Tcp: GATE CSE 2021 Set 1 | Question: 44 top



A TCP server application is programmed to listen on port number  $P$  on host  $S$ . A TCP client is connected to the TCP server over the network.

Consider that while the TCP connection was active, the server machine  $S$  crashed and rebooted. Assume that the client does not use the TCP keepalive timer. Which of the following behaviors is/are possible?

- A. If the client was waiting to receive a packet, it may wait indefinitely
- B. The TCP server application on  $S$  can listen on  $P$  after reboot
- C. If the client sends a packet after the server reboot, it will receive a RST segment
- D. If the client sends a packet after the server reboot, it will receive a FIN segment

gatecse-2021-set1 multiple-selects computer-networks tcp 2-marks

[Answer key](#)

### 2.31.11 Tcp: GATE CSE 2021 Set 1 | Question: 45 top



Consider two hosts  $P$  and  $Q$  connected through a router  $R$ . The maximum transfer unit (MTU) value of the link between  $P$  and  $R$  is 1500 bytes, and between  $R$  and  $Q$  is 820 bytes.

A TCP segment of size 1400 bytes was transferred from  $P$  to  $Q$  through  $R$ , with IP identification value as 0x1234. Assume that the IP header size is 20 bytes. Further, the packet is allowed to be fragmented, i.e., Don't Fragment (DF) flag in the IP header is *not* set by  $P$ .

Which of the following statements is/are correct?

- A. Two fragments are created at  $R$  and the IP datagram size carrying the second fragment is 620 bytes.
- B. If the second fragment is lost,  $R$  will resend the fragment with the IP identification value 0x1234.
- C. If the second fragment is lost,  $P$  is required to resend the whole TCP segment.
- D. TCP destination port can be determined by analysing *only* the second fragment.

gatecse-2021-set1 computer-networks tcp 2-marks multiple-selects

[Answer key](#)

### 2.31.12 Tcp: GATE CSE 2021 Set 2 | Question: 7 top



Consider the three-way handshake mechanism followed during TCP connection establishment between hosts  $P$  and  $Q$ . Let  $X$  and  $Y$  be two random 32-bit starting sequence numbers chosen by  $P$  and  $Q$  respectively. Suppose  $P$  sends a TCP connection request message to  $Q$  with a TCP segment having SYN bit = 1, SEQ number =  $X$ , and ACK bit = 0. Suppose  $Q$  accepts the connection request. Which one of the following choices represents the information present in the TCP segment header that is sent by  $Q$  to  $P$ ?

- A. SYN bit = 1, SEQ number =  $X + 1$ , ACK bit = 0, ACK number =  $Y$ , FIN bit = 0
- B. SYN bit = 0, SEQ number =  $X + 1$ , ACK bit = 0, ACK number =  $Y$ , FIN bit = 1
- C. SYN bit = 1, SEQ number =  $Y$ , ACK bit = 1, ACK number =  $X + 1$ , FIN bit = 0
- D. SYN bit = 1, SEQ number =  $Y$ , ACK bit = 1, ACK number =  $X$ , FIN bit = 0

gatecse-2021-set2 computer-networks tcp 1-mark

[Answer key](#)

### 2.31.13 Tcp: GATE CSE 2022 | Question: 50 top



Consider the data transfer using TCP over a 1 Gbps link. Assuming that the maximum segment lifetime (MSL) is set to 60 seconds, the minimum number of bits required for the sequence number field of the TCP header, to prevent the sequence number space from wrapping around during the MSL is \_\_\_\_\_.

gatecse-2022 numerical-answers computer-networks tcp 2-marks

[Answer key](#)

### 2.31.14 Tcp: GATE CSE 2023 | Question: 40 top



Suppose you are asked to design a new reliable byte-stream transport protocol like TCP. This protocol, named myTCP, runs over a 100 Mbps network with Round Trip Time of 150 milliseconds and the maximum segment lifetime of 2 minutes.

Which of the following is/are valid lengths of the **Sequence Number** field in the myTCP header?

- A. 30 bits      B. 32 bits      C. 34 bits      D. 36 bits

gatecse-2023 computer-networks tcp multiple-selects 2-marks

**Answer key**

### 2.31.15 Tcp: GATE IT 2004 | Question: 23 top



Which one of the following statements is FALSE?

- A. TCP guarantees a minimum communication rate  
B. TCP ensures in-order delivery  
C. TCP reacts to congestion by reducing sender window size  
D. TCP employs retransmission to compensate for packet loss

gateit-2004 computer-networks tcp normal

**Answer key**

### 2.31.16 Tcp: GATE IT 2004 | Question: 28 top



In TCP, a unique sequence number is assigned to each

- A. byte      B. word      C. segment      D. message

gateit-2004 computer-networks tcp normal

**Answer key**

### 2.31.17 Tcp: GATE IT 2007 | Question: 13 top



Consider the following statements about the timeout value used in TCP.

- The timeout value is set to the RTT (Round Trip Time) measured during TCP connection establishment for the entire duration of the connection.
- Appropriate RTT estimation algorithm is used to set the timeout value of a TCP connection.
- Timeout value is set to twice the propagation delay from the sender to the receiver.

Which of the following choices hold?

- A. (i) is false, but (ii) and (iii) are true  
C. (i) and (ii) are false, but (iii) is true  
B. (i) and (iii) are false, but (ii) is true  
D. (i), (ii) and (iii) are false

gateit-2007 computer-networks tcp normal

**Answer key**

### 2.31.18 Tcp: GATE IT 2007 | Question: 14 top



Consider a *TCP* connection in a state where there are no outstanding *ACKs*. The sender sends two segments back to back. The sequence numbers of the first and second segments are 230 and 290 respectively. The first segment was lost, but the second segment was received correctly by the receiver. Let *X* be the amount of data carried in the first segment (in bytes), and *Y* be the *ACK* number sent by the receiver. The values of *X* and *Y* (in that order) are

- A. 60 and 290      B. 230 and 291      C. 60 and 231      D. 60 and 230

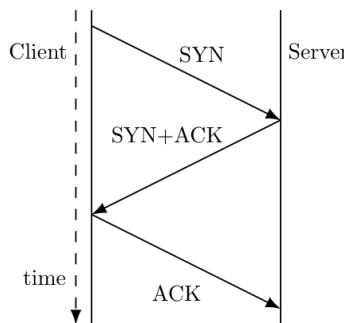
gateit-2007 computer-networks tcp normal

**Answer key**

### 2.31.19 Tcp: GATE IT 2008 | Question: 69 [top](#)



The three way handshake for TCP connection establishment is shown below.



Which of the following statements are TRUE?

- S1 : Loss of SYN + ACK from the server will not establish a connection  
S2 : Loss of ACK from the client cannot establish the connection  
S3 : The server moves LISTEN → SYN\_RECV → SYN\_SENT → ESTABLISHED in the state machine on no packet loss  
S4 : The server moves LISTEN → SYN\_RECV → ESTABLISHED in the state machine on no packet loss

- A. S2 and S3 only    B. S1 and S4 only    C. S1 and S3 only    D. S2 and S4 only

gateit-2008 computer-networks tcp normal

[Answer key](#)

### 2.32

### Token Bucket (2) [top](#)



### 2.32.1 Token Bucket: GATE CSE 2008 | Question: 58 [top](#)

A computer on a 10Mbps network is regulated by a token bucket. The token bucket is filled at a rate of 2Mbps. It is initially filled to capacity with 16Megabits. What is the maximum duration for which the computer can transmit at the full 10Mbps?

- A. 1.6 seconds    B. 2 seconds    C. 5 seconds    D. 8 seconds

gatecse-2008 computer-networks token-bucket

[Answer key](#)

### 2.32.2 Token Bucket: GATE CSE 2016 Set 1 | Question: 54 [top](#)



For a host machine that uses the token bucket algorithm for congestion control, the token bucket has a capacity of 1 megabyte and the maximum output rate is 20 megabytes per second. Tokens arrive at a rate to sustain output at a rate of 10 megabytes per second. The token bucket is currently full and the machine needs to send 12 megabytes of data. The minimum time required to transmit the data is \_\_\_\_\_ seconds.

gatecse-2016-set1 computer-networks token-bucket normal numerical-answers

[Answer key](#)

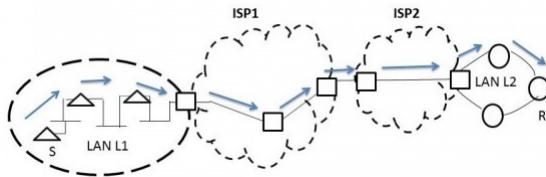
### 2.33

### Token Ring (1) [top](#)



### 2.33.1 Token Ring: GATE CSE 2014 Set 2 | Question: 25 [top](#)

In the diagram shown below,  $L_1$  is an Ethernet LAN and  $L_2$  is a Token-Ring LAN. An IP packet originates from sender  $S$  and traverses to  $R$ , as shown. The links within each ISP and across the two ISPs, are all point-to-point optical links. The initial value of the TTL field is 32. The maximum possible value of the TTL field when  $R$  receives the datagram is \_\_\_\_\_.



gatecse-2014-set2 computer-networks numerical-answers lan-technologies ethernet token-ring normal

[Answer key](#)

2.34

Udp (4) [top](#)

#### 2.34.1 Udp: GATE CSE 2005 | Question: 23 [top](#)



Packets of the same session may be routed through different paths in:

- A. TCP, but not UDP
- B. TCP and UDP
- C. UDP, but not TCP
- D. Neither TCP nor UDP

gatecse-2005 computer-networks tcp udp easy

[Answer key](#)



#### 2.34.2 Udp: GATE CSE 2013 | Question: 12 [top](#)



The transport layer protocols used for real time multimedia, file transfer, DNS and email, respectively are

- A. TCP, UDP, UDP and TCP
- B. UDP, TCP, TCP and UDP
- C. UDP, TCP, UDP and TCP
- D. TCP, UDP, TCP and UDP

gatecse-2013 computer-networks tcp udp easy

[Answer key](#)



#### 2.34.3 Udp: GATE CSE 2017 Set 2 | Question: 18 [top](#)



Consider socket API on a Linux machine that supports connected UDP sockets. A connected UDP socket is a UDP socket on which connect function has already been called. Which of the following statements is/are CORRECT?

- I. A connected UDP socket can be used to communicate with multiple peers simultaneously.
- II. A process can successfully call connect function again for an already connected UDP socket.
- A. I only
- B. II only
- C. Both I and II
- D. Neither I nor II

gatecse-2017-set2 computer-networks udp

[Answer key](#)



#### 2.34.4 Udp: GATE IT 2006 | Question: 69 [top](#)



A program on machine  $X$  attempts to open a  $UDP$  connection to port 5376 on a machine  $Y$ , and a  $TCP$  connection to port 8632 on machine  $Z$ . However, there are no applications listening at the corresponding ports on  $Y$  and  $Z$ . An  $ICMP$  Port Unreachable error will be generated by

- A.  $Y$  but not  $Z$
- B.  $Z$  but not  $Y$
- C. Neither  $Y$  nor  $Z$
- D. Both  $Y$  and  $Z$

gateit-2006 computer-networks tcp udp normal

[Answer key](#)

2.35

Wifi (1) [top](#)

#### 2.35.1 Wifi: GATE CSE 2016 Set 2 | Question: 54 [top](#)



For the IEEE 802.11 MAC protocol for wireless communication, which of the following statements is/are TRUE?

- I. At least three non-overlapping channels are available for transmissions.

- II. The RTS-CTS mechanism is used for collision detection.  
 III. Unicast frames are ACKed.

A. All I, II, and III      B. I and III only      C. II and III only      D. II only

gatecse-2016-set2 computer-networks wifi normal

**Answer key**

## Answer Keys

2.0.1	4	2.0.2	7.07:7.09	2.1.1	A	2.1.2	C	2.1.3	C
2.1.4	C	2.1.5	B	2.1.6	6	2.1.7	B	2.1.8	C
2.1.9	D	2.1.10	C	2.2.1	A	2.2.2	A	2.3.2	B
2.3.3	B	2.4.1	D	2.4.2	C	2.4.3	1100 : 1300	2.4.4	0.4404
2.4.5	C	2.4.6	50	2.4.7	B	2.5.1	B	2.5.2	C
2.5.3	C	2.5.4	A	2.6.1	D	2.6.2	200	2.6.3	C
2.6.4	A	2.6.5	B	2.7.1	C	2.7.2	B	2.7.3	A
2.7.4	C	2.7.5	B;C	2.7.6	0.5	2.7.7	B	2.7.8	A
2.8.1	3 : 4	2.8.2	A	2.8.3	C	2.8.4	B	2.8.5	A
2.8.6	B	2.8.7	C	2.8.8	N/A	2.9.1	B	2.9.2	B
2.9.3	D	2.9.4	C	2.9.5	C	2.10.1	Q-Q	2.11.1	N/A
2.12.1	A	2.13.1	C;D	2.14.1	D	2.14.2	D	2.14.3	B
2.14.4	C	2.14.5	C	2.14.6	256	2.14.7	9	2.15.1	C
2.15.2	D	2.15.3	D	2.15.4	A	2.15.5	B	2.15.6	C
2.15.8	D	2.16.1	D	2.16.2	A	2.16.3	3	2.16.4	D
2.17.1	D	2.18.1	D	2.18.2	12	2.18.3	B	2.18.4	C
2.19.1	N/A	2.19.2	D	2.19.3	D	2.19.4	C	2.19.5	A
2.20.1	D	2.20.2	A	2.20.3	B	2.20.4	C	2.20.5	B
2.20.6	C	2.21.1	D	2.21.2	C	2.21.3	A	2.21.4	C
2.21.5	C	2.21.6	50 : 52	2.21.7	C	2.21.8	D	2.21.9	B
2.22.3	1575	2.22.4	B	2.23.1	130 : 140	2.24.1	B	2.25.1	B
2.25.2	A	2.25.3	1	2.25.4	C	2.25.5	D	2.25.6	A;C
2.25.7	C	2.25.8	A	2.25.9	C	2.25.10	D	2.26.1	C
2.27.2	B	2.27.3	B	2.27.4	C	2.27.5	C	2.27.6	D
2.27.7	C	2.27.9	8	2.27.10	4	2.27.11	C	2.27.12	B
2.27.13	B	2.27.14	A	2.27.15	A	2.28.1	D	2.28.2	C
2.28.3	C	2.28.4	B	2.29.1	320	2.29.3	86.5 : 89.5	2.29.4	B
2.29.5	D	2.29.6	B	2.30.1	D	2.30.2	A	2.30.3	D
2.30.4	C	2.30.6	C	2.30.7	D	2.30.8	A	2.30.9	A
2.30.10	158	2.30.11	C	2.30.12	B	2.30.13	B;D	2.30.14	3
2.30.15	C	2.30.16	D	2.30.17	C	2.30.18	D	2.30.19	C
2.30.20	B	2.31.1	A	2.31.2	C	2.31.3	B	2.31.4	C

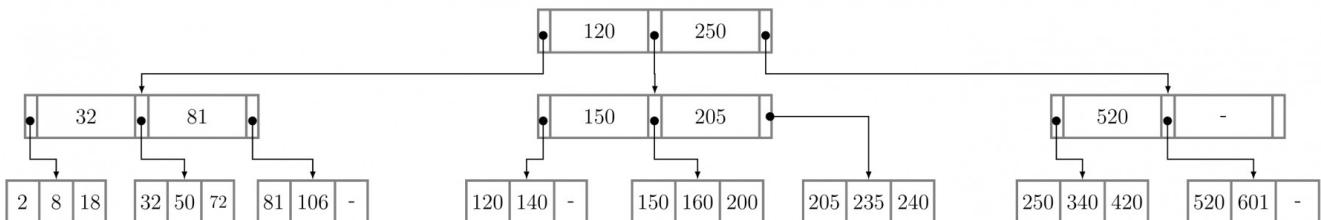
2.31.5	A	2.31.6	C	2.31.7	D	2.31.8	34 : 35	2.31.10	A;B;C
2.31.11	A;C	2.31.12	C	2.31.14	B;C;D	2.31.15	A	2.31.16	A
2.31.17	B	2.31.18	D	2.31.19	B	2.32.1	B	2.32.2	1.10:1.19
2.33.1	26	2.34.1	B	2.34.2	C	2.34.3	B	2.34.4	D
2.35.1	B								



## 3.1

B Tree (28) top ↗3.1.1 B Tree: GATE CSE 1989 | Question: 12a top ↗

The below figure shows a  $B^+$  tree where only key values are indicated in the records. Each block can hold upto three records. A record with a key value 34 is inserted into the  $B^+$  tree. Obtain the modified  $B^+$  tree after insertion.



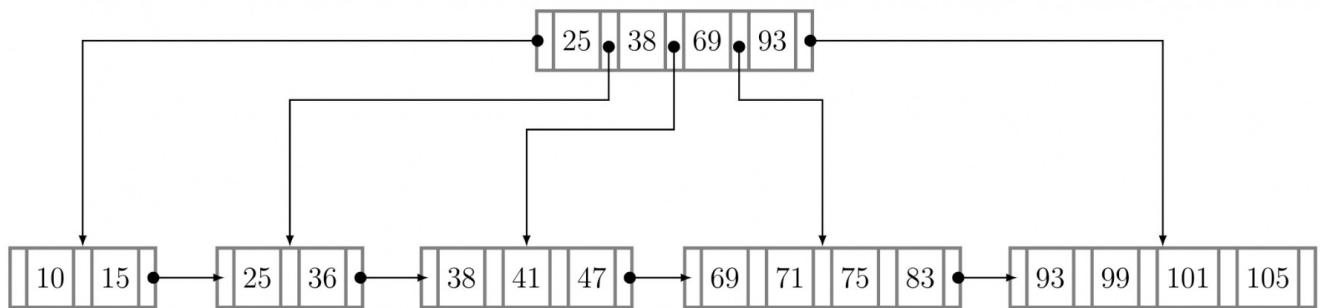
descriptive gate1989 databases b-tree

[Answer key ↗](#)

3.1.2 B Tree: GATE CSE 1994 | Question: 14a top ↗

Consider  $B^+$  - tree of order  $d$  shown in figure. (A  $B^+$  - tree of order  $d$  contains between  $d$  and  $2d$  keys in each node)

Draw the resulting  $B^+$  - tree after 100 is inserted in the figure below.



gate1994 databases b-tree normal descriptive

[Answer key ↗](#)

3.1.3 B Tree: GATE CSE 1994 | Question: 14b top ↗

For a  $B^+$  - tree of order  $d$  with  $n$  leaf nodes, the number of nodes accessed during a search is  $O(\_)$ .

gate1994 databases b-tree normal descriptive

[Answer key ↗](#)

3.1.4 B Tree: GATE CSE 1997 | Question: 19 top ↗

A  $B^+$  - tree of order  $d$  is a tree in which each internal node has between  $d$  and  $2d$  key values. An internal node with  $M$  key values has  $M + 1$  children. The root (if it is an internal node) has between 1 and  $2d$  key values. The distance of a node from the root is the length of the path from the root to the node. All leaves are at the same distance from the root. The height of the tree is the distance of a leaf from the root.

- What is the total number of key values in the internal nodes of a  $B^+$ -tree with  $l$  leaves ( $l \geq 2$ )?
- What is the maximum number of internal nodes in a  $B^+$  - tree of order 4 with 52 leaves?
- What is the minimum number of leaves in a  $B^+$ -tree of order  $d$  and height  $h$  ( $h \geq 1$ )?



**Answer key****3.1.5 B Tree: GATE CSE 1999 | Question: 1.25**

Which of the following is correct?

- A. B-trees are for storing data on disk and  $B^+$  trees are for main memory.
- B. Range queries are faster on  $B^+$  trees.
- C. B-trees are for primary indexes and  $B^+$  trees are for secondary indexes.
- D. The height of a  $B^+$  tree is independent of the number of records.

**Answer key****3.1.6 B Tree: GATE CSE 1999 | Question: 21**

Consider a B-tree with degree  $m$ , that is, the number of children,  $c$ , of any internal node (except the root) is such that  $m \leq c \leq 2m - 1$ . Derive the maximum and minimum number of records in the leaf nodes for such a B-tree with height  $h$ ,  $h \geq 1$ . (Assume that the root of a tree is at height 0).

**Answer key****3.1.7 B Tree: GATE CSE 2000 | Question: 1.22, UGCNET-June2012-II: 11** $B^+$ -trees are preferred to binary trees in databases because

- A. Disk capacities are greater than memory capacities
- B. Disk access is much slower than memory access
- C. Disk data transfer rates are much less than memory data transfer rates
- D. Disks are more reliable than memory

**Answer key****3.1.8 B Tree: GATE CSE 2000 | Question: 21**

(a) Suppose you are given an empty  $B^+$  tree where each node (leaf and internal) can store up to 5 key values. Suppose values  $1, 2, \dots, 10$  are inserted, in order, into the tree. Show the tree pictorially

- i. after 6 insertions, and
- ii. after all 10 insertions

Do NOT show intermediate stages.

(b) Suppose instead of splitting a node when it is full, we try to move a value to the left sibling. If there is no left sibling, or the left sibling is full, we split the node. Show the tree after values  $1, 2, \dots, 9$  have been inserted. Assume, as in (a) that each node can hold up to 5 keys.

(c) In general, suppose a  $B^+$  tree node can hold a maximum of  $m$  keys, and you insert a long sequence of keys in increasing order. Then what approximately is the average number of keys in each leaf level node.

- i. in the normal case, and
- ii. with the insertion as in (b).

**Answer key**

### 3.1.9 B Tree: GATE CSE 2001 | Question: 22 top



We wish to construct a  $B^+$  tree with fan-out (the number of pointers per node) equal to 3 for the following set of key values:

80, 50, 10, 70, 30, 100, 90

Assume that the tree is initially empty and the values are added in the order given.

- Show the tree after insertion of 10, after insertion of 30, and after insertion of 90. Intermediate trees need not be shown.
- The key values 30 and 10 are now deleted from the tree in that order show the tree after each deletion.

gatecse-2001 databases b-tree normal descriptive

Answer key

### 3.1.10 B Tree: GATE CSE 2002 | Question: 17 top



- The following table refers to search items for a key in  $B$ -trees and  $B^+$  trees.

B-tree		$B^+$ -tree	
Successful search	Unsuccessful search	Successful search	Unsuccessful search
$X_1$	$X_2$	$X_3$	$X_4$

A successful search means that the key exists in the database and unsuccessful means that it is not present in the database. Each of the entries  $X_1, X_2, X_3$  and  $X_4$  can have a value of either Constant or Variable. Constant means that the search time is the same, independent of the specific key value, where variable means that it is dependent on the specific key value chosen for the search.

Give the correct values for the entries  $X_1, X_2, X_3$  and  $X_4$  (for example  $X_1 = \text{Constant}$ ,  $X_2 = \text{Constant}$ ,  $X_3 = \text{Constant}$ ,  $X_4 = \text{Constant}$ )

- Relation  $R(A, B)$  has the following view defined on it:

```
CREATE VIEW V AS
(SELECT R1.A,R2.B
FROM R AS R1, R AS R2
WHERE R1.B=R2.A)
```

- The current contents of relation  $R$  are shown below. What are the contents of the view  $V$ ?

A	B
1	2
2	3
2	4
4	5
6	7
6	8
9	10

- The tuples  $(2, 11)$  and  $(11, 6)$  are now inserted into  $R$ . What are the additional tuples that are inserted in  $V$ ?

gatecse-2002 databases b-tree normal descriptive

Answer key

### 3.1.11 B Tree: GATE CSE 2002 | Question: 2.23, UGCNET-June2012-II: 26 [top](#)



A  $B^+$  - tree index is to be built on the *Name* attribute of the relation *STUDENT*. Assume that all the student names are of length 8 bytes, disk blocks are of size 512 bytes, and index pointers are of size 4 bytes. Given the scenario, what would be the best choice of the degree (i.e. number of pointers per node) of the  $B^+$  - tree?

- A. 16      B. 42      C. 43      D. 44

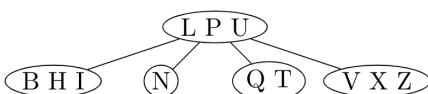
gatecse-2002 databases b-tree normal ugcnetcse-june2012-paper2

[Answer key](#)

### 3.1.12 B Tree: GATE CSE 2003 | Question: 65 [top](#)



Consider the following 2 – 3 – 4 tree (i.e., B-tree with a minimum degree of two) in which each data item is a letter. The usual alphabetical ordering of letters is used in constructing the tree.



What is the result of inserting *G* in the above tree?

- A.   
B.   
C.   
D. None of the above

gatecse-2003 databases b-tree normal

[Answer key](#)

### 3.1.13 B Tree: GATE CSE 2004 | Question: 52 [top](#)



The order of an internal node in a  $B^+$  tree index is the maximum number of children it can have. Suppose that a child pointer takes 6 bytes, the search field value takes 14 bytes, and the block size is 512 bytes. What is the order of the internal node?

- A. 24      B. 25      C. 26      D. 27

gatecse-2004 databases b-tree normal

[Answer key](#)

### 3.1.14 B Tree: GATE CSE 2005 | Question: 28 [top](#)



Which of the following is a key factor for preferring  $B^+$ -trees to binary search trees for indexing database relations?

- A. Database relations have a large number of records  
B. Database relations are sorted on the primary key  
C.  $B^+$ -trees require less memory than binary search trees  
D. Data transfer from disks is in blocks

gatecse-2005 databases b-tree normal

[Answer key](#)

### 3.1.15 B Tree: GATE CSE 2007 | Question: 63, ISRO2016-59 [top](#)



The order of a leaf node in a  $B^+$  - tree is the maximum number of (value, data record pointer) pairs it can hold. Given that the block size is 1K bytes, data record pointer is 7 bytes long, the value field is 9 bytes long and a block pointer is 6 bytes long, what is the order of the leaf node?

A. 63

B. 64

C. 67

D. 68

gatecse-2007 databases b-tree normal isro2016

Answer key

### 3.1.16 B Tree: GATE CSE 2008 | Question: 41 top

A B-tree of order 4 is built from scratch by 10 successive insertions. What is the maximum number of node splitting operations that may take place?

A. 3

B. 4

C. 5

D. 6

gatecse-2008 databases b-tree normal

Answer key

### 3.1.17 B Tree: GATE CSE 2009 | Question: 44 top

The following key values are inserted into a  $B^+$ -tree in which order of the internal nodes is 3, and that of the leaf nodes is 2, in the sequence given below. The order of internal nodes is the maximum number of tree pointers in each node, and the order of leaf nodes is the maximum number of data items that can be stored in it. The  $B^+$ -tree is initially empty

10, 3, 6, 8, 4, 2, 1

The maximum number of times leaf nodes would get split up as a result of these insertions is

A. 2

B. 3

C. 4

D. 5

gatecse-2009 databases b-tree normal

Answer key

### 3.1.18 B Tree: GATE CSE 2010 | Question: 18 top

Consider a  $B^+$ -tree in which the maximum number of keys in a node is 5. What is the minimum number of keys in any non-root node?

A. 1

B. 2

C. 3

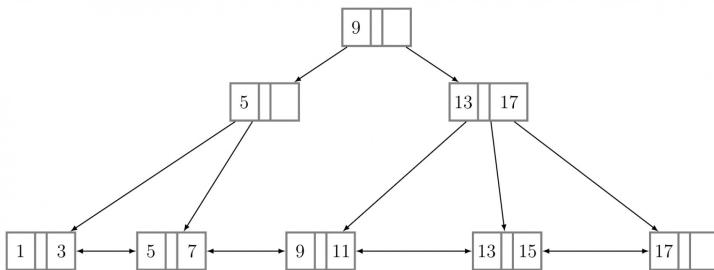
D. 4

gatecse-2010 databases b-tree easy

Answer key

### 3.1.19 B Tree: GATE CSE 2015 Set 2 | Question: 6 top

With reference to the  $B^+$ -tree index of order 1 shown below, the minimum number of nodes (including the Root node) that must be fetched in order to satisfy the following query. "Get all records with a search key greater than or equal to 7 and less than 15" is \_\_\_\_\_.



gatecse-2015-set2 databases b-tree normal numerical-answers

Answer key

### 3.1.20 B Tree: GATE CSE 2015 Set 3 | Question: 46 top

Consider a  $B^+$ -tree in which the search key is 12 bytes long, block size is 1024 bytes, record pointer is 10 bytes long and the block pointer is 8 bytes long. The maximum number of keys that can be accommodated in each non-leaf node of the tree is \_\_\_\_\_.

**Answer key****3.1.21 B Tree: GATE CSE 2016 Set 2 | Question: 21**

B+ Trees are considered BALANCED because.

- A. The lengths of the paths from the root to all leaf nodes are all equal.
- B. The lengths of the paths from the root to all leaf nodes differ from each other by at most 1.
- C. The number of children of any two non-leaf sibling nodes differ by at most 1.
- D. The number of records in any two leaf nodes differ by at most 1.

**Answer key****3.1.22 B Tree: GATE CSE 2017 Set 2 | Question: 49**

In a B+ Tree , if the search-key value is 8 bytes long , the block size is 512 bytes and the pointer size is 2 B , then the maximum order of the B+ Tree is \_\_\_\_\_

**Answer key****3.1.23 B Tree: GATE CSE 2019 | Question: 14**

Which one of the following statements is NOT correct about the B+ tree data structure used for creating an index of a relational database table?

- A. B+ Tree is a height-balanced tree
- B. Non-leaf nodes have pointers to data records
- C. Key values in each node are kept in sorted order
- D. Each leaf node has a pointer to the next leaf node

**Answer key****3.1.24 B Tree: GATE IT 2004 | Question: 79**

Consider a table  $T$  in a relational database with a key field  $K$ . A  $B$ -tree of order  $p$  is used as an access structure on  $K$ , where  $p$  denotes the maximum number of tree pointers in a B-tree index node. Assume that  $K$  is 10 bytes long; disk block size is 512 bytes; each data pointer  $P_D$  is 8 bytes long and each block pointer  $P_B$  is 5 bytes long. In order for each  $B$ -tree node to fit in a single disk block, the maximum value of  $p$  is

- A. 20
- B. 22
- C. 23
- D. 32

**Answer key****3.1.25 B Tree: GATE IT 2005 | Question: 23, ISRO2017-67**

A B-Tree used as an index for a large database table has four levels including the root node. If a new key is inserted in this index, then the maximum number of nodes that could be newly created in the process are

- A. 5
- B. 4
- C. 3
- D. 2

**Answer key****3.1.26 B Tree: GATE IT 2006 | Question: 61**

In a database file structure, the search key field is 9 bytes long, the block size is 512 bytes, a record pointer is 7 bytes and a block pointer is 6 bytes. The largest possible order of a non-leaf node in a  $B+$  tree

implementing this file structure is

- A. 23      B. 24      C. 34      D. 44

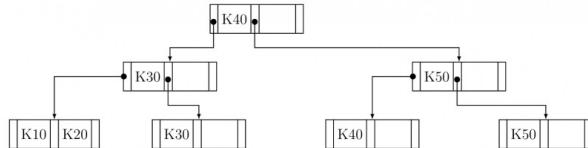
gateit-2006 databases b-tree normal

[Answer key](#)

### 3.1.27 B Tree: GATE IT 2007 | Question: 84 top ↗



Consider the  $B^+$  tree in the adjoining figure, where each node has at most two keys and three links.



Keys  $K_{15}$  and then  $K_{25}$  are inserted into this tree in that order. Exactly how many of the following nodes (disregarding the links) will be present in the tree after the two insertions?



- A. 1      B. 2      C. 3      D. 4

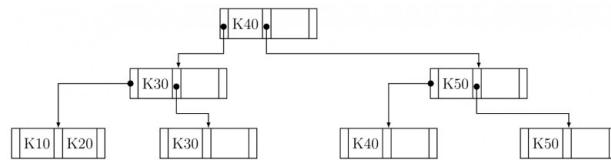
gateit-2007 databases b-tree normal

[Answer key](#)

### 3.1.28 B Tree: GATE IT 2007 | Question: 85 top ↗



Consider the  $B^+$  tree in the adjoining figure, where each node has at most two keys and three links.



Keys  $K_{15}$  and then  $K_{25}$  are inserted into this tree in that order. Now the key  $K_{50}$  is deleted from the  $B^+$  tree resulting after the two insertions made earlier. Consider the following statements about the  $B^+$  tree resulting after this deletion.

- The height of the tree remains the same.
- The node (disregarding the links) is present in the tree.
- The root node remains unchanged (disregarding the links).

Which one of the following options is true?

- A. Statements (i) and (ii) are true  
C. Statements (iii) and (i) are true
- B. Statements (ii) and (iii) are true  
D. All the statements are false

gateit-2007 databases b-tree normal

[Answer key](#)

## 3.2

### Candidate Key (5) top ↗



#### 3.2.1 Candidate Key: GATE CSE 1994 | Question: 3.7 top ↗

An instance of a relational scheme  $R(A, B, C)$  has distinct values for attribute  $A$ . Can you conclude that  $A$  is a candidate key for  $R$ ?

gate1994 databases easy database-normalization candidate-key descriptive

[Answer key](#)

### 3.2.2 Candidate Key: GATE CSE 2011 | Question: 12 top



Consider a relational table with a single record for each registered student with the following attributes:

1. **Registration\_Num:** Unique registration number for each registered student
2. **UID:** Unique identity number, unique at the national level for each citizen
3. **BankAccount\_Num:** Unique account number at the bank. A student can have multiple accounts or joint accounts. This attribute stores the primary account number.
4. **Name:** Name of the student
5. **Hostel\_Room:** Room number of the hostel

Which of the following options is **INCORRECT**?

- A. **BankAccount\_Num** is a candidate key
- B. **Registration\_Num** can be a primary key
- C. **UID** is a candidate key if all students are from the same country
- D. If  $S$  is a super key such that  $S \cap \text{UID}$  is NULL then  $S \cup \text{UID}$  is also a superkey

gatecse-2011 databases normal candidate-key

**Answer key**

### 3.2.3 Candidate Key: GATE CSE 2014 Set 2 | Question: 21 top



The maximum number of superkeys for the relation schema  $R(E, F, G, H)$  with  $E$  as the key is \_\_\_\_\_.

gatecse-2014-set2 databases numerical-answers easy candidate-key

**Answer key**

### 3.2.4 Candidate Key: GATE CSE 2014 Set 2 | Question: 22 top



Given an instance of the STUDENTS relation as shown as below

StudentID	StudentName	StudentEmail	StudentAge	CPI
2345	Shankar	shankar@math	X	9.4
1287	Swati	swati@ee	19	9.5
7853	Shankar	shankar@cse	19	9.4
9876	Swati	swati@mech	18	9.3
8765	Ganesh	ganesh@civil	19	8.7

For (StudentName, StudentAge) to be a key for this instance, the value  $X$  should NOT be equal to \_\_\_\_\_.

gatecse-2014-set2 databases numerical-answers easy candidate-key

**Answer key**

### 3.2.5 Candidate Key: GATE CSE 2014 Set 3 | Question: 22 top



A *prime attribute* of a relation scheme  $R$  is an attribute that appears

- A. in all candidate keys of  $R$
- C. in a foreign key of  $R$
- B. in some candidate key of  $R$
- D. only in the primary key of  $R$

gatecse-2014-set3 databases easy candidate-key

**Answer key**

## 3.3

### Conflict Serializable (4) top



#### 3.3.1 Conflict Serializable: GATE CSE 2017 Set 2 | Question: 44 top

Two transactions  $T_1$  and  $T_2$  are given as

$T_1 : r_1(X)w_1(X)r_1(Y)w_1(Y)$

$T_2 : r_2(Y)w_2(Y)r_2(Z)w_2(Z)$

where  $r_i(V)$  denotes a *read* operation by transaction  $T_i$  on a variable  $V$  and  $w_i(V)$  denotes a *write* operation by transaction  $T_i$  on a variable  $V$ . The total number of conflict serializable schedules that can be formed by  $T_1$  and  $T_2$  is \_\_\_\_\_

gatecse-2017-set2 databases transaction-and-concurrency numerical-answers conflict-serializable

Answer key 

### 3.3.2 Conflict Serializable: GATE CSE 2021 Set 1 | Question: 32 top

Let  $r_i(z)$  and  $w_i(z)$  denote read and write operations respectively on a data item  $z$  by a transaction  $T_i$ . Consider the following two schedules.

- $S_1 : r_1(x)r_1(y)r_2(x)r_2(y)w_2(y)w_1(x)$
- $S_2 : r_1(x)r_2(x)r_2(y)w_2(y)r_1(y)w_1(x)$

Which one of the following options is correct?

- A.  $S_1$  is conflict serializable, and  $S_2$  is not conflict serializable
- B.  $S_1$  is not conflict serializable, and  $S_2$  is conflict serializable
- C. Both  $S_1$  and  $S_2$  are conflict serializable
- D. Neither  $S_1$  nor  $S_2$  is conflict serializable

gatecse-2021-set1 databases transaction-and-concurrency conflict-serializable 2-marks

Answer key 

### 3.3.3 Conflict Serializable: GATE CSE 2021 Set 2 | Question: 32 top

Let  $S$  be the following schedule of operations of three transactions  $T_1$ ,  $T_2$  and  $T_3$  in a relational database system:

$R_2(Y), R_1(X), R_3(Z), R_1(Y)W_1(X), R_2(Z), W_2(Y), R_3(X), W_3(Z)$

Consider the statements  $P$  and  $Q$  below:

- $P$ :  $S$  is conflict-serializable.
- $Q$ : If  $T_3$  commits before  $T_1$  finishes, then  $S$  is recoverable.

Which one of the following choices is correct?

- A. Both  $P$  and  $Q$  are true
- B.  $P$  is true and  $Q$  is false
- C.  $P$  is false and  $Q$  is true
- D. Both  $P$  and  $Q$  are false

gatecse-2021-set2 databases transaction-and-concurrency conflict-serializable 2-marks

Answer key 

### 3.3.4 Conflict Serializable: GATE CSE 2022 | Question: 29 top

Let  $R_i(z)$  and  $W_i(z)$  denote read and write operations on a data element  $z$  by a transaction  $T_i$ , respectively. Consider the schedule  $S$  with four transactions.

$S : R_4(x)R_2(x)R_3(x)R_1(y)W_1(y)W_2(x)W_3(y)R_4(y)$

Which one of the following serial schedules is conflict equivalent to  $S$ ?

- A.  $T_1 \rightarrow T_3 \rightarrow T_4 \rightarrow T_2$
- B.  $T_1 \rightarrow T_4 \rightarrow T_3 \rightarrow T_2$
- C.  $T_4 \rightarrow T_1 \rightarrow T_3 \rightarrow T_2$
- D.  $T_3 \rightarrow T_1 \rightarrow T_4 \rightarrow T_2$

gatecse-2022 databases transaction-and-concurrency conflict-serializable 2-marks

Answer key 

**3.4****Data Independence (1)** top ↗**3.4.1 Data Independence: GATE CSE 1994 | Question: 3.11** top ↗

State True or False with reason

Logical data independence is easier to achieve than physical data independence.

gate1994 databases normal data-independence true-false

**Answer key** **3.5****Database Normalization (50)** top ↗**3.5.1 Database Normalization: GATE CSE 1987 | Question: 2n** top ↗

State whether the following statements are TRUE or FALSE:

A relation  $r$  with schema  $(X, Y)$  satisfies the function dependency  $X \rightarrow Y$ , The tuples  $\langle 1, 2 \rangle$  and  $\langle 2, 2 \rangle$  can both be in  $r$  simultaneously.

gate1987 databases database-normalization true-false

**Answer key** **3.5.2 Database Normalization: GATE CSE 1988 | Question: 12i** top ↗

What are the three axioms of functional dependency for the relational databases given by Armstrong.

gate1988 normal descriptive databases database-normalization

**Answer key** **3.5.3 Database Normalization: GATE CSE 1988 | Question: 12ii<sub>a</sub>** top ↗

Using Armstrong's axioms of functional dependency derive the following rules:

$$\{x \rightarrow y, x \rightarrow z\} \models x \rightarrow yz$$

(Note:  $x \rightarrow y$  denotes  $y$  is functionally dependent on  $x$ ,  $z \subseteq y$  denotes  $z$  is subset of  $y$ , and  $\models$  means derives).

gate1988 easy descriptive databases database-normalization

**Answer key** **3.5.4 Database Normalization: GATE CSE 1988 | Question: 12ii<sub>b</sub>** top ↗

Using Armstrong's axioms of functional dependency derive the following rules:

$$\{x \rightarrow y, wy \rightarrow z\} \models xw \rightarrow z$$

(Note:  $x \rightarrow y$  denotes  $y$  is functionally dependent on  $x$ ,  $z \subseteq y$  denotes  $z$  is subset of  $y$ , and  $\models$  means derives).

gate1988 normal descriptive databases database-normalization

**Answer key** **3.5.5 Database Normalization: GATE CSE 1988 | Question: 12ii<sub>c</sub>** top ↗

Using Armstrong's axioms of functional dependency derive the following rules:

$$\{x \rightarrow y, z \subset y\} \models x \rightarrow z$$

(Note:  $x \rightarrow y$  denotes  $y$  is functionally dependent on  $x$ ,  $z \subseteq y$  denotes  $z$  is subset of  $y$ , and  $\models$  means derives).

gate1988 normal descriptive databases database-normalization

**Answer key**

### 3.5.6 Database Normalization: GATE CSE 1990 | Question: 2-iv top



Match the pairs in the following questions:

(a) Secondary index	(p) Function dependency
(b) Non-procedural query language	(q) B-tree
(c) Closure of a set of attributes	(r) Domain calculus
(d) Natural join	(s) Relational algebraic operations

gate1990 match-the-following database-normalization databases

[Answer key](#)

### 3.5.7 Database Normalization: GATE CSE 1990 | Question: 3-ii top



Indicate which of the following statements are true:

- A relational database which is in 3NF may still have undesirable data redundancy because there may exist:
- A. Transitive functional dependencies
  - B. Non-trivial functional dependencies involving prime attributes on the right-side.
  - C. Non-trivial functional dependencies involving prime attributes only on the left-side.
  - D. Non-trivial functional dependencies involving only prime attributes.

gate1990 normal databases database-normalization multiple-selects

[Answer key](#)

### 3.5.8 Database Normalization: GATE CSE 1994 | Question: 3.6 top



State True or False with reason

There is always a decomposition into Boyce-Codd normal form (BCNF) that is lossless and dependency preserving.

gate1994 databases database-normalization easy true-false

[Answer key](#)

### 3.5.9 Database Normalization: GATE CSE 1995 | Question: 26 top



Consider the relation scheme  $R(A, B, C)$  with the following functional dependencies:

- $A, B \rightarrow C$ ,
- $C \rightarrow A$

- A. Show that the scheme  $R$  is in 3NF but not in BCNF.
- B. Determine the minimal keys of relation  $R$ .

gate1995 databases database-normalization normal descriptive

[Answer key](#)

### 3.5.10 Database Normalization: GATE CSE 1997 | Question: 6.9 top



For a database relation  $R(a, b, c, d)$ , where the domains  $a, b, c, d$  include only atomic values, only the following functional dependencies and those that can be inferred from them hold

- $a \rightarrow c$
- $b \rightarrow d$

This relation is

- A. in first normal form but not in second normal form
- B. in second normal form but not in first normal form
- C. in third normal form
- D. none of the above

**Answer key****3.5.11 Database Normalization: GATE CSE 1998 | Question: 1.34**

Which normal form is considered adequate for normal relational database design?

- A. 2NF      B. 5NF      C. 4NF      D. 3NF

**Answer key****3.5.12 Database Normalization: GATE CSE 1998 | Question: 26**

Consider the following database relations containing the attributes

- Book\_id
- Subject\_Category\_of\_book
- Name\_of\_Author
- Nationality\_of\_Author

With Book\_id as the primary key.

- What is the highest normal form satisfied by this relation?
- Suppose the attributes Book\_title and Author\_address are added to the relation, and the primary key is changed to {Name\_of\_Author, Book\_title}, what will be the highest normal form satisfied by the relation?

**Answer key****3.5.13 Database Normalization: GATE CSE 1999 | Question: 1.24**

Let  $R = (A, B, C, D, E, F)$  be a relation scheme with the following dependencies  $C \rightarrow F, E \rightarrow A, EC \rightarrow D, A \rightarrow B$ . Which one of the following is a key for  $R$ ?

- A. CD      B. EC      C. AE      D. AC

**Answer key****3.5.14 Database Normalization: GATE CSE 1999 | Question: 2.7, UGCNET-June2014-III: 25**

Consider the schema  $R = (S, T, U, V)$  and the dependencies  $S \rightarrow T, T \rightarrow U, U \rightarrow V$  and  $V \rightarrow S$ . Let  $R = (R1 \text{ and } R2)$  be a decomposition such that  $R1 \cap R2 \neq \emptyset$ . The decomposition is

- |                          |                        |
|--------------------------|------------------------|
| A. not in 2NF            | B. in 2NF but not 3NF  |
| C. in 3NF but not in 2NF | D. in both 2NF and 3NF |

**Answer key****3.5.15 Database Normalization: GATE CSE 2000 | Question: 2.24**

Given the following relation instance.

X	Y	Z
1	4	2
1	5	3
1	6	3
3	2	2

Which of the following functional dependencies are satisfied by the instance?

- A.  $XY \rightarrow Z$  and  $Z \rightarrow Y$
- C.  $YZ \rightarrow X$  and  $X \rightarrow Z$

- B.  $YZ \rightarrow X$  and  $Y \rightarrow Z$
- D.  $XZ \rightarrow Y$  and  $Y \rightarrow X$

gatecse-2000 databases database-normalization easy

Answer key 

### 3.5.16 Database Normalization: GATE CSE 2001 | Question: 2.23

$R(A, B, C, D)$  is a relation. Which of the following does not have a lossless join, dependency preserving  $BCNF$  decomposition?

- A.  $A \rightarrow B, B \rightarrow CD$
- C.  $AB \rightarrow C, C \rightarrow AD$

- B.  $A \rightarrow B, B \rightarrow C, C \rightarrow D$
- D.  $A \rightarrow BCD$

gatecse-2001 databases database-normalization normal

Answer key 

### 3.5.17 Database Normalization: GATE CSE 2002 | Question: 1.19

Relation  $R$  with an associated set of functional dependencies,  $F$ , is decomposed into  $BCNF$ . The redundancy (arising out of functional dependencies) in the resulting set of relations is

- A. Zero
- B. More than zero but less than that of an equivalent  $3NF$  decomposition
- C. Proportional to the size of  $F^+$
- D. Indeterminate

gatecse-2002 databases database-normalization normal

Answer key 

### 3.5.18 Database Normalization: GATE CSE 2002 | Question: 16

For relation  $R=(L, M, N, O, P)$ , the following dependencies hold:

$M \rightarrow O, NO \rightarrow P, P \rightarrow L$  and  $L \rightarrow MN$

$R$  is decomposed into  $R_1 = (L, M, N, P)$  and  $R_2 = (M, O)$ .

- A. Is the above decomposition a lossless-join decomposition? Explain.
- B. Is the above decomposition dependency-preserving? If not, list all the dependencies that are not preserved.
- C. What is the highest normal form satisfied by the above decomposition?

gatecse-2002 databases database-normalization normal descriptive

Answer key 

### 3.5.19 Database Normalization: GATE CSE 2002 | Question: 2.24

Relation  $R$  is decomposed using a set of functional dependencies,  $F$ , and relation  $S$  is decomposed using another set of functional dependencies,  $G$ . One decomposition is definitely  $BCNF$ , the other is definitely  $3NF$ , but it is not known which is which. To make a guaranteed identification, which one of the following tests should be used on the decompositions? (Assume that the closures of  $F$  and  $G$  are available).

- A. Dependency-preservation
- C.  $BCNF$  definition

- B. Lossless-join
- D.  $3NF$  definition

gatecse-2002 databases database-normalization easy

Answer key 

### 3.5.20 Database Normalization: GATE CSE 2002 | Question: 2.25

From the following instance of a relation schema  $R(A, B, C)$ , we can conclude that:

A	B	C
1	1	1
1	1	0
2	3	2
2	3	2

- A.  $A$  functionally determines  $B$  and  $B$  functionally determines  $C$   
 B.  $A$  functionally determines  $B$  and  $B$  does not functionally determine  $C$   
 C.  $B$  does not functionally determine  $C$   
 D.  $A$  does not functionally determine  $B$  and  $B$  does not functionally determine  $C$

gatecse-2002 databases database-normalization

[Answer key](#)



### 3.5.21 Database Normalization: GATE CSE 2003 | Question: 85 top

Consider the following functional dependencies in a database.

Date_of_Birth $\rightarrow$ Age	Age $\rightarrow$ Eligibility
Name $\rightarrow$ Roll_number	Roll_number $\rightarrow$ Name
Course_number $\rightarrow$ Course_name	Course_number $\rightarrow$ Instructor
(Roll_number, Course_number) $\rightarrow$ Grade	

The relation (Roll\_number, Name, Date\_of\_birth, Age) is

- A. in second normal form but not in third normal form  
 B. in third normal form but not in BCNF  
 C. in BCNF  
 D. in none of the above

gatecse-2003 databases database-normalization normal

[Answer key](#)



### 3.5.22 Database Normalization: GATE CSE 2004 | Question: 50 top

The relation scheme Student Performance (name, courseNo, rollNo, grade) has the following functional dependencies:

- name, courseNo,  $\rightarrow$  grade
- rollNo, courseNo  $\rightarrow$  grade
- name  $\rightarrow$  rollNo
- rollNo  $\rightarrow$  name

The highest normal form of this relation scheme is

- A. 2NF      B. 3NF      C. BCNF      D. 4NF

gatecse-2004 databases database-normalization normal

[Answer key](#)



### 3.5.23 Database Normalization: GATE CSE 2005 | Question: 29, UGCNET-June2015-III: 9 top

Which one of the following statements about normal forms is FALSE?

- A. BCNF is stricter than 3NF  
 B. Lossless, dependency-preserving decomposition into 3NF is always possible  
 C. Lossless, dependency-preserving decomposition into BCNF is always possible  
 D. Any relation with two attributes is in BCNF

gatecse-2005 databases database-normalization easy ugcnetcse-june2015-paper3

[Answer key](#)

### 3.5.24 Database Normalization: GATE CSE 2005 | Question: 78 [top](#)



Consider a relation scheme  $R = (A, B, C, D, E, H)$  on which the following functional dependencies hold:  $\{A \rightarrow B, BC \rightarrow D, E \rightarrow C, D \rightarrow A\}$ . What are the candidate keys R?

- A. AE, BE      B. AE, BE, DE      C. AEH, BEH, BCH    D. AEH, BEH, DEH

gatecse-2005 databases database-normalization easy

[Answer key](#)

### 3.5.25 Database Normalization: GATE CSE 2006 | Question: 70 [top](#)



The following functional dependencies are given:

$$AB \rightarrow CD, AF \rightarrow D, DE \rightarrow F, C \rightarrow G, F \rightarrow E, G \rightarrow A$$

Which one of the following options is false?

- A.  $\{CF\}^* = \{ACDEFG\}$       B.  $\{BG\}^* = \{ABCDG\}$   
 C.  $\{AF\}^* = \{ACDEFG\}$       D.  $\{AB\}^* = \{ABCDG\}$

gatecse-2006 databases database-normalization normal

[Answer key](#)

### 3.5.26 Database Normalization: GATE CSE 2007 | Question: 62, UGCNET-June2014-II: 47 [top](#)



Which one of the following statements is FALSE?

- A. Any relation with two attributes is in BCNF  
 B. A relation in which every key has only one attribute is in 2NF  
 C. A prime attribute can be transitively dependent on a key in a 3 NF relation  
 D. A prime attribute can be transitively dependent on a key in a BCNF relation

gatecse-2007 databases database-normalization normal ugcnetcse-june2014-paper2

[Answer key](#)

### 3.5.27 Database Normalization: GATE CSE 2008 | Question: 69 [top](#)



Consider the following relational schemes for a library database:

Book (Title, Author, Catalog\_no, Publisher, Year, Price)  
 Collection (Title, Author, Catalog\_no)

with the following functional dependencies:

- I. Title Author  $\rightarrow$  Catalog\_no
- II. Catalog\_no  $\rightarrow$  Title Author Publisher Year
- III. Publisher Title Year  $\rightarrow$  Price

Assume { Author, Title } is the key for both schemes. Which of the following statements is true?

- A. Both Book and Collection are in BCNF      B. Both Book and Collection are in 3NF only  
 C. Book is in 2NF and Collection in 3NF      D. Both Book and Collection are in 2NF only

gatecse-2008 databases database-normalization normal

[Answer key](#)

### 3.5.28 Database Normalization: GATE CSE 2012 | Question: 2 [top](#)



Which of the following is TRUE?

- A. Every relation in 3NF is also in BCNF

- B. A relation  $R$  is in 3NF if every non-prime attribute of  $R$  is fully functionally dependent on every key of  $R$   
 C. Every relation in BCNF is also in 3NF  
 D. No relation can be in both BCNF and 3NF

gatecse-2012 databases easy database-normalization

Answer key 

### 3.5.29 Database Normalization: GATE CSE 2013 | Question: 54 top



Relation  $R$  has eight attributes ABCDEFGH. Fields of  $R$  contain only atomic values.  $F = \{CH \rightarrow G, A \rightarrow BC, B \rightarrow CFH, E \rightarrow A, F \rightarrow EG\}$  is a set of functional dependencies ( $FDs$ ) so that  $F^+$  is exactly the set of  $FDs$  that hold for  $R$ .

How many candidate keys does the relation  $R$  have?

- A. 3      B. 4      C. 5      D. 6

gatecse-2013 databases database-normalization normal

Answer key 

### 3.5.30 Database Normalization: GATE CSE 2013 | Question: 55 top



Relation  $R$  has eight attributes ABCDEFGH. Fields of  $R$  contain only atomic values.  $F = \{CH \rightarrow G, A \rightarrow BC, B \rightarrow CFH, E \rightarrow A, F \rightarrow EG\}$  is a set of functional dependencies ( $FDs$ ) so that  $F^+$  is exactly the set of  $FDs$  that hold for  $R$ .

The relation  $R$  is

- A. in 1NF, but not in 2NF.  
 C. in 3NF, but not in BCNF.
- B. in 2NF, but not in 3NF.  
 D. in BCNF.

gatecse-2013 databases database-normalization normal

Answer key 

### 3.5.31 Database Normalization: GATE CSE 2014 Set 1 | Question: 21 top



Consider the relation scheme  $R = (E, F, G, H, I, J, K, L, M, N)$  and the set of functional dependencies

$$\{\{E, F\} \rightarrow \{G\}, \{F\} \rightarrow \{I, J\}, \{E, H\} \rightarrow \{K, L\}, \\ \{K\} \rightarrow \{M\}, \{L\} \rightarrow \{N\}\}$$

on  $R$ . What is the key for  $R$ ?

- A.  $\{E, F\}$       B.  $\{E, F, H\}$       C.  $\{E, F, H, K, L\}$       D.  $\{E\}$

gatecse-2014-set1 databases database-normalization normal

Answer key 

### 3.5.32 Database Normalization: GATE CSE 2014 Set 1 | Question: 30 top



Given the following two statements:

**S1:** Every table with two single-valued attributes is in 1NF, 2NF, 3NF and BCNF.

**S2:**  $AB \rightarrow C, D \rightarrow E, E \rightarrow C$  is a minimal cover for the set of functional dependencies  $AB \rightarrow C, D \rightarrow E, AB \rightarrow E, E \rightarrow C$ .

Which one of the following is **CORRECT**?

- A. S1 is TRUE and S2 is FALSE.  
 C. S1 is FALSE and S2 is TRUE.
- B. Both S1 and S2 are TRUE.  
 D. Both S1 and S2 are FALSE.

gatecse-2014-set1 databases database-normalization normal

Answer key 

### 3.5.33 Database Normalization: GATE CSE 2015 Set 3 | Question: 20 top



Consider the relation  $X(P, Q, R, S, T, U)$  with the following set of functional dependencies

$$F = \{$$
$$\{P, R\} \rightarrow \{S, T\},$$
$$\{P, S, U\} \rightarrow \{Q, R\}$$
$$\}$$

Which of the following is the trivial functional dependency in  $F^+$ , where  $F^+$  is closure to F?

- A.  $\{P, R\} \rightarrow \{S, T\}$       B.  $\{P, R\} \rightarrow \{R, T\}$   
C.  $\{P, S\} \rightarrow \{S\}$       D.  $\{P, S, U\} \rightarrow \{Q\}$

gatecse-2015-set3 databases database-normalization easy

Answer key

### 3.5.34 Database Normalization: GATE CSE 2016 Set 1 | Question: 21 top



Which of the following is NOT a superkey in a relational schema with attributes  $V, W, X, Y, Z$  and primary key  $V Y$ ?

- A.  $VXYZ$       B.  $VWXZ$       C.  $VWXY$       D.  $VWXYZ$

gatecse-2016-set1 databases database-normalization easy

Answer key

### 3.5.35 Database Normalization: GATE CSE 2016 Set 1 | Question: 23 top



A database of research articles in a journal uses the following schema.

(VOLUME, NUMBER, STARTPAGE, ENDPAGE, TITLE, YEAR, PRICE)

The primary key is '(VOLUME, NUMBER, STARTPAGE, ENDPAGE)

and the following functional dependencies exist in the schema.

- (VOLUME, NUMBER, STARTPAGE, ENDPAGE)  $\rightarrow$  TITLE  
(VOLUME, NUMBER)  $\rightarrow$  YEAR  
(VOLUME, NUMBER, STARTPAGE, ENDPAGE)  $\rightarrow$  PRICE

The database is redesigned to use the following schemas

(VOLUME, NUMBER, STARTPAGE, ENDPAGE, TITLE, PRICE)

(VOLUME, NUMBER, YEAR)

Which is the weakest normal form that the new database satisfies, but the old one does not?

- A. 1NF      B. 2NF      C. 3NF      D. BCNF

gatecse-2016-set1 databases database-normalization normal

Answer key

### 3.5.36 Database Normalization: GATE CSE 2017 Set 1 | Question: 16 top



The following functional dependencies hold true for the relational schema  $R\{V, W, X, Y, Z\}$ :

$$\begin{aligned} V &\rightarrow W \\ VW &\rightarrow X \\ Y &\rightarrow VX \\ Y &\rightarrow Z \end{aligned}$$

Which of the following is irreducible equivalent for this set of functional dependencies?

- A.  $V \rightarrow W$   
 $V \rightarrow X$   
 $Y \rightarrow V$   
 $Y \rightarrow Z$   
B.  $V \rightarrow W$

- $W \rightarrow X$   
 $Y \rightarrow V$   
 $Y \rightarrow Z$   
**C.**  $V \rightarrow W$   
 $V \rightarrow X$   
 $Y \rightarrow V$   
 $Y \rightarrow X$   
 $Y \rightarrow Z$   
**D.**  $V \rightarrow W$   
 $W \rightarrow X$   
 $Y \rightarrow V$   
 $Y \rightarrow X$   
 $Y \rightarrow Z$

gatecse-2017-set1 databases database-normalization normal

[Answer key](#)

### 3.5.37 Database Normalization: GATE CSE 2018 | Question: 42 top



Consider the following four relational schemas. For each schema , all non-trivial functional dependencies are listed, The **bolded** attributes are the respective primary keys.

**Schema I:** Registration(rollno, courses)

Field ‘courses’ is a set-valued attribute containing the set of courses a student has registered for.

Non-trivial functional dependency

$\text{rollno} \rightarrow \text{courses}$

**Schema II:** Registration (rollno, coursid, email)

Non-trivial functional dependencies:

$\text{rollno}, \text{courseid} \rightarrow \text{email}$

$\text{email} \rightarrow \text{rollno}$

**Schema III:** Registration (rollno, courseid, marks, grade)

Non-trivial functional dependencies:

$\text{rollno}, \text{courseid}, \rightarrow \text{marks}, \text{grade}$

$\text{marks} \rightarrow \text{grade}$

**Schema IV:** Registration (rollno, courseid, credit)

Non-trivial functional dependencies:

$\text{rollno}, \text{courseid} \rightarrow \text{credit}$

$\text{courseid} \rightarrow \text{credit}$

Which one of the relational schemas above is in 3NF but not in BCNF?

- A. Schema I      B. Schema II      C. Schema III      D. Schema IV

gatecse-2018 databases database-normalization normal 2-marks

[Answer key](#)

### 3.5.38 Database Normalization: GATE CSE 2019 | Question: 32 top



Let the set of functional dependencies  $F = \{QR \rightarrow S, R \rightarrow P, S \rightarrow Q\}$  hold on a relation schema  $X = (PQRS)$ .  $X$  is not in BCNF. Suppose  $X$  is decomposed into two schemas  $Y$  and  $Z$ , where  $Y = (PR)$  and  $Z = (QRS)$ .

Consider the two statements given below.

- I. Both  $Y$  and  $Z$  are in BCNF
- II. Decomposition of  $X$  into  $Y$  and  $Z$  is dependency preserving and lossless

Which of the above statements is/are correct?

- A. Both I and II      B. I only      C. II only      D. Neither I nor II

gatecse-2019 databases database-normalization 2-marks

[Answer key](#)

### 3.5.39 Database Normalization: GATE CSE 2020 | Question: 36 [top](#)



Consider a relational table  $R$  that is in  $3NF$ , but not in BCNF. Which one of the following statements is TRUE?

- A.  $R$  has a nontrivial functional dependency  $X \rightarrow A$ , where  $X$  is not a superkey and  $A$  is a prime attribute.
- B.  $R$  has a nontrivial functional dependency  $X \rightarrow A$ , where  $X$  is not a superkey and  $A$  is a non-prime attribute and  $X$  is not a proper subset of any key.
- C.  $R$  has a nontrivial functional dependency  $X \rightarrow A$ , where  $X$  is not a superkey and  $A$  is a non-prime attribute and  $X$  is a proper subset of some key
- D. A cell in  $R$  holds a set instead of an atomic value.

gatecse-2020 databases database-normalization 2-marks

[Answer key](#)

### 3.5.40 Database Normalization: GATE CSE 2021 Set 1 | Question: 33 [top](#)



Consider the relation  $R(P, Q, S, T, X, Y, Z, W)$  with the following functional dependencies.

$$PQ \rightarrow X; \quad P \rightarrow YX; \quad Q \rightarrow Y; \quad Y \rightarrow ZW$$

Consider the decomposition of the relation  $R$  into the constituent relations according to the following two decomposition schemes.

- $D_1 : R = [(P, Q, S, T); (P, T, X); (Q, Y); (Y, Z, W)]$
- $D_2 : R = [(P, Q, S); (T, X); (Q, Y); (Y, Z, W)]$

Which one of the following options is correct?

- A.  $D_1$  is a lossless decomposition, but  $D_2$  is a lossy decomposition
- B.  $D_1$  is a lossy decomposition, but  $D_2$  is a lossless decomposition
- C. Both  $D_1$  and  $D_2$  are lossless decompositions
- D. Both  $D_1$  and  $D_2$  are lossy decompositions

gatecse-2021-set1 databases database-normalization 2-marks

[Answer key](#)

### 3.5.41 Database Normalization: GATE CSE 2021 Set 2 | Question: 40 [top](#)



Suppose the following functional dependencies hold on a relation  $U$  with attributes  $P, Q, R, S$ , and  $T$ :

- $P \rightarrow QR$
- $RS \rightarrow T$

Which of the following functional dependencies can be inferred from the above functional dependencies?

- A.  $PS \rightarrow T$       B.  $R \rightarrow T$       C.  $P \rightarrow R$       D.  $PS \rightarrow Q$

gatecse-2021-set2 multiple-selects databases database-normalization 2-marks

[Answer key](#)

### 3.5.42 Database Normalization: GATE CSE 2022 | Question: 21 [top](#)



Consider a relation  $R(A, B, C, D, E)$  with the following three functional dependencies.

$$AB \rightarrow C; \quad BC \rightarrow D; \quad C \rightarrow E;$$

The number of superkeys in the relation  $R$  is \_\_\_\_\_.

gatecse-2022 numerical-answers databases database-normalization 1-mark

Answer key 

### 3.5.43 Database Normalization: GATE CSE 2022 | Question: 4

In a relational data model, which one of the following statements is TRUE?

- A. A relation with only two attributes is always in BCNF.
- B. If all attributes of a relation are prime attributes, then the relation is in BCNF.
- C. Every relation has at least one non-prime attribute.
- D. BCNF decompositions preserve functional dependencies.

gatecse-2022 databases database-normalization 1-mark

Answer key 

### 3.5.44 Database Normalization: GATE IT 2004 | Question: 75

A relation Empdtl is defined with attributes empcode (unique), name, street, city, state and pincode. For any pincode, there is only one city and state. Also, for any given street, city and state, there is just one pincode. In normalization terms, Empdtl is a relation in

- A. 1NF only
- B. 2NF and hence also in 1NF
- C. 3NF and hence also in 2NF and 1NF
- D. BCNF and hence also in 3NF, 2NF and 1NF

gateit-2004 databases database-normalization normal

Answer key 

### 3.5.45 Database Normalization: GATE IT 2005 | Question: 22

A table has fields  $F_1, F_2, F_3, F_4, F_5$  with the following functional dependencies

- $F_1 \rightarrow F_3, F_2 \rightarrow F_4, (F_1 \cdot F_2) \rightarrow F_5$

In terms of Normalization, this table is in

- A. 1 NF
- B. 2 NF
- C. 3 NF
- D. None of these

gateit-2005 databases database-normalization easy

Answer key 

### 3.5.46 Database Normalization: GATE IT 2005 | Question: 70

In a schema with attributes  $A, B, C, D$  and  $E$  following set of functional dependencies are given

- $A \rightarrow B$
- $A \rightarrow C$
- $CD \rightarrow E$
- $B \rightarrow D$
- $E \rightarrow A$

Which of the following functional dependencies is NOT implied by the above set?

- A.  $CD \rightarrow AC$
- B.  $BD \rightarrow CD$
- C.  $BC \rightarrow CD$
- D.  $AC \rightarrow BC$

gateit-2005 databases database-normalization normal

Answer key 

### 3.5.47 Database Normalization: GATE IT 2006 | Question: 60

Consider a relation  $R$  with five attributes  $V, W, X, Y$ , and  $Z$ . The following functional dependencies hold:  $YV \rightarrow W, WX \rightarrow Z$ , and  $ZY \rightarrow V$ .

Which of the following is a candidate key for  $R$ ?

- A.  $VXZ$       B.  $VXY$       C.  $VWXY$       D.  $VWXYZ$

gateit-2006 databases database-normalization normal

[Answer key](#)

### 3.5.48 Database Normalization: GATE IT 2008 | Question: 61 [top](#)

Let  $R(A, B, C, D)$  be a relational schema with the following functional dependencies :  $A \rightarrow B$ ,  $B \rightarrow C$ ,  $C \rightarrow D$  and  $D \rightarrow B$ . The decomposition of  $R$  into  $(A, B)$ ,  $(B, C)$ ,  $(B, D)$

- A. gives a lossless join, and is dependency preserving
- B. gives a lossless join, but is not dependency preserving
- C. does not give a lossless join, but is dependency preserving
- D. does not give a lossless join and is not dependency preserving

gateit-2008 databases database-normalization normal

[Answer key](#)

### 3.5.49 Database Normalization: GATE IT 2008 | Question: 62 [top](#)

Let  $R(A, B, C, D, E, P, G)$  be a relational schema in which the following functional dependencies are known to hold:  $AB \rightarrow CD$ ,  $DE \rightarrow P$ ,  $C \rightarrow E$ ,  $P \rightarrow C$  and  $B \rightarrow G$ . The relational schema  $R$  is

- A. in BCNF
- B. in 3NF, but not in BCNF
- C. in 2NF, but not in 3NF
- D. not in 2NF

gateit-2008 databases database-normalization normal

[Answer key](#)

### 3.5.50 Database Normalization: GATE2001-1.23, UGCNET-June2012-III: 18 [top](#)

Consider a schema  $R(A, B, C, D)$  and functional dependencies  $A \rightarrow B$  and  $C \rightarrow D$ . Then the decomposition of  $R$  into  $R_1(A, B)$  and  $R_2(C, D)$  is

- A. dependency preserving and lossless join
- B. lossless join but not dependency preserving
- C. dependency preserving but not lossless join
- D. not dependency preserving and not lossless join

gate1998 databases ugcnetcse-june2012-paper3 database-normalization

[Answer key](#)

## 3.6

### Er Diagram (10) [top](#)

#### 3.6.1 Er Diagram: GATE CSE 2005 | Question: 75 [top](#)

Let  $E_1$  and  $E_2$  be two entities in an  $E/R$  diagram with simple-valued attributes.  $R_1$  and  $R_2$  are two relationships between  $E_1$  and  $E_2$ , where  $R_1$  is one-to-many and  $R_2$  is many-to-many.  $R_1$  and  $R_2$  do not have any attributes of their own. What is the minimum number of tables required to represent this situation in the relational model?

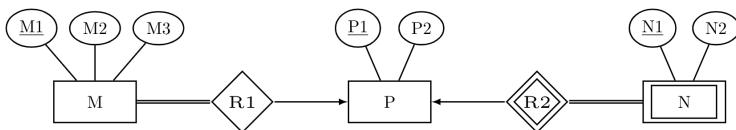
- A. 2      B. 3      C. 4      D. 5

gatecse-2005 databases er-diagram normal

[Answer key](#)

#### 3.6.2 Er Diagram: GATE CSE 2008 | Question: 82 [top](#)

Consider the following ER diagram



The minimum number of tables needed to represent  $M, N, P, R1, R2$  is

- A. 2      B. 3      C. 4      D. 5

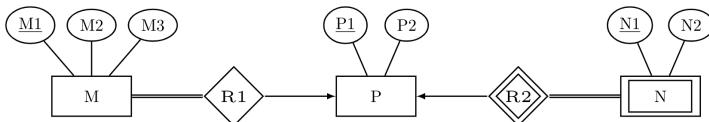
gatecse-2008 databases er-diagram normal

[Answer key](#)



### 3.6.3 Er Diagram: GATE CSE 2008 | Question: 83 top

Consider the following ER diagram



The minimum number of tables needed to represent  $M, N, P, R1, R2$  is

Which of the following is a correct attribute set for one of the tables for the minimum number of tables needed to represent  $M, N, P, R1, R2$ ?

- A.  $M1, M2, M3, P1$    B.  $M1, P1, N1, N2$    C.  $M1, P1, N1$    D.  $M1, P1$

gatecse-2008 databases er-diagram normal

[Answer key](#)



### 3.6.4 Er Diagram: GATE CSE 2012 | Question: 14 top

Given the basic ER and relational models, which of the following is **INCORRECT**?

- A. An attribute of an entity can have more than one value
- B. An attribute of an entity can be composite
- C. In a row of a relational table, an attribute can have more than one value
- D. In a row of a relational table, an attribute can have exactly one value or a NULL value

gatecse-2012 databases normal er-diagram

[Answer key](#)



### 3.6.5 Er Diagram: GATE CSE 2015 Set 1 | Question: 41 top

Consider an Entity-Relationship (ER) model in which entity sets  $E_1$  and  $E_2$  are connected by an  $m : n$  relationship  $R_{12}$ .  $E_1$  and  $E_3$  are connected by a  $1 : n$  ( $1$  on the side of  $E_1$  and  $n$  on the side of  $E_3$ ) relationship  $R_{13}$ .

$E_1$  has two-singled attributes  $a_{11}$  and  $a_{12}$  of which  $a_{11}$  is the key attribute.  $E_2$  has two singled-valued attributes  $a_{21}$  and  $a_{22}$  of which  $a_{21}$  is the key attribute.  $E_3$  has two single-valued attributes  $a_{31}$  and  $a_{32}$  of which  $a_{31}$  is the key attribute. The relationships do not have any attributes.

If a relational model is derived from the above ER model, then the minimum number of relations that would be generated if all relation are in 3NF is \_\_\_\_\_.

gatecse-2015-set1 databases er-diagram normal numerical-answers

[Answer key](#)



### 3.6.6 Er Diagram: GATE CSE 2017 Set 2 | Question: 17 top

An ER model of a database consists of entity types  $A$  and  $B$ . These are connected by a relationship  $R$  which does not have its own attribute. Under which one of the following conditions, can the relational table for  $R$  be merged with that of  $A$ ?

- A. Relationship  $R$  is one-to-many and the participation of  $A$  in  $R$  is total  
 B. Relationship  $R$  is one-to-many and the participation of  $A$  in  $R$  is partial  
 C. Relationship  $R$  is many-to-one and the participation of  $A$  in  $R$  is total  
 D. Relationship  $R$  is many-to-one and the participation of  $A$  in  $R$  is partial

gatecse-2017-set2 databases er-diagram normal

[Answer key](#)

### 3.6.7 Er Diagram: GATE CSE 2018 | Question: 11 top

In an Entity-Relationship (ER) model, suppose  $R$  is a many-to-one relationship from entity set E1 to entity set E2. Assume that E1 and E2 participate totally in  $R$  and that the cardinality of E1 is greater than the cardinality of E2.

Which one of the following is true about  $R$ ?

- A. Every entity in E1 is associated with exactly one entity in E2  
 B. Some entity in E1 is associated with more than one entity in E2  
 C. Every entity in E2 is associated with exactly one entity in E1  
 D. Every entity in E2 is associated with at most one entity in E1

gatecse-2018 databases er-diagram normal 1-mark

[Answer key](#)

### 3.6.8 Er Diagram: GATE CSE 2020 | Question: 14 top

Which one of the following is used to represent the supporting many-one relationships of a weak entity set in an entity-relationship diagram?

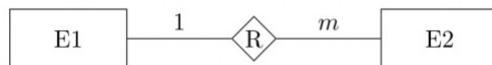
- |                                     |  |
|-------------------------------------|--|
| A. Diamonds with double/bold border | B. Rectangles with double/bold border        |
| C. Ovals with double/bold border    | D. Ovals that contain underlined identifiers |

gatecse-2020 databases er-diagram 1-mark

[Answer key](#)

### 3.6.9 Er Diagram: GATE IT 2004 | Question: 73 top

Consider the following entity relationship diagram (ERD), where two entities  $E1$  and  $E2$  have a relation  $R$  of cardinality 1:m.



The attributes of  $E1$  are  $A11$ ,  $A12$  and  $A13$  where  $A11$  is the key attribute. The attributes of  $E2$  are  $A21$ ,  $A22$  and  $A23$  where  $A21$  is the key attribute and  $A23$  is a multi-valued attribute. Relation  $R$  does not have any attribute. A relational database containing minimum number of tables with each table satisfying the requirements of the third normal form ( $3NF$ ) is designed from the above ERD. The number of tables in the database is

- A. 2                    B. 3                    C. 5                    D. 4

gateit-2004 databases er-diagram normal

[Answer key](#)

### 3.6.10 Er Diagram: GATE IT 2005 | Question: 21 top

Consider the entities 'hotel room', and 'person' with a many to many relationship 'lodging' as shown below:



If we wish to store information about the rent payment to be made by person (s) occupying different hotel rooms, then this information should appear as an attribute of

- A. Person
- B. Hotel Room
- C. Lodging
- D. None of these

gateit-2005 databases er-diagram easy

[Answer key](#)

3.7

**Indexing (12)** [top](#)

### 3.7.1 Indexing: GATE CSE 1989 | Question: 4-xiv [top](#)

For secondary key processing which of the following file organizations is preferred? Give a one line justification:

- A. Indexed sequential file
- B. Two-way linked list.
- C. Inverted file organization.
- D. Sequential file organization.

gate1989 normal databases indexing descriptive

[Answer key](#)

### 3.7.2 Indexing: GATE CSE 1990 | Question: 10b [top](#)

One giga bytes of data are to be organized as an indexed-sequential file with a uniform blocking factor 8. Assuming a block size of 1 Kilo bytes and a block referencing pointer size of 32 bits, find out the number of levels of indexing that would be required and the size of the index at each level. Determine also the size of the master index. The referencing capability (fanout ratio) per block of index storage may be considered to be 32.

gate1990 databases indexing descriptive

[Answer key](#)

### 3.7.3 Indexing: GATE CSE 1993 | Question: 14 [top](#)

An ISAM (indexed sequential) file consists of records of size 64 bytes each, including key field of size 14 bytes. An address of a disk block takes 2 bytes. If the disk block size is 512 bytes and there are 16K records, compute the size of the data and index areas in terms of number blocks. How many levels of tree do you have for the index?

gate1993 databases indexing normal descriptive

[Answer key](#)

### 3.7.4 Indexing: GATE CSE 1998 | Question: 1.35 [top](#)

There are five records in a database.

Name	Age	Occupation	Category
Rama	27	CON	A
Abdul	22	ENG	A
Jennifer	28	DOC	B
Maya	32	SER	D
Dev	24	MUS	C

There is an index file associated with this and it contains the values 1, 3, 2, 5 and 4. Which one of the fields is the index built from?

- A. Age
- B. Name
- C. Occupation
- D. Category

gate1998 databases indexing normal

[Answer key](#)

### 3.7.5 Indexing: GATE CSE 2008 | Question: 16, ISRO2016-60 top



A clustering index is defined on the fields which are of type

- |                         |                             |
|-------------------------|-----------------------------|
| A. non-key and ordering | B. non-key and non-ordering |
| C. key and ordering     | D. key and non-ordering     |

gatecse-2008 databases indexing isro2016

[Answer key](#)

### 3.7.6 Indexing: GATE CSE 2008 | Question: 70 top



Consider a file of 16384 records. Each record is 32 bytes long and its key field is of size 6 bytes. The file is ordered on a non-key field, and the file organization is unspanned. The file is stored in a file system with block size 1024 bytes, and the size of a block pointer is 10 bytes. If the secondary index is built on the key field of the file, and a multi-level index scheme is used to store the secondary index, the number of first-level and second-level blocks in the multi-level index are respectively

- A. 8 and 0      B. 128 and 6      C. 256 and 4      D. 512 and 5

gatecse-2008 databases indexing normal

[Answer key](#)

### 3.7.7 Indexing: GATE CSE 2011 | Question: 39 top



Consider a relational table  $r$  with sufficient number of records, having attributes  $A_1, A_2, \dots, A_n$  and let  $1 \leq p \leq n$ . Two queries  $Q1$  and  $Q2$  are given below.

- $Q1 : \pi_{A_1, \dots, A_p} (\sigma_{A_p=c} (r))$  where  $c$  is a constant
- $Q2 : \pi_{A_1, \dots, A_p} (\sigma_{c_1 \leq A_p \leq c_2} (r))$  where  $c_1$  and  $c_2$  are constants.

The database can be configured to do ordered indexing on  $A_p$  or hashing on  $A_p$ . Which of the following statements is **TRUE**?

- A. Ordered indexing will always outperform hashing for both queries  
B. Hashing will always outperform ordered indexing for both queries  
C. Hashing will outperform ordered indexing on  $Q1$ , but not on  $Q2$   
D. Hashing will outperform ordered indexing on  $Q2$ , but not on  $Q1$

gatecse-2011 databases indexing normal

[Answer key](#)

### 3.7.8 Indexing: GATE CSE 2013 | Question: 15 top



An index is clustered, if

- A. it is on a set of fields that form a candidate key  
B. it is on a set of fields that include the primary key  
C. the data records of the file are organized in the same order as the data entries of the index  
D. the data records of the file are organized not in the same order as the data entries of the index

gatecse-2013 databases indexing normal

[Answer key](#)

### 3.7.9 Indexing: GATE CSE 2015 Set 1 | Question: 24 top



A file is organized so that the ordering of the data records is the same as or close to the ordering of data entries in some index. Then that index is called

- A. Dense      B. Sparse      C. Clustered      D. Unclustered

gatecse-2015-set1 databases indexing easy

[Answer key](#)

### 3.7.10 Indexing: GATE CSE 2020 | Question: 54 top

Consider a database implemented using B+ tree for file indexing and installed on a disk drive with block size of 4 KB. The size of search key is 12 bytes and the size of tree/disk pointer is 8 bytes. Assume that the database has one million records. Also assume that no node of the B+ tree and no records are present initially in main memory. Consider that each record fits into one disk block. The minimum number of disk accesses required to retrieve any record in the database is \_\_\_\_\_

gatecse-2020 numerical-answers databases b-tree indexing 2-marks

Answer key 

### 3.7.11 Indexing: GATE CSE 2021 Set 2 | Question: 21 top

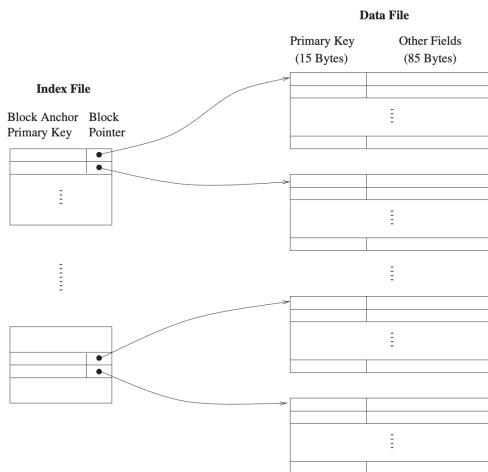
A data file consisting of 1,50,000 student-records is stored on a hard disk with block size of 4096 bytes. The data file is sorted on the primary key RollNo. The size of a record pointer for this disk is 7 bytes. Each student-record has a candidate key attribute called ANum of size 12 bytes. Suppose an index file with records consisting of two fields, ANum value and the record pointer to the corresponding student record, is built and stored on the same disk. Assume that the records of data file and index file are not split across disk blocks. The number of blocks in the index file is \_\_\_\_\_

gatecse-2021-set2 numerical-answers databases indexing 1-mark

Answer key 

### 3.7.12 Indexing: GATE CSE 2023 | Question: 52 top

Consider a database of fixed-length records, stored as an ordered file. The database has 25,000 records, with each record being 100 bytes, of which the primary key occupies 15 bytes. The data file is block-aligned in that each data record is fully contained within a block. The database is indexed by a primary index file, which is also stored as a block-aligned ordered file. The figure below depicts this indexing scheme.



Suppose the block size of the file system is 1024 bytes, and a pointer to a block occupies 5 bytes. The system uses binary search on the index file to search for a record with a given key. You may assume that a binary search on an index file of  $b$  blocks takes  $\lceil \log_2 b \rceil$  block accesses in the worst case.

Given a key, the number of block accesses required to identify the block in the data file that may contain a record with the key, in the worst case, is \_\_\_\_\_.

gatecse-2023 databases file-system indexing numerical-answers 2-marks

Answer key 

## 3.8

### Joins (7) top

#### 3.8.1 Joins: GATE CSE 2004 | Question: 14 top

Consider the following relation schema pertaining to a students database:

- Students (rollno, name, address)
- Enroll (rollno, courseno, coursename)

where the primary keys are shown underlined. The number of tuples in the student and Enroll tables are 120 and 8 respectively. What are the maximum and minimum number of tuples that can be present in (Student \* Enroll), where '\*' denotes natural join?

- A. 8,8      B. 120,8      C. 960,8      D. 960,120

gatecse-2004 databases easy joins natural-join

[Answer key](#)

### 3.8.2 Joins: GATE CSE 2012 | Question: 50 top



Consider the following relations  $A$ ,  $B$  and  $C$ :

A		
ID	Name	Age
12	Arun	60
15	Shreya	24
99	Rohit	11

B		
ID	Name	Age
15	Shreya	24
25	Hari	40
98	Rohit	20
99	Rohit	11

C		
ID	Phone	Area
10	2200	02
99	2100	01

How many tuples does the result of the following relational algebra expression contain? Assume that the schema of  $A \cup B$  is the same as that of  $A$ .

$$(A \cup B) \bowtie_{A.Id > 40 \vee C.Id < 15} C$$

- A. 7      B. 4      C. 5      D. 9

gatecse-2012 databases joins normal

[Answer key](#)

### 3.8.3 Joins: GATE CSE 2014 Set 2 | Question: 30 top



Consider a join (relation algebra) between relations  $r(R)$  and  $s(S)$  using the nested loop method. There are 3 buffers each of size equal to disk block size, out of which one buffer is reserved for intermediate results. Assuming  $\text{size}(r(R)) < \text{size}(s(S))$ , the join will have fewer number of disk block accesses if

- A. relation  $r(R)$  is in the outer loop.
- B. relation  $s(S)$  is in the outer loop.
- C. join selection factor between  $r(R)$  and  $s(S)$  is more than 0.5.
- D. join selection factor between  $r(R)$  and  $s(S)$  is less than 0.5.

gatecse-2014-set2 databases normal joins

[Answer key](#)

### 3.8.4 Joins: GATE IT 2005 | Question: 82a top



A database table  $T_1$  has 2000 records and occupies 80 disk blocks. Another table  $T_2$  has 400 records and occupies 20 disk blocks. These two tables have to be joined as per a specified join condition that needs to be evaluated for every pair of records from these two tables. The memory buffer space available can hold exactly one block of records for  $T_1$  and one block of records for  $T_2$  simultaneously at any point in time. No index is available on either table.

If Nested-loop join algorithm is employed to perform the join, with the most appropriate choice of table to be used in outer loop, the number of block accesses required for reading the data are

- A. 800000      B. 40080      C. 32020      D. 100

gateit-2005 databases normal joins

[Answer key](#)

### 3.8.5 Joins: GATE IT 2005 | Question: 82b top ↗



A database table  $T_1$  has 2000 records and occupies 80 disk blocks. Another table  $T_2$  has 400 records and occupies 20 disk blocks. These two tables have to be joined as per a specified join condition that needs to be evaluated for every pair of records from these two tables. The memory buffer space available can hold exactly one block of records for  $T_1$  and one block of records for  $T_2$  simultaneously at any point in time. No index is available on either table.

If, instead of Nested-loop join, Block nested-loop join is used, again with the most appropriate choice of table in the outer loop, the reduction in number of block accesses required for reading the data will be

- A. 0      B. 30400      C. 38400      D. 798400

gateit-2005 databases normal joins

[Answer key ↗](#)

### 3.8.6 Joins: GATE IT 2006 | Question: 14 top ↗



Consider the relations  $r_1(P, Q, R)$  and  $r_2(R, S, T)$  with primary keys P and R respectively. The relation  $r_1$  contains 2000 tuples and  $r_2$  contains 2500 tuples. The maximum size of the join  $r_1 \bowtie r_2$  is :

- A. 2000      B. 2500      C. 4500      D. 5000

gateit-2006 databases joins natural-join normal

[Answer key ↗](#)

### 3.8.7 Joins: GATE IT 2007 | Question: 68 top ↗



Consider the following relation schemas :

- b-Schema = (b-name, b-city, assets)
- a-Schema = (a-num, b-name, bal)
- d-Schema = (c-name, a-number)

Let branch, account and depositor be respectively instances of the above schemas. Assume that account and depositor relations are much bigger than the branch relation.

Consider the following query:

$\Pi_{c\text{-name}} (\sigma_{b\text{-city} = "Agra"} \wedge \text{bal} < 0 \text{ (branch} \bowtie \text{account} \bowtie \text{depositor)})$

Which one of the following queries is the most efficient version of the above query ?

- A.  $\Pi_{c\text{-name}} (\sigma_{\text{bal} < 0} (\sigma_{b\text{-city} = "Agra"} \text{ branch} \bowtie \text{account}) \bowtie \text{depositor})$   
B.  $\Pi_{c\text{-name}} (\sigma_{b\text{-city} = "Agra"} \text{ branch} \bowtie (\sigma_{\text{bal} < 0} \text{ account} \bowtie \text{depositor}))$   
C.  $\Pi_{c\text{-name}} ((\sigma_{b\text{-city} = "Agra"} \text{ branch} \bowtie \sigma_{b\text{-city} = "Agra"} \wedge \text{bal} < 0 \text{ account}) \bowtie \text{depositor})$   
D.  $\Pi_{c\text{-name}} (\sigma_{b\text{-city} = "Agra"} \text{ branch} \bowtie (\sigma_{b\text{-city} = "Agra"} \wedge \text{bal} < 0 \text{ account} \bowtie \text{depositor}))$

gateit-2007 databases joins relational-algebra normal

[Answer key ↗](#)

## 3.9

### Multivalued Dependency 4nf (1) top ↗



#### 3.9.1 Multivalued Dependency 4nf: GATE IT 2007 | Question: 67 top ↗

Consider the following implications relating to functional and multivalued dependencies given below, which may or may not be correct.

- i. if  $A \rightarrow\!\!\rightarrow B$  and  $A \rightarrow\!\!\rightarrow C$  then  $A \rightarrow BC$
- ii. if  $A \rightarrow B$  and  $A \rightarrow C$  then  $A \rightarrow\!\!\rightarrow BC$
- iii. if  $A \rightarrow\!\!\rightarrow BC$  and  $A \rightarrow B$  then  $A \rightarrow C$
- iv. if  $A \rightarrow BC$  and  $A \rightarrow B$  then  $A \rightarrow\!\!\rightarrow C$

Exactly how many of the above implications are valid?

A. 0

B. 1

C. 2

D. 3

gateit-2007 databases database-normalization multivalued-dependency-4nf normal

Answer key 

3.10

Natural Join (3) 

3.10.1 Natural Join: GATE CSE 2005 | Question: 30 

Let  $r$  be a relation instance with schema  $R = (A, B, C, D)$ . We define  $r_1 = \pi_{A,B,C}(R)$  and  $r_2 = \pi_{A,D}(r)$ . Let  $s = r_1 * r_2$  where  $*$  denotes natural join. Given that the decomposition of  $r$  into  $r_1$  and  $r_2$  is lossy, which one of the following is TRUE?

- A.  $s \subset r$       B.  $r \cup s = r$       C.  $r \subset s$       D.  $r * s = s$

gatecse-2005 databases relational-algebra natural-join normal

Answer key 

3.10.2 Natural Join: GATE CSE 2010 | Question: 43 

The following functional dependencies hold for relations  $R(A, B, C)$  and  $S(B, D, E)$ .

- $B \rightarrow A$
- $A \rightarrow C$

The relation  $R$  contains 200 tuples and the relation  $S$  contains 100 tuples. What is the maximum number of tuples possible in the natural join  $R \bowtie S$ ?

- A. 100      B. 200      C. 300      D. 2000

gatecse-2010 databases normal natural-join database-normalization

Answer key 

3.10.3 Natural Join: GATE CSE 2015 Set 2 | Question: 32 

Consider two relations  $R_1(A, B)$  with the tuples  $(1, 5), (3, 7)$  and  $R_2(A, C) = (1, 7), (4, 9)$ .

Assume that  $R(A, B, C)$  is the full natural outer join of  $R_1$  and  $R_2$ . Consider the following tuples of the form  $(A, B, C)$ :

$a = (1, 5, null), b = (1, null, 7), c = (3, null, 9), d = (4, 7, null), e = (1, 5, 7),$   
 $f = (3, 7, null), g = (4, null, 9).$

Which one of the following statements is correct?

- A.  $R$  contains  $a, b, e, f, g$  but not  $c, d$ .  
C.  $R$  contains  $e, f, g$  but not  $a, b$ .
- B.  $R$  contains all  $a, b, c, d, e, f, g$ .  
D.  $R$  contains  $e$  but not  $f, g$ .

gatecse-2015-set2 databases normal natural-join

Answer key 

3.11

Referential Integrity (4) 

3.11.1 Referential Integrity: GATE CSE 1997 | Question: 6.10, ISRO2016-54 

Let  $R(a, b, c)$  and  $S(d, e, f)$  be two relations in which  $d$  is the foreign key of  $S$  that refers to the primary key of  $R$ . Consider the following four operations  $R$  and  $S$

- I. Insert into  $R$
- II. Insert into  $S$
- III. Delete from  $R$
- IV. Delete from  $S$

Which of the following can cause violation of the referential integrity constraint above?

- A. Both I and IV      B. Both II and III      C. All of these      D. None of these

gate1997 databases referential-integrity easy isro2016

[Answer key](#)

### 3.11.2 Referential Integrity: GATE CSE 2005 | Question: 76 top ↗



The following table has two attributes  $A$  and  $C$  where  $A$  is the primary key and  $C$  is the foreign key referencing  $A$  with on-delete cascade.

A	C
2	4
3	4
4	3
5	2
7	2
9	5
6	4

The set of all tuples that must be additionally deleted to preserve referential integrity when the tuple  $(2, 4)$  is deleted is:

- A.  $(3, 4)$  and  $(6, 4)$   
 B.  $(5, 2)$  and  $(7, 2)$   
 C.  $(5, 2), (7, 2)$  and  $(9, 5)$   
 D.  $(3, 4), (4, 3)$  and  $(6, 4)$

gatecse-2005 databases referential-integrity normal

[Answer key](#)

### 3.11.3 Referential Integrity: GATE CSE 2017 Set 2 | Question: 19 top ↗



Consider the following tables  $T1$  and  $T2$ .

$T1$		$T2$	
P	Q	R	S
2	2	2	2
3	8	8	3
7	3	3	2
5	8	9	7
6	9	5	7
8	5	7	2
9	8		

In table  $T1$  **P** is the primary key and **Q** is the foreign key referencing **R** in table  $T2$  with on-delete cascade and on-update cascade. In table  $T2$ , **R** is the primary key and **S** is the foreign key referencing **P** in table  $T1$  with on-delete set NULL and on-update cascade. In order to delete record  $\langle 3, 8 \rangle$  from the table  $T1$ , the number of additional records that need to be deleted from table  $T1$  is \_\_\_\_\_

gatecse-2017-set2 databases numerical-answers referential-integrity normal

[Answer key](#)

### 3.11.4 Referential Integrity: GATE CSE 2021 Set 2 | Question: 6 top ↗



Consider the following statements  $S1$  and  $S2$  about the relational data model:

- $S1$ : A relation scheme can have at most one foreign key.
- $S2$ : A foreign key in a relation scheme  $R$  cannot be used to refer to tuples of  $R$ .

Which one of the following choices is correct?

- A. Both  $S_1$  and  $S_2$  are true  
C.  $S_1$  is false and  $S_2$  is true  
B.  $S_1$  is true and  $S_2$  is false  
D. Both  $S_1$  and  $S_2$  are false

gatecse-2021-set2 databases referential-integrity 1-mark

Answer key 

3.12

Relational Algebra (27) 

### 3.12.1 Relational Algebra: GATE CSE 1992 | Question: 13b

Suppose we have a database consisting of the following three relations:

FREQUENTS	(CUSTOMER, HOTEL)
SERVES	(HOTEL, SNACKS)
LIKES	(CUSTOMER, SNACKS)

The first indicates the hotels each customer visits, the second tells which snacks each hotel serves and last indicates which snacks are liked by each customer. Express the following query in relational algebra:

Print the hotels the serve the snack that customer Rama likes.

gate1992 databases relational-algebra normal descriptive

Answer key 

### 3.12.2 Relational Algebra: GATE CSE 1994 | Question: 13

Consider the following relational schema:

- COURSES (cno, cname)
- STUDENTS (rollno, sname, age, year)
- REGISTERED\_FOR (cno, rollno)

The underlined attributes indicate the primary keys for the relations. The 'year' attribute for the STUDENTS relation indicates the year in which the student is currently studying (First year, Second year etc.)

- A. Write a relational algebra query to print the roll number of students who have registered for cno 322.  
B. Write a SQL query to print the age and year of the youngest student in each year.

gate1994 databases relational-algebra sql normal descriptive

Answer key 

### 3.12.3 Relational Algebra: GATE CSE 1994 | Question: 3.8

Give a relational algebra expression using only the minimum number of operators from  $(\cup, -)$  which is equivalent to  $R \cap S$ . 

gate1994 databases relational-algebra normal descriptive

Answer key 

### 3.12.4 Relational Algebra: GATE CSE 1995 | Question: 27

Consider the relation scheme.

AUTHOR	(ANAME, INSTITUTION, ACITY, AGE)
PUBLISHER	(PNAME, PCITY)
BOOK	(TITLE, ANAME, PNAME)

Express the following queries using (one or more of) SELECT, PROJECT, JOIN and DIVIDE operations.

- A. Get the names of all publishers.
- B. Get values of all attributes of all authors who have published a book for the publisher with PNAME='TECHNICAL PUBLISHERS'.
- C. Get the names of all authors who have published a book for any publisher located in Madras

gate1995 databases relational-algebra normal descriptive

[Answer key](#)

### 3.12.5 Relational Algebra: GATE CSE 1996 | Question: 27 [top](#)



A library relational database system uses the following schema

- USERS (User#, User Name, Home Town)
- BOOKS (Book#, Book Title, Author Name)
- ISSUED (Book#, User#, Date)

Explain in one English sentence, what each of the following relational algebra queries is designed to determine

- $\sigma_{\text{User}\#=6} (\pi_{\text{User}\#, \text{Book Title}} ((\text{USERS} \bowtie \text{ISSUED}) \bowtie \text{BOOKS}))$
- $\pi_{\text{Author Name}} (\text{BOOKS} \bowtie \sigma_{\text{Home Town}= \text{Delhi}} (\text{USERS} \bowtie \text{ISSUED}))$

gate1996 databases relational-algebra descriptive

[Answer key](#)

### 3.12.6 Relational Algebra: GATE CSE 1997 | Question: 76-a [top](#)



Consider the following relational database schema:

- EMP (eno name, age)
- PROJ (pno name)
- INVOLVED (eno, pno)

EMP contains information about employees. PROJ about projects and involved about which employees involved in which projects. The underlined attributes are the primary keys for the respective relations.

What is the relational algebra expression containing one or more of  $\{\sigma, \pi, \times, \rho, -\}$  which is equivalent to SQL query.

`select eno from EMP||INVOLVED where EMP.eno=INVOLVED.eno and INVOLVED.pno=3`

gate1997 databases sql relational-algebra descriptive

[Answer key](#)

### 3.12.7 Relational Algebra: GATE CSE 1998 | Question: 1.33 [top](#)



Given two union compatible relations  $R_1(A, B)$  and  $R_2(C, D)$ , what is the result of the operation  $R_1 \bowtie_{A=C \wedge B=D} R_2$ ?

- A.  $R_1 \cup R_2$       B.  $R_1 \times R_2$       C.  $R_1 - R_2$       D.  $R_1 \cap R_2$

gate1998 normal relational-algebra

[Answer key](#)

### 3.12.8 Relational Algebra: GATE CSE 1998 | Question: 27 [top](#)



Consider the following relational database schemes:

- COURSES (Cno, Name)
- PRE\_REQ(Cno, Pre\_Cno)
- COMPLETED (Student\_no, Cno)

COURSES gives the number and name of all the available courses.

PRE\_REQ gives the information about which courses are pre-requisites for a given course.

COMPLETED indicates what courses have been completed by students

Express the following using relational algebra:

List all the courses for which a student with Student\_no 2310 has completed all the pre-requisites.

gate1998 databases relational-algebra normal descriptive

[Answer key](#)

### 3.12.9 Relational Algebra: GATE CSE 1999 | Question: 1.18, ISRO2016-53 [top](#)

Consider the join of a relation  $R$  with a relation  $S$ . If  $R$  has  $m$  tuples and  $S$  has  $n$  tuples then the maximum and minimum sizes of the join respectively are

- A.  $m + n$  and 0      B.  $mn$  and 0      C.  $m + n$  and  $|m - n|$  D.  $mn$  and  $m + n$

gate1999 databases relational-algebra easy isro2016

[Answer key](#)

### 3.12.10 Relational Algebra: GATE CSE 2000 | Question: 1.23, ISRO2016-57 [top](#)

Given the relations

- employee (name, salary, dept-no), and
- department (dept-no, dept-name,address),

Which of the following queries cannot be expressed using the basic relational algebra operations ( $\sigma, \pi, \times, \bowtie, \cup, \cap, -$ )?

- A. Department address of every employee  
B. Employees whose name is the same as their department name  
C. The sum of all employees' salaries  
D. All employees of a given department

gatecse-2000 databases relational-algebra easy isro2016

[Answer key](#)

### 3.12.11 Relational Algebra: GATE CSE 2001 | Question: 1.24 [top](#)

Suppose the adjacency relation of vertices in a graph is represented in a table  $\text{Adj}(X, Y)$ . Which of the following queries cannot be expressed by a relational algebra expression of constant length?

- A. List all vertices adjacent to a given vertex  
B. List all vertices which have self loops  
C. List all vertices which belong to cycles of less than three vertices  
D. List all vertices reachable from a given vertex

gatecse-2001 databases relational-algebra normal

[Answer key](#)

### 3.12.12 Relational Algebra: GATE CSE 2001 | Question: 1.25 [top](#)

Let  $r$  and  $s$  be two relations over the relation schemes  $R$  and  $S$  respectively, and let  $A$  be an attribute in  $R$ . The relational algebra expression  $\sigma_{A=a}(r \bowtie s)$  is always equal to

- A.  $\sigma_{A=a}(r)$   
C.  $\sigma_{A=a}(r) \bowtie s$
- B.  $r$   
D. None of the above

gatecse-2001 databases relational-algebra

[Answer key](#)

### 3.12.13 Relational Algebra: GATE CSE 2002 | Question: 15 top



A university placement center maintains a relational database of companies that interview students on campus and make job offers to those successful in the interview. The schema of the database is given below:

COMPANY( <u>cname</u> , clocation)	STUDENT(srollno, sname, sdegree)
INTERVIEW( <u>cname</u> , <u>srollno</u> , <u>idate</u> )	OFFER( <u>cname</u> , <u>srollno</u> , osalary)

The COMPANY relation gives the name and location of the company. The STUDENT relation gives the student's roll number, name and the degree program for which the student is registered in the university. The INTERVIEW relation gives the date on which a student is interviewed by a company. The OFFER relation gives the salary offered to a student who is successful in a company's interview. The key for each relation is indicated by the underlined attributes

- Write a **relational algebra** expressions (using only the operators  $\bowtie, \sigma, \pi, \cup, -$ ) for the following queries.
  - List the *rollnumbers* and *names* of students who attended at least one interview but did not receive *any* job offer.
  - List the *rollnumbers* and *names* of students who went for interviews and received job offers from *every* company with which they interviewed.
- Write an SQL query to list, for each degree program in which more than *five* students were offered jobs, the name of the degree and the average offered salary of students in this degree program.

gatecse-2002 databases normal descriptive relational-algebra sql

[Answer key](#)

### 3.12.14 Relational Algebra: GATE CSE 2003 | Question: 30 top



Consider the following SQL query

**Select distinct**  $a_1, a_2, \dots, a_n$   
**from**  $r_1, r_2, \dots, r_m$   
**where** P

For an arbitrary predicate P, this query is equivalent to which of the following relational algebra expressions?

- A.  $\Pi_{a_1, a_2, \dots, a_n} \sigma_p (r_1 \times r_2 \times \dots \times r_m)$
- B.  $\Pi_{a_1, a_2, \dots, a_n} \sigma_p (r_1 \bowtie r_2 \bowtie \dots \bowtie r_m)$
- C.  $\Pi_{a_1, a_2, \dots, a_n} \sigma_p (r_1 \cup r_2 \cup \dots \cup r_m)$
- D.  $\Pi_{a_1, a_2, \dots, a_n} \sigma_p (r_1 \cap r_2 \cap \dots \cap r_m)$

gatecse-2003 databases relational-algebra normal

[Answer key](#)

### 3.12.15 Relational Algebra: GATE CSE 2004 | Question: 51 top



Consider the relation Student (name, sex, marks), where the primary key is shown underlined, pertaining to students in a class that has at least one boy and one girl. What does the following relational algebra expression produce? (Note:  $\rho$  is the rename operator).

$$\pi_{name} \{ \sigma_{sex=female} (\text{Student}) \} - \pi_{name} (\text{Student} \bowtie_{(sex=female \wedge x=male \wedge marks \leq m)} \rho_{n,x,m} (\text{Student}))$$

- A. names of girl students with the highest marks
- B. names of girl students with more marks than some boy student
- C. names of girl students with marks not less than some boy student
- D. names of girl students with more marks than all the boy students

gatecse-2004 databases relational-algebra normal

[Answer key](#)

### 3.12.16 Relational Algebra: GATE CSE 2007 | Question: 59 top



Information about a collection of students is given by the relation  $\text{studInfo}(\text{studId}, \text{name}, \text{sex})$ . The relation  $\text{enroll}(\text{studId}, \text{courseId})$  gives which student has enrolled for (or taken) what course(s). Assume that every course is taken by at least one male and at least one female student. What does the following relational algebra expression represent?

$$\pi_{\text{courseId}} ((\pi_{\text{studId}} (\sigma_{\text{sex}=\text{"female"}} (\text{studInfo})) \times \pi_{\text{courseId}} (\text{enroll})) - \text{enroll})$$

- A. Courses in which all the female students are enrolled.
- B. Courses in which a proper subset of female students are enrolled.
- C. Courses in which only male students are enrolled.
- D. None of the above

gatecse-2007 databases relational-algebra normal

Answer key

### 3.12.17 Relational Algebra: GATE CSE 2008 | Question: 68 top



Let R and S be two relations with the following schema

$$R(P, Q, R1, R2, R3)$$

$$S(P, Q, S1, S2)$$

where  $\{P, Q\}$  is the key for both schemas. Which of the following queries are equivalent?

- I.  $\Pi_P (R \bowtie S)$
- II.  $\Pi_P (R) \bowtie \Pi_P (S)$
- III.  $\Pi_P (\Pi_{P,Q} (R) \cap \Pi_{P,Q} (S))$
- IV.  $\Pi_P (\Pi_{P,Q} (R) - (\Pi_{P,Q} (R) - \Pi_{P,Q} (S)))$

- A. Only I and II
- B. Only I and III
- C. Only I, II and III
- D. Only I, III and IV

gatecse-2008 databases relational-algebra normal

Answer key

### 3.12.18 Relational Algebra: GATE CSE 2012 | Question: 43 top



Suppose  $R_1(A, B)$  and  $R_2(C, D)$  are two relation schemas. Let  $r_1$  and  $r_2$  be the corresponding relation instances.  $B$  is a foreign key that refers to  $C$  in  $R_2$ . If data in  $r_1$  and  $r_2$  satisfy referential integrity constraints, which of the following is **ALWAYS TRUE**?

- A.  $\prod_B (r_1) - \prod_C (r_2) = \emptyset$
- B.  $\prod_C (r_2) - \prod_B (r_1) = \emptyset$
- C.  $\prod_B (r_1) = \prod_C (r_2)$
- D.  $\prod_B (r_1) - \prod_C (r_2) \neq \emptyset$

gatecse-2012 databases relational-algebra normal

Answer key

### 3.12.19 Relational Algebra: GATE CSE 2014 Set 3 | Question: 21 top



What is the optimized version of the relation algebra expression  $\pi_{A1}(\pi_{A2}(\sigma_{F1}(\sigma_{F2}(r))))$ , where  $A1, A2$  are sets of attributes in  $r$  with  $A1 \subset A2$  and  $F1, F2$  are Boolean expressions based on the attributes in  $r$ ?

- A.  $\pi_{A1}(\sigma_{(F1 \wedge F2)}(r))$
- B.  $\pi_{A1}(\sigma_{(F1 \vee F2)}(r))$
- C.  $\pi_{A2}(\sigma_{(F1 \wedge F2)}(r))$
- D.  $\pi_{A2}(\sigma_{(F1 \vee F2)}(r))$

gatecse-2014-set3 databases relational-algebra easy

Answer key

### 3.12.20 Relational Algebra: GATE CSE 2014 Set 3 | Question: 30 top



Consider the relational schema given below, where **eld** of the relation **dependent** is a foreign key referring to **empId** of the relation **employee**. Assume that every employee has at least one associated dependent in the **dependent** relation.

**employee (empId, empName, empAge)**

**dependent (depId, eId, depName, depAge)**

Consider the following relational algebra query:

$\Pi_{empId} (employee) - \Pi_{empId} (employee \bowtie_{(empId=eID) \wedge (empAge \leq depAge)} dependent)$

The above query evaluates to the set of **empIds** of employees whose age is greater than that of

- A. some dependent.
- B. all dependents.
- C. some of his/her dependents.
- D. all of his/her dependents.

gatecse-2014-set3 databases sql relational-algebra normal

Answer key



### 3.12.21 Relational Algebra: GATE CSE 2015 Set 1 | Question: 7 top

SELECT operation in SQL is equivalent to

- A. The selection operation in relational algebra
- B. The selection operation in relational algebra, except that SELECT in SQL retains duplicates
- C. The projection operation in relational algebra
- D. The projection operation in relational algebra, except that SELECT in SQL retains duplicates

gatecse-2015-set1 databases sql relational-algebra easy

Answer key



### 3.12.22 Relational Algebra: GATE CSE 2017 Set 1 | Question: 46 top



Consider a database that has the relation schema CR(StudentName, CourseName). An instance of the schema CR is as given below.

StudentName	CourseName
SA	CA
SA	CB
SA	CC
SB	CB
SB	CC
SC	CA
SC	CB
SC	CC
SD	CA
SD	CB
SD	CC
SD	CD
SE	CD
SE	CA
SE	CB
SF	CA
SF	CB
SF	CC

The following query is made on the database.

- $T1 \leftarrow \pi_{CourseName} (\sigma_{StudentName=SA} (CR))$
- $T2 \leftarrow CR \div T1$

The number of rows in  $T2$  is \_\_\_\_\_.

gatecse-2017-set1 databases relational-algebra normal numerical-answers

[Answer key](#)

### 3.12.23 Relational Algebra: GATE CSE 2018 | Question: 41 top

Consider the relations  $r(A, B)$  and  $s(B, C)$ , where  $s.B$  is a primary key and  $r.B$  is a foreign key referencing  $s.B$ . Consider the query

$$Q : r \bowtie (\sigma_{B < 5}(s))$$

Let LOJ denote the natural left outer-join operation. Assume that  $r$  and  $s$  contain no null values.

Which of the following is NOT equivalent to  $Q$ ?

- |   |                                       |
|---|---------------------------------------|
| A. $\sigma_{B < 5}(r \bowtie s)$        | B. $\sigma_{B < 5}(r \text{ LOJ } s)$ |
| C. $r \text{ LOJ } (\sigma_{B < 5}(s))$ | D. $\sigma_{B < 5}(r) \text{ LOJ } s$ |

gatecse-2018 databases relational-algebra normal 2-marks

[Answer key](#)

### 3.12.24 Relational Algebra: GATE CSE 2019 | Question: 55 top

Consider the following relations  $P(X, Y, Z)$ ,  $Q(X, Y, T)$  and  $R(Y, V)$ .



Table: P		
X	Y	Z
X1	Y1	Z1
X1	Y1	Z2
X2	Y2	Z2
X2	Y4	Z4

Table: Q		
X	Y	T
X2	Y1	2
X1	Y2	5
X1	Y1	6
X3	Y3	1

Table: R	
Y	V
Y1	V1
Y3	V2
Y2	V3
Y2	V2

How many tuples will be returned by the following relational algebra query?

$$\Pi_x(\sigma_{(P.Y=R.Y \wedge R.V=V2)} (P \times R)) - \Pi_x(\sigma_{(Q.Y=R.Y \wedge Q.T>2)} (Q \times R))$$

Answer: \_\_\_\_\_

gatecse-2019 numerical-answers databases relational-algebra 2-marks

[Answer key](#)



### 3.12.25 Relational Algebra: GATE CSE 2021 Set 1 | Question: 27 top

The following relation records the age of 500 employees of a company, where  $empNo$  (indicating the employee number) is the key:

$$\text{empAge}(\underline{\text{empNo}}, \underline{\text{age}})$$

Consider the following relational algebra expression:

$$\Pi_{empNo}(\text{empAge} \bowtie_{(\text{age} > \text{age1})} \rho_{empNo1, \text{age1}}(\text{empAge}))$$



What does the above expression generate?

- A. Employee numbers of only those employees whose age is the maximum  
 B. Employee numbers of only those employees whose age is more than the age of exactly one other employee  
 C. Employee numbers of all employees whose age is not the minimum  
 D. Employee numbers of all employees whose age is the minimum

gatecse-2021-set1 databases relational-algebra 2-marks

[Answer key](#)

### 3.12.26 Relational Algebra: GATE CSE 2022 | Question: 15 top



Consider the following three relations in a relational database.

Employee(eId, Name), Brand(bId, bName), Own(eId, bId)

Which of the following relational algebra expressions return the set of *elds* who own all the brands?

- A.  $\Pi_{eId} (\Pi_{eId, bId} (Own) / \Pi_{bId} (Brand))$   
 B.  $\Pi_{eId} (Own) - \Pi_{eId} ((\Pi_{eId} (Own) \times \Pi_{bId} (Brand)) - \Pi_{eId, bId} (Own))$   
 C.  $\Pi_{eId} (\Pi_{eId, bId} (Own) / \Pi_{bId} (Own))$   
 D.  $\Pi_{eId} ((\Pi_{eId} (Own) \times \Pi_{bId} (Own)) / \Pi_{bId} (Brand))$

gatecse-2022 databases relational-algebra multiple-selects 1-mark

[Answer key](#)

### 3.12.27 Relational Algebra: GATE IT 2005 | Question: 68 top



A table 'student' with schema (roll, name, hostel, marks), and another table 'hobby' with schema (roll, hobbyname) contains records as shown below:

Table: student

Roll	Name	Hostel	Marks
1798	Manoj Rathor	7	95
2154	Soumic Banerjee	5	68
2369	Gumma Reddy	7	86
2581	Pradeep pendse	6	92
2643	Suhas Kulkarni	5	78
2711	Nitin Kadamb	8	72
2872	Kiran Vora	5	92
2926	Manoj Kunkalikar	5	94
2959	Hemant Karkhanis	7	88
3125	Rajesh Doshi	5	82

Table: hobby

Roll	Hobby Name
1798	chess
1798	music
2154	music
2369	swimming
2581	cricket
2643	chess
2643	hockey
2711	volleyball
2872	football
2926	cricket
2959	photography
3125	music
3125	chess

The following SQL query is executed on the above tables:

```
select hostel
from student natural join hobby
where marks >= 75 and roll between 2000 and 3000;
```

Relations  $S$  and  $H$  with the same schema as those of these two tables respectively contain the same information as tuples. A new relation  $S'$  is obtained by the following relational algebra operation:

$$S' = \Pi_{\text{hostel}} ((\sigma_{s.roll=H.roll} (\sigma_{marks>75} \text{ and } roll > 2000 \text{ and } roll < 3000) (S)) \times (H))$$

The difference between the number of rows output by the SQL statement and the number of tuples in  $S'$  is

- A. 6      B. 4      C. 2      D. 0

gateit-2005 databases sql relational-algebra normal

[Answer key](#)

3.13

**Relational Calculus (14)** [top](#)

### 3.13.1 Relational Calculus: GATE CSE 1993 | Question: 23 [top](#)



The following relations are used to store data about students, courses, enrollment of students in courses and teachers of courses. Attributes for primary key in each relation are marked by '\*'.

Students (rollno\*, sname, saddr)  
courses (cno\*, cname)  
enroll(rollno\*, cno\*, grade)  
teach(tno\*, tname, cao\*)

(cno is course number cname is course name, tno is teacher number, tname is teacher name, sname is student name, etc.)

Write a SQL query for retrieving roll number and name of students who got A grade in at least one course taught by teacher names Ramesh for the above relational database.

gate1993 databases sql relational-calculus normal descriptive

[Answer key](#)

### 3.13.2 Relational Calculus: GATE CSE 1993 | Question: 24 [top](#)



The following relations are used to store data about students, courses, enrollment of students in courses and teachers of courses. Attributes for primary key in each relation are marked by '\*'.

- students(rollno\*, sname, saddr)
- courses(cno\*, cname)
- enroll(rollno\*, cno\*, grade)
- teach(tno\*, tname, cao\*)

(cno is course number, cname is course name, tno is teacher number, tname is teacher name, sname is student name, etc.)

For the relational database given above, the following functional dependencies hold:

- rollno → sname, saddr
- cno → cname
- tno → tname
- rollno, cno → grade

- Is the database in 3<sup>rd</sup> normal form (3NF)?
- If yes, prove that it is in 3NF. If not, normalize the relations so that they are in 3NF (without proving).

gate1993 databases sql relational-calculus normal descriptive

[Answer key](#)

### 3.13.3 Relational Calculus: GATE CSE 1998 | Question: 2.19 [top](#)



Which of the following query transformations (i.e., replacing the l.h.s. expression by the r.h.s expression) is incorrect? R1 and R2 are relations, C1 and C2 are selection conditions and A1 and A2 are attributes of R1.

- $\sigma_{C_1}(\sigma_{C_2}(R_1)) \rightarrow \sigma_{C_2}(\sigma_{C_1}(R_1))$
- $\sigma_{C_1}(\pi_{A_1}(R_1)) \rightarrow \pi_{A_1}(\sigma_{C_1}(R_1))$
- $\sigma_{C_1}(R_1 \cup R_2) \rightarrow \sigma_{C_1}(R_1) \cup \sigma_{C_1}(R_2)$
- $\pi_{A_1}(\sigma_{C_1}(R_1)) \rightarrow \sigma_{C_1}(\pi_{A_1}(R_1))$

**Answer key****3.13.4 Relational Calculus: GATE CSE 1999 | Question: 1.19**

The relational algebra expression equivalent to the following tuple calculus expression:

$\{t \mid t \in r \wedge (t[A] = 10 \wedge t[B] = 20)\}$  is

- A.  $\sigma_{(A=10 \wedge B=20)}(r)$
- B.  $\sigma_{(A=10)}(r) \cup \sigma_{(B=20)}(r)$
- C.  $\sigma_{(A=10)}(r) \cap \sigma_{(B=20)}(r)$
- D.  $\sigma_{(A=10)}(r) - \sigma_{(B=20)}(r)$

**Answer key****3.13.5 Relational Calculus: GATE CSE 2001 | Question: 2.24**

Which of the following relational calculus expression is not safe?

- A.  $\{t \mid \exists u \in R_1 (t[A] = u[A]) \wedge \neg \exists s \in R_2 (t[A] = s[A])\}$
- B.  $\{t \mid \forall u \in R_1 (u[A] = "x") \Rightarrow \exists s \in R_2 (t[A] = s[A] \wedge s[A] = u[A])\}$
- C.  $\{t \mid \neg(t \in R_1)\}$
- D.  $\{t \mid \exists u \in R_1 (t[A] = u[A]) \wedge \exists s \in R_2 (t[A] = s[A])\}$

**Answer key****3.13.6 Relational Calculus: GATE CSE 2002 | Question: 1.20**

With regards to the expressive power of the formal relational query languages, which of the following statements is true?

- A. Relational algebra is more powerful than relational calculus
- B. Relational algebra has the same power as relational calculus
- C. Relational algebra has the same power as safe relational calculus
- D. None of the above

**Answer key****3.13.7 Relational Calculus: GATE CSE 2004 | Question: 13**

Let  $R_1(\underline{A}, B, C)$  and  $R_2(\underline{D}, E)$  be two relation schema, where the primary keys are shown underlined, and let  $C$  be a foreign key in  $R_1$  referring to  $R_2$ . Suppose there is no violation of the above referential integrity constraint in the corresponding relation instances  $r_1$  and  $r_2$ . Which of the following relational algebra expressions would necessarily produce an empty relation?

- A.  $\Pi_D(r_2) - \Pi_C(r_1)$
- B.  $\Pi_C(r_1) - \Pi_D(r_2)$
- C.  $\Pi_D(r_1 \bowtie_{C \neq D} r_2)$
- D.  $\Pi_C(r_1 \bowtie_{C=D} r_2)$

**Answer key****3.13.8 Relational Calculus: GATE CSE 2007 | Question: 60**

Consider the relation **employee**(name, sex, supervisorName) with *name* as the key, *supervisorName* gives the name of the supervisor of the employee under consideration. What does the following Tuple Relational Calculus query produce?

$\{e.name \mid \text{employee}(e) \wedge (\forall x) [\neg \text{employee}(x) \vee x.supervisorName \neq e.name \vee x.sex = "male"]\}$

- A. Names of employees with a male supervisor.
- B. Names of employees with no immediate male subordinates.

- C. Names of employees with no immediate female subordinates.  
 D. Names of employees with a female supervisor.

gatecse-2007 databases relational-calculus normal

[Answer key](#)

### 3.13.9 Relational Calculus: GATE CSE 2008 | Question: 15 [top](#)



Which of the following tuple relational calculus expression(s) is/are equivalent to  $\forall t \in r (P(t))$ ?

- I.  $\neg \exists t \in r (P(t))$
  - II.  $\exists t \notin r (P(t))$
  - III.  $\neg \exists t \in r (\neg P(t))$
  - IV.  $\exists t \notin r (\neg P(t))$
- A. I only      B. II only      C. III only      D. III and IV only

gatecse-2008 databases relational-calculus normal

[Answer key](#)

### 3.13.10 Relational Calculus: GATE CSE 2009 | Question: 45 [top](#)



Let  $R$  and  $S$  be relational schemes such that  $R = \{a, b, c\}$  and  $S = \{c\}$ . Now consider the following queries on the database:

1.  $\pi_{R-S}(r) - \pi_{R-S}(\pi_{R-S}(r) \times s - \pi_{R-S,S}(r))$
2.  $\{t \mid t \in \pi_{R-S}(r) \wedge \forall u \in s (\exists v \in r (u = v[S] \wedge t = v[R - S]))\}$
3.  $\{t \mid t \in \pi_{R-S}(r) \wedge \forall v \in r (\exists u \in s (u = v[S] \wedge t = v[R - S]))\}$
4. 

```
Select R.a,R.b  
      From R,S  
     Where R.c = S.c
```

Which of the above queries are equivalent?

- A. 1 and 2      B. 1 and 3      C. 2 and 4      D. 3 and 4

gatecse-2009 databases relational-calculus difficult

[Answer key](#)

### 3.13.11 Relational Calculus: GATE CSE 2013 | Question: 35 [top](#)



Consider the following relational schema.

- Students(rollno: integer, sname: string)
- Courses(courseno: integer, cname: string)
- Registration(rollno: integer, courseno: integer, percent: real)

Which of the following queries are equivalent to this query in English?

*"Find the distinct names of all students who score more than 90% in the course numbered 107"*

- I. 

```
SELECT DISTINCT S.sname FROM Students as S, Registration  
      as R WHERE  
      R.rollno=S.rollno AND R.courseno=107 AND R.percent >90
```
- II.  $\prod_{sname} (\sigma_{courseno=107 \wedge percent>90} (Registration \bowtie Students))$
- III.  $\{T \mid \exists S \in Students, \exists R \in Registration (S.rollno = R.rollno \wedge R.courseno = 107 \wedge R.percent > 90 \wedge T.sname = S.sname)\}$
- IV.  $\{\langle S_N \rangle \mid \exists S_R \exists R_P (\langle S_R, S_N \rangle \in Students \wedge \langle S_R, 107, R_P \rangle \in Registration \wedge R_P > 90)\}$

- A. I, II, III and IV      B. I, II and III only  
 C. I, II and IV only      D. II, III and IV only

**Answer key****3.13.12 Relational Calculus: GATE IT 2006 | Question: 15**

Which of the following relational query languages have the same expressive power?

- I. Relational algebra
  - II. Tuple relational calculus restricted to safe expressions
  - III. Domain relational calculus restricted to safe expressions
- A. II and III only      B. I and II only      C. I and III only      D. I, II and III

**Answer key****3.13.13 Relational Calculus: GATE IT 2007 | Question: 65**

Consider a selection of the form  $\sigma_{A \leq 100}(r)$ , where  $r$  is a relation with 1000 tuples. Assume that the attribute values for  $A$  among the tuples are uniformly distributed in the interval  $[0, 500]$ . Which one of the following options is the best estimate of the number of tuples returned by the given selection query ?

- A. 50      B. 100      C. 150      D. 200

**Answer key****3.13.14 Relational Calculus: GATE IT 2008 | Question: 75**

Consider the following relational schema:

- Student(school-id, sch-roll-no, sname, saddress)
- School(school-id, sch-name, sch-address, sch-phone)
- Enrolment(school-id, sch-roll-no, erollno, examname)
- ExamResult(erollno, examname, marks)

Consider the following tuple relational calculus query.

$\{t \mid \exists E \in \text{Enrolment} \ t = E.\text{school-id} \wedge \mid\{x \mid x \in \text{Enrolment} \wedge x.\text{school-id} = t \wedge (\exists B \in \text{ExamResult} \ B.\text{erollno} = x.\text{erollno} \wedge B.\text{marks} > 35)\}\mid\}$

If a student needs to score more than 35 marks to pass an exam, what does the query return?

- A. The empty set
- B. schools with more than 35% of its students enrolled in some exam or the other
- C. schools with a pass percentage above 35% over all exams taken together
- D. schools with a pass percentage above 35% over each exam

**Answer key****3.14****Relational Model (1)****3.14.1 Relational Model: GATE CSE 2023 | Question: 6**

Which one of the options given below refers to the degree (or arity) of a relation in relational database systems?

- A. Number of attributes of its relation schema.
- B. Number of tuples stored in the relation.
- C. Number of entries in the relation.
- D. Number of distinct domains of its relation schema.

**Answer key****3.15****Safe Query (1)****3.15.1 Safe Query: GATE CSE 2017 Set 1 | Question: 41**

Consider a database that has the relation schemas EMP(EmpId, EmpName, DeptId), and DEPT(DeptName, DeptId). Note that the DeptId can be permitted to be NULL in the relation EMP. Consider the following queries on the database expressed in tuple relational calculus.

- $\{t \mid \exists u \in \text{EMP}(t[\text{EmpName}] = u[\text{EmpName}] \wedge \forall v \in \text{DEPT}(t[\text{DeptId}] \neq v[\text{DeptId}]))\}$
- $\{t \mid \exists u \in \text{EMP}(t[\text{EmpName}] = u[\text{EmpName}] \wedge \exists v \in \text{DEPT}(t[\text{DeptId}] \neq v[\text{DeptId}]))\}$
- $\{t \mid \exists u \in \text{EMP}(t[\text{EmpName}] = u[\text{EmpName}] \wedge \exists v \in \text{DEPT}(t[\text{DeptId}] = v[\text{DeptId}]))\}$

Which of the above queries are safe?

- A. I and II only      B. I and III only      C. II and III only      D. I, II and III

**Answer key****3.16****Sql (54)****3.16.1 Sql: GATE CSE 1988 | Question: 12iii**

Describe the relational algebraic expression giving the relation returned by the following SQL query.

```
Select SNAME
from S
Where SNOin
  (select SNO
   from SP
   where PNOin
     (select PNO
      from P
      Where COLOUR='BLUE'))
```

**Answer key****3.16.2 Sql: GATE CSE 1988 | Question: 12iv**

```
Select SNAME
from S
Where SNOin
  (select SNO
   from SP
   where PNOin
     (select PNO
      from P
      Where COLOUR='BLUE'))
```

What relations are being used in the above SQL query? Given at least two attributes of each of these relations.

**Answer key****3.16.3 Sql: GATE CSE 1990 | Question: 10-a**

Consider the following relational database:

- employees (eno, ename, address, basic-salary)
- projects (pno, pname, nos-of-staffs-allotted)
- working (pno, eno, pjob)

The queries regarding data in the above database are formulated below in SQL. Describe in ENGLISH sentences

the two queries that have been posted:

i. `SELECT ename  
FROM employees  
WHERE eno IN  
(SELECT eno  
FROM working  
GROUP BY eno  
HAVING COUNT(*)=  
(SELECT COUNT(*  
FROM projects))`

ii. `SELECT pname  
FROM projects  
WHERE pno IN  
(SELECT pno  
FROM projects  
MINUS  
SELECT DISTINCT pno  
FROM working);`

gate1990 descriptive databases sql

[Answer key](#)

#### 3.16.4 Sql: GATE CSE 1991 | Question: 12,b [top](#)



Suppose a database consist of the following relations:

SUPPLIER (SCODE,SNAME,CITY).

PART (PCODE,PNAME,PDESC,CITY).

PROJECTS (PRCODE,PRNAME,PRCITY).

SPPR (SCODE,PCODE,PRCODE,QTY).

Write algebraic solution to the following :

- i. Get SCODE values for suppliers who supply to both projects PR1 and PR2.
- ii. Get PRCODE values for projects supplied by at least one supplier not in the same city.

sql gate1991 normal databases descriptive

[Answer key](#)

#### 3.16.5 Sql: GATE CSE 1991 | Question: 12-a [top](#)



Suppose a database consist of the following relations:

SUPPLIER (SCODE,SNAME,CITY).

PART (PCODE,PNAME,PDESC,CITY).

PROJECTS (PRCODE,PRNAME,PRCITY).

SPPR (SCODE,PCODE,PRCODE,QTY).

Write SQL programs corresponding to the following queries:

- i. Print PCODE values for parts supplied to any project in DEHLI by a supplier in DELHI.
- ii. Print all triples <CITY, PCODE, CITY> such that a supplier in first city supplies the specified part to a project in the second city, but do not print the triples in which the two CITY values are same.

gate1991 databases sql normal descriptive

[Answer key](#)

#### 3.16.6 Sql: GATE CSE 1997 | Question: 76-b [top](#)



Consider the following relational database schema:

- EMP (eno name, age)
- PROJ (pno name)

- INVOLVED (eno, pno)

EMP contains information about employees. PROJ about projects and involved about which employees involved in which projects. The underlined attributes are the primary keys for the respective relations.

State in English (in not more than 15 words)

What the following relational algebra expressions are designed to determine

- $\Pi_{eno}(\text{INVOLVED}) - \Pi_{eno}((\Pi_{eno}(\text{INVOLVED}) \times \Pi_{pno}(\text{PROJ})) - \text{INVOLVED})$
- $\Pi_{age}(\text{EMP}) - \Pi_{age}(\sigma_{E.\text{age} < Emp.\text{age}}((\rho E(\text{EMP}) \times \text{EMP}))$

(Note:  $\rho E(\text{EMP})$  conceptually makes a copy of EMP and names it  $E$  ( $\rho$  is called the rename operator))

gate1997 databases sql descriptive normal

**Answer key** 

### 3.16.7 Sql: GATE CSE 1998 | Question: 7-a top



Suppose we have a database consisting of the following three relations.

- FREQUENTS (student, parlor) giving the parlors each student visits.
- SERVES (parlor, ice-cream) indicating what kind of ice-creams each parlor serves.
- LIKES (student, ice-cream) indicating what ice-creams each student likes.

(Assume that each student likes at least one ice-cream and frequents at least one parlor)

Express the following in SQL:

Print the students that frequent at least one parlor that serves some ice-cream that they like.

gate1998 databases sql descriptive

**Answer key** 

### 3.16.8 Sql: GATE CSE 1999 | Question: 2.25 top



Which of the following is/are correct?

- An SQL query automatically eliminates duplicates
- An SQL query will not work if there are no indexes on the relations
- SQL permits attribute names to be repeated in the same relation
- None of the above

gate1999 databases sql easy

**Answer key** 

### 3.16.9 Sql: GATE CSE 1999 | Question: 22-a top



Consider the set of relations

- EMP (Employee-no, Dept-no, Employee-name, Salary)
- DEPT (Dept-no, Dept-name, Location)

Write an SQL query to:

- Find all employees names who work in departments located at 'Calcutta' and whose salary is greater than Rs.50,000.
- Calculate, for each department number, the number of employees with a salary greater than Rs. 1,00,000.

gate1999 databases sql easy descriptive

**Answer key** 

### 3.16.10 Sql: GATE CSE 1999 | Question: 22-b top



Consider the set of relations

- EMP (Employee-no, Dept-no, Employee-name, Salary)
- DEPT (Dept-no, Dept-name, Location)

Write an SQL query to:

Calculate, for each department number, the number of employees with a salary greater than Rs. 1,00,000

gate1999 databases sql descriptive easy

[Answer key](#)

### 3.16.11 Sql: GATE CSE 2000 | Question: 2.25 top



Given relations r(w, x) and s(y, z) the result of

select distinct w, x  
from r, s

is guaranteed to be same as r, provided.

- A. r has no duplicates and s is non-empty  
B. r and s have no duplicates  
C. s has no duplicates and r is non-empty  
D. r and s have the same number of tuples

gatecse-2000 databases sql

[Answer key](#)

### 3.16.12 Sql: GATE CSE 2000 | Question: 2.26 top



In SQL, relations can contain null values, and comparisons with null values are treated as unknown. Suppose all comparisons with a null value are treated as false. Which of the following pairs is not equivalent?

- A.  $x = 5 \quad \text{not}(\text{not}(x = 5))$   
B.  $x = 5 \quad x > 4 \text{ and } x < 6$ , where  $x$  is an integer  
C.  $x \neq 5 \quad \text{not}(x = 5)$   
D. none of the above

gatecse-2000 databases sql normal

[Answer key](#)

### 3.16.13 Sql: GATE CSE 2000 | Question: 22 top



Consider a bank database with only one relation

transaction (transno, acctno, date, amount)

The amount attribute value is positive for deposits and negative for withdrawals.

- a. Define an SQL view TP containing the information (acctno, T1.date, T2.amount)  
for every pair of transaction T1, T2 and such that T1 and T2 are transaction on the same account and the date of T2 is  $\leq$  the date of T1.  
b. Using only the above view TP, write a query to find for each account the minimum balance it ever reached (not including the 0 balance when the account is created). Assume there is at most one transaction per day on each account and each account has at least one transaction since it was created. To simplify your query, break it up into 2 steps by defining an intermediate view V.

gatecse-2000 databases sql normal descriptive

[Answer key](#)

### 3.16.14 Sql: GATE CSE 2001 | Question: 2.25 [top](#)

Consider a relation geq which represents "greater than or equal to", that is,  $(x, y) \in \text{geq}$  only if  $y \geq x$ .



```
create table geq
(
    ib integer not null,
    ub integer not null,
    primary key ib,
    foreign key (ub) references geq on delete cascade
);
```

Which of the following is possible if tuple  $(x,y)$  is deleted?

- A. A tuple  $(z,w)$  with  $z > y$  is deleted
- B. A tuple  $(z,w)$  with  $z > x$  is deleted
- C. A tuple  $(z,w)$  with  $w < x$  is deleted
- D. The deletion of  $(x,y)$  is prohibited

gatecse-2001 databases sql normal

[Answer key](#)

### 3.16.15 Sql: GATE CSE 2001 | Question: 21-a [top](#)

Consider a relation examinee (regno, name, score), where regno is the primary key to score is a real number.



Write a relational algebra using  $(\Pi, \sigma, \rho, \times)$  to find the list of names which appear more than once in examinee.

gatecse-2001 databases sql normal descriptive

[Answer key](#)

### 3.16.16 Sql: GATE CSE 2001 | Question: 21-b [top](#)



Consider a relation examinee (regno, name, score), where regno is the primary key to score is a real number.

Write an SQL query to list the *regno* of examinees who have a score greater than the average score.

gatecse-2001 databases sql normal descriptive

[Answer key](#)

### 3.16.17 Sql: GATE CSE 2001 | Question: 21-c [top](#)



Consider a relation examinee (regno, name, score), where regno is the primary key to score is a real number.

Suppose the relation appears (regno, centr\_code) specifies the center where an examinee appears. Write an SQL query to list the centr\_code having an examinee of score greater than 80.

gatecse-2001 databases sql normal descriptive

[Answer key](#)

### 3.16.18 Sql: GATE CSE 2003 | Question: 86 [top](#)



Consider the set of relations shown below and the SQL query that follows.

Students: (Roll\_number, Name, Date\_of\_birth)

Courses: (Course\_number, Course\_name, Instructor)

Grades: (Roll\_number, Course\_number, Grade)

```
Select distinct Name
from Students, Courses, Grades
where Students.Roll_number=Grades.Roll_number
and Courses.Instructor = 'Korth'
and Courses.Course_number = Grades.Course_number
and Grades.Grade = 'A'
```

Which of the following sets is computed by the above query?

- A. Names of students who have got an A grade in all courses taught by Korth  
 B. Names of students who have got an A grade in all courses  
 C. Names of students who have got an A grade in at least one of the courses taught by Korth  
 D. None of the above

gatecse-2003 databases sql easy

[Answer key](#)

### 3.16.19 Sql: GATE CSE 2004 | Question: 53 [top](#)



The employee information in a company is stored in the relation

- Employee (name, sex, salary, deptName)

Consider the following SQL query

```
Select deptName
  From Employee
  Where sex = 'M'
  Group by deptName
  Having avg(salary) >
    (select avg (salary) from Employee)
```

It returns the names of the department in which

- the average salary is more than the average salary in the company
- the average salary of male employees is more than the average salary of all male employees in the company
- the average salary of male employees is more than the average salary of employees in same the department
- the average salary of male employees is more than the average salary in the company

gatecse-2004 databases sql normal

[Answer key](#)

### 3.16.20 Sql: GATE CSE 2005 | Question: 77, ISRO2016-55 [top](#)



The relation **book** (*title, price*) contains the titles and prices of different books. Assuming that no two books have the same price, what does the following SQL query list?

```
select title
  from book as B
 where (select count(*)
       from book as T
      where T.price>B.price) < 5
```

- Titles of the four most expensive books
- Title of the fifth most inexpensive book
- Title of the fifth most expensive book
- Titles of the five most expensive books

gatecse-2005 databases sql easy isro2016

[Answer key](#)

### 3.16.21 Sql: GATE CSE 2006 | Question: 67 [top](#)



Consider the relation account (customer, balance) where the customer is a primary key and there are no null values. We would like to rank customers according to decreasing balance. The customer with the largest balance gets rank 1. Ties are not broke but ranks are skipped: if exactly two customers have the largest balance they each get rank 1 and rank 2 is not assigned.

Query1:

```
select A.customer, count(B.customer)
  from account A, account B
```

```
where A.balance <=B.balance  
group by A.customer
```

### Query2:

```
select A.customer, 1+count(B.customer)  
from account A, account B  
where A.balance < B.balance  
group by A.customer
```

Consider these statements about Query1 and Query2.

1. Query1 will produce the same row set as Query2 for some but not all databases.
2. Both Query1 and Query 2 are a correct implementation of the specification
3. Query1 is a correct implementation of the specification but Query2 is not
4. Neither Query1 nor Query2 is a correct implementation of the specification
5. Assigning rank with a pure relational query takes less time than scanning in decreasing balance order assigning ranks using ODBC.

Which two of the above statements are correct?

- A. 2 and 5      B. 1 and 3      C. 1 and 4      D. 3 and 5

gatecse-2006 databases sql normal

[Answer key](#) 

### 3.16.22 Sql: GATE CSE 2006 | Question: 68 [top](#)

Consider the relation enrolled (student, course) in which (student, course) is the primary key, and the relation paid (student, amount) where student is the primary key. Assume no null values and no foreign keys or integrity constraints.

Given the following four queries:

Query1:

```
select student from enrolled where student in (select student from paid)
```

Query2:

```
select student from paid where student in (select student from enrolled)
```

Query3:

```
select E.student from enrolled E, paid P where E.student = P.student
```

Query4:

```
select student from paid where exists  
(select * from enrolled where enrolled.student = paid.student)
```

Which one of the following statements is correct?

- A. All queries return identical row sets for any database
- B. Query2 and Query4 return identical row sets for all databases but there exist databases for which Query1 and Query2 return different row sets
- C. There exist databases for which Query3 returns strictly fewer rows than Query2
- D. There exist databases for which Query4 will encounter an integrity violation at runtime

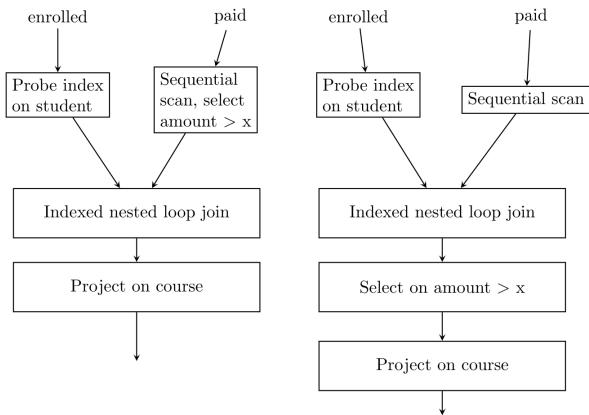
gatecse-2006 databases sql normal

[Answer key](#) 

### 3.16.23 Sql: GATE CSE 2006 | Question: 69 [top](#)

Consider the relation enrolled (student, course) in which (student, course) is the primary key, and the relation paid (student, amount) where student is the primary key. Assume no null values and no foreign keys or integrity constraints. Assume that amounts 6000, 7000, 8000, 9000 and 10000 were each paid by 20% of the students. Consider these query plans (Plan 1 on left, Plan 2 on right) to "list all courses taken by students who have

*paid more than x"*



A disk seek takes  $4ms$ , disk data transfer bandwidth is  $300 \text{ MB/s}$  and checking a tuple to see if amount is greater than  $x$  takes  $10\mu\text{s}$ . Which of the following statements is correct?

- A. Plan 1 and Plan 2 will not output identical row sets for all databases
- B. A course may be listed more than once in the output of Plan 1 for some databases
- C. For  $x = 5000$ , Plan 1 executes faster than Plan 2 for all databases
- D. For  $x = 9000$ , Plan 1 executes slower than Plan 2 for all databases

gatecse-2006 databases sql normal

[Answer key](#)

### 3.16.24 Sql: GATE CSE 2007 | Question: 61 [top](#)

Consider the table **employee**(*empld*, name, department, salary) and the two queries  $Q_1, Q_2$  below. Assuming that department 5 has more than one employee, and we want to find the employees who get higher salary than anyone in the department 5, which one of the statements is **TRUE** for any arbitrary employee table?

$Q_1 :$   
Select e.empld  
From employee e  
Where not exists  
(Select \* From employee s Where s.department = "5" and s.salary >= e.salary)

$Q_2 :$   
Select e.empld  
From employee e  
Where e.salary > Any  
(Select distinct salary From employee s Where s.department = "5")

- A.  $Q_1$  is the correct query
- B.  $Q_2$  is the correct query
- C. Both  $Q_1$  and  $Q_2$  produce the same answer
- D. Neither  $Q_1$  nor  $Q_2$  is the correct query

gatecse-2007 databases sql normal verbal-aptitude

[Answer key](#)

### 3.16.25 Sql: GATE CSE 2009 | Question: 55 [top](#)

Consider the following relational schema:

**Suppliers**(*sid*:integer , sname:string, city:string, street:string)

**Parts**(*pid*:integer , pname:string, color:string)

**Catalog**(*sid*:integer, *pid*:integer , cost:real)

Consider the following relational query on the above database:

SELECT S.sname

```

FROM Suppliers S
WHERE S.sid NOT IN (SELECT C.sid
                      FROM Catalog C
                      WHERE C.pid NOT IN (SELECT P.pid
                                           FROM Parts P
                                           WHERE P.color<>'blue'))

```

Assume that relations corresponding to the above schema are not empty. Which one of the following is the correct interpretation of the above query?

- A. Find the names of all suppliers who have supplied a non-blue part.
- B. Find the names of all suppliers who have not supplied a non-blue part.
- C. Find the names of all suppliers who have supplied only non-blue part.
- D. Find the names of all suppliers who have not supplied only blue parts.

gatecse-2009 databases sql normal

[Answer key](#)

### 3.16.26 Sql: GATE CSE 2009 | Question: 56 [top](#)



Consider the following relational schema:

**Suppliers**(sid:integer , sname:string, city:string, street:string)

**Parts**(pid:integer , pname:string, color:string)

**Catalog**(sid:integer, pid:integer , cost:real)

Assume that, in the suppliers relation above, each supplier and each street within a city has unique name, and (sname, city) forms a candidate key. No other functional dependencies are implied other than those implied by primary and candidate keys. Which one of the following is TRUE about the above schema?

- |  |   |
|--|---|
| A. The schema is in BCNF               | B. The schema is in 3NF but not in BCNF |
| C. The schema is in 2NF but not in 3NF | D. The schema is not in 2NF             |

gatecse-2009 databases sql database-normalization normal

[Answer key](#)

### 3.16.27 Sql: GATE CSE 2010 | Question: 19 [top](#)



A relational schema for a train reservation database is given below.

- **passenger(pid, pname, age)**
- **reservation(pid, class, tid)**

Passenger		
<b>pid</b>	<b>pname</b>	<b>Age</b>
0	Sachine	65
1	Rahul	66
2	Sourav	67
3	Anil	69

Reservation		
<b>pid</b>	<b>class</b>	<b>tid</b>
0	AC	8200
1	AC	8201
2	SC	8201
5	AC	8203
1	SC	8204
3	AC	8202

What **uids** are returned by the following SQL query for the above instance of the tables?

```

SELECT pid
FROM Reservation
WHERE class='AC' AND
      EXISTS (SELECT *
              FROM Passenger

```

```
WHERE age>65 AND  
Passenger.pid=Reservation.pid)
```

- A. 1,0      B. 1,2      C. 1,3      D. 1,5

gatecse-2010 databases sql normal

Answer key 

### 3.16.28 Sql: GATE CSE 2011 | Question: 32



Consider a database table T containing two columns X and Y each of type integer. After the creation of the table, one record (X=1, Y=1) is inserted in the table.

Let MX and MY denote the respective maximum values of X and Y among all records in the table at any point in time. Using MX and MY, new records are inserted in the table 128 times with X and Y values being  $MX+1, 2*MY+1$  respectively. It may be noted that each time after the insertion, values of MX and MY change.

What will be the output of the following SQL query after the steps mentioned above are carried out?

```
SELECT Y FROM T WHERE X=7;
```

- A. 127      B. 255      C. 129      D. 257

gatecse-2011 databases sql normal

Answer key 

### 3.16.29 Sql: GATE CSE 2011 | Question: 46



Database table by name Loan\_Records is given below.

Borrower	Bank_Manager	Loan_Amount
Ramesh	Sunderajan	10000.00
Suresh	Ramgopal	5000.00
Mahesh	Sunderajan	7000.00

What is the output of the following SQL query?

```
SELECT count(*)  
FROM (  
    SELECT Borrower, Bank_Manager FROM Loan_Records) AS S  
    NATURAL JOIN  
    (SELECT Bank_Manager, Loan_Amount FROM Loan_Records) AS T  
)
```

- A. 3      B. 9      C. 5      D. 6

gatecse-2011 databases sql normal

Answer key 

### 3.16.30 Sql: GATE CSE 2012 | Question: 15



Which of the following statements are **TRUE** about an SQL query?

- P : An SQL query can contain a HAVING clause even if it does not have a GROUP BY clause  
Q : An SQL query can contain a HAVING clause only if it has a GROUP BY clause  
R : All attributes used in the GROUP BY clause must appear in the SELECT clause  
S : Not all attributes used in the GROUP BY clause need to appear in the SELECT clause

- A. P and R      B. P and S      C. Q and R      D. Q and S

gatecse-2012 databases easy sql ambiguous

Answer key 

### 3.16.31 Sql: GATE CSE 2012 | Question: 51 [top](#)



Consider the following relations *A*, *B* and *C*:

A		
<b>Id</b>	<b>Name</b>	<b>Age</b>
12	Arun	60
15	Shreya	24
99	Rohit	11

B		
<b>Id</b>	<b>Name</b>	<b>Age</b>
15	Shreya	24
25	Hari	40
98	Rohit	20
99	Rohit	11

C		
<b>Id</b>	<b>Phone</b>	<b>Area</b>
10	2200	02
99	2100	01

How many tuples does the result of the following SQL query contain?

```
SELECT A.Id  
FROM A  
WHERE A.Age > ALL (SELECT B.Age  
                     FROM B  
                     WHERE B.Name = 'Arun')
```

- A. 4      B. 3      C. 0      D. 1

gatecse-2012 databases normal sql

[Answer key](#)

### 3.16.32 Sql: GATE CSE 2014 Set 1 | Question: 22 [top](#)



Given the following statements:

**S1:** A foreign key declaration can always be replaced by an equivalent check assertion in SQL.

**S2:** Given the table *R(a, b, c)* where *a* and *b* together form the primary key, the following is a valid table definition.

```
CREATE TABLE S (  
    a INTEGER,  
    d INTEGER,  
    e INTEGER,  
    PRIMARY KEY (d),  
    FOREIGN KEY (a) REFERENCES R)
```

Which one of the following statements is **CORRECT**?

- A. S1 is TRUE and S2 is FALSE      B. Both S1 and S2 are TRUE  
C. S1 is FALSE and S2 is TRUE      D. Both S1 and S2 are FALSE

gatecse-2014-set1 databases normal sql

[Answer key](#)

### 3.16.33 Sql: GATE CSE 2014 Set 1 | Question: 54 [top](#)



Given the following schema:

```
employees(emp-id, first-name, last-name, hire-date, dept-id, salary)  
departments(dept-id, dept-name, manager-id, location-id)
```

You want to display the last names and hire dates of all latest hires in their respective departments in the location ID 1700. You issue the following query:

```
SQL>SELECT last-name, hire-date  
      FROM employees  
      WHERE (dept-id, hire-date) IN  
            (SELECT dept-id, MAX(hire-date))  
      FROM employees JOIN departments USING(dept-id)  
      WHERE location-id = 1700  
      GROUP BY dept-id;
```

What is the outcome?

- A. It executes but does not give the correct result

- B. It executes and gives the correct result.  
 C. It generates an error because of pairwise comparison.  
 D. It generates an error because of the GROUP BY clause cannot be used with table joins in a sub-query.

gatecse-2014-set1 databases sql normal

[Answer key](#)

### 3.16.34 Sql: GATE CSE 2014 Set 2 | Question: 54 top

SQL allows duplicate tuples in relations, and correspondingly defines the multiplicity of tuples in the result of joins. Which one of the following queries always gives the same answer as the nested query shown below:

`select * from R where a in (select S.a from S)`

- A. select R.\* from R, S where R.a=S.a  
 B. select distinct R.\* from R,S where R.a=S.a  
 C. select R.\* from R,(select distinct a from S) as S1 where R.a=S1.a  
 D. select R.\* from R,S where R.a=S.a and is unique R

gatecse-2014-set2 databases sql normal

[Answer key](#)

### 3.16.35 Sql: GATE CSE 2014 Set 3 | Question: 54 top

Consider the following relational schema:

employee (emplId,empName,empDept)

customer (custId,custName,salesRepId,rating)

**salesRepId** is a foreign key referring to **emplId** of the employee relation. Assume that each employee makes a sale to at least one customer. What does the following query return?

```
SELECT empName FROM employee E
WHERE NOT EXISTS (SELECT custId
                   FROM customer C
                   WHERE C.salesRepId = E.emplId
                   AND C.rating <> 'GOOD');
```

- A. Names of all the employees with at least one of their customers having a 'GOOD' rating.  
 B. Names of all the employees with at most one of their customers having a 'GOOD' rating.  
 C. Names of all the employees with none of their customers having a 'GOOD' rating.  
 D. Names of all the employees with all their customers having a 'GOOD' rating.

gatecse-2014-set3 databases sql easy

[Answer key](#)

### 3.16.36 Sql: GATE CSE 2015 Set 1 | Question: 27 top

Consider the following relation:

Student	
<u>Roll_No</u>	<u>Student_Name</u>
1	Raj
2	Rohit
3	Raj

Performance		
<u>Roll_No</u>	<u>Course</u>	<u>Marks</u>
1	Math	80
1	English	70
2	Math	75
3	English	80
2	Physics	65
3	Math	80

Consider the following SQL query.

```

SELECT S.Student_Name, Sum(P.Marks)
FROM Student S, Performance P
WHERE S.Roll_No= P.Roll_No
GROUP BY S.STUDENT_Name

```

The numbers of rows that will be returned by the SQL query is \_\_\_\_\_.

gatecse-2015-set1 databases sql normal numerical-answers

[Answer key](#)

### 3.16.37 Sql: GATE CSE 2015 Set 3 | Question: 3 top



Consider the following relation

Cinema(*theater, address, capacity*)

Which of the following options will be needed at the end of the SQL query

```

SELECT P1.address
FROM Cinema P1

```

such that it always finds the addresses of theaters with maximum capacity?

- A. WHERE P1.capacity >= All (select P2.capacity from Cinema P2)
- B. WHERE P1.capacity >= Any (select P2.capacity from Cinema P2)
- C. WHERE P1.capacity > All (select max(P2.capacity) from Cinema P2)
- D. WHERE P1.capacity > Any (select max(P2.capacity) from Cinema P2)

gatecse-2015-set3 databases sql normal

[Answer key](#)

### 3.16.38 Sql: GATE CSE 2016 Set 2 | Question: 52 top



Consider the following database table named water\_schemes:

Water_schemes		
scheme_no	district_name	capacity
1	Ajmer	20
1	Bikaner	10
2	Bikaner	10
3	Bikaner	20
1	Churu	10
2	Churu	20
1	Dungargarh	10

The number of tuples returned by the following SQL query is \_\_\_\_\_.

```

with total (name, capacity) as
  select district_name, sum(capacity)
  from water_schemes
  group by district_name
with total_avg (capacity) as
  select avg(capacity)
  from total
select name
  from total, total_avg
  where total.capacity >= total_avg.capacity

```

gatecse-2016-set2 databases sql normal numerical-answers

[Answer key](#)

**3.16.39 Sql: GATE CSE 2017 Set 1 | Question: 23**

Consider a database that has the relation schema EMP (Empld, EmpName, and DeptName). An instance of the schema EMP and a SQL query on it are given below:

EMP		
Empld	EmpName	DeptName
1	XYA	AA
2	XYB	AA
3	XYC	AA
4	XYD	AA
5	XYE	AB
6	XYF	AB
7	XYG	AB
8	XYH	AC
9	XYI	AC
10	XYJ	AC
11	XYK	AD
12	XYL	AD
13	XYM	AE

```
SELECT AVG(EC.Num)
FROM EC
WHERE (DeptName, Num) IN
    (SELECT DeptName, COUNT(Empld) AS
     EC(DeptName, Num)
    FROM EMP
    GROUP BY DeptName)
```

The output of executing the SQL query is \_\_\_\_\_.

gatecse-2017-set1 databases sql numerical-answers

**Answer key**

**3.16.40 Sql: GATE CSE 2017 Set 2 | Question: 46**

Consider the following database table named top\_scorer.

top_scorer		
player	country	goals
Klose	Germany	16
Ronaldo	Brazil	15
G Muller	Germany	14
Fontaine	France	13
Pele	Brazil	12
Klinsmann	Germany	11
Kocsis	Hungary	11
Batistuta	Argentina	10
Cubillas	Peru	10
Lato	Poland	10
Lineker	England	10
T Muller	Germany	10
Rahn	Germany	10

Consider the following SQL query:

```
SELECT ta.player FROM top_scorer AS ta
WHERE ta.goals > ALL (SELECT tb.goals
    FROM top_scorer AS tb
    WHERE tb.country = 'Spain')
AND ta.goals > ANY (SELECT tc.goals
    FROM top_scorer AS tc
    WHERE tc.country='Germany')
```

The number of tuples returned by the above SQL query is \_\_\_\_\_

gatecse-2017-set2 databases sql numerical-answers

**Answer key** 

### 3.16.41 Sql: GATE CSE 2018 | Question: 12 top



Consider the following two tables and four queries in SQL.

Book (isbn, bname), Stock(isbn, copies)

Query 1:

```
SELECT B.isbn, S.copies FROM Book B INNER JOIN Stock S ON B.isbn=S.isbn;
```

Query 2:

```
SELECT B.isbn, S.copies FROM Book B LEFT OUTER JOIN Stock S ON B.isbn=S.isbn;
```

Query 3:

```
SELECT B.isbn, S.copies FROM Book B RIGHT OUTER JOIN Stock S ON B.isbn=S.isbn
```

Query 4:

```
SELECT B.isbn, S.copies FROM Book B FULL OUTER JOIN Stock S ON B.isbn=S.isbn
```

Which one of the queries above is certain to have an output that is a superset of the outputs of the other three queries?

- A. Query 1
- B. Query 2
- C. Query 3
- D. Query 4

gatecse-2018 databases sql easy 1-mark

**Answer key** 

### 3.16.42 Sql: GATE CSE 2019 | Question: 51 top



A relational database contains two tables Student and Performance as shown below:

Table: student	
Roll_no	Student_name
1	Amit
2	Priya
3	Vinit
4	Rohan
5	Smita

Table: Performance		
Roll_no	Subject_code	Marks
1	A	86
1	B	95
1	C	90
2	A	89
2	C	92
3	C	80

The primary key of the Student table is Roll\_no. For the performance table, the columns Roll\_no. and Subject\_code together form the primary key. Consider the SQL query given below:

```
SELECT S.Student_name, sum(P.Marks)
FROM Student S, Performance P
WHERE P.Marks > 84
GROUP BY S.Student_name;
```

The number of rows returned by the above SQL query is \_\_\_\_\_

gatecse-2019 numerical-answers databases sql 2-marks

Answer key

### 3.16.43 Sql: GATE CSE 2020 | Question: 13 top



Consider a relational database containing the following schemas.

Catalogue		
sno	pno	cost
S1	P1	150
S1	P2	50
S1	P3	100
S2	P4	200
S2	P5	250
S3	P1	250
S3	P2	150
S3	P5	300
S3	P4	250

Suppliers		
sno	sname	location
S1	M/s Royal furniture	Delhi
S2	M/s Balaji furniture	Bangalore
S3	M/s Premium furniture	Chennai

Parts		
pno	pname	part_spec
P1	Table	Wood
P2	Chair	Wood
P3	Table	Steel
P4	Almirah	Steel
P5	Almirah	Wood

The primary key of each table is indicated by underlining the constituent fields.

```
SELECT s.sno, s.sname
FROM Suppliers s, Catalogue c
WHERE s.sno=c.sno AND
cost > (SELECT AVG(cost)
FROM Catalogue
WHERE pno = 'P4'
GROUP BY pno);
```

The number of rows returned by the above SQL query is

- A. 4      B. 5      C. 0      D. 2

gatecse-2020 databases sql 1-mark

Answer key

### 3.16.44 Sql: GATE CSE 2021 Set 1 | Question: 23 top



A relation  $r(A, B)$  in a relational database has 1200 tuples. The attribute  $A$  has integer values ranging from 6 to 20, and the attribute  $B$  has integer values ranging from 1 to 20. Assume that the attributes  $A$  and  $B$  are independently distributed.

The estimated number of tuples in the output of  $\sigma_{(A>10) \vee (B=18)}(r)$  is \_\_\_\_\_.

gatecse-2021-set1 databases sql numerical-answers 1-mark

[Answer key](#)

### 3.16.45 Sql: GATE CSE 2021 Set 2 | Question: 31 top



The relation scheme given below is used to store information about the employees of a company, where **empId** is the key and **deptId** indicates the department to which the employee is assigned. Each employee is assigned to exactly one department.

**emp(empId, name, gender, salary, deptId)**

Consider the following SQL query:

```
select deptId, count(*)
from emp
where gender = "female" and salary > (select avg(salary)from emp)
group by deptId;
```

The above query gives, for each department in the company, the number of female employees whose salary is greater than the average salary of

- A. employees in the department  
B. employees in the company  
C. female employees in the department  
D. female employees in the company

gatecse-2021-set2 databases sql easy 2-marks

[Answer key](#)

### 3.16.46 Sql: GATE CSE 2022 | Question: 46 top



Consider the relational database with the following four schemas and their respective instances.

- Student(sNo, sName, dNo) Dept(dNo, dName)
- Course(cNo, cName, dNo) Register(sNo, cNo)

	Students	
sNo	sName	dNo
S01	James	D01
S02	Rocky	D01
S03	Jackson	D02
S04	Jane	D01
S05	Milli	D02

	Depth	
dNo	dName	
C11	DS	D01
C12	OS	D01
C21	DE	D02
C22	PT	D02
C23	CV	D03

	Course	
cNo	cName	dNo
C11	DS	D01
C12	OS	D01
C21	DE	D02
C22	PT	D02
C23	CV	D03

	Register
sNo	cNo
S01	C11
S01	C12
S02	C11
S03	C21
S03	C22
S03	C23
S04	C11
S04	C12
S05	C11
S05	C21

### SQL query

```
SELECT * FROM Student AS S WHERE NOT EXISTS
(SELECT cNo FROM Course WHERE dNo = "D01"
```

EXCEPT

```
SELECT cNo FROM Register WHERE sNo = S.sNo)
```

The number of rows returned by the above SQL query is \_\_\_\_\_.

gatecse-2022 databases sql 2-marks

Answer key 

### 3.16.47 Sql: GATE CSE 2023 | Question: 51

Consider the following table named Student in a relational database. The primary key of this table is rollNum.

Student

rollNum	name	gender	marks
1	Naman	M	62
2	Aliya	F	70
3	Aliya	F	80
4	James	M	82
5	Swati	F	65

The SQL query below is executed on this database.

```
SELECT *  
FROM Student  
WHERE gender = 'F' AND  
marks > 65;
```

The number of rows returned by the query is \_\_\_\_\_.

gatecse-2023 databases sql numerical-answers 2-marks

Answer key 

### 3.16.48 Sql: GATE IT 2004 | Question: 74

A relational database contains two tables student and department in which student table has columns roll\_no, name and dept\_id and department table has columns dept\_id and dept\_name. The following insert statements were executed successfully to populate the empty tables:

```
Insert into department values (1, 'Mathematics')  
Insert into department values (2, 'Physics')  
Insert into student values (1, 'Navin', 1)  
Insert into student values (2, 'Mukesh', 2)  
Insert into student values (3, 'Gita', 1)
```

How many rows and columns will be retrieved by the following SQL statement?

Select \* from student, department

- A. 0 row and 4 columns  
B. 3 rows and 4 columns  
C. 3 rows and 5 columns  
D. 6 rows and 5 columns

gateit-2004 databases sql normal

Answer key 

### 3.16.49 Sql: GATE IT 2004 | Question: 76

A table T1 in a relational database has the following rows and columns:

Roll no.	Marks
1	10
2	20
3	30
4	NULL

The following sequence of SQL statements was successfully executed on table T1.

```
Update T1 set marks = marks + 5  
Select avg(marks) from T1
```

What is the output of the select statement?

- A. 18.75      B. 20      C. 25      D. Null

gateit-2004 databases sql normal

[Answer key](#)

### 3.16.50 Sql: GATE IT 2004 | Question: 78 top ↗



Consider two tables in a relational database with columns and rows as follows:

Table: Student

Roll_no	Name	Dept_id
1	ABC	1
2	DEF	1
3	GHI	2
4	JKL	3

Table: Department

Dept_id	Dept_name
1	A
2	B
3	C

Roll\_no is the primary key of the Student table, Dept\_id is the primary key of the Department table and Student.Dept\_id is a foreign key from Department.Dept\_id

What will happen if we try to execute the following two SQL statements?

- update Student set Dept\_id = Null where Roll\_no = 1
- update Department set Dept\_id = Null where Dept\_id = 1

A. Both i and ii will fail  
C. i will succeed but ii will fail

B. i will fail but ii will succeed  
D. Both i and ii will succeed

gateit-2004 databases sql normal

[Answer key](#)

### 3.16.51 Sql: GATE IT 2005 | Question: 69 top ↗



In an inventory management system implemented at a trading corporation, there are several tables designed to hold all the information. Amongst these, the following two tables hold information on which items are supplied by which suppliers, and which warehouse keeps which items along with the stock-level of these items.

Supply = (supplierid, itemcode)

Inventory = (itemcode, warehouse, stocklevel)

For a specific information required by the management, following SQL query has been written

```
Select distinct STMP.supplierid  
From Supply as STMP  
Where not unique (Select ITMP.supplierid  
From Inventory, Supply as ITMP  
Where STMP.supplierid = ITMP.supplierid  
And ITMP.itemcode = Inventory.itemcode  
And Inventory.warehouse = 'Nagpur');
```

For the warehouse at Nagpur, this query will find all suppliers who

- A. do not supply any item  
C. supply one or more items
- B. supply exactly one item  
D. supply two or more items

gateit-2005 databases sql normal

[Answer key](#)

**3.16.52 Sql: GATE IT 2006 | Question: 84**



Consider a database with three relation instances shown below. The primary keys for the Drivers and Cars relation are *did* and *cid* respectively and the records are stored in ascending order of these primary keys as given in the tables. No indexing is available in the database.

D: Drivers relation

did	dname	rating	age
22	Karthikeyan	7	25
29	Salman	1	33
31	Boris	8	55
32	Amoldt	8	25
58	Schumacher	10	35
64	Sachin	7	35
71	Senna	10	16
74	Sachin	9	35
85	Rahul	3	25
95	Ralph	3	53

R: Reserves relation

did	Cid	day
22	101	10 / 10 / 06
22	102	10 / 10 / 06
22	103	08 / 10 / 06
22	104	07 / 10 / 06
31	102	10 / 11 / 16
31	103	06 / 11 / 16
31	104	12 / 11 / 16
64	101	05 / 09 / 06
64	102	08 / 09 / 06
74	103	08 / 09 / 06

C: Cars relation

Cid	Cname	colour
101	Renault	blue
102	Renault	red
103	Ferrari	green
104	Jaguar	red

What is the output of the following SQL query?

```
select D.dname
from Drivers D
where D.did in (
    select R.did
    from Cars C, Reserves R
    where R.cid = C.cid and C.colour = 'red'
    intersect
    select R.did
    from Cars C, Reserves R
    where R.cid = C.cid and C.colour = 'green'
)
```

- A. Karthikeyan, Boris  
 C. Karthikeyan, Boris, Sachin

- B. Sachin, Salman  
 D. Schumacher, Senna

gateit-2006 databases sql normal

Answer key

**3.16.53 Sql: GATE IT 2006 | Question: 85**



Consider a database with three relation instances shown below. The primary keys for the Drivers and Cars relation are *did* and *cid* respectively and the records are stored in ascending order of these primary keys as given in the tables. No indexing is available in the database.

D: Drivers relation

<b>did</b>	<b>dname</b>	<b>rating</b>	<b>age</b>
22	Karthikeyan	7	25
29	Salman	1	33
31	Boris	8	55
32	Amoldt	8	25
58	Schumacher	10	35
64	Sachin	7	35
71	Senna	10	16
74	Sachin	9	35
85	Rahul	3	25
95	Ralph	3	53

R: Reserves relation

<b>did</b>	<b>Cid</b>	<b>day</b>
22	101	10 – 10 – 06
22	102	10 – 10 – 06
22	103	08 – 10 – 06
22	104	07 – 10 – 06
31	102	10 – 11 – 16
31	103	06 – 11 – 16
31	104	12 – 11 – 16
64	101	05 – 09 – 06
64	102	08 – 09 – 06
74	103	08 – 09 – 06

C: Cars relation

<b>Cid</b>	<b>Cname</b>	<b>colour</b>
101	Renault	blue
102	Renault	red
103	Ferrari	green
104	Jaguar	red

```

select D.dname
from Drivers D
where D.did in (
    select R.did
    from Cars C, Reserves R
    where R.cid = C.cid and C.colour = 'red'
    intersect
    select R.did
    from Cars C, Reserves R
    where R.cid = C.cid and C.colour = 'green'
)

```

Let  $n$  be the number of comparisons performed when the above SQL query is optimally executed. If linear search is used to locate a tuple in a relation using primary key, then  $n$  lies in the range:

- A. 36 – 40      B. 44 – 48      C. 60 – 64      D. 100 – 104

gateit-2006 databases sql normal

Answer key 

### 3.16.54 Sql: GATE IT 2008 | Question: 74 top ↗



Consider the following relational schema:

- Student(school-id, sch-roll-no, sname, saddress)
- School(school-id, sch-name, sch-address, sch-phone)
- Enrolment(school-id, sch-roll-no, erollno, examname)
- ExamResult(erollno, examname, marks)

What does the following SQL query output?

```

SELECT sch-name, COUNT (*)
FROM School C, Enrolment E, ExamResult R
WHERE E.school-id = C.school-id
AND
E.examname = R.examname AND E.erollno = R.erollno
AND
R.marks = 100 AND S.school-id IN (SELECT school-id
                                    FROM student
                                    GROUP BY school-id
                                    HAVING COUNT (*) > 200)
GROUP By school-id

```

- A. for each school with more than 200 students appearing in exams, the name of the school and the number of 100s scored by its students
- B. for each school with more than 200 students in it, the name of the school and the number of 100s scored by its students
- C. for each school with more than 200 students in it, the name of the school and the number of its students scoring 100 in at least one exam
- D. nothing; the query has a syntax error

gateit-2008 databases sql normal

[Answer key](#)

3.17

Timestamp Ordering (1) [top](#)

### 3.17.1 Timestamp Ordering: GATE CSE 2017 Set 1 | Question: 42 [top](#)



In a database system, unique timestamps are assigned to each transaction using Lamport's logical clock. Let  $TS(T_1)$  and  $TS(T_2)$  be the timestamps of transactions  $T_1$  and  $T_2$  respectively. Besides,  $T_1$  holds a lock on the resource  $R$ , and  $T_2$  has requested a conflicting lock on the same resource  $R$ . The following algorithm is used to prevent deadlocks in the database system assuming that a killed transaction is restarted with the same timestamp.

```

if  $TS(T_2) < TS(T_1)$  then
     $T_1$  is killed
else  $T_2$  waits.

```

Assume any transaction that is not killed terminates eventually. Which of the following is TRUE about the database system that uses the above algorithm to prevent deadlocks?

- A. The database system is both deadlock-free and starvation-free.
- B. The database system is deadlock-free, but not starvation-free.
- C. The database system is starvation-free, but not deadlock-free.
- D. The database system is neither deadlock-free nor starvation-free.

gatecse-2017-set1 databases timestamp-ordering deadlock-prevention-avoidance-detection normal

[Answer key](#)

3.18

Transaction And Concurrency (28) [top](#)



### 3.18.1 Transaction And Concurrency: GATE CSE 1999 | Question: 2.6 [top](#)

For the schedule given below, which of the following is correct:

- |   |         |
|---|---------|
| 1 | Read A  |
| 2 | Read B  |
| 3 | Write A |
| 4 | Read A  |
| 5 | Write A |
| 6 | Write B |
| 7 | Read B  |
| 8 | Write B |

- A. This schedule is serializable and can occur in a scheme using 2PL protocol
- B. This schedule is serializable but cannot occur in a scheme using 2PL protocol
- C. This schedule is not serializable but can occur in a scheme using 2PL protocol
- D. This schedule is not serializable and cannot occur in a scheme using 2PL protocol

**Answer key****3.18.2 Transaction And Concurrency: GATE CSE 2003 | Question: 29, ISRO2009-73**

Which of the following scenarios may lead to an irrecoverable error in a database system?

- A. A transaction writes a data item after it is read by an uncommitted transaction
- B. A transaction reads a data item after it is read by an uncommitted transaction
- C. A transaction reads a data item after it is written by a committed transaction
- D. A transaction reads a data item after it is written by an uncommitted transaction

**Answer key****3.18.3 Transaction And Concurrency: GATE CSE 2003 | Question: 87**

Consider three data items  $D_1$ ,  $D_2$ , and  $D_3$ , and the following execution schedule of transactions  $T_1$ ,  $T_2$ , and  $T_3$ . In the diagram,  $R(D)$  and  $W(D)$  denote the actions reading and writing the data item  $D$  respectively.

<b>T1</b>	<b>T2</b>	<b>T3</b>
	R( $D_3$ ); R( $D_2$ ); W( $D_2$ );	
R( $D_1$ ); W( $D_1$ );		R( $D_2$ ); R( $D_3$ );
	R( $D_1$ ); R( $D_2$ ); W( $D_2$ );	W( $D_2$ ); W( $D_3$ );  W( $D_1$ );

Which of the following statements is correct?

- A. The schedule is serializable as  $T_2; T_3; T_1$
- B. The schedule is serializable as  $T_2; T_1; T_3$
- C. The schedule is serializable as  $T_3; T_2; T_1$
- D. The schedule is not serializable

**Answer key****3.18.4 Transaction And Concurrency: GATE CSE 2006 | Question: 20, ISRO2015-17**

Consider the following log sequence of two transactions on a bank account, with initial balance 12000, that transfer 2000 to a mortgage payment and then apply a 5% interest.

1. T1 start
2. T1 B old = 12000 new = 10000

3. T1 M old = 0 new = 2000
4. T1 commit
5. T2 start
6. T2 B old = 10000 new = 10500
7. T2 commit

Suppose the database system crashes just before log record 7 is written. When the system is restarted, which one statement is true of the recovery procedure?

- A. We must redo log record 6 to set B to 10500
- B. We must undo log record 6 to set B to 10000 and then redo log records 2 and 3
- C. We need not redo log records 2 and 3 because transaction T1 has committed
- D. We can apply redo and undo operations in arbitrary order because they are idempotent

gatecse-2006 databases transaction-and-concurrency normal isro2015

[Answer key](#)

### 3.18.5 Transaction And Concurrency: GATE CSE 2007 | Question: 64 [top](#)

Consider the following schedules involving two transactions. Which one of the following statements is TRUE?

- $S_1 : r_1(X); r_1(Y); r_2(X); r_2(Y); w_2(Y); w_1(X)$
- $S_2 : r_1(X); r_2(X); r_2(Y); w_2(Y); r_1(Y); w_1(X)$

- A. Both  $S_1$  and  $S_2$  are conflict serializable.
- B.  $S_1$  is conflict serializable and  $S_2$  is not conflict serializable.
- C.  $S_1$  is not conflict serializable and  $S_2$  is conflict serializable.
- D. Both  $S_1$  and  $S_2$  are not conflict serializable.

gatecse-2007 databases transaction-and-concurrency normal

[Answer key](#)

### 3.18.6 Transaction And Concurrency: GATE CSE 2009 | Question: 43 [top](#)

Consider two transactions  $T_1$  and  $T_2$ , and four schedules  $S_1, S_2, S_3, S_4$ , of  $T_1$  and  $T_2$  as given below:

$T_1 : R_1[x]W_1[x]W_1[y]$

$T_2 : R_2[x]R_2[y]W_2[y]$

$S_1 : R_1[x]R_2[x]R_2[y]W_1[x]W_1[y]W_2[y]$

$S_2 : R_1[x]R_2[x]R_2[y]W_1[x]W_2[y]W_1[y]$

$S_3 : R_1[x]W_1[x]R_2[x]W_1[y]R_2[y]W_2[y]$

$S_4 : R_2[x]R_2[y]R_1[x]W_1[x]W_1[y]W_2[y]$

Which of the above schedules are conflict-serializable?

- A.  $S_1$  and  $S_2$
- B.  $S_2$  and  $S_3$
- C.  $S_3$  only
- D.  $S_4$  only

gatecse-2009 databases transaction-and-concurrency normal

[Answer key](#)

### 3.18.7 Transaction And Concurrency: GATE CSE 2010 | Question: 20 [top](#)

Which of the following concurrency control protocols ensure both conflict serializability and freedom from deadlock?

- I. 2-phase locking
  - II. Time-stamp ordering
- A. I only
  - B. II only
  - C. Both I and II
  - D. Neither I nor II

**Answer key****3.18.8 Transaction And Concurrency: GATE CSE 2010 | Question: 42**

Consider the following schedule for transactions  $T_1$ ,  $T_2$  and  $T_3$ :

<b>T1</b>	<b>T2</b>	<b>T3</b>
Read(X)		
	Read(Y)	
		Read(Y)
	Write(Y)	
Write(X)		
		Write(X)
	Read(X)	
	Write(X)	

Which one of the schedules below is the correct serialization of the above?

- A.  $T_1 \rightarrow T_3 \rightarrow T_2$   
 B.  $T_2 \rightarrow T_1 \rightarrow T_3$   
 C.  $T_2 \rightarrow T_3 \rightarrow T_1$   
 D.  $T_3 \rightarrow T_1 \rightarrow T_2$

**Answer key****3.18.9 Transaction And Concurrency: GATE CSE 2012 | Question: 27**

Consider the following transactions with data items  $P$  and  $Q$  initialized to zero:

$T_1$	read (P); read (Q); if P = 0 then Q := Q + 1; write (Q)
$T_2$	read (Q); read (P); if Q = 0 then P := P + 1; write (P)

Any non-serial interleaving of  $T_1$  and  $T_2$  for concurrent execution leads to

- A. a serializable schedule  
 B. a schedule that is not conflict serializable  
 C. a conflict serializable schedule  
 D. a schedule for which a precedence graph cannot be drawn

**Answer key****3.18.10 Transaction And Concurrency: GATE CSE 2014 Set 1 | Question: 29**

Consider the following four schedules due to three transactions (indicated by the subscript) using *read* and *write* on a data item  $x$ , denoted by  $r(x)$  and  $w(x)$  respectively. Which one of them is conflict serializable?

- A.  $r_1(x); r_2(x); w_1(x); r_3(x); w_2(x);$

- B.  $r_2(x); r_1(x); w_2(x); r_3(x); w_1(x);$   
 C.  $r_3(x); r_2(x); r_1(x); w_2(x); w_1(x);$   
 D.  $r_2(x); w_2(x); r_3(x); r_1(x); w_1(x);$

gatecse-2014-set1 databases transaction-and-concurrency normal

Answer key 

### 3.18.11 Transaction And Concurrency: GATE CSE 2014 Set 2 | Question: 29 top



Consider the following schedule **S** of transactions  $T1, T2, T3, T4$ :

T1	T2	T3	T4
	Reads(X)	Writes(X) Commit	
Writes(X) Commit	Writes(Y) Reads(Z) Commit		Reads(X) Reads(Y) Commit

Which one of the following statements is CORRECT?

- A. **S** is conflict-serializable but not recoverable  
 B. **S** is not conflict-serializable but is recoverable  
 C. **S** is both conflict-serializable and recoverable  
 D. **S** is neither conflict-serializable nor is it recoverable

gatecse-2014-set2 databases transaction-and-concurrency normal

Answer key 

### 3.18.12 Transaction And Concurrency: GATE CSE 2014 Set 3 | Question: 29 top



Consider the transactions  $T1, T2$ , and  $T3$  and the schedules  $S1$  and  $S2$  given below.

- $T1 : r1(X); r1(Z); w1(X); w1(Z)$
- $T2 : r2(Y); r2(Z); w2(Z)$
- $T3 : r3(Y); r3(X); w3(Y)$
- $S1 : r1(X); r3(Y); r3(X); r2(Y); r2(Z); w3(Y); w2(Z); r1(Z); w1(X); w1(Z)$
- $S2 : r1(X); r3(Y); r2(Y); r3(X); r1(Z); r2(Z); w3(Y); w1(X); w2(Z); w1(Z)$

Which one of the following statements about the schedules is **TRUE**?

- A. Only  $S1$  is conflict-serializable.  
 C. Both  $S1$  and  $S2$  are conflict-serializable.  
 B. Only  $S2$  is conflict-serializable.  
 D. Neither  $S1$  nor  $S2$  is conflict-serializable.

gatecse-2014-set3 databases transaction-and-concurrency normal

Answer key 

### 3.18.13 Transaction And Concurrency: GATE CSE 2015 Set 2 | Question: 1 top



Consider the following transaction involving two bank accounts  $x$  and  $y$ .

`read(x); x:=x-50; write(x); read(y); y:=y+50; write(y)`

The constraint that the sum of the accounts  $x$  and  $y$  should remain constant is that of

- A. Atomicity      B. Consistency      C. Isolation      D. Durability

gatecse-2015-set2 databases transaction-and-concurrency easy

[Answer key](#)

### 3.18.14 Transaction And Concurrency: GATE CSE 2015 Set 2 | Question: 46 top



Consider a simple checkpointing protocol and the following set of operations in the log.

(start, T4); (write, T4, y, 2, 3); (start, T1); (commit, T4); (write, T1, z, 5, 7);  
(checkpoint);  
(start, T2); (write, T2, x, 1, 9); (commit, T2); (start, T3); (write, T3, z, 7, 2);

If a crash happens now and the system tries to recover using both undo and redo operations, what are the contents of the undo list and the redo list?

- A. Undo: T3, T1; Redo: T2  
C. Undo: none; Redo: T2, T4, T3, T1  
B. Undo: T3, T1; Redo: T2, T4  
D. Undo: T3, T1, T4; Redo: T2

gatecse-2015-set2 databases transaction-and-concurrency normal

[Answer key](#)

### 3.18.15 Transaction And Concurrency: GATE CSE 2015 Set 3 | Question: 29 top



Consider the partial Schedule  $S$  involving two transactions  $T1$  and  $T2$ . Only the *read* and the *write* operations have been shown. The *read* operation on data item  $P$  is denoted by  $\text{read}(P)$  and *write* operation on data item  $P$  is denoted by  $\text{write}(P)$ .

Time Instance	Schedule S	
	Transaction ID <b>T1</b>	<b>T2</b>
1	read(A)	
2	write(A)	
3		read(C)
4		write(C)
5		read(B)
6		write(B)
7		read(A)
8		commit
9	read(B)	

Suppose that the transaction  $T1$  fails immediately after time instance 9. Which of the following statements is correct?

- A.  $T2$  must be aborted and then both  $T1$  and  $T2$  must be re-started to ensure transaction atomicity  
B. Schedule  $S$  is non-recoverable and cannot ensure transaction atomicity  
C. Only  $T2$  must be aborted and then re-started to ensure transaction atomicity  
D. Schedule  $S$  is recoverable and can ensure transaction atomicity and nothing else needs to be done

gatecse-2015-set3 databases transaction-and-concurrency normal

[Answer key](#)

### 3.18.16 Transaction And Concurrency: GATE CSE 2016 Set 1 | Question: 22 top



Which one of the following is NOT a part of the ACID properties of database transactions?

- A. Atomicity      B. Consistency      C. Isolation      D. Deadlock-freedom

**Answer key****3.18.17 Transaction And Concurrency: GATE CSE 2016 Set 1 | Question: 51**

Consider the following two phase locking protocol. Suppose a transaction  $T$  accesses (for read or write operations), a certain set of objects  $\{O_1, \dots, O_k\}$ . This is done in the following manner:

- Step 1.  $T$  acquires exclusive locks to  $O_1, \dots, O_k$  in increasing order of their addresses.
- Step 2. The required operations are performed .
- Step 3. All locks are released

This protocol will

- A. guarantee serializability and deadlock-freedom
- B. guarantee neither serializability nor deadlock-freedom
- C. guarantee serializability but not deadlock-freedom
- D. guarantee deadlock-freedom but not serializability.

**Answer key****3.18.18 Transaction And Concurrency: GATE CSE 2016 Set 2 | Question: 22**

Suppose a database schedule  $S$  involves transactions  $T_1, \dots, T_n$ . Construct the precedence graph of  $S$  with vertices representing the transactions and edges representing the conflicts. If  $S$  is serializable, which one of the following orderings of the vertices of the precedence graph is guaranteed to yield a serial schedule?

- |                        |   |
|------------------------|---|
| A. Topological order   | B. Depth-first order                          |
| C. Breadth-first order | D. Ascending order of the transaction indices |

**Answer key****3.18.19 Transaction And Concurrency: GATE CSE 2016 Set 2 | Question: 51**

Consider the following database schedule with two transactions  $T_1$  and  $T_2$ .

$$S = r_2(X); r_1(X); r_2(Y); w_1(X); r_1(Y); w_2(X); a_1; a_2$$

Where  $r_i(Z)$  denotes a read operation by transaction  $T_i$  on a variable  $Z$ ,  $w_i(Z)$  denotes a write operation by  $T_i$  on a variable  $Z$  and  $a_i$  denotes an abort by transaction  $T_i$ .

Which one of the following statements about the above schedule is **TRUE**?

- |   |   |
|---|---|
| A. $S$ is non-recoverable.              | B. $S$ is recoverable, but has a cascading abort. |
| C. $S$ does not have a cascading abort. | D. $S$ is strict.                                 |

**Answer key****3.18.20 Transaction And Concurrency: GATE CSE 2019 | Question: 11**

Consider the following two statements about database transaction schedules:

- I. Strict two-phase locking protocol generates conflict serializable schedules that are also recoverable.
- II. Timestamp-ordering concurrency control protocol with Thomas' Write Rule can generate view serializable schedules that are not conflict serializable

Which of the above statements is/are **TRUE**?

- A. I only
- B. II only
- C. Both I and II
- D. Neither I nor II

**Answer key**

### 3.18.21 Transaction And Concurrency: GATE CSE 2020 | Question: 37 top



Consider a schedule of transactions  $T_1$  and  $T_2$ :

$T_1$	$RA$			$RC$		$WD$		$WB$	Commit	
$T_2$		$RB$	$WB$		$RD$		$WC$			Commit

Here, RX stands for “Read(X)” and WX stands for “Write(X)”. Which one of the following schedules is conflict equivalent to the above schedule?

A.

$T_1$				$RA$	$RC$	$WD$	$WB$		Commit	
$T_2$	$RB$	$WB$	$RD$					$WC$		Commit

B.

$T_1$	$RA$	$RC$	$WD$	$WB$					Commit	
$T_2$					$RB$	$WB$	$RD$	$WC$		Commit

C.

$T_1$	$RA$	$RC$	$WD$				$WB$		Commit	
$T_2$				$RB$	$WB$	$RD$		$WC$		Commit

D.

$T_1$					$RA$	$RC$	$WD$	$WB$	Commit	
$T_2$	$RB$	$WB$	$RD$	$WC$						Commit

gatecse-2020 databases transaction-and-concurrency 2-marks

Answer key

### 3.18.22 Transaction And Concurrency: GATE CSE 2021 Set 1 | Question: 13 top



Suppose a database system crashes again while recovering from a previous crash. Assume checkpointing is not done by the database either during the transactions or during recovery.

Which of the following statements is/are correct?

- A. The same undo and redo list will be used while recovering again
- B. The system cannot recover any further
- C. All the transactions that are already undone and redone will not be recovered again
- D. The database will become inconsistent

gatecse-2021-set1 multiple-selects databases transaction-and-concurrency 1-mark

Answer key

### 3.18.23 Transaction And Concurrency: GATE IT 2004 | Question: 21 top



Which level of locking provides the highest degree of concurrency in a relational database ?

- A. Page
- B. Table
- C. Row
- D. Page, table and row level locking allow the same degree of concurrency

gateit-2004 databases normal transaction-and-concurrency

Answer key

### 3.18.24 Transaction And Concurrency: GATE IT 2004 | Question: 77 top



Consider the following schedule  $S$  of transactions  $T_1$  and  $T_2$  :

T1	T2
Read(A) A = A - 10	Read(A) Temp = 0.2*A Write(A) Read(B)
Write(A) Read(B) B = B + 10 Write(B)	B = B + Temp Write(B)

Which of the following is TRUE about the schedule  $S$  ?

- A.  $S$  is serializable only as  $T1, T2$
- B.  $S$  is serializable only as  $T2, T1$
- C.  $S$  is serializable both as  $T1, T2$  and  $T2, T1$
- D.  $S$  is not serializable either as  $T1, T2$  or as  $T2, T1$

gateit-2004 databases transaction-and-concurrency normal

[Answer key](#)

### 3.18.25 Transaction And Concurrency: GATE IT 2005 | Question: 24 top

Amongst the ACID properties of a transaction, the 'Durability' property requires that the changes made to the database by a successful transaction persist

- A. Except in case of an Operating System crash
- B. Except in case of a Disk crash
- C. Except in case of a power failure
- D. Always, even if there is a failure of any kind

gateit-2005 databases transaction-and-concurrency easy

[Answer key](#)

### 3.18.26 Transaction And Concurrency: GATE IT 2005 | Question: 67 top

A company maintains records of sales made by its salespersons and pays them commission based on each individual's total sales made in a year. This data is maintained in a table with following schema:

`salesinfo = (salespersonid, totalsales, commission)`

In a certain year, due to better business results, the company decides to further reward its salespersons by enhancing the commission paid to them as per the following formula:

If  $\text{commission} \leq 50000$ , enhance it by 2%

If  $50000 < \text{commission} \leq 100000$ , enhance it by 4%

If  $\text{commission} > 100000$ , enhance it by 6%

The IT staff has written three different SQL scripts to calculate enhancement for each slab, each of these scripts is to run as a separate transaction as follows:

T1

```
Update salesinfo
Set commission = commission * 1.02
Where commission <= 50000;
```

T2  
**Update** salesinfo  
**Set** commission = commission \* 1.04  
**Where** commission > 50000 and  
commission is < = 100000;

T3  
**Update** salesinfo  
**Set** commission = commission \* 1.06  
**Where** commission > 100000;

Which of the following options of running these transactions will update the commission of all salespersons correctly

- A. Execute T1 followed by T2 followed by T3
- B. Execute T2, followed by T3; T1 running concurrently throughout
- C. Execute T3 followed by T2; T1 running concurrently throughout
- D. Execute T3 followed by T2 followed by T1

gateit-2005 databases transaction-and-concurrency normal

**Answer key**

### 3.18.27 Transaction And Concurrency: GATE IT 2007 | Question: 66 top



Consider the following two transactions: *T1* and *T2*.

<i>T1</i> : read (A); read (B); If $A = 0$ then $B \leftarrow B + 1$ ; write (B);	<i>T2</i> : read (B); read (A); If $B \neq 0$ then $A \leftarrow A - 1$ ; write (A);
--	---

Which of the following schemes, using shared and exclusive locks, satisfy the requirements for strict two phase locking for the above transactions?

<i>S1</i> : lock S(A); read (A); lock S(B); read (B); If $A = 0$ then $B \leftarrow B + 1$ ; write (B); commit; unlock (A); unlock (B);	<i>S2</i> : lock S(B); read (B); lock S(A); read (A); If $B \neq 0$ then $A \leftarrow A - 1$ ; write (A); commit; unlock (B); unlock (A);
--	---

<i>S1</i> : lock X(A); read (A); lock X(B); read (B); If $A = 0$ then $B \leftarrow B + 1$ ; write (B); unlock (A); commit; unlock (B);	<i>S2</i> : lock X(B); read (B); lock X(A); read (A); If $B \neq 0$ then $A \leftarrow A - 1$ ; write (A); unlock (A); commit; unlock (A);
--	---

	<i>S1</i> : lock S(A); read (A); lock X(B); read (B); If $A = 0$ then $B \leftarrow B + 1$ ; write (B); unlock (A); commit; unlock (B);	<i>S2</i> : lock S(B); read (B); lock X(A); read (A); If $B \neq 0$ then $A \leftarrow A - 1$ ; write (A); unlock (B); commit; unlock (A);
C.	<i>S1</i> : lock S(A); read (A); lock X(B); read (B); If $A = 0$ then $B \leftarrow B + 1$ ; write (B); unlock (A); unlock (B); commit;	<i>S2</i> : lock S(B); read (B); lock X(A); read (A); If $B \neq 0$ then $A \leftarrow A - 1$ ; write (A); unlock (B); unlock (A); commit;

---

D.	<i>S1</i> : lock S(A); read (A); lock X(B); read (B); If $A = 0$ then $B \leftarrow B + 1$ ; write (B); unlock (A); unlock (B); commit;	<i>S2</i> : lock S(B); read (B); lock X(A); read (A); If $B \neq 0$ then $A \leftarrow A - 1$ ; write (A); unlock (A); unlock (A); commit;
----	--	---

gateit-2007 databases transaction-and-concurrency normal

Answer key 

### 3.18.28 Transaction And Concurrency: GATE IT 2008 | Question: 63 top ↴



Consider the following three schedules of transactions T1, T2 and T3. [Notation: In the following NYO represents the action Y (R for read, W for write) performed by transaction N on object O.]

(S1)	2RA	2WA	3RC	2WB	3WA	3WC	1RA	1RB	1WA	1WB
(S2)	3RC	2RA	2WA	2WB	3WA	1RA	1RB	1WA	1WB	3WC
(S3)	2RA	3RC	3WA	2WA	2WB	3WC	1RA	1RB	1WA	1WB

Which of the following statements is TRUE?

- A. S1, S2 and S3 are all conflict equivalent to each other
- B. No two of S1, S2 and S3 are conflict equivalent to each other
- C. S2 is conflict equivalent to S3, but not to S1
- D. S1 is conflict equivalent to S2, but not to S3

gateit-2008 databases transaction-and-concurrency normal

Answer key 

## Answer Keys

3.1.1	N/A	3.1.2	N/A	3.1.3	N/A	3.1.4	N/A	3.1.5	B
3.1.6	N/A	3.1.7	B	3.1.8	N/A	3.1.9	N/A	3.1.10	N/A
3.1.11	C	3.1.12	B	3.1.13	C	3.1.14	D	3.1.15	A

3.1.16	C	3.1.17	C	3.1.19	5	3.1.20	50	3.1.21	A
3.1.22	52	3.1.23	B	3.1.24	C	3.1.25	A	3.1.26	C
3.1.27	A	3.1.28	A	3.2.1	N/A	3.2.2	A	3.2.4	19
3.2.5	B	3.3.1	54	3.3.2	B	3.3.3	B	3.3.4	A
3.4.1	False	3.5.1	True	3.5.2	N/A	3.5.3	N/A	3.5.4	N/A
3.5.5	N/A	3.5.6	N/A	3.5.8	False	3.5.9	N/A	3.5.10	A
3.5.11	D	3.5.12	N/A	3.5.13	B	3.5.14	D	3.5.15	B
3.5.17	A	3.5.18	N/A	3.5.20	C	3.5.21	D	3.5.22	B
3.5.23	C	3.5.24	D	3.5.25	C	3.5.26	D	3.5.27	C
3.5.28	C	3.5.29	B	3.5.30	A	3.5.31	B	3.5.32	A
3.5.33	C	3.5.34	B	3.5.35	B	3.5.36	A	3.5.37	B
3.5.38	C	3.5.39	A	3.5.40	A	3.5.41	A;C;D	3.5.42	8
3.5.43	A	3.5.44	B	3.5.45	A	3.5.46	B	3.5.47	B
3.5.48	A	3.5.49	D	3.6.1	B	3.6.2	B	3.6.3	A
3.6.4	C	3.6.5	4	3.6.6	C	3.6.7	A	3.6.8	A
3.6.9	B	3.6.10	C	3.7.1	N/A	3.7.2	N/A	3.7.3	3
3.7.4	C	3.7.5	A	3.7.6	C	3.7.7	C	3.7.8	C
3.7.9	C	3.7.10	4	3.7.11	698 : 698	3.7.12	6	3.8.1	A
3.8.3	A	3.8.5	B	3.8.6	A	3.8.7	A	3.9.1	C
3.10.1	C	3.10.2	A	3.10.3	C	3.11.1	B	3.11.2	C
3.11.4	D	3.12.1	N/A	3.12.2	N/A	3.12.3	N/A	3.12.4	N/A
3.12.5	N/A	3.12.6	N/A	3.12.7	D	3.12.8	N/A	3.12.9	B
3.12.10	C	3.12.11	D	3.12.12	C	3.12.13	N/A	3.12.14	A
3.12.15	D	3.12.17	D	3.12.18	A	3.12.19	A	3.12.20	D
3.12.21	D	3.12.22	4	3.12.23	C	3.12.24	1	3.12.25	C
3.12.26	A;B	3.12.27	B	3.13.1	N/A	3.13.2	N/A	3.13.3	D
3.13.4	C	3.13.5	C	3.13.6	C	3.13.7	B	3.13.8	C
3.13.9	C	3.13.10	A	3.13.11	A	3.13.12	D	3.13.13	D
3.13.14	C	3.14.1	A	3.15.1	D	3.16.1	N/A	3.16.2	N/A
3.16.3	N/A	3.16.4	N/A	3.16.5	N/A	3.16.6	N/A	3.16.7	N/A
3.16.8	D	3.16.9	N/A	3.16.10	N/A	3.16.11	A	3.16.12	C
3.16.13	N/A	3.16.14	C	3.16.15	N/A	3.16.16	N/A	3.16.17	N/A
3.16.18	C	3.16.19	D	3.16.21	C	3.16.22	B	3.16.23	C
3.16.24	A	3.16.25	X	3.16.26	A	3.16.27	C	3.16.28	A
3.16.29	C	3.16.30	C	3.16.31	B	3.16.32	D	3.16.33	B
3.16.34	C	3.16.35	D	3.16.36	2	3.16.37	A	3.16.38	2
3.16.39	2.6	3.16.40	7	3.16.41	D	3.16.42	5	3.16.43	A
3.16.44	819 : 820 ; 205 : 205	3.16.45	B	3.16.46	2	3.16.47	2	3.16.48	D
3.16.49	C	3.16.50	C	3.16.51	D	3.16.52	A	3.16.53	B
3.16.54	D	3.17.1	A	3.18.1	D	3.18.2	D	3.18.3	D

3.18.4	B	3.18.5	C	3.18.6	B	3.18.7	B	3.18.8	A
3.18.9	B	3.18.10	D	3.18.12	A	3.18.13	B	3.18.14	A
3.18.15	B	3.18.16	D	3.18.17	A	3.18.18	A	3.18.19	C
3.18.20	C	3.18.21	A	3.18.22	A	3.18.23	C	3.18.24	X
3.18.25	D	3.18.26	D	3.18.27	C	3.18.28	D		



## 4.1

8085 Microprocessor (1) [top](#)4.1.1 8085 Microprocessor: GATE CSE 1998 | Question: 1.17 [top](#)

The octal representation of an integer is  $(342)_8$ . If this were to be treated as an eight-bit integer in an 8085 based computer, its decimal equivalent is

- A. 226      B. -98      C. 76      D. -30

gate1998 digital-logic number-representation normal 8085-microprocessor

[Answer key](#)

## 4.2

Adder (10) [top](#)4.2.1 Adder: GATE CSE 1988 | Question: 4ii [top](#)

Using binary full adders and other logic gates (if necessary), design an adder for adding 4-bit number (including sign) in  $2's$  complement notation.

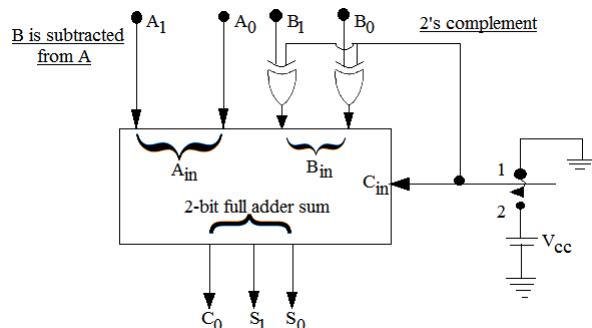
gate1988 digital-logic descriptive adder

[Answer key](#)

4.2.2 Adder: GATE CSE 1990 | Question: 1-i [top](#)

Fill in the blanks:

In the two bit full-adder/subtractor unit shown in below figure, when the switch is in position 2 \_\_\_\_\_ using \_\_\_\_\_ arithmetic.



gate1990 digital-logic adder fill-in-the-blanks

[Answer key](#)

4.2.3 Adder: GATE CSE 1993 | Question: 9 [top](#)

Assume that only half adders are available in your laboratory. Show that any binary function can be implemented using half adders only.

gate1993 digital-logic combinational-circuit adder descriptive

[Answer key](#)

4.2.4 Adder: GATE CSE 1997 | Question: 2.5 [top](#)

An  $N$ -bit carry lookahead adder, where  $N$  is a multiple of 4, employs ICs 74181 (4 bit ALU) and 74182 (4 bit carry lookahead generator).

The minimum addition time using the best architecture for this adder is

- A. proportional to  $N$       B. proportional to  $\log N$   
 C. a constant      D. None of the above

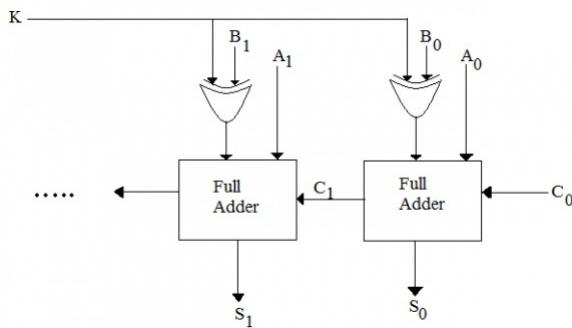
**Answer key****4.2.5 Adder: GATE CSE 1999 | Question: 2.16**

The number of full and half-adders required to add 16-bit numbers is

- A. 8 half-adders, 8 full-adders
- B. 1 half-adder, 15 full-adders
- C. 16 half-adders, 0 full-adders
- D. 4 half-adders, 12 full-adders

**Answer key****4.2.6 Adder: GATE CSE 2003 | Question: 46**

Consider the ALU shown below.



If the operands are in 2's complement representation, which of the following operations can be performed by suitably setting the control lines  $K$  and  $C_0$  only (+ and – denote addition and subtraction respectively)?

- A.  $A + B$ , and  $A - B$ , but not  $A + 1$
- B.  $A + B$ , and  $A + 1$ , but not  $A - B$
- C.  $A + B$ , but not  $A - B$  or  $A + 1$
- D.  $A + B$ , and  $A - B$ , and  $A + 1$

**Answer key****4.2.7 Adder: GATE CSE 2004 | Question: 62**

A 4-bit carry look ahead adder, which adds two 4-bit numbers, is designed using AND, OR, NOT, NAND, NOR gates only. Assuming that all the inputs are available in both complemented and uncomplemented forms and the delay of each gate is one time unit, what is the overall propagation delay of the adder? Assume that the carry network has been implemented using two-level AND-OR logic.

- A. 4 time units
- B. 6 time units
- C. 10 time units
- D. 12 time units

**Answer key****4.2.8 Adder: GATE CSE 2015 Set 2 | Question: 48**

A half adder is implemented with XOR and AND gates. A full adder is implemented with two half adders and one OR gate. The propagation delay of an XOR gate is twice that of an AND/OR gate. The propagation delay of an AND/OR gate is 1.2 microseconds. A 4-bit-ripple-carry binary adder is implemented by using four full adders. The total propagation time of this 4-bit binary adder in microseconds is \_\_\_\_\_.

**Answer key****4.2.9 Adder: GATE CSE 2016 Set 1 | Question: 33**

Consider a carry look ahead adder for adding two  $n$ -bit integers, built using gates of fan-in at most two. The time to perform addition using this adder is

- A.  $\Theta(1)$   
 C.  $\Theta(\sqrt{n})$
- B.  $\Theta(\log(n))$   
 D.  $\Theta(n)$

gatecse-2016-set1 digital-logic adder normal

Answer key 



#### 4.2.10 Adder: GATE CSE 2016 Set 2 | Question: 07

Consider an eight-bit ripple-carry adder for computing the sum of  $A$  and  $B$ , where  $A$  and  $B$  are integers represented in 2's complement form. If the decimal value of  $A$  is one, the decimal value of  $B$  that leads to the longest latency for the sum to stabilize is \_\_\_\_\_

gatecse-2016-set2 digital-logic adder normal numerical-answers

Answer key 

### 4.3

#### Array Multiplier (2)



#### 4.3.1 Array Multiplier: GATE CSE 1999 | Question: 1.21

The maximum gate delay for any output to appear in an array multiplier for multiplying two  $n$  bit numbers is

- A.  $O(n^2)$       B.  $O(n)$       C.  $O(\log n)$       D.  $O(1)$

gate1999 digital-logic normal array-multiplier

Answer key 



#### 4.3.2 Array Multiplier: GATE CSE 2003 | Question: 11

Consider an array multiplier for multiplying two  $n$  bit numbers. If each gate in the circuit has a unit delay, the total delay of the multiplier is

- A.  $\Theta(1)$       B.  $\Theta(\log n)$       C.  $\Theta(n)$       D.  $\Theta(n^2)$

gatecse-2003 digital-logic normal array-multiplier

Answer key 

### 4.4

#### Binary Codes (2)



#### 4.4.1 Binary Codes: GATE CSE 2006 | Question: 40

Consider numbers represented in 4-bit Gray code. Let  $h_3h_2h_1h_0$  be the Gray code representation of a number  $n$  and let  $g_3g_2g_1g_0$  be the Gray code of  $(n+1)(\text{modulo}16)$  value of the number. Which one of the following functions is correct?

- A.  $g_0(h_3h_2h_1h_0) = \sum(1, 2, 3, 6, 10, 13, 14, 15)$   
 B.  $g_1(h_3h_2h_1h_0) = \sum(4, 9, 10, 11, 12, 13, 14, 15)$   
 C.  $g_2(h_3h_2h_1h_0) = \sum(2, 4, 5, 6, 7, 12, 13, 15)$   
 D.  $g_3(h_3h_2h_1h_0) = \sum(0, 1, 6, 7, 10, 11, 12, 13)$

gatecse-2006 digital-logic number-representation binary-codes normal

Answer key 



#### 4.4.2 Binary Codes: GATE CSE 2017 Set 2 | Question: 34

Consider the binary code that consists of only four valid codewords as given below:

00000, 01011, 10101, 11110

Let the minimum Hamming distance of the code  $p$  and the maximum number of erroneous bits that can be corrected by the code be  $q$ . Then the values of  $p$  and  $q$  are

- A.  $p = 3$  and  $q = 1$     B.  $p = 3$  and  $q = 2$     C.  $p = 4$  and  $q = 1$     D.  $p = 4$  and  $q = 2$

gatecse-2017-set2 digital-logic binary-codes

Answer key 

**4.5****Boolean Algebra (31)** [top](#)**4.5.1 Boolean Algebra: GATE CSE 1987 | Question: 1-II** [top](#)

The total number of Boolean functions which can be realised with four variables is:

- A. 4      B. 17      C. 256      D. 65,536

gate1987 digital-logic boolean-algebra functions combinatory

**Answer key** **4.5.2 Boolean Algebra: GATE CSE 1987 | Question: 12-a** [top](#)

The Boolean expression  $A \oplus B \oplus A$  is equivalent to

- A.  $AB + \bar{A} \bar{B}$       B.  $\bar{A}B + A\bar{B}$   
C.  $B$       D.  $\bar{A}$

gate1987 digital-logic boolean-algebra easy

**Answer key** **4.5.3 Boolean Algebra: GATE CSE 1988 | Question: 2-iii** [top](#)

Let  $*$  be defined as a Boolean operation given as  $x * y = \bar{x} \bar{y} + xy$  and let  $C = A * B$ . If  $C = 1$  then prove that  $A = B$ .

gate1988 descriptive digital-logic boolean-algebra

**Answer key** **4.5.4 Boolean Algebra: GATE CSE 1989 | Question: 4-x** [top](#)

A switching function is said to be neutral if the number of input combinations for which its value is 1 is equal to the number of input combinations for which its value is 0. Compute the number of neutral switching functions of  $n$  variables (for a given  $n$ ).

gate1989 descriptive digital-logic boolean-algebra

**Answer key** **4.5.5 Boolean Algebra: GATE CSE 1989 | Question: 5-a** [top](#)

Find values of Boolean variables  $A, B, C$  which satisfy the following equations:

- $A + B = 1$
- $AC = BC$
- $A + C = 1$
- $AB = 0$

gate1989 descriptive digital-logic boolean-algebra

**Answer key** **4.5.6 Boolean Algebra: GATE CSE 1992 | Question: 02-i** [top](#)

The operation which is commutative but not associative is:

- A. AND      B. OR      C. EX-OR      D. NAND

gate1992 easy digital-logic boolean-algebra multiple-selects

**Answer key** **4.5.7 Boolean Algebra: GATE CSE 1994 | Question: 4** [top](#)

- A. Let  $*$  be a Boolean operation defined as  $A * B = AB + \bar{A} \bar{B}$ . If  $C = A * B$  then evaluate and fill in the

blanks:

- i.  $A * A = \underline{\hspace{2cm}}$
- ii.  $C * A = \underline{\hspace{2cm}}$

B. Solve the following boolean equations for the values of  $A, B$  and  $C$ :

$$\begin{aligned}AB + \overline{AC} &= 1 \\AC + B &= 0\end{aligned}$$

gate1994 digital-logic normal boolean-algebra descriptive

[Answer key](#)



#### 4.5.8 Boolean Algebra: GATE CSE 1995 | Question: 2.5 [top](#)

What values of  $A, B, C$  and  $D$  satisfy the following simultaneous Boolean equations?

$$\overline{A} + AB = 0, AB = AC, AB + A\overline{C} + CD = \overline{C}D$$

- A.  $A = 1, B = 0, C = 0, D = 1$
- B.  $A = 1, B = 1, C = 0, D = 0$
- C.  $A = 1, B = 0, C = 1, D = 1$
- D.  $A = 1, B = 0, C = 0, D = 0$

gate1995 digital-logic boolean-algebra easy

[Answer key](#)



#### 4.5.9 Boolean Algebra: GATE CSE 1997 | Question: 2-1 [top](#)

Let  $*$  be defined as  $x * y = \bar{x} + y$ . Let  $z = x * y$ . Value of  $z * x$  is

- A.  $\bar{x} + y$
- B.  $x$
- C. 0
- D. 1

gate1997 digital-logic normal boolean-algebra

[Answer key](#)



#### 4.5.10 Boolean Algebra: GATE CSE 1998 | Question: 1.13 [top](#)

What happens when a bit-string is XORed with itself  $n$ -times as shown:

$$[B \oplus (B \oplus (B \oplus (B \dots n \text{ times})))]$$

- A. complements when  $n$  is even
- B. complements when  $n$  is odd
- C. divides by  $2^n$  always
- D. remains unchanged when  $n$  is even

gate1998 digital-logic normal boolean-algebra

[Answer key](#)



#### 4.5.11 Boolean Algebra: GATE CSE 1998 | Question: 2.8 [top](#)

Which of the following operations is commutative but not associative?

- A. AND
- B. OR
- C. NAND
- D. EXOR

gate1998 digital-logic easy boolean-algebra

[Answer key](#)



#### 4.5.12 Boolean Algebra: GATE CSE 1999 | Question: 1.7 [top](#)

Which of the following expressions is not equivalent to  $\bar{x}$ ?

- A.  $x \text{ NAND } x$
- B.  $x \text{ NOR } x$
- C.  $x \text{ NAND } 1$
- D.  $x \text{ NOR } 1$

gate1999 digital-logic easy boolean-algebra

[Answer key](#)



#### 4.5.13 Boolean Algebra: GATE CSE 2000 | Question: 2.10 [top](#)

The simultaneous equations on the Boolean variables  $x, y, z$  and  $w$ ,

- $x + y + z = 1$
- $xy = 0$
- $xz + w = 1$
- $xy + \bar{z}\bar{w} = 0$

have the following solution for  $x, y, z$  and  $w$ , respectively:

- |            |            |
|------------|------------|
| A. 0 1 0 0 | B. 1 1 0 1 |
| C. 1 0 1 1 | D. 1 0 0 0 |

gatecse-2000 digital-logic boolean-algebra easy

[Answer key](#) 



#### 4.5.14 Boolean Algebra: GATE CSE 2002 | Question: 2-3 top

Let  $f(A, B) = A' + B$ . Simplified expression for function  $f(f(x + y, y), z)$  is

- A.  $x' + z$       B.  $xyz$       C.  $xy' + z$       D. None of the above

gatecse-2002 digital-logic boolean-algebra normal

[Answer key](#) 



#### 4.5.15 Boolean Algebra: GATE CSE 2004 | Question: 17 top

A Boolean function  $x'y' + xy + x'y$  is equivalent to

- A.  $x' + y'$       B.  $x + y$       C.  $x + y'$       D.  $x' + y$

gatecse-2004 digital-logic easy boolean-algebra

[Answer key](#) 



#### 4.5.16 Boolean Algebra: GATE CSE 2007 | Question: 32 top

Let  $f(w, x, y, z) = \sum(0, 4, 5, 7, 8, 9, 13, 15)$ . Which of the following expressions are NOT equivalent to  $f$ ?

P:  $x'y'z' + w'xy' + wy'z + xz$

Q:  $w'y'z' + wx'y' + xz$

R:  $w'y'z' + wx'y' + xyz + xy'z$

S:  $x'y'z' + wx'y' + w'y$

- A. P only      B. Q and S      C. R and S      D. S only

gatecse-2007 digital-logic normal boolean-algebra

[Answer key](#) 



#### 4.5.17 Boolean Algebra: GATE CSE 2007 | Question: 33 top

Define the connective  $*$  for the Boolean variables  $X$  and  $Y$  as:

$$X * Y = XY + X'Y'.$$

Let  $Z = X * Y$ . Consider the following expressions  $P, Q$  and  $R$ .

$$\begin{aligned} P : X &= Y * Z, \\ Q : Y &= X * Z, \\ R : X * Y * Z &= 1 \end{aligned}$$

Which of the following is **TRUE**?

- A. Only  $P$  and  $Q$  are valid.  
 B. Only  $Q$  and  $R$  are valid.  
 C. Only  $P$  and  $R$  are valid.  
 D. All  $P, Q, R$  are valid.

gatecse-2007 digital-logic normal boolean-algebra

Answer key

#### 4.5.18 Boolean Algebra: GATE CSE 2008 | Question: 26



If  $P, Q, R$  are Boolean variables, then

$(P + \bar{Q})(P \cdot \bar{Q} + P \cdot R)(\bar{P} \cdot \bar{R} + \bar{Q})$  simplifies to

- A.  $P \cdot \bar{Q}$       B.  $P \cdot \bar{R}$       C.  $P \cdot \bar{Q} + R$       D.  $P \cdot \bar{R} + Q$

gatecse-2008   easy   digital-logic   boolean-algebra

Answer key

#### 4.5.19 Boolean Algebra: GATE CSE 2012 | Question: 6



The truth table

X	Y	(X,Y)
0	0	0
0	1	0
1	0	1
1	1	1

represents the Boolean function

- A.  $X$       B.  $X + Y$       C.  $X \oplus Y$       D.  $Y$

gatecse-2012   digital-logic   easy   boolean-algebra

Answer key

#### 4.5.20 Boolean Algebra: GATE CSE 2013 | Question: 21



Which one of the following expressions does **NOT** represent exclusive NOR of  $x$  and  $y$ ?

- A.  $xy + x'y'$       B.  $x \oplus y'$   
C.  $x' \oplus y$       D.  $x' \oplus y'$

gatecse-2013   digital-logic   easy   boolean-algebra

Answer key

#### 4.5.21 Boolean Algebra: GATE CSE 2014 Set 3 | Question: 55



Let  $\oplus$  denote the exclusive OR (XOR) operation. Let '1' and '0' denote the binary constants. Consider the following Boolean expression for  $F$  over two variables  $P$  and  $Q$ :

$$F(P, Q) = ((1 \oplus P) \oplus (P \oplus Q)) \oplus ((P \oplus Q) \oplus (Q \oplus 0))$$

The equivalent expression for  $F$  is

- A.  $P + Q$       B.  $\overline{P + Q}$   
C.  $P \oplus Q$       D.  $\overline{P \oplus Q}$

gatecse-2014-set3   digital-logic   normal   boolean-algebra

Answer key

#### 4.5.22 Boolean Algebra: GATE CSE 2015 Set 1 | Question: 39



Consider the operations

$$f(X, Y, Z) = X'YZ + XY' + Y'Z' \text{ and } g(X, Y, Z) = X'YZ + X'YZ' + XY$$

Which one of the following is correct?

- A. Both  $\{f\}$  and  $\{g\}$  are functionally complete  
B. Only  $\{f\}$  is functionally complete  
C. Only  $\{g\}$  is functionally complete  
D. Neither  $\{f\}$  nor  $\{g\}$  is functionally complete

**Answer key****4.5.23 Boolean Algebra: GATE CSE 2015 Set 2 | Question: 37**

The number of min-terms after minimizing the following Boolean expression is \_\_\_\_\_.

$$[D' + AB' + A'C + AC'D + A'C'D']'$$

**Answer key****4.5.24 Boolean Algebra: GATE CSE 2016 Set 1 | Question: 06**

Consider the Boolean operator # with the following properties :

 $x\#0 = x, x\#1 = \bar{x}, x\#x = 0$  and  $x\#\bar{x} = 1$ . Then  $x\#y$  is equivalent to

- |                          |                                |
|--------------------------|--------------------------------|
| A. $x\bar{y} + \bar{x}y$ | B. $x\bar{y} + \bar{x}\bar{y}$ |
| C. $\bar{x}y + xy$       | D. $xy + \bar{x}\bar{y}$       |

**Answer key****4.5.25 Boolean Algebra: GATE CSE 2016 Set 2 | Question: 08**Let,  $x_1 \oplus x_2 \oplus x_3 \oplus x_4 = 0$  where  $x_1, x_2, x_3, x_4$  are Boolean variables, and  $\oplus$  is the XOR operator.Which one of the following must always be **TRUE**?

- A.  $x_1x_2x_3x_4 = 0$
- B.  $x_1x_3 + x_2 = 0$
- C.  $\bar{x}_1 \oplus \bar{x}_3 = \bar{x}_2 \oplus \bar{x}_4$
- D.  $x_1 + x_2 + x_3 + x_4 = 0$

**Answer key****4.5.26 Boolean Algebra: GATE CSE 2017 Set 2 | Question: 27**If  $w, x, y, z$  are Boolean variables, then which one of the following is INCORRECT?

- |  |   |
|--|---|
| A. $wx + w(x + y) + x(x + y) = x + wy$                     | B. $\overline{w\bar{x}(y + \bar{z})} + \bar{w}x = \bar{w} + x + \bar{y}z$ |
| C. $(w\bar{x}(y + x\bar{z}) + \bar{w}\bar{x})y = x\bar{y}$ | D. $(w + y)(wxy + wyz) = wxy + wyz$                                       |

**Answer key****4.5.27 Boolean Algebra: GATE CSE 2018 | Question: 4**Let  $\oplus$  and  $\odot$  denote the Exclusive OR and Exclusive NOR operations, respectively. Which one of the following is NOT CORRECT?

- A.  $\overline{P \oplus Q} = P \odot Q$
- B.  $\overline{P} \oplus Q = P \odot Q$
- C.  $\overline{P} \oplus \overline{Q} = P \oplus Q$
- D.  $P \oplus \overline{P} \oplus Q = (P \odot \overline{P} \odot \overline{Q})$

**Answer key**

#### 4.5.28 Boolean Algebra: GATE CSE 2019 | Question: 6 top



Which one of the following is NOT a valid identity?

- A.  $(x \oplus y) \oplus z = x \oplus (y \oplus z)$
- B.  $(x + y) \oplus z = x \oplus (y + z)$
- C.  $x \oplus y = x + y$ , if  $xy = 0$
- D.  $x \oplus y = (xy + x'y')'$

gatecse-2019 digital-logic boolean-algebra 1-mark

[Answer key](#)

#### 4.5.29 Boolean Algebra: GATE CSE 2021 Set 1 | Question: 42 top



Consider the following Boolean expression.

$$F = (X + Y + Z)(\bar{X} + Y)(\bar{Y} + Z)$$

Which of the following Boolean expressions is/are equivalent to  $\bar{F}$  (complement of  $F$ )?

- A.  $(\bar{X} + \bar{Y} + \bar{Z})(X + \bar{Y})(Y + \bar{Z})$
- B.  $X\bar{Y} + \bar{Z}$
- C.  $(X + \bar{Z})(\bar{Y} + \bar{Z})$
- D.  $X\bar{Y} + Y\bar{Z} + \bar{X}\bar{Y}\bar{Z}$

gatecse-2021-set1 multiple-selects digital-logic boolean-algebra 2-marks

[Answer key](#)

#### 4.5.30 Boolean Algebra: GATE IT 2004 | Question: 44 top



The function  $A\bar{B}C + \bar{A}BC + ABC + \bar{A}\bar{B}C + A\bar{B}\bar{C}$  is equivalent to

- A.  $A\bar{C} + AB + \bar{A}C$
- B.  $A\bar{B} + A\bar{C} + \bar{A}C$
- C.  $\bar{A}B + A\bar{C} + A\bar{B}$
- D.  $\bar{A}B + AC + A\bar{B}$

gateit-2004 digital-logic boolean-algebra easy

[Answer key](#)

#### 4.5.31 Boolean Algebra: GATE IT 2005 | Question: 7 top



Which of the following expressions is equivalent to  $(A \oplus B) \oplus C$

- A.  $(A + B + C)(\bar{A} + \bar{B} + \bar{C})$
- B.  $(A + B + C)(\bar{A} + \bar{B} + C)$
- C.  $ABC + \bar{A}(B \oplus C) + \bar{B}(A \oplus C)$
- D. None of these

gateit-2005 digital-logic normal boolean-algebra

[Answer key](#)

### 4.6

#### Booths Algorithm (6) top



##### 4.6.1 Booths Algorithm: GATE CSE 1990 | Question: 8b top

State the Booth's algorithm for multiplication of two numbers. Draw a block diagram for the implementation of the Booth's algorithm for determining the product of two 8-bit signed numbers.

gate1990 descriptive digital-logic booths-algorithm

[Answer key](#)

##### 4.6.2 Booths Algorithm: GATE CSE 1996 | Question: 1.23 top



Booth's algorithm for integer multiplication gives worst performance when the multiplier pattern is

- A. 101010...1010
- B. 100000...0001
- C. 111111...1111
- D. 011111...1110

gate1996 digital-logic booths-algorithm normal

[Answer key](#)

#### 4.6.3 Booths Algorithm: GATE CSE 1999 | Question: 1.20 top



Booth's coding in 8 bits for the decimal number  $-57$  is:

- A.  $0 - 100 + 1000$    B.  $0 - 100 + 100 - 1$    C.  $0 - 1 + 100 - 10$    D.  $100 - 10 + 100 - 1$

gate1999 digital-logic number-representation booths-algorithm normal

[Answer key](#)

#### 4.6.4 Booths Algorithm: GATE IT 2005 | Question: 8 top



Using Booth's Algorithm for multiplication, the multiplier  $-57$  will be recoded as

- A.  $0 - 100100 - 1$   
C.  $0 - 1001000$       B.  $11000111$   
D.  $0100 - 1001$

gateit-2005 digital-logic booths-algorithm normal

[Answer key](#)

#### 4.6.5 Booths Algorithm: GATE IT 2006 | Question: 38 top



When multiplicand  $Y$  is multiplied by multiplier  $X = x_{n-1}x_{n-2}\dots x_0$  using bit-pair recoding in Booth's algorithm, partial products are generated according to the following table.

Row	$x_{i+1}$	$x_i$	$x_{i-1}$	Partial Product
1	0	0	0	0
2	0	0	1	$Y$
3	0	1	0	$Y$
4	0	1	1	$2Y$
5	1	0	0	?
6	1	0	1	$-Y$
7	1	1	0	$-Y$
8	1	1	1	?

The partial products for rows 5 and 8 are

- A.  $2Y$  and  $Y$       B.  $-2Y$  and  $2Y$       C.  $-2Y$  and 0      D. 0 and  $Y$

gateit-2006 digital-logic booths-algorithm difficult

[Answer key](#)

#### 4.6.6 Booths Algorithm: GATE IT 2008 | Question: 42 top



The two numbers given below are multiplied using the Booth's algorithm.

Multiplicand :  $0101\ 1010\ 1110\ 1110$

Multiplier:  $0111\ 0111\ 1011\ 1101$

How many additions/Subtractions are required for the multiplication of the above two numbers?

- A. 6      B. 8      C. 10      D. 12

gateit-2008 digital-logic booths-algorithm normal

[Answer key](#)

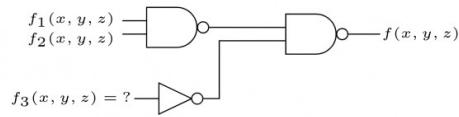
4.7

#### Canonical Normal Form (7) top



##### 4.7.1 Canonical Normal Form: GATE CSE 2002 | Question: 2-1 top

Consider the following logic circuit whose inputs are functions  $f_1, f_2, f_3$  and output is  $f$



Given that

- $f_1(x, y, z) = \Sigma(0, 1, 3, 5)$
- $f_2(x, y, z) = \Sigma(6, 7)$ , and
- $f(x, y, z) = \Sigma(1, 4, 5)$ .

$f_3$  is

- A.  $\Sigma(1, 4, 5)$   
 C.  $\Sigma(0, 1, 3, 5)$   
 B.  $\Sigma(6, 7)$   
 D. None of the above

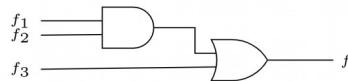
gatecse-2002 digital-logic normal canonical-normal-form circuit-output

[Answer key](#)



#### 4.7.2 Canonical Normal Form: GATE CSE 2008 | Question: 8 [top](#)

Given  $f_1$ ,  $f_3$  and  $f$  in canonical sum of products form (in decimal) for the circuit



$$f_1 = \Sigma m(4, 5, 6, 7, 8)$$

$$f_3 = \Sigma m(1, 6, 15)$$

$$f = \Sigma m(1, 6, 8, 15)$$

then  $f_2$  is

- A.  $\Sigma m(4, 6)$   
 C.  $\Sigma m(6, 8)$   
 B.  $\Sigma m(4, 8)$   
 D.  $\Sigma m(4, 6, 8)$

gatecse-2008 digital-logic canonical-normal-form easy

[Answer key](#)



#### 4.7.3 Canonical Normal Form: GATE CSE 2010 | Question: 6 [top](#)

The minterm expansion of  $f(P, Q, R) = PQ + QR + PR$  is

- A.  $m_2 + m_4 + m_6 + m_7$   
 C.  $m_0 + m_1 + m_6 + m_7$   
 B.  $m_0 + m_1 + m_3 + m_5$   
 D.  $m_2 + m_3 + m_4 + m_5$

gatecse-2010 digital-logic canonical-normal-form normal

[Answer key](#)



#### 4.7.4 Canonical Normal Form: GATE CSE 2015 Set 3 | Question: 43 [top](#)

The total number of prime implicants of the function  $f(w, x, y, z) = \sum(0, 2, 4, 5, 6, 10)$  is \_\_\_\_\_

gatecse-2015-set3 digital-logic canonical-normal-form normal numerical-answers

[Answer key](#)



#### 4.7.5 Canonical Normal Form: GATE CSE 2015 Set 3 | Question: 44 [top](#)

Given the function  $F = P' + QR$ , where  $F$  is a function in three Boolean variables  $P, Q$  and  $R$  and  $P' = !P$ , consider the following statements.

- (S1)  $F = \sum(4, 5, 6)$   
 (S2)  $F = \sum(0, 1, 2, 3, 7)$   
 (S3)  $F = \Pi(4, 5, 6)$



$$(S4)F = \Pi(0, 1, 2, 3, 7)$$

Which of the following is true?

- A. (S1)-False, (S2)-True, (S3)-True, (S4)-False
- B. (S1)-True, (S2)-False, (S3)-False, (S4)-True
- C. (S1)-False, (S2)-False, (S3)-True, (S4)-True
- D. (S1)-True, (S2)-True, (S3)-False, (S4)-False

gatecse-2015-set3 digital-logic canonical-normal-form normal

[Answer key](#)

#### 4.7.6 Canonical Normal Form: GATE CSE 2019 | Question: 50 [top](#)

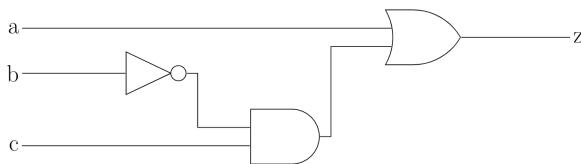
What is the minimum number of 2-input NOR gates required to implement a 4-variable function expressed in sum-of-minterms form as  $f = \Sigma(0, 2, 5, 7, 8, 10, 13, 15)$ ? Assume that all the inputs and their complements are available. Answer: \_\_\_\_\_

gatecse-2019 numerical-answers digital-logic canonical-normal-form 2-marks

[Answer key](#)

#### 4.7.7 Canonical Normal Form: GATE CSE 2020 | Question: 28 [top](#)

Consider the Boolean function  $z(a, b, c)$ .



Which one of the following minterm lists represents the circuit given above?

- A.  $z = \sum(0, 1, 3, 7)$
- B.  $z = \sum(1, 4, 5, 6, 7)$
- C.  $z = \sum(2, 4, 5, 6, 7)$
- D.  $z = \sum(2, 3, 5)$

gatecse-2020 digital-logic canonical-normal-form 2-marks

[Answer key](#)

### 4.8

#### Carry Generator (2) [top](#)

##### 4.8.1 Carry Generator: GATE CSE 2006 | Question: 36 [top](#)

Given two three bit numbers  $a_2a_1a_0$  and  $b_2b_1b_0$  and  $c$  the carry in, the function that represents the carry generate function when these two numbers are added is:

- A.  $a_2b_2 + a_2a_1b_1 + a_2a_1a_0b_0 + a_2a_0b_1b_0 + a_1b_2b_1 + a_1a_0b_2b_0 + a_0b_2b_1b_0$
- B.  $a_2b_2 + a_2b_1b_0 + a_2a_1b_1b_0 + a_1a_0b_2b_1 + a_1a_0b_2 + a_1a_0b_2b_0 + a_2a_0b_1b_0$
- C.  $a_2 + b_2 + (a_2 \oplus b_2)(a_1 + b_1 + (a_1 \oplus b_1) + (a_0 + b_0))$
- D.  $a_2b_2 + \overline{a_2}a_1b_1 + \overline{a_2}\overline{a_1}a_0b_0 + \overline{a_2}a_0\overline{b_1}b_0 + a_1\overline{b_2}b_1 + \overline{a_1}a_0\overline{b_2}b_0 + a_0\overline{b_2}\overline{b_1}b_0$

gatecse-2006 digital-logic normal carry-generator

[Answer key](#)

##### 4.8.2 Carry Generator: GATE CSE 2007 | Question: 35 [top](#)

In a look-ahead carry generator, the carry generate function  $G_i$  and the carry propagate function  $P_i$  for inputs  $A_i$  and  $B_i$  are given by:

$$P_i = A_i \oplus B_i \text{ and } G_i = A_i B_i$$

The expressions for the sum bit  $S_i$  and the carry bit  $C_{i+1}$  of the look ahead carry adder are given by:

$S_i = P_i \oplus C_i$  and  $C_{i+1} = G_i + P_i C_i$ , where  $C_0$  is the input carry.

Consider a two-level logic implementation of the look-ahead carry generator. Assume that all  $P_i$  and  $G_i$  are available for the carry generator circuit and that the AND and OR gates can have any number of inputs. The number of AND gates and OR gates needed to implement the look-ahead carry generator for a 4-bit adder with  $S_3, S_2, S_1, S_0$  and  $C_4$  as its outputs are respectively:

- A. 6,3      B. 10,4      C. 6,4      D. 10,5

gatecse-2007 digital-logic normal carry-generator adder

[Answer key](#)

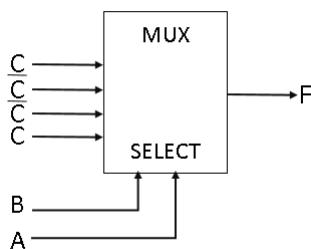
4.9

Circuit Output (40) [top](#)



4.9.1 Circuit Output: GATE CSE 1987 | Question: 1-IV [top](#)

The output  $F$  of the below multiplexer circuit can be represented by



- A.  $AB + B\bar{C} + \bar{C}A + \bar{B}\bar{C}$   
 B.  $A \oplus B \oplus C$   
 C.  $A \oplus B$   
 D.  $\bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C}$

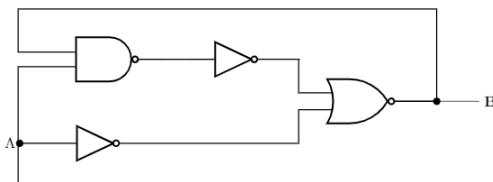
gate1987 digital-logic combinational-circuit multiplexer circuit-output

[Answer key](#)



4.9.2 Circuit Output: GATE CSE 1989 | Question: 4-ix [top](#)

Explain the behaviour of the following logic circuit with level input  $A$  and output  $B$ .



gate1989 descriptive digital-logic circuit-output

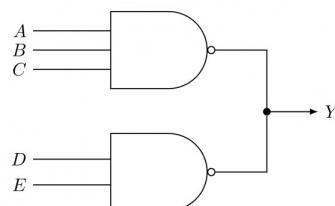
[Answer key](#)



4.9.3 Circuit Output: GATE CSE 1990 | Question: 3-i [top](#)

Choose the correct alternatives (More than one may be correct).

Two NAND gates having open collector outputs are tied together as shown in below figure.



The logic function  $Y$ , implemented by the circuit is,

A.  $Y = ABC + DE$

C.  $Y = ABC \cdot DE$

gate1990 normal digital-logic circuit-output

[Answer key](#)

B.  $Y = \overline{ABC + DE}$

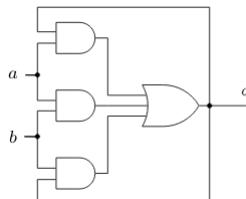
D.  $Y = \overline{ABC} \cdot \overline{DE}$



#### 4.9.4 Circuit Output: GATE CSE 1991 | Question: 5-a [top](#)

Analyse the circuit in Fig below and complete the following table

a	b	$Q_n$
0	0	
0	1	
1	0	
1	1	



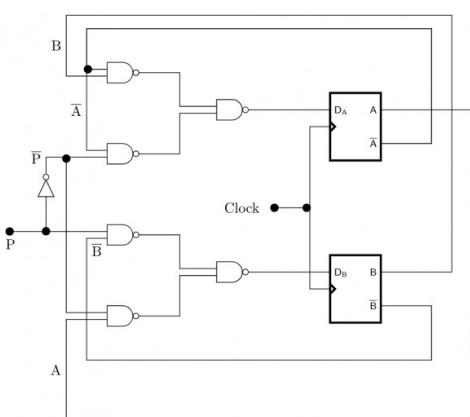
gate1991 digital-logic normal circuit-output sequential-circuit descriptive

[Answer key](#)



#### 4.9.5 Circuit Output: GATE CSE 1993 | Question: 19 [top](#)

A control algorithm is implemented by the NAND – gate circuitry given in figure below, where  $A$  and  $B$  are state variable implemented by  $D$  flip-flops, and  $P$  is control input. Develop the state transition table for this controller.



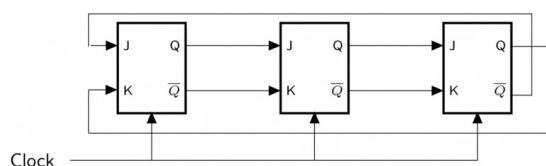
gate1993 digital-logic sequential-circuit flip-flop circuit-output normal descriptive

[Answer key](#)



#### 4.9.6 Circuit Output: GATE CSE 1993 | Question: 6-3 [top](#)

For the initial state of 000, the function performed by the arrangement of the J-K flip-flops in figure is:



- A. Shift Register  
 C. Mod- 6 Counter  
 E. None of the above

- B. Mod- 3 Counter  
 D. Mod- 2 Counter

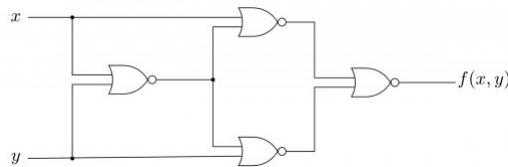
gate1993 digital-logic sequential-circuit flip-flop digital-counter circuit-output multiple-selects

[Answer key](#)

#### 4.9.7 Circuit Output: GATE CSE 1993 | Question: 6.1 [top](#)



Identify the logic function performed by the circuit shown in figure.



- A. exclusive OR      B. exclusive NOR      C. NAND      D. NOR      E. None of the above

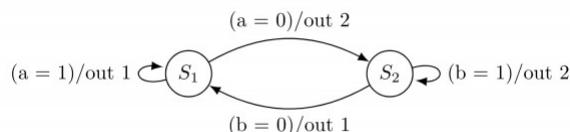
gate1993 digital-logic combinational-circuit circuit-output normal

[Answer key](#)

#### 4.9.8 Circuit Output: GATE CSE 1993 | Question: 6.2 [top](#)



If the state machine described in figure should have a stable state, the restriction on the inputs is given by



- A.  $a \cdot b = 1$   
 C.  $\bar{a} + \bar{b} = 0$   
 E.  $\overline{a + b} = 1$
- B.  $a + b = 1$   
 D.  $\overline{a \cdot b} = 1$

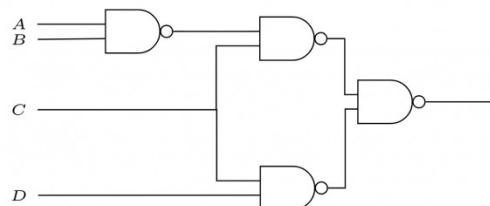
gate1993 digital-logic normal circuit-output sequential-circuit

[Answer key](#)

#### 4.9.9 Circuit Output: GATE CSE 1994 | Question: 1.8 [top](#)



The logic expression for the output of the circuit shown in figure below is:



- A.  $\overline{AC} + \overline{BC} + CD$   
 C.  $ABC + \overline{C} \overline{D}$
- B.  $\overline{AC} + \overline{BC} + CD$   
 D.  $\overline{A} \overline{B} + \overline{B} \overline{C} + CD$

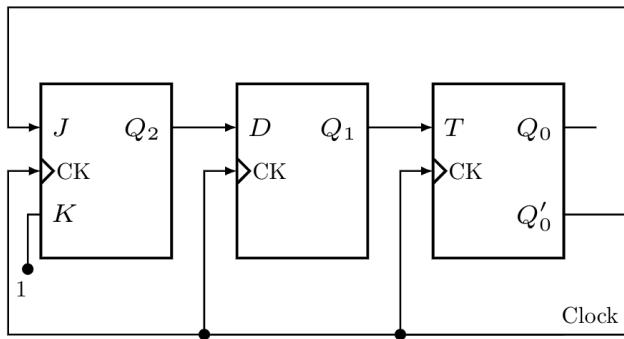
gate1994 digital-logic circuit-output normal

[Answer key](#)

#### 4.9.10 Circuit Output: GATE CSE 1994 | Question: 11 [top](#)



Find the contents of the flip-flop  $Q_2, Q_1$  and  $Q_0$  in the circuit of figure, after giving four clock pulses to the clock terminal. Assume  $Q_2Q_1Q_0 = 000$  initially.



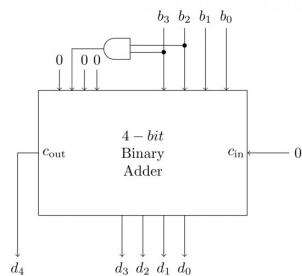
gate1994 digital-logic sequential-circuit digital-counter circuit-output normal descriptive

[Answer key](#)

#### 4.9.11 Circuit Output: GATE CSE 1996 | Question: 2.21 [top](#)



Consider the circuit in below figure which has a four bit binary number  $b_3 b_2 b_1 b_0$  as input and a five bit binary number,  $d_4 d_3 d_2 d_1 d_0$  as output.



- A. Binary to Hex conversion
- B. Binary to BCD conversion
- C. Binary to Gray code conversion
- D. Binary to radix – 12 conversion

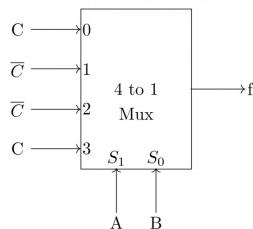
gate1996 digital-logic circuit-output normal

[Answer key](#)

#### 4.9.12 Circuit Output: GATE CSE 1996 | Question: 2.22 [top](#)



Consider the circuit in figure.  $f$  implements



- A.  $\overline{ABC} + \overline{AB}\overline{C} + ABC$
- B.  $A + B + C$
- C.  $A \oplus B \oplus C$
- D.  $AB + BC + CA$

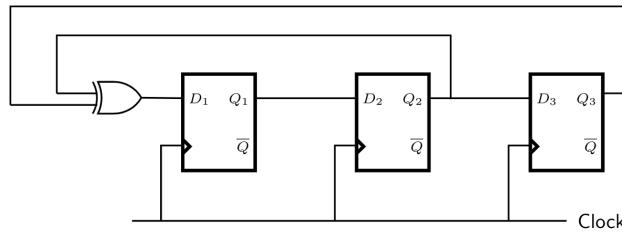
gate1996 digital-logic circuit-output easy multiplexer

[Answer key](#)

#### 4.9.13 Circuit Output: GATE CSE 1996 | Question: 24-a [top](#)



Consider the synchronous sequential circuit in the below figure



Draw a state diagram, which is implemented by the circuit. Use the following names for the states corresponding to the values of flip-flops as given below.

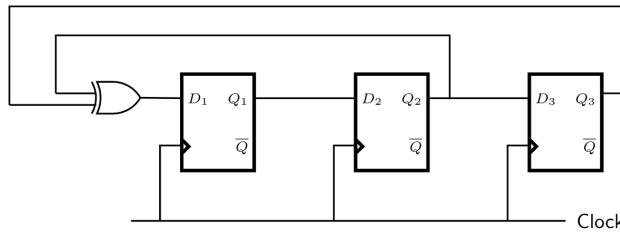
Q1	Q2	Q3	State
0	0	0	S <sub>0</sub>
0	0	1	S <sub>1</sub>
—	—	—	—
—	—	—	—
—	—	—	—
1	1	1	S <sub>7</sub>

gate1996 digital-logic circuit-output normal descriptive

**Answer key**

#### 4.9.14 Circuit Output: GATE CSE 1996 | Question: 24-b

Consider the synchronous sequential circuit in the below figure



Given that the initial state of the circuit is S<sub>4</sub>, identify the set of states, which are not reachable.

gate1996 normal digital-logic circuit-output descriptive

**Answer key**

#### 4.9.15 Circuit Output: GATE CSE 1997 | Question: 5.5

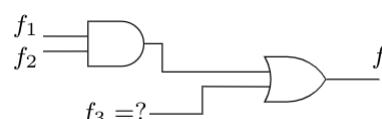


Consider a logic circuit shown in figure below. The functions f<sub>1</sub>, f<sub>2</sub> and f (in canonical sum of products form in decimal notation) are :

$$f_1(w, x, y, z) = \sum 8, 9, 10$$

$$f_2(w, x, y, z) = \sum 7, 8, 12, 13, 14, 15$$

$$f(w, x, y, z) = \sum 8, 9$$

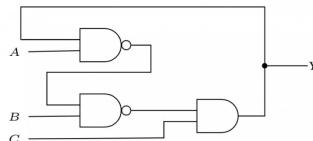


The function f<sub>3</sub> is

- A.  $\sum 9, 10$       B.  $\sum 9$       C.  $\sum 1, 8, 9$       D.  $\sum 8, 10, 15$

**Answer key****4.9.16 Circuit Output: GATE CSE 1999 | Question: 2.8**

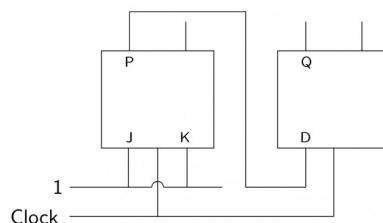
Consider the circuit shown below. In a certain steady state, the line  $Y$  is at '1'. What are the possible values of  $A, B$  and  $C$  in this state?



- A.  $A = 0, B = 0, C = 1$
- B.  $A = 0, B = 1, C = 1$
- C.  $A = 1, B = 0, C = 1$
- D.  $A = 1, B = 1, C = 1$

**Answer key****4.9.17 Circuit Output: GATE CSE 2000 | Question: 2.12**

The following arrangement of master-slave flip flops

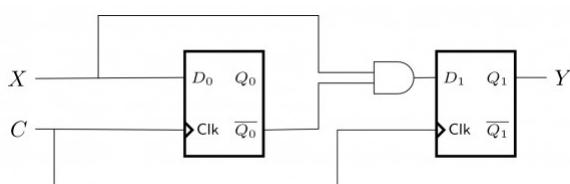


has the initial state of  $P, Q$  as 0, 1 (respectively). After three clock cycles the output state  $P, Q$  is (respectively),

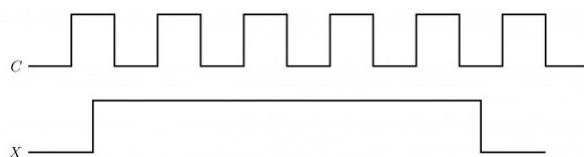
- A. 1,0
- B. 1,1
- C. 0,0
- D. 0,1

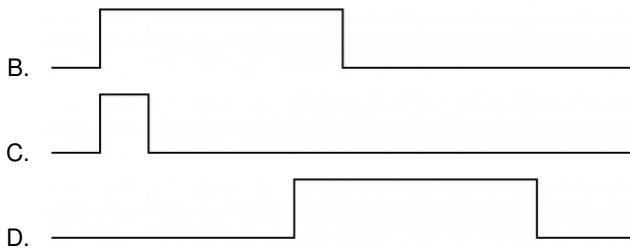
**Answer key****4.9.18 Circuit Output: GATE CSE 2001 | Question: 2.8**

Consider the following circuit with initial state  $Q_0 = Q_1 = 0$ . The D Flip-flops are positive edged triggered and have set up times 20 nanosecond and hold times 0.



Consider the following timing diagrams of  $X$  and  $C$ . The clock period of  $C \geq 40$  nanosecond. Which one is the correct plot of  $Y$ ?





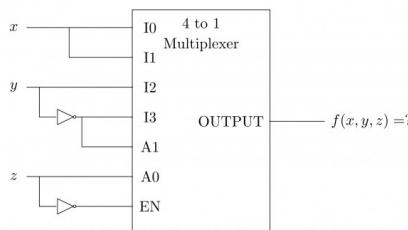
gatecse-2001 digital-logic circuit-output normal

[Answer key](#)

#### 4.9.19 Circuit Output: GATE CSE 2002 | Question: 2.2 [top](#)



Consider the following multiplexer where  $I_0, I_1, I_2, I_3$  are four data input lines selected by two address line combinations  $A_1A_0 = 00, 01, 10, 11$  respectively and  $f$  is the output of the multiplexor. EN is the Enable input.



The function  $f(x, y, z)$  implemented by the above circuit is

- A.  $xyz'$       B.  $xy + z$       C.  $x + y$       D. None of the above

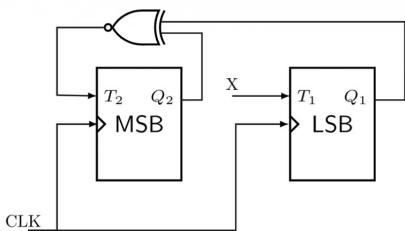
gatecse-2002 digital-logic circuit-output normal

[Answer key](#)

#### 4.9.20 Circuit Output: GATE CSE 2004 | Question: 61 [top](#)



Consider the partial implementation of a  $2-bit$  counter using  $T$  flip-flops following the sequence  $0 - 2 - 3 - 1 - 0$ , as shown below.



To complete the circuit, the input  $X$  should be

- A.  $Q_2^c$       B.  $Q_2 + Q_1$       C.  $(Q_1 + Q_2)^c$       D.  $Q_1 \oplus Q_2$

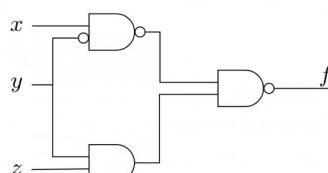
gatecse-2004 digital-logic circuit-output normal

[Answer key](#)

#### 4.9.21 Circuit Output: GATE CSE 2005 | Question: 15 [top](#)



Consider the following circuit.



Which one of the following is TRUE?

- A.  $f$  is independent of  $x$
- B.  $f$  is independent of  $y$
- C.  $f$  is independent of  $z$
- D. None of  $x, y, z$  is redundant

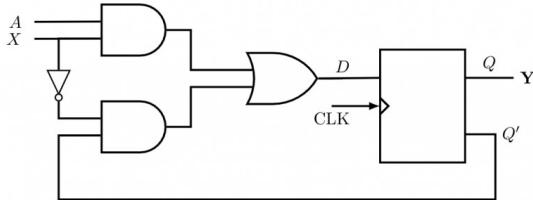
gatecse-2005 digital-logic circuit-output normal

[Answer key](#)

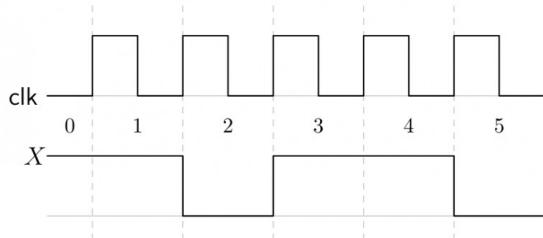
#### 4.9.22 Circuit Output: GATE CSE 2005 | Question: 62 [top](#)



Consider the following circuit involving a positive edge triggered D FF.



Consider the following timing diagram. Let  $A_i$  represents the logic level on the line  $A$  in the  $i$ -th clock period.



Let  $A'$  represent the complement of  $A$ . The correct output sequence on  $Y$  over the clock periods 1 through 5 is:

- A.  $A_0 A_1 A'_1 A_3 A_4$
- B.  $A_0 A_1 A'_1 A_3 A_4$
- C.  $A_1 A_2 A'_2 A_3 A_4$
- D.  $A_1 A'_2 A_3 A_4 A'_5$

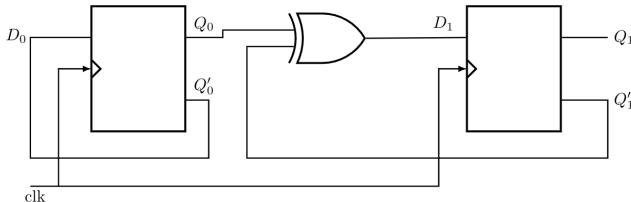
gatecse-2005 digital-logic circuit-output normal

[Answer key](#)

#### 4.9.23 Circuit Output: GATE CSE 2005 | Question: 64 [top](#)



Consider the following circuit:



The flip-flops are positive edge triggered  $D$  FFs. Each state is designated as a two-bit string  $Q_0 Q_1$ . Let the initial state be 00. The state transition sequence is

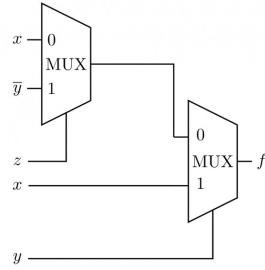
- A.  $00 \rightarrow 11 \rightarrow 01$
- B.  $00 \rightarrow 11$
- C.  $00 \rightarrow 10 \rightarrow 01 \rightarrow 11$
- D.  $00 \rightarrow 11 \rightarrow 01 \rightarrow 10$

gatecse-2005 digital-logic circuit-output

[Answer key](#)

#### 4.9.24 Circuit Output: GATE CSE 2006 | Question: 35 [top](#)





Consider the circuit above. Which one of the following options correctly represents  $f(x, y, z)$

- A.  $x\bar{z} + xy + \bar{y}z$   
 B.  $x\bar{z} + xy + \bar{y}\bar{z}$   
 C.  $xz + xy + \bar{y}z$   
 D.  $xz + x\bar{y} + \bar{y}z$

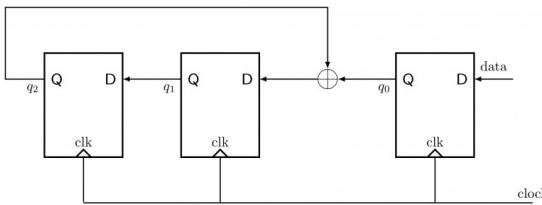
gatecse-2006 digital-logic circuit-output normal

Answer key

#### 4.9.25 Circuit Output: GATE CSE 2006 | Question: 37 top



Consider the circuit in the diagram. The  $\oplus$  operator represents Ex-OR. The D flip-flops are initialized to zeroes (cleared).



The following data: 100110000 is supplied to the “data” terminal in nine clock cycles. After that the values of  $q_2 q_1 q_0$  are:

- A. 000      B. 001      C. 010      D. 101

gatecse-2006 digital-logic circuit-output easy

Answer key

#### 4.9.26 Circuit Output: GATE CSE 2006 | Question: 8 top



You are given a free running clock with a duty cycle of 50% and a digital waveform  $f$  which changes only at the negative edge of the clock. Which one of the following circuits (using clocked D flip-flops) will delay the phase of  $f$  by 180°?



gatecse-2006 digital-logic normal circuit-output

Answer key

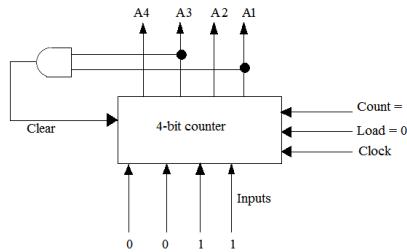
#### 4.9.27 Circuit Output: GATE CSE 2007 | Question: 36 top



The control signal functions of a 4-bit binary counter are given below (where X is “don’t care”):

Clear	Clock	Load	Count	Function
1	X	X	X	Clear to 0
0	X	0	0	No Change
0	↑	1	X	Load Input
0	↑	0	1	Count Next

The counter is connected as follows:



Assume that the counter and gate delays are negligible. If the counter starts at 0, then it cycles through the following sequence:

- A. 0,3,4      B. 0,3,4,5      C. 0,1,2,3,4      D. 0,1,2,3,4,5

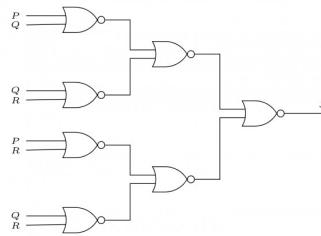
gatecse-2007 digital-logic circuit-output normal

[Answer key](#)

#### 4.9.28 Circuit Output: GATE CSE 2010 | Question: 31



What is the boolean expression for the output  $f$  of the combinational logic circuit of NOR gates given below?



- A.  $\overline{Q + R}$   
 C.  $\overline{P + R}$   
 B.  $\overline{P + Q}$   
 D.  $\overline{P + Q + R}$

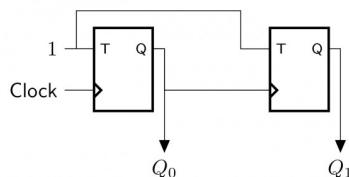
gatecse-2010 digital-logic circuit-output normal

[Answer key](#)

#### 4.9.29 Circuit Output: GATE CSE 2010 | Question: 32



In the sequential circuit shown below, if the initial value of the output  $Q_1Q_0$  is 00. What are the next four values of  $Q_1Q_0$ ?



- A. 11, 10, 01, 00  
 C. 10, 00, 01, 11  
 B. 10, 11, 01, 00  
 D. 11, 10, 00, 01

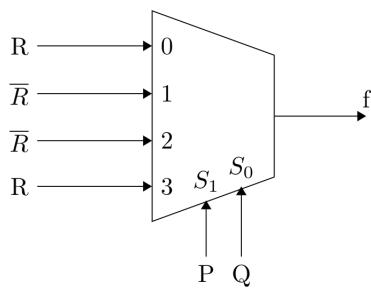
gatecse-2010 digital-logic circuit-output normal

[Answer key](#)

#### 4.9.30 Circuit Output: GATE CSE 2010 | Question: 9



The Boolean expression of the output  $f$  of the multiplexer shown below is



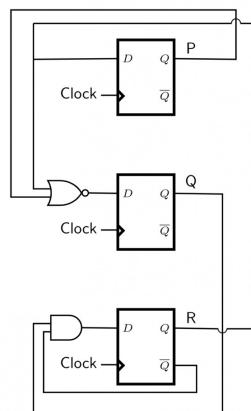
- A.  $\overline{P \oplus Q \oplus R}$   
 B.  $P \oplus Q \oplus R$   
 C.  $P + Q + R$   
 D.  $\overline{P + Q + R}$

gatecse-2010 digital-logic circuit-output easy

[Answer key](#)

#### 4.9.31 Circuit Output: GATE CSE 2011 | Question: 50

Consider the following circuit involving three D-type flip-flops used in a certain type of counter configuration.



If at some instance prior to the occurrence of the clock edge,  $P, Q$  and  $R$  have a value 0, 1 and 0 respectively, what shall be the value of  $PQR$  after the clock edge?

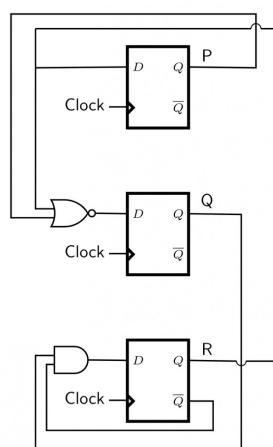
- A. 000      B. 001      C. 010      D. 011

gatecse-2011 digital-logic circuit-output flip-flop normal

[Answer key](#)

#### 4.9.32 Circuit Output: GATE CSE 2011 | Question: 51

Consider the following circuit involving three D-type flip-flops used in a certain type of counter configuration.



If all the flip-flops were reset to 0 at power on, what is the total number of distinct outputs (states) represented by

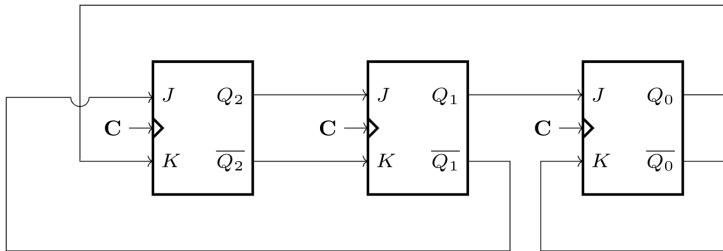
$PQR$  generated by the counter?

- A. 3      B. 4      C. 5      D. 6

gatecse-2011 digital-logic circuit-output normal

Answer key 

4.9.33 Circuit Output: GATE CSE 2014 Set 3 | Question: 45 



The above synchronous sequential circuit built using JK flip-flops is initialized with  $Q_2Q_1Q_0 = 000$ . The state sequence for this circuit for the next 3 clock cycles is

- A. 001,010,011      B. 111,110,101  
C. 100,110,111      D. 100,011,001

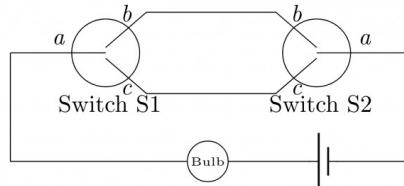
gatecse-2014-set3 digital-logic circuit-output normal

Answer key 

4.9.34 Circuit Output: GATE IT 2005 | Question: 10 



A two-way switch has three terminals  $a$ ,  $b$  and  $c$ . In ON position (logic value 1),  $a$  is connected to  $b$ , and in OFF position,  $a$  is connected to  $c$ . Two of these two-way switches  $S1$  and  $S2$  are connected to a bulb as shown below.



Which of the following expressions, if true, will always result in the lighting of the bulb ?

- A.  $S1\bar{S2}$       B.  $S1 + S2$   
C.  $\bar{S1} \oplus S2$       D.  $S1 \oplus S2$

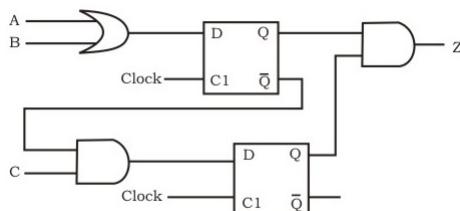
gateit-2005 digital-logic circuit-output normal

Answer key 

4.9.35 Circuit Output: GATE IT 2005 | Question: 43 



Which of the following input sequences will always generate a 1 at the output  $z$  at the end of the third cycle?



A	B	C
0	0	0
1	0	1
1	1	1

gateit-2005

digital-logic

circuit-output

normal

A	B	C
1	0	1
1	1	0
1	1	1

circuit-output

normal

A	B	C
0	1	1
1	0	1
1	1	1

A	B	C
0	0	1
1	1	0
1	1	1

gateit-2005

digital-logic

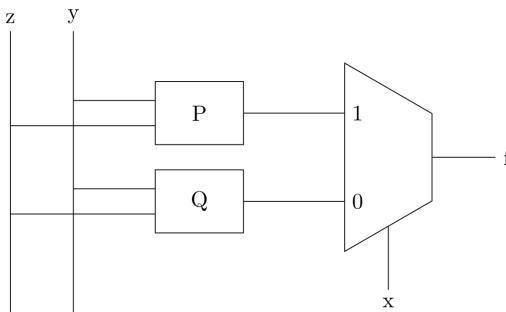
circuit-output

normal

Answer key

**4.9.36 Circuit Output: GATE IT 2006 | Question: 36** 

The majority function is a Boolean function  $f(x, y, z)$  that takes the value 1 whenever a majority of the variables  $x, y, z$  are 1. In the circuit diagram for the majority function shown below, the logic gates for the boxes labeled  $P$  and  $Q$  are, respectively,



A. XOR,AND

B. XOR,XOR

C. OR,OR

D. OR,AND

gateit-2006

digital-logic

circuit-output

normal

Answer key

**4.9.37 Circuit Output: GATE IT 2007 | Question: 38** 

The following expression was to be realized using 2-input AND and OR gates. However, during the fabrication all 2-input AND gates were mistakenly substituted by 2-input NAND gates.  
 $(a \cdot b) \cdot c + (a' \cdot c) \cdot d + (b \cdot c) \cdot d + a \cdot d$

What is the function finally realized ?

A. 1

C.  $a' + b + c' + d'$ B.  $a' + b' + c' + d'$ D.  $a' + b' + c + d'$ 

gateit-2007

digital-logic

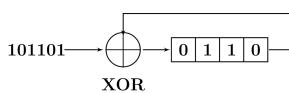
circuit-output

normal

Answer key

**4.9.38 Circuit Output: GATE IT 2007 | Question: 40** 

What is the final value stored in the linear feedback shift register if the input is 101101?



A. 0110

B. 1011

C. 1101

D. 1111

gateit-2007

digital-logic

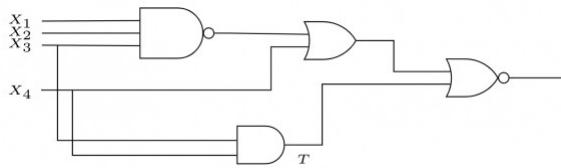
circuit-output

normal

Answer key

**4.9.39 Circuit Output: GATE IT 2007 | Question: 45** 

The line  $T$  in the following figure is permanently connected to the ground.



Which of the following inputs ( $X_1X_2X_3X_4$ ) will detect the fault ?

- A. 0000      B. 0111      C. 1111      D. None of these

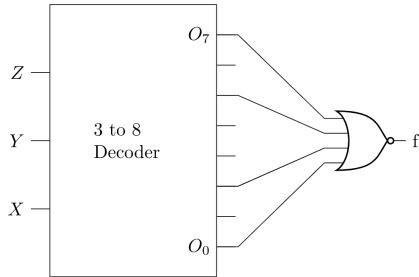
gateit-2007 digital-logic circuit-output normal

[Answer key](#)

#### 4.9.40 Circuit Output: GATE IT 2008 | Question: 9 top



What Boolean function does the circuit below realize?



- A.  $xz + \bar{x}\bar{z}$   
 B.  $x\bar{z} + \bar{x}z$   
 C.  $\bar{x}\bar{y} + yz$   
 D.  $xy + \bar{y}\bar{z}$

gateit-2008 digital-logic circuit-output normal

[Answer key](#)

#### 4.10

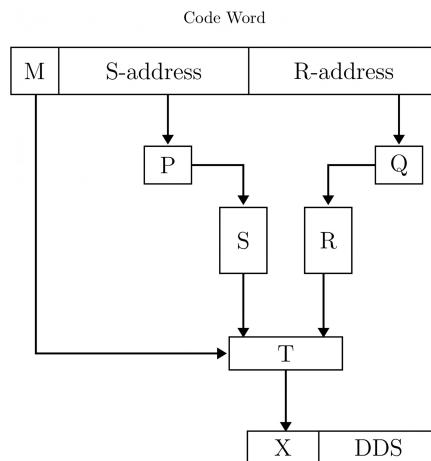
#### Combinational Circuit (1) top



#### 4.10.1 Combinational Circuit: GATE CSE 2022 | Question: 30 top



Consider a digital display system (DDS) shown in the figure that displays the contents of register X. A 16-bit code word is used to load a word in X, either from S or from R. S is a 1024-word memory segment and R is a 32-word register file. Based on the value of mode bit M, T selects an input word to load in X. P and Q interface with the corresponding bits in the code word to choose the addressed word. Which one of the following represents the functionality of P, Q, and T?



- A. P is 10 : 1 multiplexer;  
 B. P is 10 :  $2^{10}$  decoder;  
 C. P is 10 :  $2^{10}$  decoder;  
 D. P is 1 : 10 de-multiplexer;
- Q is 5 : 1 multiplexer;  
 Q is 5 :  $2^5$  decoder;  
 Q is 5 :  $2^5$  decoder;  
 Q is 1 : 5 de-multiplexer;
- T is 2 : 1 multiplexer  
 T is 2 : 1 encoder  
 T is 2 : 1 multiplexer  
 T is 2 : 1 multiplexer

**Answer key****4.11****Conjunctive Normal Form (1)** top**4.11.1 Conjunctive Normal Form: GATE CSE 2007 | Question: 48** top

Which of the following is TRUE about formulae in Conjunctive Normal Form?

- A. For any formula, there is a truth assignment for which at least half the clauses evaluate to true.
- B. For any formula, there is a truth assignment for which all the clauses evaluate to true.
- C. There is a formula such that for each truth assignment, at most one-fourth of the clauses evaluate to true.
- D. None of the above.

**Answer key****4.12****Decoder (2)** top**4.12.1 Decoder: GATE CSE 2007 | Question: 8, ISRO2011-31** top

How many 3-to-8 line decoders with an enable input are needed to construct a 6-to-64 line decoder without using any other logic gates?

- A. 7
- B. 8
- C. 9
- D. 10

**Answer key****4.12.2 Decoder: GATE CSE 2020 | Question: 20** top

If there are  $m$  input lines and  $n$  output lines for a decoder that is used to uniquely address a byte addressable 1 KB RAM, then the minimum value of  $m + n$  is \_\_\_\_\_.

**Answer key****4.13****Digital Circuits (7)** top**4.13.1 Digital Circuits: GATE CSE 1992 | Question: 02-ii** top

All digital circuits can be realized using only

- A. Ex-OR gates
- B. Multiplexers
- C. Half adders
- D. OR gates

**Answer key****4.13.2 Digital Circuits: GATE CSE 1996 | Question: 5** top

A logic network has two data inputs  $A$  and  $B$ , and two control inputs  $C_0$  and  $C_1$ . It implements the function  $F$  according to the following table.

$C_1$	$C_0$	$F$
0	0	$\overline{A + B}$
0	1	$A + B$
1	0	$A \oplus B$

Implement the circuit using one 4 to 1 Multiplexer, one 2-input Exclusive OR gate, one 2-input AND gate, one

2-input OR gate and one Inverter.

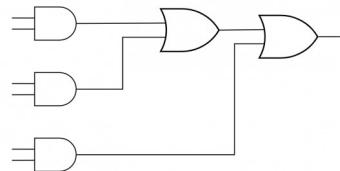
gate1996 digital-logic normal digital-circuits descriptive

Answer key 

#### 4.13.3 Digital Circuits: GATE CSE 2002 | Question: 7



- A. Express the function  $f(x, y, z) = xy' + yz'$  with only one complement operation and one or more AND/OR operations. Draw the logic circuit implementing the expression obtained, using a single NOT gate and one or more AND/OR gates.
- B. Transform the following logic circuit (without expressing its switching function) into an equivalent logic circuit that employs only 6 NAND gates each with 2-inputs.



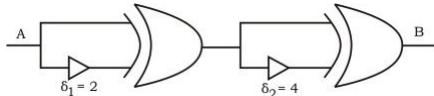
gatecse-2002 digital-logic normal descriptive digital-circuits

Answer key 

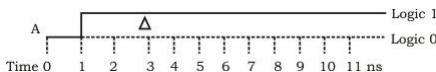
#### 4.13.4 Digital Circuits: GATE CSE 2003 | Question: 47



Consider the following circuit composed of XOR gates and non-inverting buffers.



The non-inverting buffers have delays  $\delta_1 = 2\text{ns}$  and  $\delta_2 = 4\text{ns}$  as shown in the figure. Both XOR gates and all wires have zero delays. Assume that all gate inputs, outputs, and wires are stable at logic level 0 at time 0. If the following waveform is applied at input  $A$ , how many transition(s) (change of logic levels) occur(s) at  $B$  during the interval from 0 to 10 ns?



- A. 1      B. 2      C. 3      D. 4

gatecse-2003 digital-logic digital-circuits

Answer key 

#### 4.13.5 Digital Circuits: GATE CSE 2011 | Question: 13



Which one of the following circuits is **NOT** equivalent to a 2-input *XNOR* (exclusive *NOR*) gate?



A.

gatecse-2011 digital-logic normal digital-circuits

Answer key 

#### 4.13.6 Digital Circuits: GATE CSE 2013 | Question: 5



In the following truth table,  $V = 1$  if and only if the input is valid.

Inputs				Outputs		
$D_0$	$D_1$	$D_2$	$D_3$	$X_0$	$X_1$	$V$
0	0	0	0	x	x	0
1	0	0	0	0	0	1
x	1	0	0	0	1	1
x	x	1	0	1	0	1
x	x	x	1	1	1	1

What function does the truth table represent?

- A. Priority encoder
- B. Decoder
- C. Multiplexer
- D. Demultiplexer

gatecse-2013 digital-logic normal digital-circuits

[Answer key](#)

#### 4.13.7 Digital Circuits: GATE CSE 2014 Set 3 | Question: 8 top



Consider the following combinational function block involving four Boolean variables  $x, y, a, b$  where  $x, a, b$  are inputs and  $y$  is the output.

```
f(x, a, b, y)
{
    if(x is 1) y = a;
    else y = b;
}
```

Which one of the following digital logic blocks is the most suitable for implementing this function?

- A. Full adder
- B. Priority encoder
- C. Multiplexor
- D. Flip-flop

gatecse-2014-set3 digital-logic easy digital-circuits

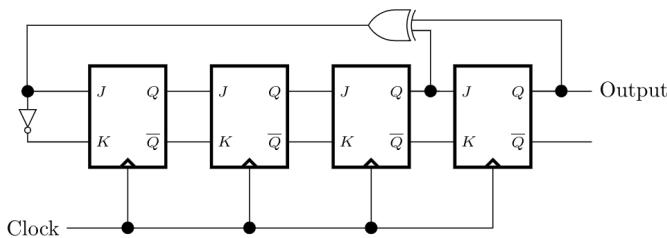
[Answer key](#)

#### 4.14

#### Digital Counter (16) top



#### 4.14.1 Digital Counter: GATE CSE 1987 | Question: 1-III top



The above circuit produces the output sequence:

- |                        |                        |
|------------------------|------------------------|
| A. 1111 1111 0000 0000 | B. 1111 0000 1111 0000 |
| C. 1111 0001 0011 0101 | D. 1010 1010 1010 1010 |

gate1987 digital-logic sequential-circuit flip-flop digital-counter

[Answer key](#)

#### 4.14.2 Digital Counter: GATE CSE 1987 | Question: 10c top



Give a minimal DFA that performs as a mod - 3, 1's counter, i.e. outputs a 1 each time the number of 1's in the input sequence is a multiple of 3.

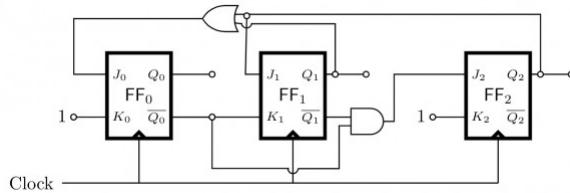
gate1987 digital-logic digital-counter descriptive

[Answer key](#)

#### 4.14.3 Digital Counter: GATE CSE 1990 | Question: 5-C top



For the synchronous counter shown in Fig.3, write the truth table of  $Q_0$ ,  $Q_1$ , and  $Q_2$  after each pulse, starting from  $Q_0 = Q_1 = Q_2 = 0$  and determine the counting sequence and also the modulus of the counter.



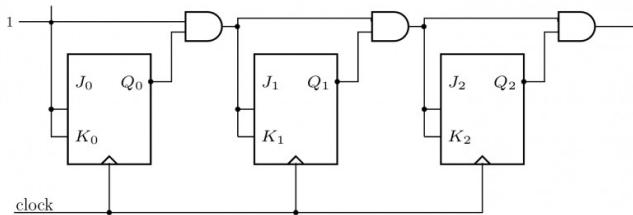
gate1990 descriptive digital-logic sequential-circuit flip-flop digital-counter

[Answer key](#)

#### 4.14.4 Digital Counter: GATE CSE 1991 | Question: 5-C top



Find the maximum clock frequency at which the counter in the figure below can be operated. Assume that the propagation delay through each flip flop and each AND gate is 10 ns. Also, assume that the setup time for the  $JK$  inputs of the flip flops is negligible.



gate1991 digital-logic sequential-circuit flip-flop digital-counter

[Answer key](#)

#### 4.14.5 Digital Counter: GATE CSE 1994 | Question: 2-1 top



The number of flip-flops required to construct a binary modulo  $N$  counter is \_\_\_\_\_

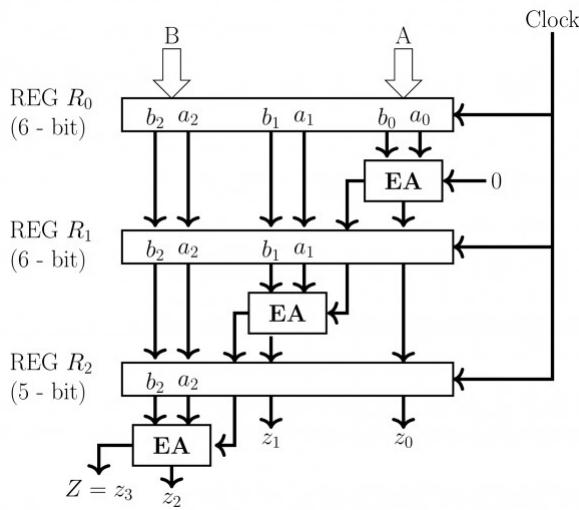
gate1994 digital-logic sequential-circuit flip-flop digital-counter fill-in-the-blanks

[Answer key](#)

#### 4.14.6 Digital Counter: GATE CSE 2002 | Question: 8 top



Consider the following circuit.  $A = a_2a_1a_0$  and  $B = b_2b_1b_0$  are three bit binary numbers input to the circuit. The output is  $Z = z_3z_2z_1z_0$ . R0, R1 and R2 are registers with loading clock shown. The registers are loaded with their input data with the falling edge of a clock pulse (signal CLOCK shown) and appears as shown. The bits of input number A, B and the full adders are as shown in the circuit. Assume Clock period is greater than the settling time of all circuits.



- a. For 8 clock pulses on the CLOCK terminal and the inputs  $A, B$  as shown, obtain the output  $Z$  (sequence of 4-bit values of  $Z$ ). Assume initial contents of  $R_0, R_1$  and  $R_2$  as all zeros.

A	110	011	111	101	000	000	000	000
B	101	101	011	110	000	000	000	000
Clock No	1	2	3	4	5	6	7	8

- b. What does the circuit implement?

gatecse-2002 digital-logic normal descriptive digital-counter

Answer key

#### 4.14.7 Digital Counter: GATE CSE 2011 | Question: 15 top



The minimum number of D flip-flops needed to design a mod-258 counter is

- A. 9      B. 8      C. 512      D. 258

gatecse-2011 digital-logic normal descriptive digital-counter

Answer key

#### 4.14.8 Digital Counter: GATE CSE 2014 Set 2 | Question: 7 top



Let  $k = 2^n$ . A circuit is built by giving the output of an  $n$ -bit binary counter as input to an  $n$ -to- $2^n$  bit decoder. This circuit is equivalent to a

- A.  $k$ -bit binary up counter.  
B.  $k$ -bit binary down counter.  
C.  $k$ -bit ring counter.  
D.  $k$ -bit Johnson counter.

gatecse-2014-set2 digital-logic normal descriptive digital-counter

Answer key

#### 4.14.9 Digital Counter: GATE CSE 2015 Set 1 | Question: 20 top



Consider a 4-bit Johnson counter with an initial value of 0000. The counting sequence of this counter is

- A. 0,1,3,7,15,14,12,8,0  
B. 0,1,3,5,7,9,11,13,15,0  
C. 0,2,4,6,8,10,12,14,0  
D. 0,8,12,14,15,7,3,1,0

gatecse-2015-set1 digital-logic digital-counter easy

Answer key

#### 4.14.10 Digital Counter: GATE CSE 2015 Set 2 | Question: 7 top



The minimum number of JK flip-flops required to construct a synchronous counter with the count sequence

$(0, 0, 1, 1, 2, 2, 3, 3, 0, 0, \dots)$  is \_\_\_\_\_.

gatecse-2015-set2 digital-logic digital-counter normal numerical-answers

Answer key

#### 4.14.11 Digital Counter: GATE CSE 2016 Set 1 | Question: 8

We want to design a synchronous counter that counts the sequence  $0 - 1 - 0 - 2 - 0 - 3$  and then repeats. The minimum number of J-K flip-flops required to implement this counter is \_\_\_\_\_.

gatecse-2016-set1 digital-logic digital-counter flip-flop normal numerical-answers

Answer key

#### 4.14.12 Digital Counter: GATE CSE 2017 Set 2 | Question: 42

The next state table of a 2-bit saturating up-counter is given below.

$Q_1$	$Q_0$	$Q_1^+$	$Q_0^+$
0	0	0	1
0	1	1	0
1	0	1	1
1	1	1	1

The counter is built as a synchronous sequential circuit using  $T$  flip-flops. The expressions for  $T_1$  and  $T_0$  are

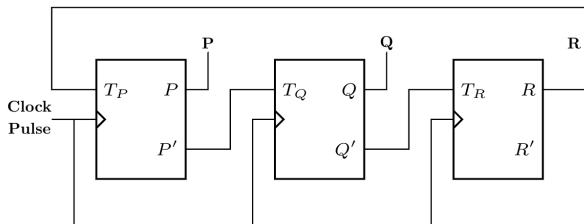
- A.  $T_1 = Q_1 Q_0, T_0 = \bar{Q}_1 \bar{Q}_0$
- B.  $T_1 = \bar{Q}_1 Q_0, T_0 = \bar{Q}_1 + \bar{Q}_0$
- C.  $T_1 = Q_1 + Q_0, T_0 = \bar{Q}_1 \bar{Q}_0$
- D.  $T_1 = \bar{Q}_1 Q_0, T_0 = Q_1 + Q_0$

gatecse-2017-set2 digital-logic digital-counter

Answer key

#### 4.14.13 Digital Counter: GATE CSE 2021 Set 1 | Question: 28

Consider a 3-bit counter, designed using  $T$  flip-flops, as shown below:



Assuming the initial state of the counter given by PQR as 000, what are the next three states?

- A. 011, 101, 000
- B. 001, 010, 111
- C. 011, 101, 111
- D. 001, 010, 000

gatecse-2021-set1 digital-logic sequential-circuit digital-counter 2-marks

Answer key

#### 4.14.14 Digital Counter: GATE IT 2005 | Question: 11

How many pulses are needed to change the contents of a 8-bit up counter from 10101100 to 00100111 (rightmost bit is the LSB)?

- A. 134
- B. 133
- C. 124
- D. 123

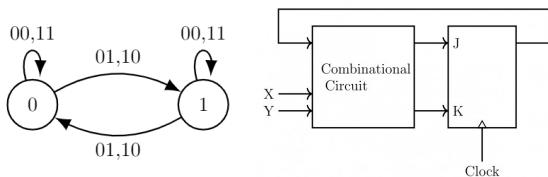
gateit-2005 digital-logic digital-counter normal

Answer key

#### 4.14.15 Digital Counter: GATE IT 2008 | Question: 37 [top](#)



Consider the following state diagram and its realization by a JK flip flop



The combinational circuit generates J and K in terms of x, y and Q.

The Boolean expressions for J and K are :

- A.  $\overline{x \oplus y}$  and  $\overline{x \oplus y}$
- B.  $\overline{x \oplus y}$  and  $x \oplus y$
- C.  $x \oplus y$  and  $\overline{x \oplus y}$
- D.  $x \oplus y$  and  $x \oplus y$

gateit-2008 digital-logic boolean-algebra normal digital-counter

[Answer key](#)

#### 4.14.16 Digital Counter: GATE1992-04-C [top](#)



Design a 3-bit counter using D-flip flops such that not more than one flip-flop changes state between any two consecutive states.

gate1992 digital-logic sequential-circuit flip-flop digital-counter normal descriptive

[Answer key](#)

#### 4.15

#### Dual Function (1) [top](#)

##### 4.15.1 Dual Function: GATE CSE 2014 Set 2 | Question: 6 [top](#)



The dual of a Boolean function  $F(x_1, x_2, \dots, x_n, +, \cdot, ', )$ , written as  $F^D$  is the same expression as that of  $F$  with  $+$  and  $\cdot$  swapped.  $F$  is said to be self-dual if  $F = F^D$ . The number of self-dual functions with  $n$  Boolean variables is

- A.  $2^n$
- B.  $2^{n-1}$
- C.  $2^{2^n}$
- D.  $2^{2^{n-1}}$

gatecse-2014-set2 digital-logic normal dual-function

[Answer key](#)

#### 4.16

#### Finite Automata (1) [top](#)

##### 4.16.1 Finite Automata: GATE CSE 1996 | Question: 2.23 [top](#)



Consider the following state table for a sequential machine. The number of states in the minimized machine will be

		Input	
		0	1
Present State	A	D,0	B,1
	B	A,0	C,1
	C	A,0	B,1
	D	A,1	C,1
		Next state, Output	

- A. 4
- B. 3
- C. 2
- D. 1

gate1996 normal finite-automata

[Answer key](#)

#### 4.17

#### Fixed Point Representation (2) [top](#)

#### 4.17.1 Fixed Point Representation: GATE CSE 2017 Set 1 | Question: 7

The  $n$ -bit fixed-point representation of an unsigned real number  $X$  uses  $f$  bits for the fraction part. Let  $i = n - f$ . The range of decimal values for  $X$  in this representation is

- A.  $2^{-f}$  to  $2^i$
- B.  $2^{-f}$  to  $(2^i - 2^{-f})$
- C. 0 to  $2^i$
- D. 0 to  $(2^i - 2^{-f})$

gatecse-2017-set1 digital-logic number-representation fixed-point-representation

[Answer key](#) 

#### 4.17.2 Fixed Point Representation: GATE CSE 2018 | Question: 33

Consider the unsigned 8-bit fixed point binary number representation, below,

$$b_7 \ b_6 \ b_5 \ b_4 \ b_3 \cdot b_2 \ b_1 \ b_0$$

where the position of the primary point is between  $b_3$  and  $b_2$ . Assume  $b_7$  is the most significant bit. Some of the decimal numbers listed below **cannot** be represented **exactly** in the above representation:

- i. 31.500
- ii. 0.875
- iii. 12.100
- iv. 3.001

Which one of the following statements is true?

- A. None of i, ii, iii, iv can be exactly represented
- B. Only ii cannot be exactly represented
- C. Only iii and iv cannot be exactly represented
- D. Only i and ii cannot be exactly represented

gatecse-2018 digital-logic number-representation fixed-point-representation normal 2-marks

[Answer key](#) 

#### 4.18

#### Flip Flop (6)

##### 4.18.1 Flip Flop: GATE CSE 2001 | Question: 11

A sequential circuit takes an input stream of 0's and 1's and produces an output stream of 0's and 1's. Initially it replicates the input on its output until two consecutive 0's are encountered on the input. From then onward, it produces an output stream, which is the bit-wise complement of input stream until it encounters two consecutive 1's, whereupon the process repeats. An example input and output stream is shown below.

The input stream: 101100|01001011|011

The desired output: 101100|10110100|011

J-K master-slave flip-flops are to be used to design the circuit.

- a. Give the state transition diagram
- b. Give the minimized sum-of-product expression for J and K inputs of one of its state flip-flops

gatecse-2001 digital-logic normal descriptive flip-flop

[Answer key](#) 

##### 4.18.2 Flip Flop: GATE CSE 2004 | Question: 18, ISRO2007-31

In an SR latch made by cross-coupling two NAND gates, if both S and R inputs are set to 0, then it will result in

- A.  $Q = 0, Q' = 1$
- B.  $Q = 1, Q' = 0$
- C.  $Q = 1, Q' = 1$
- D. Indeterminate states

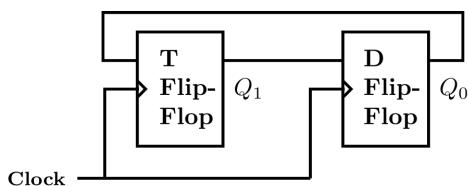
**Answer key****4.18.3 Flip Flop: GATE CSE 2015 Set 1 | Question: 37**

A positive edge-triggered  $D$  flip-flop is connected to a positive edge-triggered  $JK$  flip-flop as follows. The  $Q$  output of the  $D$  flip-flop is connected to both the  $J$  and  $K$  inputs of the  $JK$  flip-flop, while the  $Q$  output of the  $JK$  flip-flop is connected to the input of the  $D$  flip-flop. Initially, the output of the  $D$  flip-flop is set to logic one and the output of the  $JK$  flip-flop is cleared. Which one of the following is the bit sequence (including the initial state) generated at the  $Q$  output of the  $JK$  flip-flop when the flip-flops are connected to a free-running common clock? Assume that  $J = K = 1$  is the toggle mode and  $J = K = 0$  is the state holding mode of the  $JK$  flip-flops. Both the flip-flops have non-zero propagation delays.

- A. 0110110...
- B. 0100100...
- C. 011101110...
- D. 011001100...

**Answer key****4.18.4 Flip Flop: GATE CSE 2017 Set 1 | Question: 33**

Consider a combination of  $T$  and  $D$  flip-flops connected as shown below. The output of the  $D$  flip-flop is connected to the input of the  $T$  flip-flop and the output of the  $T$  flip-flop is connected to the input of the  $D$  flip-flop.

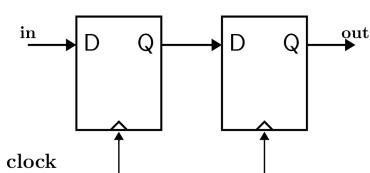


Initially, both  $Q_0$  and  $Q_1$  are set to 1 (before the 1<sup>st</sup> clock cycle). The outputs

- A.  $Q_1Q_0$  after the 3<sup>rd</sup> cycle are 11 and after the 4<sup>th</sup> cycle are 00 respectively.
- B.  $Q_1Q_0$  after the 3<sup>rd</sup> cycle are 11 and after the 4<sup>th</sup> cycle are 01 respectively.
- C.  $Q_1Q_0$  after the 3<sup>rd</sup> cycle are 00 and after the 4<sup>th</sup> cycle are 11 respectively.
- D.  $Q_1Q_0$  after the 3<sup>rd</sup> cycle are 01 and after the 4<sup>th</sup> cycle are 01 respectively.

**Answer key****4.18.5 Flip Flop: GATE CSE 2018 | Question: 22**

Consider the sequential circuit shown in the figure, where both flip-flops used are positive edge-triggered  $D$  flip-flops.



The number of states in the state transition diagram of this circuit that have a transition back to the same state on some value of "in" is \_\_\_\_\_

**Answer key**

#### 4.18.6 Flip Flop: GATE IT 2007 | Question: 7 [top](#)



Which of the following input sequences for a cross-coupled  $R - S$  flip-flop realized with two  $NAND$  gates may lead to an oscillation?

- A. 11,00      B. 01,10      C. 10,01      D. 00,11

gateit-2007 digital-logic normal flip-flop

[Answer key](#)

#### 4.19

#### Floating Point Representation (9) [top](#)



##### 4.19.1 Floating Point Representation: GATE CSE 1987 | Question: 1-vii [top](#)

The exponent of a floating-point number is represented in excess- $N$  code so that:

- A. The dynamic range is large.  
B. The precision is high.  
C. The smallest number is represented by all zeros.  
D. Overflow is avoided.

gate1987 digital-logic number-representation floating-point-representation

[Answer key](#)

##### 4.19.2 Floating Point Representation: GATE CSE 1989 | Question: 1-vi [top](#)



Consider an excess -50 representation for floating point numbers with 4 BCD digit mantissa and 2 BCD digit exponent in normalised form. The minimum and maximum positive numbers that can be represented are \_\_\_\_\_ and \_\_\_\_\_ respectively.

descriptive gate1989 digital-logic number-representation floating-point-representation

[Answer key](#)

##### 4.19.3 Floating Point Representation: GATE CSE 1990 | Question: 1-iv-a [top](#)



A 32-bit floating-point number is represented by a 7-bit signed exponent, and a 24-bit fractional mantissa. The base of the scale factor is 16,  
The range of the exponent is \_\_\_\_\_

gate1990 digital-logic number-representation floating-point-representation fill-in-the-blanks

[Answer key](#)

##### 4.19.4 Floating Point Representation: GATE CSE 1990 | Question: 1-iv-b [top](#)



A 32-bit floating-point number is represented by a 7-bit signed exponent, and a 24-bit fractional mantissa. The base of the scale factor is 16,  
The range of the exponent is \_\_\_\_\_, if the scale factor is represented in excess-64 format.

gate1990 digital-logic number-representation floating-point-representation fill-in-the-blanks

[Answer key](#)

##### 4.19.5 Floating Point Representation: GATE CSE 1997 | Question: 72 [top](#)



Following floating point number format is given

$f$  is a fraction represented by a 6-bit mantissa (includes sign bit) in sign magnitude form,  $e$  is a 4-bit exponent (includes sign bit) in sign magnitude form and  $n = (f, e) = f \cdot 2^e$  is a floating point number. Let  $A = 54.75$  in decimal and  $B = 9.75$  in decimal

- Represent  $A$  and  $B$  as floating point numbers in the above format.
- Show the steps involved in floating point addition of  $A$  and  $B$ .
- What is the percentage error (up to one position beyond decimal point) in the addition operation in (b)?

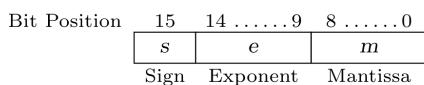
gate1997 digital-logic floating-point-representation normal descriptive

[Answer key](#)

#### 4.19.6 Floating Point Representation: GATE CSE 2003 | Question: 43 top



The following is a scheme for floating point number representation using 16 bits.



Let  $s$ ,  $e$ , and  $m$  be the numbers represented in binary in the sign, exponent, and mantissa fields respectively. Then the floating point number represented is:

$$\begin{cases} (-1)^s (1 + m \times 2^{-9}) 2^{e-31}, & \text{if the exponent } \neq 111111 \\ 0, & \text{otherwise} \end{cases}$$

What is the maximum difference between two successive real numbers representable in this system?

- A.  $2^{-40}$       B.  $2^{-9}$       C.  $2^{22}$       D.  $2^{31}$

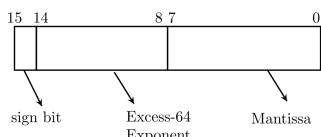
gatecse-2003 digital-logic number-representation floating-point-representation normal

[Answer key](#)

#### 4.19.7 Floating Point Representation: GATE CSE 2005 | Question: 85-a top



Consider the following floating-point format.



Mantissa is a pure fraction in sign-magnitude form.

The decimal number  $0.239 \times 2^{13}$  has the following hexadecimal representation (without normalization and rounding off):

- A. 0D 24      B. 0D 4D      C. 4D 0D      D. 4D 3D

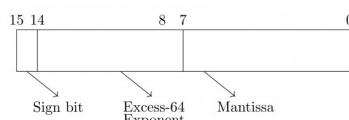
gatecse-2005 digital-logic number-representation floating-point-representation normal

[Answer key](#)

#### 4.19.8 Floating Point Representation: GATE CSE 2005 | Question: 85-b top



Consider the following floating-point format.



Mantissa is a pure fraction in sign-magnitude form.

The normalized representation for the above format is specified as follows. The mantissa has an implicit 1 preceding the binary (radix) point. Assume that only 0's are padded in while shifting a field.

The normalized representation of the above number ( $0.239 \times 2^{13}$ ) is:

- A. 0A 20      B. 11 34      C. 49 D0      D. 4A E8

gatecse-2005 digital-logic number-representation floating-point-representation normal

[Answer key](#)

#### 4.19.9 Floating Point Representation: GATE CSE 2020 | Question: 29 top



Consider three registers  $R1$ ,  $R2$ , and  $R3$  that store numbers in IEEE-754 single precision floating point format. Assume that  $R1$  and  $R2$  contain the values (in hexadecimal notation)  $0x42200000$  and

0xC1200000, respectively.

If  $R3 = \frac{R1}{R2}$ , what is the value stored in  $R3$ ?

- A. 0x40800000      B. 0xC0800000      C. 0x83400000      D. 0xC8500000

gatecse-2020 floating-point-representation digital-logic 2-marks

[Answer key](#)

4.20

Functional Completeness (4) [top](#)

#### 4.20.1 Functional Completeness: GATE CSE 1989 | Question: 4-iii [top](#)



Show that  $\{\text{NOR}\}$  is a functionally complete set of Boolean operations.

gate1989 descriptive digital-logic functional-completeness

[Answer key](#)

#### 4.20.2 Functional Completeness: GATE CSE 1998 | Question: 5 [top](#)



The implication gate, shown below has two inputs ( $x$  and  $y$ ); the output is 1 except when  $x = 1$  and  $y = 0$ , realize  $f = \bar{x}y + x\bar{y}$  using only four implication gates.



Show that the implication gate is functionally complete.

gate1998 digital-logic functional-completeness descriptive

[Answer key](#)

#### 4.20.3 Functional Completeness: GATE CSE 1999 | Question: 2.9 [top](#)



Which of the following sets of component(s) is/are sufficient to implement any arbitrary Boolean function?

- A. XOR gates, NOT gates
- B. 2 to 1 multiplexers
- C. AND gates, XOR gates
- D. Three-input gates that output  $(A \cdot B) + C$  for the inputs  $A, B$  and  $C$ .

gate1999 digital-logic normal functional-completeness multiple-selects

[Answer key](#)

#### 4.20.4 Functional Completeness: GATE IT 2008 | Question: 1 [top](#)



A set of Boolean connectives is functionally complete if all Boolean functions can be synthesized using those. Which of the following sets of connectives is NOT functionally complete?

- A. EX-NOR
- B. implication, negation
- C. OR, negation
- D. NAND

gateit-2008 digital-logic easy functional-completeness

[Answer key](#)

4.21

Ieee Representation (7) [top](#)

#### 4.21.1 Ieee Representation: GATE CSE 2008 | Question: 4 [top](#)



In the IEEE floating point representation the hexadecimal value 0x00000000 corresponds to

- A. The normalized value  $2^{-127}$
- B. The normalized value  $2^{-126}$
- C. The normalized value  $+0$
- D. The special value  $+0$

**Answer key****4.21.2 IEEE Representation: GATE CSE 2012 | Question: 7**

The decimal value 0.5 in IEEE single precision floating point representation has

- A. fraction bits of 000...000 and exponent value of 0
- B. fraction bits of 000...000 and exponent value of -1
- C. fraction bits of 100...000 and exponent value of 0
- D. no exact representation

**Answer key****4.21.3 IEEE Representation: GATE CSE 2014 Set 2 | Question: 45**

The value of a float type variable is represented using the single-precision 32-bit floating point format of IEEE-754 standard that uses 1 bit for sign, 8 bits for biased exponent and 23 bits for the mantissa. A float type variable  $X$  is assigned the decimal value of -14.25. The representation of  $X$  in hexadecimal notation is

- A. C1640000H
- B. 416C0000H
- C. 41640000H
- D. C16C0000H

**Answer key****4.21.4 IEEE Representation: GATE CSE 2017 Set 2 | Question: 12**

Given the following binary number in 32-bit (single precision) IEEE-754 format :

00111110011011010000000000000000

The decimal value closest to this floating-point number is :

- A.  $1.45 \times 10^1$
- B.  $1.45 \times 10^{-1}$
- C.  $2.27 \times 10^{-1}$
- D.  $2.27 \times 10^1$

**Answer key****4.21.5 IEEE Representation: GATE CSE 2021 Set 1 | Question: 24**

Consider the following representation of a number in IEEE 754 single-precision floating point format with a bias of 127.

$S : 1$      $E : 10000001$      $F : 1111000000000000000000000$

Here  $S$ ,  $E$  and  $F$  denote the sign, exponent, and fraction components of the floating point representation.

The decimal value corresponding to the above representation (rounded to 2 decimal places) is \_\_\_\_\_.

**Answer key****4.21.6 IEEE Representation: GATE CSE 2021 Set 2 | Question: 4**

The format of the single-precision floating point representation of a real number as per the IEEE 754 standard is as follows:



Which one of the following choices is correct with respect to the *smallest* normalized positive number represented using the standard?

- A. exponent = 00000000 and mantissa = 00000000000000000000000000000000  
 B. exponent = 00000000 and mantissa = 00000000000000000000000000000001  
 C. exponent = 00000001 and mantissa = 00000000000000000000000000000000  
 D. exponent = 00000001 and mantissa = 00000000000000000000000000000001

gatecse-2021-set2 digital-logic number-representation ieee-representation 1-mark

[Answer key](#)



#### 4.21.7 Ieee Representation: GATE IT 2008 | Question: 7

The following bit pattern represents a floating point number in IEEE 754 single precision format  
**1 10000011 10100000000000000000000000000000**

The value of the number in decimal form is

- A. -10      B. -13      C. -26      D. None of the above

gateit-2008 digital-logic number-representation floating-point-representation ieee-representation normal

[Answer key](#)



#### 4.22

#### K Map (19)

#### 4.22.1 K Map: GATE CSE 1987 | Question: 16-a

A Boolean function  $f$  is to be realized only by NOR gates. Its  $K$ -map is given below:

		ab	00	01	11	10
		c	0	0	1	1
		1	0	1	1	1
			0	0	1	1

The realization is

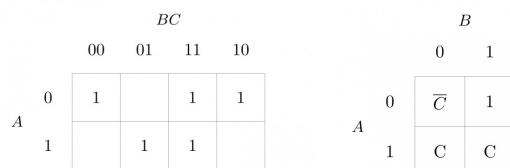
- A.      B.      C.      D.
- 

gate1987 digital-logic k-map

[Answer key](#)



#### 4.22.2 K Map: GATE CSE 1988 | Question: 3a-b



The Karnaugh map of a function of  $(A, B, C)$  is shown on the left hand side of the above figure.

The reduced form of the same map is shown on the right hand side, in which the variable  $C$  is entered in the map itself. Discuss,

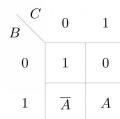
- a. The methodology by which the reduced map has been derived and
- b. the rules (or steps) by which the boolean function can be derived from the entries in the reduced map.

gate1988 descriptive digital-logic k-map

Answer key 

### 4.22.3 K Map: GATE CSE 1992 | Question: 01-i

The Boolean function in sum of products form where K-map is given below (figure) is \_\_\_\_\_



gate1992 digital-logic k-map normal fill-in-the-blanks

Answer key 

### 4.22.4 K Map: GATE CSE 1995 | Question: 15-a

Implement a circuit having the following output expression using an inverter and a nand gate

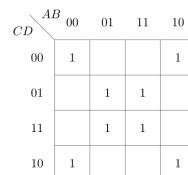
$$Z = \overline{A} + \overline{B} + C$$

gate1995 digital-logic k-map normal descriptive

Answer key 

### 4.22.5 K Map: GATE CSE 1995 | Question: 15-b

What is the equivalent minimal Boolean expression (in sum of products form) for the Karnaugh map given below?

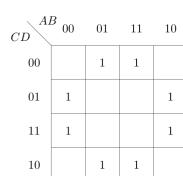


gate1995 digital-logic boolean-algebra k-map normal descriptive

Answer key 

### 4.22.6 K Map: GATE CSE 1996 | Question: 2.24

What is the equivalent Boolean expression in product-of-sums form for the Karnaugh map given in Fig



- A.  $B\overline{D} + \overline{B}D$
- B.  $(B + \overline{C} + D)(\overline{B} + C + \overline{D})$
- C.  $(B + D)(\overline{B} + \overline{D})$
- D.  $(B + \overline{D})(\overline{B} + D)$

gate1996 digital-logic k-map easy

Answer key 

#### 4.22.7 K Map: GATE CSE 1998 | Question: 2.7 top



The function represented by the Karnaugh map given below is

		BC			
		00	01	10	11
A	0	1	0	0	1
	1	1	0	0	1

- A.  $A \cdot B$       B.  $AB + BC + CA$     C.  $\overline{B} \oplus \overline{C}$       D.  $A \cdot BC$

gate1998 digital-logic k-map normal

[Answer key](#)

#### 4.22.8 K Map: GATE CSE 1999 | Question: 1.8 top



Which of the following functions implements the Karnaugh map shown below?

		CD			
		00	01	11	10
AB	00	0	0	1	0
	01	X	X	1	X
11	0	1	1	0	
10	0	1	1	0	

- A.  $\bar{A}B + CD$   
 C.  $AD + \bar{A}\bar{B}$       B.  $D(C + A)$   
 D.  $(C + D)(\bar{C} + D) + (A + B)$

gate1999 digital-logic k-map easy

[Answer key](#)

#### 4.22.9 K Map: GATE CSE 2000 | Question: 2.11 top



Which functions does NOT implement the Karnaugh map given below?

		wz			
		00	01	11	10
xy	00	0	X	0	0
	01	0	X	1	1
11	1	1	1	1	
10	0	X	0	0	

- A.  $(w + x)y$   
 C.  $(w + x)(\bar{w} + y)(\bar{x} + y)$       B.  $xy + yw$   
 D. None of the above

gatecse-2000 digital-logic k-map normal

[Answer key](#)

#### 4.22.10 K Map: GATE CSE 2001 | Question: 1.11 top



Given the following karnaugh map, which one of the following represents the minimal Sum-Of-Products of the map?

		wx			
		00	01	11	10
yz	00	0	X	0	X
	01	X	1	X	1
11	0	X	1	0	
10	0	1	X	0	

- A.  $XY + Y'Z$       B.  $WX'Y' + XY + XZW'X + Y'Z + XYD$ . D.  $XZ + Y$

gatecse-2001 k-map digital-logic normal

[Answer key](#)

#### 4.22.11 K Map: GATE CSE 2002 | Question: 1.12 top



Minimum sum of product expression for  $f(w, x, y, z)$  shown in Karnaugh-map below

		wx	00	01	11	10
		yz	00	01	11	10
		00	0	1	1	0
		01	X	0	0	1
		11	X	0	0	1
		10	0	1	1	X

- A.  $xz + y'z$       B.  $xz' + zx'$       C.  $x'y + zx'$       D. None of the above

gatecse-2002 digital-logic k-map normal

[Answer key](#)

#### 4.22.12 K Map: GATE CSE 2003 | Question: 45 top



The literal count of a Boolean expression is the sum of the number of times each literal appears in the expression. For example, the literal count of  $(xy + xz')$  is 4. What are the minimum possible literal counts of the product-of-sum and sum-of-product representations respectively of the function given by the following Karnaugh map? Here,  $X$  denotes "don't care"

		zw	00	01	11	10
		xy	00	01	11	10
		00	X	1	0	1
		01	0	1	X	0
		11	1	X	X	0
		10	X	0	0	X

- A. (11,9)      B. (9,13)      C. (9,10)      D. (11,11)

gatecse-2003 digital-logic k-map normal

[Answer key](#)

#### 4.22.13 K Map: GATE CSE 2008 | Question: 5 top



In the Karnaugh map shown below,  $X$  denotes a don't care term. What is the minimal form of the function represented by the Karnaugh map?

		ab	00	01	11	10
		cd	00	1	1	
		00	1	1		1
		01	X			
		11	X			
		10	1	1		X

- A.  $\bar{b}.\bar{d} + \bar{a}.\bar{d}$       B.  $\bar{a}.\bar{b} + \bar{b}.\bar{d} + \bar{a}.b.\bar{d}$   
 C.  $\bar{b}.\bar{d} + \bar{a}.b.\bar{d}$       D.  $\bar{a}.\bar{b} + \bar{b}.\bar{d} + \bar{a}.d$

gatecse-2008 digital-logic k-map easy

Answer key

#### 4.22.14 K Map: GATE CSE 2012 | Question: 30



What is the minimal form of the Karnaugh map shown below? Assume that  $X$  denotes a don't care term

		ab	00	01	11	10	
		cd	00	01	11	10	
00	01	00	1	X	X	1	
		01	X			1	
11	10	00					
		01				X	
		ab	00	01	11	10	
		cd	00	01	11	10	

- A.  $\bar{b}\bar{d}$   
B.  $\bar{b}\bar{d} + \bar{b}\bar{c}$   
C.  $\bar{b}\bar{d} + a\bar{b}\bar{c}\bar{d}$   
D.  $\bar{b}\bar{d} + \bar{b}\bar{c} + \bar{c}\bar{d}$

gatecse-2012 digital-logic k-map easy

Answer key

#### 4.22.15 K Map: GATE CSE 2017 Set 1 | Question: 21



Consider the Karnaugh map given below, where  $X$  represents "don't care" and blank represents 0.

		ba	00	01	11	10
		dc	00	01	11	10
00	01	00		X	X	
		01	1			X
11	10	00	1			1
		01		X	X	

Assume for all inputs  $(a, b, c, d)$ , the respective complements  $(\bar{a}, \bar{b}, \bar{c}, \bar{d})$  are also available. The above logic is implemented using 2-input NOR gates only. The minimum number of gates required is \_\_\_\_\_.

gatecse-2017-set1 digital-logic k-map numerical-answers normal

Answer key

#### 4.22.16 K Map: GATE CSE 2019 | Question: 30



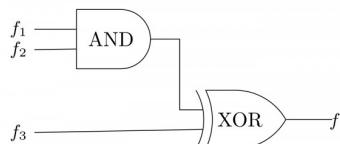
Consider three 4-variable functions  $f_1, f_2$ , and  $f_3$ , which are expressed in sum-of-minterms as

$$f_1 = \Sigma(0, 2, 5, 8, 14),$$

$$f_2 = \Sigma(2, 3, 6, 8, 14, 15),$$

$$f_3 = \Sigma(2, 7, 11, 14)$$

For the following circuit with one AND gate and one XOR gate the output function  $f$  can be expressed as:



- A.  $\Sigma(7, 8, 11)$   
B.  $\Sigma(2, 7, 8, 11, 14)$   
C.  $\Sigma(2, 14)$   
D.  $\Sigma(0, 2, 3, 5, 6, 7, 8, 11, 14, 15)$

gatecse-2019 digital-logic k-map digital-circuits 2-marks

Answer key

#### 4.22.17 K Map: GATE IT 2006 | Question: 35 top



The boolean function for a combinational circuit with four inputs is represented by the following Karnaugh map.

		PQ	00	01	11	10
		RS	00	01	11	10
			1	0	0	1
		00	0	0	1	1
		01	1	1	1	0
		11	1	0	0	1
		10	0	1	0	1

Which of the product terms given below is an essential prime implicant of the function?

- A. QRS      B. PQS      C. PQ'S'      D. Q'S'

gateit-2006 digital-logic k-map normal

Answer key

#### 4.22.18 K Map: GATE IT 2007 | Question: 78 top



Consider the following expression

$$ad\bar{d} + \bar{a}\bar{c} + b\bar{c}d$$

Which of the following Karnaugh Maps correctly represents the expression?

A.

		cd	00	01	11	10
		ab	00	X	X	
		00	X	X		
		01	X			
		11	X	X	X	
		10	X	X		X

B.

		cd	00	01	11	10
		ab	00	X	X	
		00	X	X		
		01	X			
		11	X	X	X	
		10	X			X

C.

		cd	00	01	11	10
		ab	00	X	X	
		00	X	X		
		01	X			
		11	X	X	X	
		10	X			X

D.

		cd	00	01	11	10
		ab	00	X	X	
		00	X	X		
		01	X			
		11	X	X	X	
		10	X			X

gateit-2007 digital-logic k-map normal

Answer key

#### 4.22.19 K Map: GATE IT 2007 | Question: 79 top



Consider the following expression

$$ad\bar{d} + \bar{a}\bar{c} + b\bar{c}d$$

Which of the following expressions does not correspond to the Karnaugh Map obtained for the given expression?

- A.  $\bar{c}\bar{d} + ad\bar{d} + ab\bar{c} + \bar{a}\bar{c}d$   
B.  $\bar{a}\bar{c} + \bar{c}\bar{d} + ad\bar{d} + ab\bar{c}d$   
C.  $\bar{a}\bar{c} + ad\bar{d} + ab\bar{c} + \bar{c}d$   
D.  $\bar{b}\bar{c}\bar{d} + ac\bar{d} + \bar{a}\bar{c} + ab\bar{c}$

gateit-2007 digital-logic k-map normal

Answer key

### 4.23

#### Little Endian Big Endian (1) top

#### 4.23.1 Little Endian Big Endian: GATE CSE 2021 Set 2 | Question: 44 top



If the numerical value of a 2-byte unsigned integer on a little endian computer is 255 more than that on a big endian computer, which of the following choices represent(s) the unsigned integer on a little endian computer?

- A. 0x6665      B. 0x0001      C. 0x4243      D. 0x0100

gatecse-2021-set2 multiple-selects digital-logic number-representation little-endian-big-endian 2-marks

Answer key

**4.24.1 Memory Interfacing: GATE CSE 1995 | Question: 2.2** [top](#) 

The capacity of a memory unit is defined by the number of words multiplied by the number of bits/word. How many separate address and data lines are needed for a memory of  $4K \times 16$ ?

- A. 10 address, 16 data lines
- B. 11 address, 8 data lines
- C. 12 address, 16 data lines
- D. 12 address, 12 data lines

gate1995 digital-logic memory-interfacing normal

[Answer key](#) 

**4.24.2 Memory Interfacing: GATE CSE 2010 | Question: 7** [top](#) 

The main memory unit with a capacity of 4 megabytes is built using  $1M \times 1$ -bit DRAM chips. Each DRAM chip has 1K rows of cells with 1K cells in each row. The time taken for a single refresh operation is 100 nanoseconds. The time required to perform one refresh operation on all the cells in the memory unit is

- A. 100 nanoseconds
- B.  $100 \times 2^{10}$  nanoseconds
- C.  $100 \times 2^{20}$  nanoseconds
- D.  $3200 \times 2^{20}$  nanoseconds

gatecse-2010 digital-logic memory-interfacing normal

[Answer key](#) 

**4.24.3 Memory Interfacing: GATE IT 2005 | Question: 9** [top](#) 

A dynamic RAM has a memory cycle time of 64 nsec. It has to be refreshed 100 times per msec and each refresh takes 100 nsec. What percentage of the memory cycle time is used for refreshing?

- A. 10
- B. 6.4
- C. 1
- D. 0.64

gateit-2005 digital-logic memory-interfacing normal

[Answer key](#) 

**4.25.1 Min No Gates: GATE CSE 2000 | Question: 9** [top](#) 

Design a logic circuit to convert a single digit BCD number to the number modulo six as follows (Do not detect illegal input):

- A. Write the truth table for all bits. Label the input bits  $I_1, I_2, \dots$  with  $I_1$  as the least significant bit. Label the output bits  $R_1, R_2, \dots$  with  $R_1$  as the least significant bit. Use 1 to signify truth.
- B. Draw one circuit for each output bit using, *altogether*, two two-input AND gates, one two-input OR gate and two NOT gates.

gatecse-2000 digital-logic min-no-gates descriptive

[Answer key](#) 

**4.25.2 Min No Gates: GATE CSE 2004 | Question: 58** [top](#) 

A circuit outputs a digit in the form of 4 bits. 0 is represented by 0000, 1 by 0001, ..., 9 by 1001. A combinational circuit is to be designed which takes these 4 bits as input and outputs 1 if the digit  $\geq 5$ , and 0 otherwise. If only AND, OR and NOT gates may be used, what is the minimum number of gates required?

- A. 2
- B. 3
- C. 4
- D. 5

gatecse-2004 digital-logic normal min-no-gates

[Answer key](#) 

**4.25.3 Min No Gates: GATE CSE 2009 | Question: 6** [top](#) 

What is the minimum number of gates required to implement the Boolean function  $(AB+C)$  if we have to use only 2-input NOR gates?

A. 2

B. 3

C. 4

D. 5

gatecse-2009 digital-logic min-no-gates normal

Answer key 

#### 4.25.4 Min No Gates: GATE IT 2004 | Question: 8



What is the minimum number of NAND gates required to implement a 2-input EXCLUSIVE-OR function without using any other logic gate?

A. 2

B. 4

C. 5

D. 6

gateit-2004 digital-logic min-no-gates normal

Answer key 

4.26

#### Min Product Of Sums (2)



##### 4.26.1 Min Product Of Sums: GATE CSE 1990 | Question: 5-a

Find the minimum product of sums of the following expression

$$f = ABC + \bar{A} \bar{B} \bar{C}$$

gate1990 digital-logic boolean-algebra min-product-of-sums canonical-normal-form descriptive

Answer key 

##### 4.26.2 Min Product Of Sums: GATE CSE 2017 Set 2 | Question: 28



Given  $f(w, x, y, z) = \sum_m(0, 1, 2, 3, 7, 8, 10) + \sum_d(5, 6, 11, 15)$ ; where  $d$  represents the 'don't-care' condition in Karnaugh maps. Which of the following is a minimum product-of-sums (POS) form of  $f(w, x, y, z)$ ?

- A.  $f = (\bar{w} + z)(\bar{x} + z)$   
C.  $f = (w + z)(\bar{x} + z)$

- B.  $f = (\bar{w} + z)(x + z)$   
D.  $f = (w + \bar{z})(\bar{x} + z)$

gatecse-2017-set2 digital-logic min-product-of-sums

Answer key 

4.27

#### Min Sum Of Products Form (13)

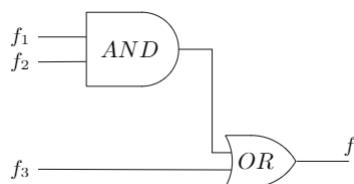


##### 4.27.1 Min Sum Of Products Form: GATE CSE 1988 | Question: 2-v

Three switching functions  $f_1$ ,  $f_2$  and  $f_3$  are expressed below as sum of minterms.

- $f_1(w, x, y, z) = \sum 0, 1, 2, 3, 5, 12$
- $f_2(w, x, y, z) = \sum 0, 1, 2, 10, 13, 14, 15$
- $f_3(w, x, y, z) = \sum 2, 4, 5, 8$

Express the function  $f$  realised by the circuit shown in the below figure as the sum of minterms (in decimal notation).



gate1988 descriptive digital-logic easy circuit-output min-sum-of-products-form

Answer key 

#### 4.27.2 Min Sum Of Products Form: GATE CSE 1991 | Question: 5-b top

Find the minimum sum of products form of the logic function  $f(A, B, C, D) = \sum_m(0, 2, 8, 10, 15) + \sum_d(3, 11, 12, 14)$  where  $m$  and  $d$  represent minterm and don't care term respectively.

gate1991 digital-logic boolean-algebra min-sum-of-products-form descriptive

Answer key 



#### 4.27.3 Min Sum Of Products Form: GATE CSE 1997 | Question: 71 top

$$\text{Let } f = (\bar{w} + y)(\bar{x} + y)(w + \bar{x} + z)(\bar{w} + z)(\bar{x} + z)$$

- A. Express  $f$  as the minimal sum of products. Write only the answer.
- B. If the output line is stuck at 0, for how many input combinations will the value of  $f$  be correct?

gate1997 digital-logic min-sum-of-products-form numerical-answers

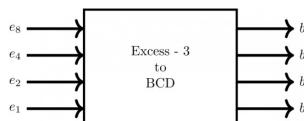
Answer key 



#### 4.27.4 Min Sum Of Products Form: GATE CSE 2001 | Question: 10 top



- a. Is the 3-variable function  $f = \Sigma(0, 1, 2, 4)$  its self-dual? Justify your answer.
- b. Give a minimal product-of-sum form of the  $b$  output of the following excess-3 to BCD converter.



gatecse-2001 digital-logic normal descriptive min-sum-of-products-form

Answer key 



#### 4.27.5 Min Sum Of Products Form: GATE CSE 2005 | Question: 18 top



The switching expression corresponding to  $f(A, B, C, D) = \Sigma(1, 4, 5, 9, 11, 12)$  is:

- A.  $BC'D' + A'C'D + AB'D$
- B.  $ABC' + ACD + B'C'D$
- C.  $ACD' + A'BC' + AC'D'$
- D.  $A'BD + ACD' + BCD'$

gatecse-2005 digital-logic normal min-sum-of-products-form

Answer key 



#### 4.27.6 Min Sum Of Products Form: GATE CSE 2007 | Question: 9 top



Consider the following Boolean function of four variables:

$$f(w, x, y, z) = \Sigma(1, 3, 4, 6, 9, 11, 12, 14)$$

The function is

- A. independent of one variables.
- B. independent of two variables.
- C. independent of three variables.
- D. dependent on all variables

gatecse-2007 digital-logic normal min-sum-of-products-form k-map

Answer key 



#### 4.27.7 Min Sum Of Products Form: GATE CSE 2011 | Question: 14 top



The simplified SOP (Sum of Product) from the Boolean expression

$$(P + \bar{Q} + R) \cdot (P + \bar{Q} + R) \cdot (P + Q + R)$$

is

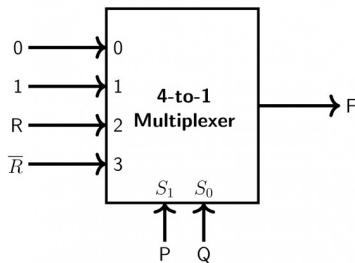
- A.  $(\bar{P} \cdot Q + \bar{R})$       B.  $(P + \bar{Q} \cdot \bar{R})$       C.  $(\bar{P} \cdot Q + R)$       D.  $(P \cdot Q + R)$

gatecse-2011 digital-logic normal min-sum-of-products-form

Answer key 

#### 4.27.8 Min Sum Of Products Form: GATE CSE 2014 Set 1 | Question: 45

Consider the 4-to-1 multiplexer with two select lines  $S_1$  and  $S_0$  given below



The minimal sum-of-products form of the Boolean expression for the output  $F$  of the multiplexer is

- A.  $\bar{P}Q + Q\bar{R} + P\bar{Q}R$   
B.  $\bar{P}Q + \bar{P}Q\bar{R} + PQ\bar{R} + P\bar{Q}R$   
C.  $\bar{P}QR + \bar{P}Q\bar{R} + Q\bar{R} + P\bar{Q}R$   
D.  $P\bar{Q}\bar{R}$

gatecse-2014-set1 digital-logic normal multiplexer min-sum-of-products-form

Answer key 

#### 4.27.9 Min Sum Of Products Form: GATE CSE 2014 Set 1 | Question: 7

Consider the following Boolean expression for  $F$ :

$$F(P, Q, R, S) = PQ + \bar{P}QR + \bar{P}QRS$$

The minimal sum-of-products form of  $F$  is

- A.  $PQ + QR + QS$   
B.  $P + Q + R + S$   
C.  $\bar{P} + \bar{Q} + \bar{R} + \bar{S}$   
D.  $\bar{P}R + \bar{R}\bar{P}S + P$

gatecse-2014-set1 digital-logic normal min-sum-of-products-form

Answer key 



#### 4.27.10 Min Sum Of Products Form: GATE CSE 2014 Set 3 | Question: 7

Consider the following minterm expression for  $F$ :

$$F(P, Q, R, S) = \sum 0, 2, 5, 7, 8, 10, 13, 15$$

The minterms 2, 7, 8 and 13 are 'do not care' terms. The minimal sum-of-products form for  $F$  is

- A.  $Q\bar{S} + \bar{Q}S$   
B.  $\bar{Q}\bar{S} + QS$   
C.  $\bar{Q}\bar{R}\bar{S} + \bar{Q}R\bar{S} + Q\bar{R}S + QRS$   
D.  $\bar{P}\bar{Q}\bar{S} + \bar{P}QS + PQS + P\bar{Q}\bar{S}$

gatecse-2014-set3 digital-logic min-sum-of-products-form normal

Answer key 



#### 4.27.11 Min Sum Of Products Form: GATE CSE 2018 | Question: 49

Consider the minterm list form of a Boolean function  $F$  given below.

$$F(P, Q, R, S) = \Sigma m(0, 2, 5, 7, 9, 11) + d(3, 8, 10, 12, 14)$$



Here,  $m$  denotes a minterm and  $d$  denotes a don't care term. The number of essential prime implicants of the function  $F$  is \_\_\_\_\_

gatecse-2018 digital-logic min-sum-of-products-form numerical-answers 2-marks

Answer key 

#### 4.27.12 Min Sum Of Products Form: GATE CSE 2021 Set 2 | Question: 52



Consider a Boolean function  $f(w, x, y, z)$  such that

$$\begin{aligned}f(w, 0, 0, z) &= 1 \\f(1, x, 1, z) &= x + z \\f(w, 1, y, z) &= wz + y\end{aligned}$$

The number of literals in the minimal sum-of-products expression of  $f$  is \_\_\_\_\_

gatecse-2021-set2 digital-logic boolean-algebra min-sum-of-products-form numerical-answers 2-marks

Answer key 

#### 4.27.13 Min Sum Of Products Form: GATE IT 2008 | Question: 8



Consider the following Boolean function of four variables

$$f(A, B, C, D) = \Sigma(2, 3, 6, 7, 8, 9, 10, 11, 12, 13)$$

The function is

- A. independent of one variable
- B. independent of two variables
- C. independent of three variable
- D. dependent on all the variables

gateit-2008 digital-logic normal min-sum-of-products-form

Answer key 

### 4.28

#### Multiplexer (13)



#### 4.28.1 Multiplexer: GATE CSE 1990 | Question: 5-b

Show with the help of a block diagram how the Boolean function :

$$f = AB + BC + CA$$

can be realised using only a 4 : 1 multiplexer.

gate1990 descriptive digital-logic combinational-circuit multiplexer

Answer key 

#### 4.28.2 Multiplexer: GATE CSE 1998 | Question: 1.14



A multiplexer with a  $4 - bit$  data select input is a

- A. 4 : 1 multiplexer
- B. 2 : 1 multiplexer
- C. 16 : 1 multiplexer
- D. 8 : 1 multiplexer

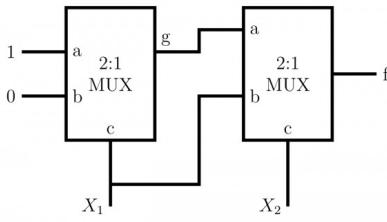
gate1998 digital-logic multiplexer easy

Answer key 

#### 4.28.3 Multiplexer: GATE CSE 2001 | Question: 2.11



Consider the circuit shown below. The output of a 2 : 1 MUX is given by the function  $(ac' + bc)$ .



Which of the following is true?

- A.  $f = X'_1 + X_2$
- C.  $f = X_1 X_2 + X'_1 X'_2$
- B.  $f = X'_1 X_2 + X_1 X'_2$
- D.  $f = X_1 + X'_2$

gatecse-2001 digital-logic normal multiplexer

[Answer key](#)

#### 4.28.4 Multiplexer: GATE CSE 2004 | Question: 60 top ↗

Consider a multiplexer with  $X$  and  $Y$  as data inputs and  $Z$  as the control input.  $Z = 0$  selects input  $X$ , and  $Z = 1$  selects input  $Y$ . What are the connections required to realize the 2-variable Boolean function  $f = T + R$ , without using any additional hardware?

- A.  $R$  to  $X$ ,  $1$  to  $Y$ ,  $T$  to  $Z$
- C.  $T$  to  $X$ ,  $R$  to  $Y$ ,  $0$  to  $Z$
- B.  $T$  to  $X$ ,  $R$  to  $Y$ ,  $T$  to  $Z$
- D.  $R$  to  $X$ ,  $0$  to  $Y$ ,  $T$  to  $Z$

gatecse-2004 digital-logic normal multiplexer

[Answer key](#)

#### 4.28.5 Multiplexer: GATE CSE 2007 | Question: 34 top ↗

Suppose only one multiplexer and one inverter are allowed to be used to implement any Boolean function of  $n$  variables. What is the minimum size of the multiplexer needed?

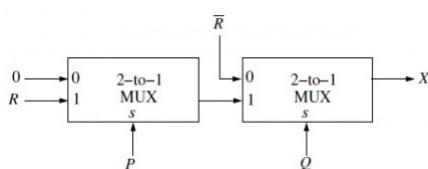
- A.  $2^n$  line to 1 line
- C.  $2^{n-1}$  line to 1 line
- B.  $2^{n+1}$  line to 1 line
- D.  $2^{n-2}$  line to 1 line

gatecse-2007 digital-logic normal multiplexer

[Answer key](#)

#### 4.28.6 Multiplexer: GATE CSE 2016 Set 1 | Question: 30 top ↗

Consider the two cascade 2 to 1 multiplexers as shown in the figure .



The minimal sum of products form of the output  $X$  is

- A.  $\bar{P} \bar{Q} + PQR$
- C.  $PQ + \bar{P} \bar{Q}R$
- B.  $\bar{P} Q + QR$
- D.  $\bar{Q} \bar{R} + PQR$

gatecse-2016-set1 digital-logic multiplexer normal

[Answer key](#)

#### 4.28.7 Multiplexer: GATE CSE 2020 | Question: 19 top ↗

A multiplexer is placed between a group of 32 registers and an accumulator to regulate data movement such that at any given point in time the content of only one register will move to the accumulator. The number of select lines needed for the multiplexer is \_\_\_\_\_.

gatecse-2020 numerical-answers digital-logic multiplexer 1-mark

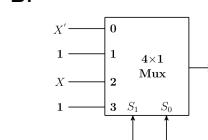
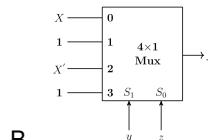
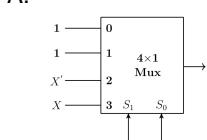
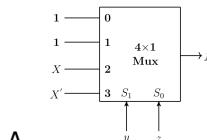
[Answer key](#)

#### 4.28.8 Multiplexer: GATE CSE 2021 Set 2 | Question: 5



Which one of the following circuits implements the Boolean function given below?

$$f(x, y, z) = m_0 + m_1 + m_3 + m_4 + m_5 + m_6, \text{ where } m_i \text{ is the } i^{\text{th}} \text{ minterm.}$$



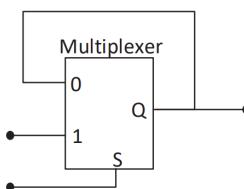
gatecse-2021-set2 digital-logic combinational-circuit multiplexer 1-mark

[Answer key](#)

#### 4.28.9 Multiplexer: GATE CSE 2023 | Question: 11



The output of a 2-input multiplexer is connected back to one of its inputs as shown in the figure.



Match the functional equivalence of this circuit to one of the following options.

- A. D Flip-flop      B. D Latch      C. Half-adder      D. Demultiplexer

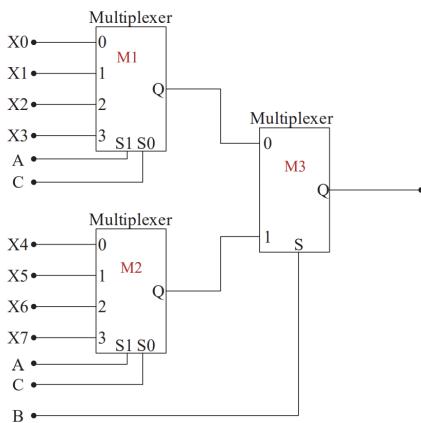
gatecse-2023 digital-logic combinational-circuit multiplexer 1-mark

[Answer key](#)

#### 4.28.10 Multiplexer: GATE CSE 2023 | Question: 34



A Boolean digital circuit is composed using two 4-input multiplexers (M1 and M2) and one 2-input multiplexer (M3) as shown in the figure. X0-X7 are the inputs of the multiplexers M1 and M2 and could be connected to either 0 or 1. The select lines of the multiplexers are connected to Boolean variables A, B and C as shown.

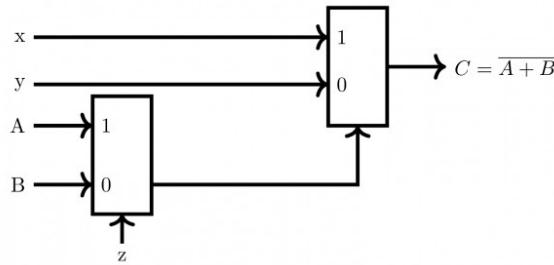


Which one of the following set of values of (X0, X1, X2, X3, X4, X5, X6, X7) will realise the Boolean function  $\overline{A} + \overline{A} \cdot \overline{C} + A \cdot \overline{B} \cdot C$ ?

- A. (1,1,0,0,1,1,1,0)      B. (1,1,0,0,1,1,0,1)  
C. (1,1,0,1,1,1,0,0)      D. (0,0,1,1,0,1,1,1)

**Answer key****4.28.11 Multiplexer: GATE IT 2005 | Question: 48**

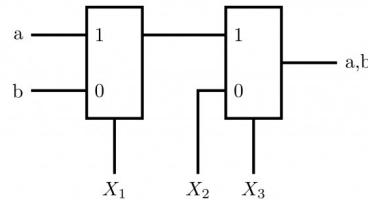
The circuit shown below implements a 2-input NOR gate using two  $2 - 4$  MUX (control signal 1 selects the upper input). What are the values of signals  $x, y$  and  $z$ ?



- A. 1,0,B      B. 1,0,A      C. 0,1,B      D. 0,1,A

**Answer key****4.28.12 Multiplexer: GATE IT 2007 | Question: 8**

The following circuit implements a two-input AND gate using two  $2 - 1$  multiplexers.



What are the values of  $X_1, X_2, X_3$ ?

- A.  $X_1 = b, X_2 = 0, X_3 = a$   
 B.  $X_1 = b, X_2 = 1, X_3 = b$   
 C.  $X_1 = a, X_2 = b, X_3 = 1$   
 D.  $X_1 = a, X_2 = 0, X_3 = b$

**Answer key****4.28.13 Multiplexer: GATE1992-04-b**

A priority encoder accepts three input signals ( $A, B$  and  $C$ ) and produces a two-bit output ( $X_1, X_0$ ) corresponding to the highest priority active input signal. Assume  $A$  has the highest priority followed by  $B$  and  $C$  has the lowest priority. If none of the inputs are active the output should be 00, design the priority encoder using  $4 : 1$  multiplexers as the main components.

**Answer key****4.29****Number Representation (51)****4.29.1 Number Representation: GATE CSE 1988 | Question: 2-vi**

Define the value of  $r$  in the following:  $\sqrt{(41)_r} = (7)_{10}$

**Answer key**

#### 4.29.2 Number Representation: GATE CSE 1990 | Question: 1-viii top<sup>d</sup>



The condition for overflow in the addition of two 2's complement numbers in terms of the carry generated by the two most significant bits is \_\_\_\_\_.

gate1990 digital-logic number-representation fill-in-the-blanks

Answer key

#### 4.29.3 Number Representation: GATE CSE 1991 | Question: 01-iii top<sup>d</sup>



Consider the number given by the decimal expression:

$$16^3 * 9 + 16^2 * 7 + 16 * 5 + 3$$

The number of 1's in the unsigned binary representation of the number is \_\_\_\_\_

gate1991 digital-logic number-representation normal numerical-answers

Answer key

#### 4.29.4 Number Representation: GATE CSE 1991 | Question: 01-v top<sup>d</sup>



When two 4-bit numbers  $A = a_3a_2a_1a_0$  and  $B = b_3b_2b_1b_0$  are multiplied, the bit  $c_1$  of the product  $C$  is given by \_\_\_\_\_

gate1991 digital-logic normal number-representation fill-in-the-blanks

Answer key

#### 4.29.5 Number Representation: GATE CSE 1992 | Question: 4-a top<sup>d</sup>



Consider addition in two's complement arithmetic. A carry from the most significant bit does not always correspond to an overflow. Explain what is the condition for overflow in two's complement arithmetic.

gate1992 digital-logic normal number-representation descriptive

Answer key

#### 4.29.6 Number Representation: GATE CSE 1993 | Question: 6.5 top<sup>d</sup>



Convert the following numbers in the given bases into their equivalents in the desired bases:

- $(110.101)_2 = (x)_{10}$
- $(1118)_{10} = (y)_H$

gate1993 digital-logic number-representation normal descriptive

Answer key

#### 4.29.7 Number Representation: GATE CSE 1994 | Question: 2.7 top<sup>d</sup>



Consider  $n$ -bit (including sign bit) 2's complement representation of integer numbers. The range of integer values,  $N$ , that can be represented is \_\_\_\_\_  $\leq N \leq$  \_\_\_\_\_.

gate1994 digital-logic number-representation easy fill-in-the-blanks

Answer key

#### 4.29.8 Number Representation: GATE CSE 1995 | Question: 18 top<sup>d</sup>



The following is an incomplete Pascal function to convert a given decimal integer (in the range  $-8$  to  $+7$ ) into a binary integer in 2's complement representation. Determine the expressions  $A$ ,  $B$ ,  $C$  that complete program.

```
function TWOSCOMP (N:integer):integer;
var
  REM, EXPONENT:integer;
```

```

BINARY :integer;
begin
  if(N>=-8) and (N<=+7) then
    begin
      if N<0 then
        N:=A;
      BINARY:=0;
      EXPONENT:=1;
      while N<>0 do
        begin
          REM:=N mod 2;
          BINARY:=BINARY + B*EXPONENT;
          EXPONENT:=EXPONENT*10;
          N:=C
        end
      TWOSCOMP:=BINARY
    end
  end;

```

gate1995 digital-logic number-representation normal descriptive

[Answer key](#)

#### 4.29.9 Number Representation: GATE CSE 1995 | Question: 2.12, ISRO2015-9 [top](#)



The number of 1's in the binary representation of  $(3 * 4096 + 15 * 256 + 5 * 16 + 3)$  are:

- A. 8      B. 9      C. 10      D. 12

gate1995 digital-logic number-representation normal isro2015

[Answer key](#)

#### 4.29.10 Number Representation: GATE CSE 1996 | Question: 1.25 [top](#)



Consider the following floating-point number representation.

31	24	23	0
Exponent		Mantissa	

The exponent is in  $2^l$ 's complement representation and the mantissa is in the sign-magnitude representation. The range of the magnitude of the normalized numbers in this representation is

- A. 0 to 1      B. 0.5 to 1      C.  $2^{-23}$  to 0.5      D. 0.5 to  $(1 - 2^{-23})$

gate1996 digital-logic number-representation normal

[Answer key](#)

#### 4.29.11 Number Representation: GATE CSE 1997 | Question: 5.4 [top](#)



Given  $\sqrt{(224)_r} = (13)_r$ .

The value of the radix  $r$  is:

- A. 10      B. 8      C. 5      D. 6

gate1997 digital-logic number-representation normal

[Answer key](#)

#### 4.29.12 Number Representation: GATE CSE 1998 | Question: 2.20 [top](#)



Suppose the domain set of an attribute consists of signed four digit numbers. What is the percentage of reduction in storage space of this attribute if it is stored as an integer rather than in character form?

- A. 80%      B. 20%      C. 60%      D. 40%

gate1998 digital-logic number-representation normal

[Answer key](#)

#### 4.29.13 Number Representation: GATE CSE 1999 | Question: 2.17 top



Zero has two representations in

- A. Sign-magnitude
- B.  $2^l$ s complement
- C.  $1^l$ s complement
- D. None of the above

gate1999 digital-logic number-representation easy multiple-selects

[Answer key](#)



#### 4.29.14 Number Representation: GATE CSE 2000 | Question: 1.6 top



The number 43 in  $2^l$ s complement representation is

- A. 01010101
- B. 11010101
- C. 00101011
- D. 10101011

gatecse-2000 digital-logic number-representation easy

[Answer key](#)



#### 4.29.15 Number Representation: GATE CSE 2000 | Question: 2.14 top



Consider the values of  $A = 2.0 \times 10^{30}$ ,  $B = -2.0 \times 10^{30}$ ,  $C = 1.0$ , and the sequence

X:= A + B	Y:= A + C
X:= X + C	Y:= Y + B

executed on a computer where floating point numbers are represented with 32 bits. The values for  $X$  and  $Y$  will be

- A.  $X = 1.0, Y = 1.0$
- B.  $X = 1.0, Y = 0.0$
- C.  $X = 0.0, Y = 1.0$
- D.  $X = 0.0, Y = 0.0$

gatecse-2000 digital-logic number-representation normal

[Answer key](#)



#### 4.29.16 Number Representation: GATE CSE 2001 | Question: 2.10 top



The  $2^l$ s complement representation of  $(-539)_{10}$  in hexadecimal is

- A. ABE
- B. DBC
- C. DE5
- D. 9E7

gatecse-2001 digital-logic number-representation easy

[Answer key](#)



#### 4.29.17 Number Representation: GATE CSE 2002 | Question: 1.14 top



The decimal value 0.25

- A. is equivalent to the binary value 0.1
- B. is equivalent to the binary value 0.01
- C. is equivalent to the binary value 0.00111
- D. cannot be represented precisely in binary

gatecse-2002 digital-logic number-representation easy

[Answer key](#)



#### 4.29.18 Number Representation: GATE CSE 2002 | Question: 1.15 top



The  $2^l$ s complement representation of the decimal value  $-15$  is

- A. 1111
- B. 11111
- C. 111111
- D. 10001

gatecse-2002 digital-logic number-representation easy

[Answer key](#)

#### 4.29.19 Number Representation: GATE CSE 2002 | Question: 1.16 top



Sign extension is a step in

- A. floating point multiplication
- B. signed 16 bit integer addition
- C. arithmetic left shift
- D. converting a signed integer from one size to another

gatecse-2002 digital-logic easy number-representation

[Answer key](#)

#### 4.29.20 Number Representation: GATE CSE 2002 | Question: 1.21 top



In  $2^l$ s complement addition, overflow

- A. is flagged whenever there is carry from sign bit addition
- B. cannot occur when a positive value is added to a negative value
- C. is flagged when the carries from sign bit and previous bit match
- D. None of the above

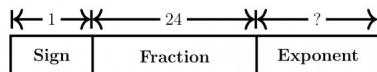
gatecse-2002 digital-logic number-representation normal

[Answer key](#)

#### 4.29.21 Number Representation: GATE CSE 2002 | Question: 9 top



Consider the following 32-bit floating-point representation scheme as shown in the format below. A value is specified by 3 fields, a one bit sign field (with 0 for positive and 1 for negative values), a 24 bit fraction field (with the binary point is at the left end of the fraction bits), and a 7 bit exponent field (in excess-64 signed integer representation, with 16 is the base of exponentiation). The sign bit is the most significant bit.



- A. It is required to represent the decimal value  $-7.5$  as a normalized floating point number in the given format. Derive the values of the various fields. Express your final answer in the hexadecimal.
- B. What is the largest value that can be represented using this format? Express your answer as the nearest power of 10.

gatecse-2002 digital-logic number-representation normal descriptive

[Answer key](#)

#### 4.29.22 Number Representation: GATE CSE 2003 | Question: 9 top



Assuming all numbers are in  $2^l$ s complement representation, which of the following numbers is divisible by 11111011?

- A. 11100111
- B. 11100100
- C. 11010111
- D. 11011011

gatecse-2003 digital-logic number-representation normal

[Answer key](#)

#### 4.29.23 Number Representation: GATE CSE 2004 | Question: 19 top



If  $73_x$  (in base-x number system) is equal to  $54_y$  (in base y-number system), the possible values of  $x$  and  $y$  are

- A. 8,16
- B. 10,12
- C. 9,13
- D. 8,11

gatecse-2004 digital-logic number-representation easy

[Answer key](#)

#### 4.29.24 Number Representation: GATE CSE 2004 | Question: 28 top



What is the result of evaluating the following two expressions using three-digit floating point arithmetic with rounding?

$$(113. + -111.) + 7.51$$

$$113. + (-111. + 7.51)$$

- A. 9.51 and 10.0 respectively
- B. 10.0 and 9.51 respectively
- C. 9.51 and 9.51 respectively
- D. 10.0 and 10.0 respectively

gatecse-2004 digital-logic number-representation normal

[Answer key](#)

#### 4.29.25 Number Representation: GATE CSE 2004 | Question: 66 top



Let  $A = 11111010$  and  $B = 00001010$  be two 8-bit 2's complement numbers. Their product in 2's complement is

- A. 11000100
- B. 10011100
- C. 10100101
- D. 11010101

gatecse-2004 digital-logic number-representation easy

[Answer key](#)

#### 4.29.26 Number Representation: GATE CSE 2005 | Question: 16, ISRO2009-18, ISRO2015-2 top



The range of integers that can be represented by an  $n$  bit 2's complement number system is:

- A.  $-2^{n-1}$  to  $(2^{n-1} - 1)$
- B.  $-(2^{n-1} - 1)$  to  $(2^{n-1} - 1)$
- C.  $-2^{n-1}$  to  $2^{n-1}$
- D.  $-(2^{n-1} + 1)$  to  $(2^{n-1} - 1)$

gatecse-2005 digital-logic number-representation easy isro2009 isro2015

[Answer key](#)

#### 4.29.27 Number Representation: GATE CSE 2005 | Question: 17 top



The hexadecimal representation of  $(657)_8$  is:

- A. 1AF
- B. D78
- C. D71
- D. 32F

gatecse-2005 digital-logic number-representation easy

[Answer key](#)

#### 4.29.28 Number Representation: GATE CSE 2006 | Question: 39 top



We consider the addition of two 2's complement numbers  $b_{n-1}b_{n-2}\dots b_0$  and  $a_{n-1}a_{n-2}\dots a_0$ . A binary adder for adding unsigned binary numbers is used to add the two numbers. The sum is denoted by  $c_{n-1}c_{n-2}\dots c_0$  and the carry-out by  $c_{out}$ . Which one of the following options correctly identifies the overflow condition?

- A.  $c_{out} \left( \overline{a_{n-1}} \oplus \overline{b_{n-1}} \right)$
- B.  $a_{n-1}b_{n-1}\overline{c_{n-1}} + \overline{a_{n-1}}\overline{b_{n-1}}c_{n-1}$
- C.  $c_{out} \oplus c_{n-1}$
- D.  $a_{n-1} \oplus b_{n-1} \oplus c_{n-1}$

gatecse-2006 digital-logic number-representation normal

[Answer key](#)

#### 4.29.29 Number Representation: GATE CSE 2008 | Question: 6 top



Let  $r$  denote number system radix. The only value(s) of  $r$  that satisfy the equation  $\sqrt{121_r} = 11_r$  is/are

- A. decimal 10
- B. decimal 11
- C. decimal 10 and 11
- D. any value  $> 2$

gatecse-2008 digital-logic number-representation normal

[Answer key](#)

#### 4.29.30 Number Representation: GATE CSE 2009 | Question: 5, ISRO2017-57

$(1217)_8$  is equivalent to

- A.  $(1217)_{16}$       B.  $(028F)_{16}$       C.  $(2297)_{10}$       D.  $(0B17)_{16}$

gatecse-2009 digital-logic number-representation isro2017

[Answer key](#) 

#### 4.29.31 Number Representation: GATE CSE 2010 | Question: 8

$P$  is a 16-bit signed integer. The 2's complement representation of  $P$  is  $(F87B)_{16}$ . The 2's complement representation of  $8 \times P$  is

- A.  $(C3D8)_{16}$       B.  $(187B)_{16}$       C.  $(F878)_{16}$       D.  $(987B)_{16}$

gatecse-2010 digital-logic number-representation normal

[Answer key](#) 

#### 4.29.32 Number Representation: GATE CSE 2013 | Question: 4

The smallest integer that can be represented by an 8-bit number in 2's complement form is

- A. -256      B. -128      C. -127      D. 0

gatecse-2013 digital-logic number-representation easy

[Answer key](#) 

#### 4.29.33 Number Representation: GATE CSE 2014 Set 1 | Question: 8

The base (or radix) of the number system such that the following equation holds is \_\_\_\_\_.

$$\frac{312}{20} = 13.1$$

gatecse-2014-set1 digital-logic number-representation numerical-answers normal

[Answer key](#) 

#### 4.29.34 Number Representation: GATE CSE 2014 Set 2 | Question: 8

Consider the equation  $(123)_5 = (x8)_y$  with  $x$  and  $y$  as unknown. The number of possible solutions is \_\_\_\_\_.

gatecse-2014-set2 digital-logic number-representation numerical-answers normal

[Answer key](#) 

#### 4.29.35 Number Representation: GATE CSE 2015 Set 3 | Question: 35

Consider the equation  $(43)_x = (y3)_8$  where  $x$  and  $y$  are unknown. The number of possible solutions is \_\_\_\_\_.

gatecse-2015-set3 digital-logic number-representation normal numerical-answers

[Answer key](#) 

#### 4.29.36 Number Representation: GATE CSE 2016 Set 1 | Question: 07

The 16-bit 2's complement representation of an integer is 1111 1111 1111 0101; its decimal representation is \_\_\_\_\_.

gatecse-2016-set1 digital-logic number-representation normal numerical-answers

[Answer key](#) 

#### 4.29.37 Number Representation: GATE CSE 2016 Set 2 | Question: 09

Let  $X$  be the number of distinct 16-bit integers in 2's complement representation. Let  $Y$  be the number of

distinct 16-bit integers in sign magnitude representation Then  $X - Y$  is\_\_\_\_\_.

gatecse-2016-set2 digital-logic number-representation normal numerical-answers

Answer key 

#### 4.29.38 Number Representation: GATE CSE 2017 Set 1 | Question: 9

When two 8-bit numbers  $A_7 \dots A_0$  and  $B_7 \dots B_0$  in 2's complement representation (with  $A_0$  and  $B_0$  as the least significant bits) are added using a **ripple-carry adder**, the sum bits obtained are  $S_7 \dots S_0$  and the carry bits are  $C_7 \dots C_0$ . An overflow is said to have occurred if

- A. the carry bit  $C_7$  is 1
- B. all the carry bits  $(C_7, \dots, C_0)$  are 1
- C.  $\left( A_7 \cdot B_7 \cdot \overline{S_7} + \overline{A_7} \cdot \overline{B_7} \cdot S_7 \right)$  is 1
- D.  $\left( A_0 \cdot B_0 \cdot \overline{S_0} + \overline{A_0} \cdot \overline{B_0} \cdot S_0 \right)$  is 1

gatecse-2017-set1 digital-logic number-representation

Answer key 

#### 4.29.39 Number Representation: GATE CSE 2017 Set 2 | Question: 1

The representation of the value of a 16-bit unsigned integer  $X$  in hexadecimal number system is BCA9. The representation of the value of  $X$  in octal number system is

- A. 571244
- B. 736251
- C. 571247
- D. 136251

gatecse-2017-set2 digital-logic number-representation

Answer key 

#### 4.29.40 Number Representation: GATE CSE 2019 | Question: 22

Two numbers are chosen independently and uniformly at random from the set  $\{1, 2, \dots, 13\}$ .

The probability (rounded off to 3 decimal places) that their 4-bit (unsigned) binary representations have the same most significant bit is \_\_\_\_\_.

gatecse-2019 numerical-answers digital-logic number-representation probability 1-mark

Answer key 

#### 4.29.41 Number Representation: GATE CSE 2019 | Question: 4

In 16-bit 2's complement representation, the decimal number  $-28$  is:

- A. 1111 1111 0001 1100
- B. 0000 0000 1110 0100
- C. 1111 1111 1110 0100
- D. 1000 0000 1110 0100

gatecse-2019 digital-logic number-representation 1-mark

Answer key 

#### 4.29.42 Number Representation: GATE CSE 2019 | Question: 8

Consider  $Z = X - Y$  where  $X, Y$  and  $Z$  are all in sign-magnitude form.  $X$  and  $Y$  are each represented in  $n$  bits. To avoid overflow, the representation of  $Z$  would require a minimum of:

- A.  $n$  bits
- B.  $n - 1$  bits
- C.  $n + 1$  bits
- D.  $n + 2$  bits

gatecse-2019 digital-logic number-representation 1-mark

Answer key 

#### 4.29.43 Number Representation: GATE CSE 2021 Set 1 | Question: 6

Let the representation of a number in base 3 be 210. What is the hexadecimal representation of the number?

A. 15

B. 21

C. D2

D. 528

gatecse-2021-set1 digital-logic number-representation normal 1-mark

[Answer key](#)

#### 4.29.44 Number Representation: GATE CSE 2021 Set 2 | Question: 18 top

If  $x$  and  $y$  are two decimal digits and  $(0.1101)_2 = (0.8xy5)_{10}$ , the decimal value of  $x + y$  is \_\_\_\_\_.

gatecse-2021-set2 numerical-answers digital-logic number-representation 1-mark

[Answer key](#)

#### 4.29.45 Number Representation: GATE CSE 2023 | Question: 22 top

A particular number is written as 132 in radix-4 representation. The same number in radix-5 representation is \_\_\_\_\_.

gatecse-2023 digital-logic number-representation numerical-answers 1-mark

[Answer key](#)

#### 4.29.46 Number Representation: GATE IT 2004 | Question: 42 top

Using a 4 – bit 2's complement arithmetic, which of the following additions will result in an overflow?

- i.  $1100 + 1100$
- ii.  $0011 + 0111$
- iii.  $1111 + 0111$

- A. i only      B. ii only      C. iii only      D. i and iii only

gateit-2004 digital-logic number-representation normal

[Answer key](#)

#### 4.29.47 Number Representation: GATE IT 2004 | Question: 43 top

The number  $(123456)_8$  is equivalent to

- A.  $(A72E)_{16}$  and  $(22130232)_4$
- C.  $(A73E)_{16}$  and  $(22130232)_4$
- B.  $(A72E)_{16}$  and  $(22131122)_4$
- D.  $(A62E)_{16}$  and  $(22120232)_4$

gateit-2004 digital-logic number-representation normal

[Answer key](#)

#### 4.29.48 Number Representation: GATE IT 2005 | Question: 47 top

$(34.4)_8 \times (23.4)_8$  evaluates to

- A.  $(1053.6)_8$       B.  $(1053.2)_8$       C.  $(1024.2)_8$       D. None of these

gateit-2005 digital-logic number-representation normal

[Answer key](#)

#### 4.29.49 Number Representation: GATE IT 2006 | Question: 7, ISRO2009-41 top

The addition of 4 – bit, two's complement, binary numbers 1101 and 0100 results in

- A. 0001 and an overflow
- C. 0001 and no overflow
- B. 1001 and no overflow
- D. 1001 and an overflow

gateit-2006 digital-logic number-representation normal isro2009

[Answer key](#)

#### 4.29.50 Number Representation: GATE IT 2007 | Question: 42 top

$(C012.25)_H - (10111001110.101)_B =$

- A.  $(135103.412)_o$       B.  $(564411.412)_o$

C.  $(564411.205)_o$

gateit-2007 digital-logic number-representation normal

Answer key 

D.  $(135103.205)_o$



#### 4.29.51 Number Representation: GATE IT 2008 | Question: 15

A processor that has the carry, overflow and sign flag bits as part of its program status word (PSW) performs addition of the following two 2's complement numbers 01001101 and 11101001. After the execution of this addition operation, the status of the carry, overflow and sign flags, respectively will be:

- A. 1,1,0      B. 1,0,0      C. 0,1,0      D. 1,0,1

gateit-2008 digital-logic number-representation normal

Answer key 

4.30

Number System (2) 



#### 4.30.1 Number System: GATE CSE 2022 | Question: 31

Consider three floating point numbers  $A$ ,  $B$  and  $C$  stored in registers  $R_A$ ,  $R_B$  and  $R_C$ , respectively as per IEEE-754 single precision floating point format. The 32-bit content stored in these registers (in hexadecimal form) are as follows.

$$R_A = 0xC1400000 \quad R_B = 0x42100000 \quad R_C = 0x41400000$$

Which one of the following is FALSE?

- A.  $A + C = 0$       B.  $C = A + B$       C.  $B = 3C$       D.  $(B - C) > 0$

gatecse-2022 digital-logic number-system number-representation 2-marks

Answer key 

#### 4.30.2 Number System: GATE CSE 2022 | Question: 8



Let  $R_1$  and  $R_2$  be two 4-bit registers that store numbers in 2's complement form. For the operation  $R_1 + R_2$ , which one of the following values of  $R_1$  and  $R_2$  gives an arithmetic overflow?

- A.  $R_1 = 1011$  and  $R_2 = 1110$   
B.  $R_1 = 1100$  and  $R_2 = 1010$   
C.  $R_1 = 0011$  and  $R_2 = 0100$   
D.  $R_1 = 1001$  and  $R_2 = 1111$

gatecse-2022 digital-logic number-system number-representation 1-mark

Answer key 

4.31

Pla (1) 



#### 4.31.1 Pla: GATE CSE 1990 | Question: 4-i

State whether the following statements are TRUE or FALSE with reason:

RAM is a combinational circuit and PLA is a sequential circuit.

gate1990 true-false digital-logic ram pla

Answer key 

4.32

Prime Implicants (2) 



#### 4.32.1 Prime Implicants: GATE CSE 1997 | Question: 5.1

Let  $f(x, y, z) = \bar{x} + \bar{y}x + xz$  be a switching function. Which one of the following is valid?

- A.  $\bar{y}x$  is a prime implicant of  $f$   
B.  $xz$  is a minterm of  $f$   
C.  $xz$  is an implicant of  $f$   
D.  $y$  is a prime implicant of  $f$

gate1997 digital-logic normal prime-implicants

Answer key 

#### 4.32.2 Prime Implicants: GATE CSE 2004 | Question: 59 top



Which are the essential prime implicants of the following Boolean function?

$$f(a, b, c) = a'c + ac' + b'c$$

- A.  $a'c$  and  $ac'$       B.  $a'c$  and  $b'c$       C.  $a'c$  only.      D.  $ac'$  and  $bc'$

gatecse-2004 digital-logic normal prime-implicants

[Answer key](#)

4.33

Rom (4) top

#### 4.33.1 Rom: GATE CSE 1993 | Question: 6.6 top



A ROM is used to store the Truth table for binary multiple units that will multiply two 4-bit numbers. The size of the ROM (number of words  $\times$  number of bits) that is required to accommodate the Truth table is M words  $\times$  N bits. Write the values of M and N.

gate1993 digital-logic normal rom descriptive

[Answer key](#)

#### 4.33.2 Rom: GATE CSE 1996 | Question: 1.21 top



A ROM is used to store the table for multiplication of two 8-bit unsigned integers. The size of ROM required is

- A.  $256 \times 16$       B.  $64K \times 8$   
C.  $4K \times 16$       D.  $64K \times 16$

gate1996 digital-logic normal rom

[Answer key](#)

#### 4.33.3 Rom: GATE CSE 2012 | Question: 19 top



The amount of ROM needed to implement a 4-bit multiplier is

- A. 64 bits      B. 128 bits      C. 1 Kbits      D. 2 Kbits

gatecse-2012 digital-logic normal rom

[Answer key](#)

#### 4.33.4 Rom: GATE IT 2004 | Question: 10 top



What is the minimum size of ROM required to store the complete truth table of an 8-bit  $\times$  8-bit multiplier?

- A.  $32K \times 16$  bits      B.  $64K \times 16$  bits  
C.  $16K \times 32$  bits      D.  $64K \times 32$  bits

gateit-2004 digital-logic normal rom

[Answer key](#)

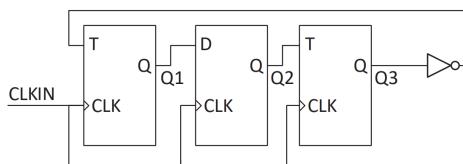
4.34

Sequential Circuit (1) top

#### 4.34.1 Sequential Circuit: GATE CSE 2023 | Question: 33 top



Consider a sequential digital circuit consisting of T flip-flops and D flip-flops as shown in the figure. CLKIN is the clock input to the circuit. At the beginning, Q1, Q2 and Q3 have values 0, 1 and 1, respectively.



Which one of the given values of (Q1, Q2, Q3) can NEVER be obtained with this digital circuit?

- A. (0,0,1)      B. (1,0,0)      C. (1,0,1)      D. (1,1,1)

gatecse-2023 digital-logic sequential-circuit flip-flop 2-marks

[Answer key](#)

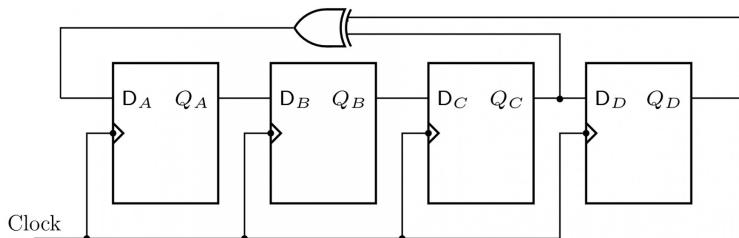
4.35

### Shift Registers (2) [top](#)

#### 4.35.1 Shift Registers: GATE CSE 1987 | Question: 13-a [top](#)



The below figure shows four D-type flip-flops connected as a shift register using a XOR gate. The initial state and three subsequent states for three clock pulses are also given.



State	$Q_A$	$Q_B$	$Q_C$	$Q_D$
Initial	1	1	1	1
After the first clock	0	1	1	1
After the second clock	0	0	1	1
After the third clock	0	0	0	1

The state  $Q_AQ_BQ_CQ_D$  after the fourth clock pulse is

- A. 0000      B. 1111      C. 1001      D. 1000

gate1987 digital-logic circuit-output sequential-circuit digital-counter shift-registers

[Answer key](#)

#### 4.35.2 Shift Registers: GATE CSE 1991 | Question: 06,a [top](#)



Using D flip-flop gates, design a parallel-in/serial-out shift register that shifts data from left to right with the following input lines:

- Clock CLK
- Three parallel data inputs  $A, B, C$
- Serial input  $S$
- Control input LOAD/SHIFT.

gate1991 digital-logic difficult sequential-circuit flip-flop shift-registers descriptive

[Answer key](#)

4.36

### Static Hazard (1) [top](#)

#### 4.36.1 Static Hazard: GATE CSE 2006 | Question: 38 [top](#)



Consider a Boolean function  $f(w, x, y, z)$ . Suppose that exactly one of its inputs is allowed to change at a time. If the function happens to be true for two input vectors  $i_1 = \langle w_1, x_1, y_1, z_1 \rangle$  and  $i_2 = \langle w_2, x_2, y_2, z_2 \rangle$ , we would like the function to remain true as the input changes from  $i_1$  to  $i_2$  ( $i_1$  and  $i_2$  differ in exactly one bit position) without becoming false momentarily. Let  $f(w, x, y, z) = \sum(5, 7, 11, 12, 13, 15)$ . Which of the following cube covers of  $f$  will ensure that the required property is satisfied?

- A.  $\bar{w}xz, w\bar{x}\bar{y}, x\bar{y}z, xyz, wyz$

- B.  $wxy, \bar{w}xz, wyz$   
 C.  $wx\bar{y}z, xz, \bar{w}xyz$   
 D.  $wx\bar{y}, wyz, wxz, \bar{w}xz, x\bar{y}z, xyz$

gatecse-2006 digital-logic min-sum-of-products-form difficult static-hazard

[Answer key](#)

4.37

### Synchronous Asynchronous Circuits (4) [top](#)

#### 4.37.1 Synchronous Asynchronous Circuits: GATE CSE 1991 | Question: 03-ii [top](#)

Advantage of synchronous sequential circuits over asynchronous ones is:

- A. faster operation  
 B. ease of avoiding problems due to hazards  
 C. lower hardware requirement  
 D. better noise immunity  
 E. none of the above

gate1991 digital-logic normal sequential-circuit synchronous-asynchronous-circuits multiple-selects

[Answer key](#)



#### 4.37.2 Synchronous Asynchronous Circuits: GATE CSE 1998 | Question: 16 [top](#)

Design a synchronous counter to go through the following states:

1, 4, 2, 3, 1, 4, 2, 3, 1, 4...

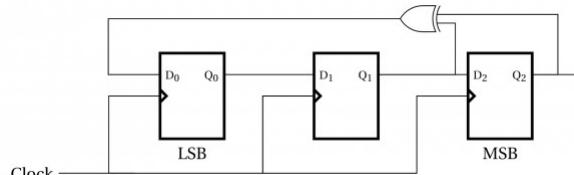
gate1998 digital-logic normal descriptive synchronous-asynchronous-circuits

[Answer key](#)



#### 4.37.3 Synchronous Asynchronous Circuits: GATE CSE 2001 | Question: 2.12 [top](#)

Consider the circuit given below with initial state  $Q_0 = 1, Q_1 = Q_2 = 0$ . The state of the circuit is given by the value  $4Q_2 + 2Q_1 + Q_0$



Which one of the following is correct state sequence of the circuit?

- A. 1, 3, 4, 6, 7, 5, 2  
 B. 1, 2, 5, 3, 7, 6, 4  
 C. 1, 2, 7, 3, 5, 6, 4  
 D. 1, 6, 5, 7, 2, 3, 4

gatecse-2001 digital-logic normal synchronous-asynchronous-circuits

[Answer key](#)



#### 4.37.4 Synchronous Asynchronous Circuits: GATE CSE 2003 | Question: 44 [top](#)

A 1-input, 2-output synchronous sequential circuit behaves as follows:

Let  $z_k, n_k$  denote the number of 0's and 1's respectively in initial  $k$  bits of the input ( $z_k + n_k = k$ ). The circuit outputs 00 until one of the following conditions holds.

- $z_k - n_k = 2$ . In this case, the output at the  $k$ -th and all subsequent clock ticks is 10.
- $n_k - z_k = 2$ . In this case, the output at the  $k$ -th and all subsequent clock ticks is 01.

What is the minimum number of states required in the state transition graph of the above circuit?

- A. 5      B. 6      C. 7      D. 8

gatecse-2003 digital-logic synchronous-asynchronous-circuits normal



## Answer Keys

4.1.1	D	4.2.1	N/A	4.2.2	N/A	4.2.3	N/A	4.2.4	B
4.2.5	B	4.2.6	A	4.2.7	B	4.2.8	19.2	4.2.9	B
4.2.10	-1	4.3.1	B	4.3.2	C	4.4.1	C	4.4.2	A
4.5.1	D	4.5.2	C	4.5.3	N/A	4.5.4	N/A	4.5.5	N/A
4.5.6	D	4.5.7	N/A	4.5.8	A	4.5.9	B	4.5.10	D
4.5.11	C	4.5.12	D	4.5.13	C	4.5.14	C	4.5.15	D
4.5.16	D	4.5.17	D	4.5.18	A	4.5.19	A	4.5.20	D
4.5.21	D	4.5.22	B	4.5.23	1	4.5.24	A	4.5.25	C
4.5.26	C	4.5.27	D	4.5.28	B	4.5.29	B;C;D	4.5.30	B
4.5.31	C	4.6.1	N/A	4.6.2	A	4.6.3	B	4.6.4	A
4.6.5	C	4.6.6	B	4.7.1	A	4.7.3	A	4.7.4	3
4.7.6	3	4.7.7	B	4.8.1	A	4.8.2	B	4.9.1	B
4.9.2	N/A	4.9.3	C	4.9.4	N/A	4.9.5	N/A	4.9.6	A;C
4.9.7	B	4.9.8	B	4.9.9	B	4.9.10	011	4.9.11	D
4.9.12	C	4.9.13	N/A	4.9.14	N/A	4.9.15	B	4.9.16	B
4.9.17	A	4.9.18	A	4.9.19	A	4.9.20	D	4.9.21	A
4.9.22	A	4.9.23	D	4.9.24	A	4.9.25	C	4.9.28	A
4.9.29	A	4.9.30	B	4.9.31	D	4.9.32	B	4.9.33	C
4.9.34	C	4.9.35	X	4.9.36	D	4.9.37	C	4.9.38	A
4.9.39	D	4.9.40	B	4.10.1	C	4.11.1	A	4.12.1	C
4.12.2	1034	4.13.1	B;C	4.13.2	N/A	4.13.3	N/A	4.13.4	D
4.13.5	D	4.13.6	A	4.13.7	C	4.14.1	C	4.14.2	N/A
4.14.3	N/A	4.14.4	33.33	4.14.5	N/A	4.14.6	N/A	4.14.7	A
4.14.8	C	4.14.9	D	4.14.10	3	4.14.11	4	4.14.12	B
4.14.13	A	4.14.14	D	4.14.15	D	4.14.16	N/A	4.15.1	D
4.16.1	B	4.17.1	D	4.18.1	N/A	4.18.2	C	4.18.3	A
4.18.4	B	4.18.5	2	4.18.6	D	4.19.1	C	4.19.2	N/A
4.19.3	N/A	4.19.4	N/A	4.19.5	N/A	4.19.6	C	4.19.7	D
4.19.8	D	4.20.1	N/A	4.20.2	N/A	4.20.3	B;C	4.20.4	A
4.21.1	D	4.21.2	B	4.21.3	A	4.21.4	C	4.21.5	-7.75 : -7.75
4.21.6	C	4.21.7	C	4.22.1	D	4.22.2	N/A	4.22.3	N/A
4.22.4	N/A	4.22.5	N/A	4.22.6	C	4.22.7	C	4.22.8	B
4.22.9	D	4.22.10	A	4.22.11	B	4.22.12	C	4.22.13	A
4.22.14	B	4.22.15	1	4.22.16	A	4.22.17	D	4.22.18	A
4.22.19	C	4.23.1	A;D	4.24.1	C	4.24.2	B	4.24.3	C
4.25.2	B	4.25.4	B	4.26.1	N/A	4.26.2	A	4.27.1	N/A
4.27.2	N/A	4.27.3	9	4.27.4	N/A	4.27.5	A	4.27.6	B

4.27.7	B	4.27.8	A	4.27.9	A	4.27.10	B	4.27.11	3
4.27.13	A	4.28.1	N/A	4.28.2	C	4.28.3	C	4.28.4	A
4.28.5	C	4.28.6	D	4.28.7	5	4.28.9	B	4.28.10	C
4.28.11	D	4.28.12	A	4.28.13	N/A	4.29.1	12	4.29.2	N/A
4.29.3	9	4.29.4	N/A	4.29.5	N/A	4.29.6	N/A	4.29.7	N/A
4.29.8	N/A	4.29.9	C	4.29.10	D	4.29.11	C	4.29.12	C
4.29.13	A;C	4.29.14	C	4.29.15	B	4.29.16	C	4.29.17	B
4.29.18	D	4.29.19	D	4.29.20	B	4.29.21	N/A	4.29.22	A
4.29.23	D	4.29.24	A	4.29.25	A	4.29.26	A	4.29.27	A
4.29.28	B	4.29.29	D	4.29.30	B	4.29.31	A	4.29.32	B
4.29.33	5	4.29.34	3	4.29.35	5	4.29.36	-11	4.29.37	1
4.29.38	C	4.29.39	D	4.29.40	0.502 : 0.504	4.29.41	C	4.29.42	C
4.29.43	A	4.29.45	110	4.29.46	B	4.29.47	A	4.29.49	C
4.29.50	A	4.29.51	B	4.30.1	B	4.30.2	B	4.31.1	False
4.32.1	C	4.32.2	A	4.33.1	N/A	4.33.2	D	4.33.3	D
4.33.4	B	4.34.1	A	4.35.1	D	4.35.2	N/A	4.36.1	D
4.37.1	B	4.37.2	N/A	4.37.3	B				



## 5.1

Context Switch (3) [top](#)5.1.1 Context Switch: GATE CSE 1999 | Question: 2.12 [top](#)

Which of the following actions is/are typically not performed by the operating system when switching context from process *A* to process *B*?

- A. Saving current register values and restoring saved register values for process *B*.
- B. Changing address translation tables.
- C. Swapping out the memory image of process *A* to the disk.
- D. Invalidating the translation look-aside buffer.

gate1999 operating-system context-switch normal

[Answer key](#)

5.1.2 Context Switch: GATE CSE 2000 | Question: 1.20, ISRO2008-47 [top](#)

Which of the following need not necessarily be saved on a context switch between processes?

- |                              |                                  |
|------------------------------|----------------------------------|
| A. General purpose registers | B. Translation look-aside buffer |
| C. Program counter           | D. All of the above              |

gatecse-2000 operating-system easy isro2008 context-switch

[Answer key](#)

5.1.3 Context Switch: GATE CSE 2011 | Question: 6, UGCNET-June2013-III: 62 [top](#)

Let the time taken to switch from user mode to kernel mode of execution be  $T_1$  while time taken to switch between two user processes be  $T_2$ . Which of the following is correct?

- |                |   |
|----------------|---|
| A. $T_1 > T_2$ | B. $T_1 = T_2$  |
| C. $T_1 < T_2$ | D. Nothing can be said about the relation between $T_1$ and $T_2$ |

gatecse-2011 operating-system context-switch easy ugcnetcse-june2013-paper3

[Answer key](#)

5.2 Deadlock Prevention Avoidance Detection (4) [top](#)5.2.1 Deadlock Prevention Avoidance Detection: GATE CSE 2018 | Question: 24 [top](#)

Consider a system with 3 processes that share 4 instances of the same resource type. Each process can request a maximum of  $K$  instances. Resources can be requested and released only one at a time. The largest value of  $K$  that will always avoid deadlock is \_\_\_\_\_

gatecse-2018 operating-system deadlock-prevention-avoidance-detection easy numerical-answers 1-mark

[Answer key](#)

5.2.2 Deadlock Prevention Avoidance Detection: GATE CSE 2018 | Question: 39 [top](#)

In a system, there are three types of resources: *E*, *F* and *G*. Four processes  $P_0$ ,  $P_1$ ,  $P_2$  and  $P_3$  execute concurrently. At the outset, the processes have declared their maximum resource requirements using a matrix named Max as given below. For example,  $\text{Max}[P_2, F]$  is the maximum number of instances of *F* that  $P_2$  would require. The number of instances of the resources allocated to the various processes at any given state is given by a matrix named Allocation.

Consider a state of the system with the Allocation matrix as shown below, and in which 3 instances of *E* and 3 instances of *F* are only resources available.

Allocation			Max				
	E	F	G	E	F		
$P_0$	1	0	1	$P_0$	4	3	1
$P_1$	1	1	2	$P_1$	2	1	4
$P_2$	1	0	3	$P_2$	1	3	3
$P_3$	2	0	0	$P_3$	5	4	1

From the perspective of deadlock avoidance, which one of the following is true?

- A. The system is in *safe* state
- B. The system is not in *safe* state, but would be *safe* if one more instance of  $E$  were available
- C. The system is not in *safe* state, but would be *safe* if one more instance of  $F$  were available
- D. The system is not in *safe* state, but would be *safe* if one more instance of  $G$  were available

gatecse-2018 operating-system deadlock-prevention-avoidance-detection normal 2-marks

[Answer key](#)

### 5.2.3 Deadlock Prevention Avoidance Detection: GATE CSE 2021 Set 2 | Question: 43 top

Consider a computer system with multiple shared resource types, with one instance per resource type. Each instance can be owned by only one process at a time. Owning and freeing of resources are done by holding a global lock ( $L$ ). The following scheme is used to own a resource instance:

```
function OWNRESOURCE(Resource R)
    Acquire lock L // a global lock
    if R is available then
        Acquire R
        Release lock L
    else
        if R is owned by another process P then
            Terminate P, after releasing all resources owned by P
            Acquire R
            Restart P
            Release lock L
        end if
    end if
end function
```



Which of the following choice(s) about the above scheme is/are correct?

- A. The scheme ensures that deadlocks will not occur
- B. The scheme may lead to live-lock
- C. The scheme may lead to starvation
- D. The scheme violates the mutual exclusion property

gatecse-2021-set2 multiple-selects operating-system deadlock-prevention-avoidance-detection 2-marks

[Answer key](#)

### 5.2.4 Deadlock Prevention Avoidance Detection: GATE IT 2004 | Question: 63 top



In a certain operating system, deadlock prevention is attempted using the following scheme. Each process is assigned a unique timestamp, and is restarted with the same timestamp if killed. Let  $P_h$  be the process holding a resource  $R$ ,  $P_r$  be a process requesting for the same resource  $R$ , and  $T(P_h)$  and  $T(P_r)$  be their timestamps respectively. The decision to wait or preempt one of the processes is based on the following algorithm.

```
if T(Pr) < T(Ph) then
    kill Pr
else wait
```

Which one of the following is TRUE?

- A. The scheme is deadlock-free, but not starvation-free
- B. The scheme is not deadlock-free, but starvation-free

- C. The scheme is neither deadlock-free nor starvation-free  
D. The scheme is both deadlock-free and starvation-free

gateit-2004 operating-system normal deadlock-prevention-avoidance-detection

[Answer key](#)

5.3

Demand Paging (1) [top](#)

#### 5.3.1 Demand Paging: GATE CSE 2022 | Question: 54 [top](#)



Consider a demand paging system with four page frames (initially empty) and LRU page replacement policy. For the following page reference string

7, 2, 7, 3, 2, 5, 3, 4, 6, 7, 7, 1, 5, 6, 1

the page fault rate, defined as the ratio of number of page faults to the number of memory accesses (*rounded off to one decimal place*) is \_\_\_\_\_.

gatecse-2022 numerical-answers operating-system page-replacement demand-paging 2-marks

[Answer key](#)

5.4

Disk (29) [top](#)

#### 5.4.1 Disk: GATE CSE 1990 | Question: 7-c [top](#)



A certain moving arm disk-storage device has the following specifications:

- Number of tracks per surface = 404
- Track storage capacity = 130030 bytes.
- Disk speed = 3600 rpm
- Average seek time = 30 m secs.

Estimate the average latency, the disk storage capacity, and the data transfer rate.

gate1990 operating-system disk descriptive

[Answer key](#)

#### 5.4.2 Disk: GATE CSE 1993 | Question: 6.7 [top](#)



A certain moving arm disk storage, with one head, has the following specifications:

- Number of tracks/recording surface = 200
- Disk rotation speed = 2400 rpm
- Track storage capacity = 62,500 bits

The average latency of this device is P ms and the data transfer rate is Q bits/sec. Write the values of P and Q.

gate1993 operating-system disk normal descriptive

[Answer key](#)

#### 5.4.3 Disk: GATE CSE 1993 | Question: 7.8 [top](#)



The root directory of a disk should be placed

- A. at a fixed address in main memory
- C. anywhere on the disk
- E. anywhere on the system disk
- B. at a fixed location on the disk
- D. at a fixed location on the system disk

gate1993 operating-system disk normal

[Answer key](#)

#### 5.4.4 Disk: GATE CSE 1995 | Question: 14 top



If the overhead for formatting a disk is 96 bytes for a 4000 byte sector,

- Compute the unformatted capacity of the disk for the following parameters:
  - Number of surfaces: 8
  - Outer diameter of the disk: 12 cm
  - Inner diameter of the disk: 4 cm
  - Inner track space: 0.1 mm
  - Number of sectors per track: 20
- If the disk in (A) is rotating at 360 rpm, determine the effective data transfer rate which is defined as the number of bytes transferred per second between disk and memory.

gate1995 operating-system disk normal descriptive

[Answer key](#)

#### 5.4.5 Disk: GATE CSE 1997 | Question: 74 top



A program  $P$  reads and processes 1000 consecutive records from a sequential file  $F$  stored on device  $D$  without using any file system facilities. Given the following

- Size of each record = 3200 bytes
- Access time of  $D$  = 10 msec
- Data transfer rate of  $D$  =  $800 \times 10^3$  bytes/second
- CPU time to process each record = 3 msec

What is the elapsed time of  $P$  if

- $F$  contains unblocked records and  $P$  does not use buffering?
- $F$  contains unblocked records and  $P$  uses one buffer (i.e., it always reads ahead into the buffer)?
- records of  $F$  are organized using a blocking factor of 2 (i.e., each block on  $D$  contains two records of  $F$ ) and  $P$  uses one buffer?

gate1997 operating-system disk

[Answer key](#)

#### 5.4.6 Disk: GATE CSE 1998 | Question: 2-9 top



Formatting for a floppy disk refers to

- arranging the data on the disk in contiguous fashion
- writing the directory
- erasing the system data
- writing identification information on all tracks and sectors

gate1998 operating-system disk normal

[Answer key](#)

#### 5.4.7 Disk: GATE CSE 1998 | Question: 25-a top



Free disk space can be used to keep track of using a free list or a bit map. Disk addresses require  $d$  bits. For a disk with  $B$  blocks,  $F$  of which are free, state the condition under which the free list uses less space than the bit map.

gate1998 operating-system disk descriptive

[Answer key](#)

#### 5.4.8 Disk: GATE CSE 1998 | Question: 25b [top](#)



Consider a disk with  $c$  cylinders,  $t$  tracks per cylinder,  $s$  sectors per track and a sector length  $s_l$ . A logical file  $d_l$  with fixed record length  $r_l$  is stored continuously on this disk starting at location  $(c_L, t_L, s_L)$ , where  $c_L, t_L$  and  $s_L$  are the cylinder, track and sector numbers, respectively. Derive the formula to calculate the disk address (i.e. cylinder, track and sector) of a logical record  $n$  assuming that  $r_l = s_l$ .

gate1998 operating-system disk descriptive

[Answer key](#)



#### 5.4.9 Disk: GATE CSE 1999 | Question: 2-18, ISRO2008-46 [top](#)



Raid configurations of the disks are used to provide

- A. Fault-tolerance
- B. High speed
- C. High data density
- D. (A) & (B)

gate1999 operating-system disk easy isro2008

[Answer key](#)



#### 5.4.10 Disk: GATE CSE 2001 | Question: 1.22 [top](#)



Which of the following requires a device driver?

- A. Register
- B. Cache
- C. Main memory
- D. Disk

gatecse-2001 operating-system disk easy

[Answer key](#)



#### 5.4.11 Disk: GATE CSE 2001 | Question: 20 [top](#)



Consider a disk with the 100 tracks numbered from 0 to 99 rotating at 3000 rpm. The number of sectors per track is 100 and the time to move the head between two successive tracks is 0.2 millisecond.

- A. Consider a set of disk requests to read data from tracks 32, 7, 45, 5 and 10. Assuming that the elevator algorithm is used to schedule disk requests, and the head is initially at track 25 moving up (towards larger track numbers), what is the total seek time for servicing the requests?
- B. Consider an initial set of 100 arbitrary disk requests and assume that no new disk requests arrive while servicing these requests. If the head is initially at track 0 and the elevator algorithm is used to schedule disk requests, what is the worse case time to complete all the requests?

gatecse-2001 operating-system disk normal descriptive

[Answer key](#)



#### 5.4.12 Disk: GATE CSE 2001 | Question: 8 [top](#)



Consider a disk with the following specifications: 20 surfaces, 1000 tracks/surface, 16 sectors/track, data density 1 KB/sector, rotation speed 3000 rpm. The operating system initiates the transfer between the disk and the memory sector-wise. Once the head has been placed on the right track, the disk reads a sector in a single scan. It reads bits from the sector while the head is passing over the sector. The read bits are formed into bytes in a serial-in-parallel-out buffer and each byte is then transferred to memory. The disk writing is exactly a complementary process.

For parts (C) and (D) below, assume memory read-write time = 0.1 microseconds/byte, interrupt driven transfer has an interrupt overhead = 0.4 microseconds, the DMA initialization, and termination overhead is negligible compared to the total sector transfer time. DMA requests are always granted.

- A. What is the total capacity of the desk?
- B. What is the data transfer rate?
- C. What is the percentage of time the CPU is required for this disk I/O for byte-wise interrupts driven transfer?
- D. What is the maximum percentage of time the CPU is held up for this disk I/O for cycle-stealing DMA transfer?

gatecse-2001 operating-system disk normal descriptive

[Answer key](#)

#### 5.4.13 Disk: GATE CSE 2003 | Question: 25, ISRO2009-12 [top](#)



Using a larger block size in a fixed block size file system leads to

- A. better disk throughput but poorer disk space utilization
- B. better disk throughput and better disk space utilization
- C. poorer disk throughput but better disk space utilization
- D. poorer disk throughput and poorer disk space utilization

gatecse-2003 operating-system disk normal isro2009

[Answer key](#)

#### 5.4.14 Disk: GATE CSE 2004 | Question: 49 [top](#)



A unix-style I-nodes has 10 direct pointers and one single, one double and one triple indirect pointers. Disk block size is 1 Kbyte, disk block address is 32 bits, and 48-bit integers are used. What is the maximum possible file size?

- A.  $2^{24}$  bytes
- B.  $2^{32}$  bytes
- C.  $2^{34}$  bytes
- D.  $2^{48}$  bytes

gatecse-2004 operating-system disk normal

[Answer key](#)

#### 5.4.15 Disk: GATE CSE 2005 | Question: 21 [top](#)



What is the swap space in the disk used for?

- A. Saving temporary html pages
- B. Saving process data
- C. Storing the super-block
- D. Storing device drivers

gatecse-2005 operating-system disk easy

[Answer key](#)

#### 5.4.16 Disk: GATE CSE 2007 | Question: 11, ISRO2009-36, ISRO2016-21 [top](#)



Consider a disk pack with 16 surfaces, 128 tracks per surface and 256 sectors per track. 512 bytes of data are stored in a bit serial manner in a sector. The capacity of the disk pack and the number of bits required to specify a particular sector in the disk are respectively:

- A. 256 Mbyte, 19 bits
- B. 256 Mbyte, 28 bits
- C. 512 Mbyte, 20 bits
- D. 64 Gbyte, 28 bits

gatecse-2007 operating-system disk normal isro2016

[Answer key](#)

#### 5.4.17 Disk: GATE CSE 2008 | Question: 32 [top](#)



For a magnetic disk with concentric circular tracks, the seek latency is not linearly proportional to the seek distance due to

- A. non-uniform distribution of requests
- B. arm starting and stopping inertia
- C. higher capacity of tracks on the periphery of the platter
- D. use of unfair arm scheduling policies

gatecse-2008 operating-system disk normal

[Answer key](#)

#### 5.4.18 Disk: GATE CSE 2009 | Question: 51 [top](#)



A hard disk has 63 sectors per track, 10 platters each with 2 recording surfaces and 1000 cylinders. The

address of a sector is given as a triple  $\langle c, h, s \rangle$ , where  $c$  is the cylinder number,  $h$  is the surface number and  $s$  is the sector number. Thus, the  $0^{th}$  sector is addresses as  $\langle 0, 0, 0 \rangle$ , the  $1^{st}$  sector as  $\langle 0, 0, 1 \rangle$ , and so on

The address  $\langle 400, 16, 29 \rangle$  corresponds to sector number:

- A. 505035      B. 505036      C. 505037      D. 505038

gatecse-2009 operating-system disk normal

[Answer key](#)

#### 5.4.19 Disk: GATE CSE 2009 | Question: 52 [top](#)

A hard disk has 63 sectors per track, 10 platters each with 2 recording surfaces and 1000 cylinders. The address of a sector is given as a triple  $\langle c, h, s \rangle$ , where  $c$  is the cylinder number,  $h$  is the surface number and  $s$  is the sector number. Thus, the  $0^{th}$  sector is addresses as  $\langle 0, 0, 0 \rangle$ , the  $1^{st}$  sector as  $\langle 0, 0, 1 \rangle$ , and so on

The address of the 1039<sup>th</sup> sector is

- A.  $\langle 0, 15, 31 \rangle$       B.  $\langle 0, 16, 30 \rangle$   
C.  $\langle 0, 16, 31 \rangle$       D.  $\langle 0, 17, 31 \rangle$

gatecse-2009 operating-system disk normal

[Answer key](#)

#### 5.4.20 Disk: GATE CSE 2011 | Question: 44 [top](#)

An application loads 100 libraries at startup. Loading each library requires exactly one disk access. The seek time of the disk to a random location is given as 10 ms. Rotational speed of disk is 6000 rpm. If all 100 libraries are loaded from random locations on the disk, how long does it take to load all libraries? (The time to transfer data from the disk block once the head has been positioned at the start of the block may be neglected.)

- A. 0.50 s      B. 1.50 s      C. 1.25 s      D. 1.00 s

gatecse-2011 operating-system disk normal

[Answer key](#)

#### 5.4.21 Disk: GATE CSE 2012 | Question: 41 [top](#)

A file system with 300 GByte disk uses a file descriptor with 8 direct block addresses, 1 indirect block address and 1 doubly indirect block address. The size of each disk block is 128 Bytes and the size of each disk block address is 8 Bytes. The maximum possible file size in this file system is

- A. 3 KBytes      B. 35 KBytes  
C. 280 KBytes      D. dependent on the size of the disk

gatecse-2012 operating-system disk normal

[Answer key](#)

#### 5.4.22 Disk: GATE CSE 2013 | Question: 29 [top](#)

Consider a hard disk with 16 recording surfaces (0 – 15) having 16384 cylinders (0 – 16383) and each cylinder contains 64 sectors (0 – 63). Data storage capacity in each sector is 512 bytes. Data are organized cylinder-wise and the addressing format is  $\langle$  cylinder no., surface no., sector no.  $\rangle$ . A file of size 42797 KB is stored in the disk and the starting disk location of the file is  $\langle 1200, 9, 40 \rangle$ . What is the cylinder number of the last sector of the file, if it is stored in a contiguous manner?

- A. 1281      B. 1282      C. 1283      D. 1284

gatecse-2013 operating-system disk normal

[Answer key](#)

#### 5.4.23 Disk: GATE CSE 2015 Set 1 | Question: 48 [top](#)

Consider a disk pack with a seek time of 4 milliseconds and rotational speed of 10000 rotations per minute (RPM). It has 600 sectors per track and each sector can store 512 bytes of data. Consider a file stored in the disk. The file contains 2000 sectors. Assume that every sector access necessitates a seek, and the average

rotational latency for accessing each sector is half of the time for one complete rotation. The total time (in milliseconds) needed to read the entire file is \_\_\_\_\_

gatecse-2015-set1 operating-system disk normal numerical-answers

Answer key 

#### 5.4.24 Disk: GATE CSE 2015 Set 2 | Question: 49

Consider a typical disk that rotates at 15000 rotations per minute (RPM) and has a transfer rate of  $50 \times 10^6$  bytes/sec. If the average seek time of the disk is twice the average rotational delay and the controller's transfer time is 10 times the disk transfer time, the average time (in milliseconds) to read or write a 512-byte sector of the disk is \_\_\_\_\_

gatecse-2015-set2 operating-system disk normal numerical-answers

Answer key 

#### 5.4.25 Disk: GATE CSE 2018 | Question: 53

Consider a storage disk with 4 platters (numbered as 0, 1, 2 and 3), 200 cylinders (numbered as 0, 1, ..., 199), and 256 sectors per track (numbered as 0, 1, ..., 255). The following 6 disk requests of the form [sector number, cylinder number, platter number] are received by the disk controller at the same time:

[120, 72, 2], [180, 134, 1], [60, 20, 0], [212, 86, 3], [56, 116, 2], [118, 16, 1]

Currently head is positioned at sector number 100 of cylinder 80, and is moving towards higher cylinder numbers. The average power dissipation in moving the head over 100 cylinders is 20 milliwatts and for reversing the direction of the head movement once is 15 milliwatts. Power dissipation associated with rotational latency and switching of head between different platters is negligible.

The total power consumption in milliwatts to satisfy all of the above disk requests using the Shortest Seek Time First disk scheduling algorithm is \_\_\_\_\_

gatecse-2018 operating-system disk numerical-answers 2-marks

Answer key 

#### 5.4.26 Disk: GATE IT 2005 | Question: 63

In a computer system, four files of size 11050 bytes, 4990 bytes, 5170 bytes and 12640 bytes need to be stored. For storing these files on disk, we can use either 100 byte disk blocks or 200 byte disk blocks (but can't mix block sizes). For each block used to store a file, 4 bytes of bookkeeping information also needs to be stored on the disk. Thus, the total space used to store a file is the sum of the space taken to store the file and the space taken to store the book keeping information for the blocks allocated for storing the file. A disk block can store either bookkeeping information for a file or data from a file, but not both.

What is the total space required for storing the files using 100 byte disk blocks and 200 byte disk blocks respectively?

- A. 35400 and 35800 bytes
- B. 35800 and 35400 bytes
- C. 35600 and 35400 bytes
- D. 35400 and 35600 bytes

gateit-2005 operating-system disk normal

Answer key 

#### 5.4.27 Disk: GATE IT 2005 | Question: 81-a

A disk has 8 equidistant tracks. The diameters of the innermost and outermost tracks are 1 cm and 8 cm respectively. The innermost track has a storage capacity of 10 MB.

What is the total amount of data that can be stored on the disk if it is used with a drive that rotates it with

- I. Constant Linear Velocity
  - II. Constant Angular Velocity?
- A. I. 80 MB; II. 2040 MB
  - B. I. 2040 MB; II 80 MB
  - C. I. 80 MB; II. 360 MB
  - D. I. 360 MB; II. 80 MB

gateit-2005 operating-system disk normal

[Answer key](#)

#### 5.4.28 Disk: GATE IT 2005 | Question: 81-b [top](#)

A disk has 8 equidistant tracks. The diameters of the innermost and outermost tracks are 1 cm and 8 cm respectively. The innermost track has a storage capacity of 10 MB.

If the disk has 20 sectors per track and is currently at the end of the 5<sup>th</sup> sector of the inner-most track and the head can move at a speed of 10 meters/sec and it is rotating at constant angular velocity of 6000 RPM, how much time will it take to read 1 MB contiguous data starting from the sector 4 of the outer-most track?

- A. 13.5 ms      B. 10 ms      C. 9.5 ms      D. 20 ms

gateit-2005 operating-system disk normal

[Answer key](#)

#### 5.4.29 Disk: GATE IT 2007 | Question: 44, ISRO2015-34 [top](#)

A hard disk system has the following parameters :

- Number of tracks = 500
- Number of sectors/track = 100
- Number of bytes /sector = 500
- Time taken by the head to move from one track to adjacent track = 1 ms
- Rotation speed = 600 rpm.

What is the average time taken for transferring 250 bytes from the disk ?

- A. 300.5 ms      B. 255.5 ms      C. 255 ms      D. 300 ms

gateit-2007 operating-system disk normal isro2015

[Answer key](#)

### 5.5

#### Disk Scheduling (14) [top](#)

##### 5.5.1 Disk Scheduling: GATE CSE 1989 | Question: 4-xii [top](#)

Disk requests come to disk driver for cylinders 10, 22, 20, 2, 40, 6 and 38, in that order at a time when the disk drive is reading from cylinder 20. The seek time is 6 msec per cylinder. Compute the total seek time if the disk arm scheduling algorithm is.

- A. First come first served.  
B. Closest cylinder next.

gate1989 descriptive operating-system disk-scheduling

[Answer key](#)

##### 5.5.2 Disk Scheduling: GATE CSE 1990 | Question: 9b [top](#)

Assuming the current disk cylinder to be 50 and the sequence for the cylinders to be 1, 36, 49, 65, 53, 12, 3, 20, 55, 16, 65 and 78 find the sequence of servicing using

- Shortest seek time first (SSTF) and
- Elevator disk scheduling policies.

gate1990 descriptive operating-system disk-scheduling

[Answer key](#)

##### 5.5.3 Disk Scheduling: GATE CSE 1995 | Question: 20 [top](#)

The head of a moving head disk with 100 tracks numbered 0 to 99 is currently serving a request at track 55. If the queue of requests kept in FIFO order is

10, 70, 75, 23, 65

which of the two disk scheduling algorithms FCFS (First Come First Served) and SSTF (Shortest Seek Time First) will require less head movement? Find the head movement for each of the algorithms.

gate1995 operating-system disk-scheduling normal descriptive

[Answer key](#)

#### 5.5.4 Disk Scheduling: GATE CSE 1997 | Question: 3.6 [top](#)



The correct matching for the following pairs is:

(A) Disk Scheduling	(1) Round robin
(B) Batch Processing	(2) SCAN
(C) Time-sharing	(3) LIFO
(D) Interrupt processing	(4) FIFO

- A. A-3 B-4 C-2 D-1   B. A-4 B-3 C-2 D-1   C. A-2 B-4 C-1 D-3   D. A-3 B-4 C-3 D-2

gate1997 operating-system normal disk-scheduling interrupts

[Answer key](#)



#### 5.5.5 Disk Scheduling: GATE CSE 1999 | Question: 1.10 [top](#)



Which of the following disk scheduling strategies is likely to give the best throughput?

- A. Farthest cylinder next      B. Nearest cylinder next  
C. First come first served      D. Elevator algorithm

gate1999 operating-system disk-scheduling normal

[Answer key](#)



#### 5.5.6 Disk Scheduling: GATE CSE 2004 | Question: 12 [top](#)



Consider an operating system capable of loading and executing a single sequential user process at a time. The disk head scheduling algorithm used is First Come First Served (FCFS). If FCFS is replaced by Shortest Seek Time First (SSTF), claimed by the vendor to give 50% better benchmark results, what is the expected improvement in the I/O performance of user programs?

- A. 50%      B. 40%      C. 25%      D. 0%

gatecse-2004 operating-system disk-scheduling normal

[Answer key](#)



#### 5.5.7 Disk Scheduling: GATE CSE 2009 | Question: 31 [top](#)



Consider a disk system with 100 cylinders. The requests to access the cylinders occur in following sequence:

4, 34, 10, 7, 19, 73, 2, 15, 6, 20

Assuming that the head is currently at cylinder 50, what is the time taken to satisfy all requests if it takes 1 ms to move from one cylinder to adjacent one and shortest seek time first policy is used?

- A. 95 ms      B. 119 ms      C. 233 ms      D. 276 ms

gatecse-2009 operating-system disk-scheduling normal

[Answer key](#)



#### 5.5.8 Disk Scheduling: GATE CSE 2014 Set 1 | Question: 19 [top](#)



Suppose a disk has 201 cylinders, numbered from 0 to 200. At some time the disk arm is at cylinder 100, and there is a queue of disk access requests for cylinders 30, 85, 90, 100, 105, 110, 135 and 145. If Shortest-Seek Time First (SSTF) is being used for scheduling the disk access, the request for cylinder 90 is serviced after servicing \_\_\_\_\_ number of requests.

**Answer key****5.5.9 Disk Scheduling: GATE CSE 2015 Set 1 | Question: 30**

Suppose the following disk request sequence (track numbers) for a disk with 100 tracks is given:

45, 20, 90, 10, 50, 60, 80, 25, 70.

Assume that the initial position of the R/W head is on track 50. The additional distance that will be traversed by the R/W head when the Shortest Seek Time First (SSTF) algorithm is used compared to the SCAN (Elevator) algorithm (assuming that SCAN algorithm moves towards 100 when it starts execution) is \_\_\_\_\_ tracks.

**Answer key****5.5.10 Disk Scheduling: GATE CSE 2016 Set 1 | Question: 48**

Cylinder a disk queue with requests for I/O to blocks on cylinders 47, 38, 121, 191, 87, 11, 92, 10. The C-LOOK scheduling algorithm is used. The head is initially at cylinder number 63, moving towards larger cylinder numbers on its servicing pass. The cylinders are numbered from 0 to 199. The total head movement (in number of cylinders) incurred while servicing these requests is \_\_\_\_\_.

**Answer key****5.5.11 Disk Scheduling: GATE CSE 2020 | Question: 35**

Consider the following five disk five disk access requests of the form (request id, cylinder number) that are present in the disk scheduler queue at a given time.

(P, 155), (Q, 85), (R, 110), (S, 30), (T, 115)

Assume the head is positioned at cylinder 100. The scheduler follows Shortest Seek Time First scheduling to service the requests.

Which one of the following statements is FALSE?

- A. T is serviced before P.
- B. Q is serviced after S, but before T.
- C. The head reverses its direction of movement between servicing of Q and P.
- D. R is serviced before P.

**Answer key****5.5.12 Disk Scheduling: GATE IT 2004 | Question: 62**

A disk has 200 tracks (numbered 0 through 199). At a given time, it was servicing the request of reading data from track 120, and at the previous request, service was for track 90. The pending requests (in order of their arrival) are for track numbers.

30 70 115 130 110 80 20 25.

How many times will the head change its direction for the disk scheduling policies SSTF(Shortest Seek Time First) and FCFS (First Come First Serve)?

- A. 2 and 3
- B. 3 and 3
- C. 3 and 4
- D. 4 and 4

**Answer key****5.5.13 Disk Scheduling: GATE IT 2007 | Question: 82**

The head of a hard disk serves requests following the shortest seek time first (SSTF) policy. The head is initially positioned at track number 180.

Which of the request sets will cause the head to change its direction after servicing every request assuming that the head does not change direction if there is a tie in SSTF and all the requests arrive before the servicing starts?

- A. 11,139,170,178,181,184,201,265  
B. 10,138,170,178,181,185,201,265  
C. 10,139,169,178,181,184,201,265  
D. 10,138,170,178,181,185,200,265

gateit-2007 operating-system disk-scheduling normal

[Answer key](#)



#### 5.5.14 Disk Scheduling: GATE IT 2007 | Question: 83 [top](#)

The head of a hard disk serves requests following the shortest seek time first (SSTF) policy.

What is the maximum cardinality of the request set, so that the head changes its direction after servicing every request if the total number of tracks are 2048 and the head can start from any track?

- A. 9      B. 10      C. 11      D. 12

gateit-2007 operating-system disk-scheduling normal

[Answer key](#)

### 5.6

#### File System (9) [top](#)



#### 5.6.1 File System: GATE CSE 1996 | Question: 23 [top](#)

A file system with a one-level directory structure is implemented on a disk with disk block size of  $4K$  bytes. The disk is used as follows:

Disk-block 0	File Allocation Table, consisting of one 8-bit entry per data block, representing the data block address of the next data block in the file
Disk-block 1	Directory, with one 32 bit entry per file:
Disk-block 2	Data-block 1;
Disk-block 3	Data-block 2; etc.

- a. What is the maximum possible number of files?  
b. What is the maximum possible file size in blocks

gate1996 operating-system disk normal file-system descriptive

[Answer key](#)



#### 5.6.2 File System: GATE CSE 2002 | Question: 2.22 [top](#)

In the index allocation scheme of blocks to a file, the maximum possible size of the file depends on

- A. the size of the blocks, and the size of the address of the blocks.  
B. the number of blocks used for the index, and the size of the blocks.  
C. the size of the blocks, the number of blocks used for the index, and the size of the address of the blocks.  
D. None of the above

gatecse-2002 operating-system normal file-system

[Answer key](#)



#### 5.6.3 File System: GATE CSE 2008 | Question: 20 [top](#)



The data blocks of a very large file in the Unix file system are allocated using

- A. continuous allocation  
C. indexed allocation  
B. linked allocation  
D. an extension of indexed allocation

gatecse-2008 file-system operating-system normal

[Answer key](#)

#### 5.6.4 File System: GATE CSE 2014 Set 2 | Question: 20 [top](#)



A FAT (file allocation table) based file system is being used and the total overhead of each entry in the FAT is 4 bytes in size. Given a  $100 \times 10^6$  bytes disk on which the file system is stored and data block size is  $10^3$  bytes, the maximum size of a file that can be stored on this disk in units of  $10^6$  bytes is \_\_\_\_\_.

gatecse-2014-set2 operating-system disk numerical-answers normal file-system

[Answer key](#)

#### 5.6.5 File System: GATE CSE 2017 Set 2 | Question: 08 [top](#)



In a file allocation system, which of the following allocation scheme(s) can be used if no external fragmentation is allowed?

1. Contiguous
  2. Linked
  3. Indexed
- A. 1 and 3 only      B. 2 only      C. 3 only      D. 2 and 3 only

gatecse-2017-set2 operating-system file-system normal

[Answer key](#)

#### 5.6.6 File System: GATE CSE 2019 | Question: 42 [top](#)



The index node (inode) of a Unix -like file system has 12 direct, one single-indirect and one double-indirect pointers. The disk block size is 4 kB, and the disk block address is 32-bits long. The maximum possible file size is (rounded off to 1 decimal place) \_\_\_\_\_ GB

gatecse-2019 numerical-answers operating-system file-system 2-marks

[Answer key](#)

#### 5.6.7 File System: GATE CSE 2021 Set 1 | Question: 15 [top](#)



Consider a linear list based directory implementation in a file system. Each directory is a list of nodes, where each node contains the file name along with the file metadata, such as the list of pointers to the data blocks. Consider a given directory `foo`.

Which of the following operations will necessarily require a full scan of `foo` for successful completion?

- A. Creation of a new file in `foo`  
B. Deletion of an existing file from `foo`  
C. Renaming of an existing file in `foo`  
D. Opening of an existing file in `foo`

gatecse-2021-set1 multiple-selects operating-system file-system 1-mark

[Answer key](#)

#### 5.6.8 File System: GATE CSE 2022 | Question: 53 [top](#)



Consider two files systems A and B, that use contiguous allocation and linked allocation, respectively. A file of size 100 blocks is already stored in A and also in B. Now, consider inserting a new block in the middle of the file (between 50<sup>th</sup> and 51<sup>st</sup> block), whose data is already available in the memory. Assume that there are enough free blocks at the end of the file and that the file control blocks are already in memory. Let the number of disk accesses required to insert a block in the middle of the file in A and B are  $n_A$  and  $n_B$ , respectively, then the value of  $n_A + n_B$  is \_\_\_\_\_.

gatecse-2022 numerical-answers operating-system file-system 2-marks

[Answer key](#)

#### 5.6.9 File System: GATE IT 2004 | Question: 67 [top](#)



In a particular Unix OS, each data block is of size 1024 bytes, each node has 10 direct data block addresses and three additional addresses: one for single indirect block, one for double indirect block and one for triple indirect block. Also, each block can contain addresses for 128 blocks. Which one of the following is approximately the maximum size of a file in the file system?

- A. 512 MB      B. 2 GB      C. 8 GB      D. 16 GB

gateit-2004 operating-system file-system normal

[Answer key](#)

5.7

## Fork System Call (6) [top](#)



### 5.7.1 Fork System Call: GATE CSE 2005 | Question: 72 [top](#)

Consider the following code fragment:

```
if (fork() == 0)
{
    a = a + 5;
    printf("%d, %p\n", a, &a);
}
else
{
    a = a - 5;
    printf ("%d, %p\n", a,& a);
```

Let  $u, v$  be the values printed by the parent process and  $x, y$  be the values printed by the child process. Which one of the following is **TRUE**?

- A.  $u = x + 10$  and  $v = y$   
 B.  $u = x + 10$  and  $v! = y$   
 C.  $u + 10 = x$  and  $v = y$   
 D.  $u + 10 = x$  and  $v! = y$

gatecse-2005 operating-system fork-system-call normal

[Answer key](#)



### 5.7.2 Fork System Call: GATE CSE 2008 | Question: 66 [top](#)

A process executes the following code

```
for(i=0; i<n; i++) fork();
```

The total number of child processes created is

- A.  $n$       B.  $2^n - 1$       C.  $2^n$       D.  $2^{n+1} - 1$

gatecse-2008 operating-system fork-system-call normal

[Answer key](#)



### 5.7.3 Fork System Call: GATE CSE 2012 | Question: 8 [top](#)

A process executes the code

```
fork();
fork();
fork();
```

The total number of **child** processes created is

- A. 3      B. 4      C. 7      D. 8

gatecse-2012 operating-system easy fork-system-call

[Answer key](#)



### 5.7.4 Fork System Call: GATE CSE 2019 | Question: 17 [top](#)

The following C program is executed on a Unix/Linux system :

```
#include<unistd.h>
int main()
{
    int i;
    for(i=0; i<10; i++)
        if(i%2 == 0)
            fork();
    return 0;
}
```

The total number of child processes created is \_\_\_\_\_.

gatecse-2019 numerical-answers operating-system fork-system-call 1-mark

Answer key

### 5.7.5 Fork System Call: GATE CSE 2023 | Question: 13

Which one or more of the following options guarantee that a computer system will transition from user mode to kernel mode?

- A. Function Call
- B. malloc Call
- C. Page Fault
- D. System Call

gatecse-2023 operating-system fork-system-call multiple-selects 1-mark

Answer key

### 5.7.6 Fork System Call: GATE IT 2004 | Question: 64

A process executes the following segment of code :

```
for(i = 1; i <= n; i++)
    fork();
```

The number of new processes created is

- A.  $n$
- B.  $((n(n + 1))/2)$
- C.  $2^n - 1$
- D.  $3^n - 1$

gateit-2004 operating-system fork-system-call easy

Answer key

## 5.8

### Inter Process Communication (1)

#### 5.8.1 Inter Process Communication: GATE CSE 1997 | Question: 3.7

I/O redirection

- A. implies changing the name of a file
- B. can be employed to use an existing file as input file for a program
- C. implies connecting 2 programs through a pipe
- D. None of the above

gate1997 operating-system normal inter-process-communication

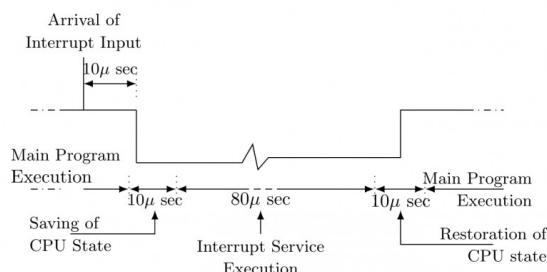
Answer key

## 5.9

### Interrupts (7)

#### 5.9.1 Interrupts: GATE CSE 1993 | Question: 6.8

The details of an interrupt cycle are shown in figure.



Given that an interrupt input arrives every 1 msec, what is the percentage of the total time that the CPU devotes for the main program execution.

**Answer key****5.9.2 Interrupts: GATE CSE 1997 | Question: 3.8**

When an interrupt occurs, an operating system

- A. ignores the interrupt
- B. always changes state of interrupted process after processing the interrupt
- C. always resumes execution of interrupted process after processing the interrupt
- D. may change state of interrupted process to 'blocked' and schedule another process.

**Answer key****5.9.3 Interrupts: GATE CSE 1998 | Question: 1.18**

Which of the following devices should get higher priority in assigning interrupts?

- A. Hard disk
- B. Printer
- C. Keyboard
- D. Floppy disk

**Answer key****5.9.4 Interrupts: GATE CSE 1999 | Question: 1.9**

Listed below are some operating system abstractions (in the left column) and the hardware components (in the right column)

(A) Thread	1. Interrupt
(B) Virtual address space	2. Memory
(C) File system	3. CPU
(D) Signal	4. Disk

- A. (A) – 2 (B) – 4 (C) – 3 (D) – 1
- B. (A) – 1 (B) – 2 (C) – 3 (D) – 4
- C. (A) – 3 (B) – 2 (C) – 4 (D) – 1
- D. (A) – 4 (B) – 1 (C) – 2 (D) – 3

**Answer key****5.9.5 Interrupts: GATE CSE 2001 | Question: 1.12**

A processor needs software interrupt to

- A. test the interrupt system of the processor
- B. implement co-routines
- C. obtain system services which need execution of privileged instructions
- D. return from subroutine

**Answer key****5.9.6 Interrupts: GATE CSE 2011 | Question: 11**

A computer handles several interrupt sources of which of the following are relevant for this question.

- Interrupt from CPU temperature sensor (raises interrupt if CPU temperature is too high)
- Interrupt from Mouse (raises interrupt if the mouse is moved or a button is pressed)

- Interrupt from Keyboard (raises Interrupt if a key is pressed or released)
- Interrupt from Hard Disk (raises Interrupt when a disk read is completed)

Which one of these will be handled at the **HIGHEST** priority?

- |                             |  |
|-----------------------------|--|
| A. Interrupt from Hard Disk | B. Interrupt from Mouse                  |
| C. Interrupt from Keyboard  | D. Interrupt from CPU temperature sensor |

gatecse-2011 operating-system interrupts normal

**Answer key** 

#### 5.9.7 Interrupts: GATE CSE 2018 | Question: 9



The following are some events that occur after a device controller issues an interrupt while process  $L$  is under execution.

- P. The processor pushes the process status of  $L$  onto the control stack
- Q. The processor finishes the execution of the current instruction
- R. The processor executes the interrupt service routine
- S. The processor pops the process status of  $L$  from the control stack
- T. The processor loads the new PC value based on the interrupt

Which of the following is the correct order in which the events above occur?

- |          |          |          |          |
|----------|----------|----------|----------|
| A. QPTRS | B. PTRSQ | C. TRPQS | D. QTPRS |
|----------|----------|----------|----------|

gatecse-2018 operating-system interrupts normal 1-mark

**Answer key** 

#### 5.10

#### Io Handling (6)



#### 5.10.1 Io Handling: GATE CSE 1996 | Question: 1.20, ISRO2008-56

Which of the following is an example of spooled device?

- A. A line printer used to print the output of a number of jobs
- B. A terminal used to enter input data to a running program
- C. A secondary storage device in a virtual memory system
- D. A graphic display device

gate1996 operating-system io-handling normal isro2008

**Answer key** 

#### 5.10.2 Io Handling: GATE CSE 1998 | Question: 1.29



Which of the following is an example of a spooled device?

- A. The terminal used to enter the input data for the C program being executed
- B. An output device used to print the output of a number of jobs
- C. The secondary memory device in a virtual storage system
- D. The swapping area on a disk used by the swapper

gate1998 operating-system io-handling easy

**Answer key** 

#### 5.10.3 Io Handling: GATE CSE 2005 | Question: 19



Which one of the following is true for a CPU having a single interrupt request line and a single interrupt grant line?

- A. Neither vectored interrupt nor multiple interrupting devices are possible

- B. Vectored interrupts are not possible but multiple interrupting devices are possible
- C. Vectored interrupts and multiple interrupting devices are both possible
- D. Vectored interrupts are possible but multiple interrupting devices are not possible

gatecse-2005 operating-system io-handling normal

[Answer key](#)

#### 5.10.4 Io Handling: GATE CSE 2005 | Question: 20 [top](#)



Normally user programs are prevented from handling I/O directly by I/O instructions in them. For CPUs having explicit I/O instructions, such I/O protection is ensured by having the I/O instruction privileged. In a CPU with memory mapped I/O, there is no explicit I/O instruction. Which one of the following is true for a CPU with memory mapped I/O?

- A. I/O protection is ensured by operating system routine(s)
- B. I/O protection is ensured by a hardware trap
- C. I/O protection is ensured during system configuration
- D. I/O protection is not possible

gatecse-2005 operating-system io-handling normal

[Answer key](#)

#### 5.10.5 Io Handling: GATE IT 2004 | Question: 11, ISRO2011-33 [top](#)



What is the bit rate of a video terminal unit with 80 characters/line, 8 bits/character and horizontal sweep time of 100  $\mu$ s (including 20  $\mu$ s of retrace time)?

- A. 8 Mbps
- B. 6.4 Mbps
- C. 0.8 Mbps
- D. 0.64 Mbps

gateit-2004 operating-system io-handling easy isro2011

[Answer key](#)

#### 5.10.6 Io Handling: GATE IT 2006 | Question: 8 [top](#)



Which of the following DMA transfer modes and interrupt handling mechanisms will enable the highest I/O band-width?

- |   |   |
|---|---|
| A. Transparent DMA and Polling interrupts | B. Cycle-stealing and Vectored interrupts |
| C. Block transfer and Vectored interrupts | D. Block transfer and Polling interrupts  |

gateit-2006 operating-system io-handling dma normal

[Answer key](#)

### 5.11

#### Least Recently Used (1) [top](#)



#### 5.11.1 Least Recently Used: GATE CSE 2023 | Question: 47 [top](#)

Consider the following two-dimensional array D in the C programming language, which is stored in row-major order:

```
int D[128][128];
```

Demand paging is used for allocating memory and each physical page frame holds 512 elements of the array D. The Least Recently Used (LRU) page-replacement policy is used by the operating system. A total of 30 physical page frames are allocated to a process which executes the following code snippet:

```
for (int i = 0; i < 128; i++)
    for (int j = 0; j < 128; j++)
        D[j][i] *= 10;
```

The number of page faults generated during the execution of this code snippet is \_\_\_\_\_.

**Answer key****5.12****Memory Management (9)****5.12.1 Memory Management: GATE CSE 1992 | Question: 12-b**

Let the page reference and the working set window be  $c c d b c e c e a d$  and 4, respectively. The initial working set at time  $t = 0$  contains the pages  $\{a, d, e\}$ , where  $a$  was referenced at time  $t = 0$ ,  $d$  was referenced at time  $t = -1$ , and  $e$  was referenced at time  $t = -2$ . Determine the total number of page faults and the average number of page frames used by computing the working set at each reference.

**Answer key****5.12.2 Memory Management: GATE CSE 1995 | Question: 5**

A computer installation has  $1000k$  of main memory. The jobs arrive and finish in the following sequences.

Job 1 requiring 200k arrives  
 Job 2 requiring 350k arrives  
 Job 3 requiring 300k arrives  
 Job 1 finishes  
 Job 4 requiring 120k arrives  
 Job 5 requiring 150k arrives  
 Job 6 requiring 80k arrives

- Draw the memory allocation table using Best Fit and First Fit algorithms.
- Which algorithm performs better for this sequence?

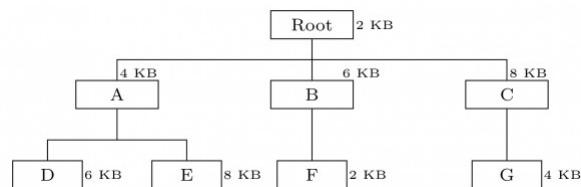
**Answer key****5.12.3 Memory Management: GATE CSE 1996 | Question: 2.18**

A 1000 Kbyte memory is managed using variable partitions but no compaction. It currently has two partitions of sizes 200 Kbyte and 260 Kbyte respectively. The smallest allocation request in Kbyte that could be denied is for

- A. 151      B. 181      C. 231      D. 541

**Answer key****5.12.4 Memory Management: GATE CSE 1998 | Question: 2.16**

The overlay tree for a program is as shown below:



What will be the size of the partition (in physical memory) required to load (and run) this program?

- A. 12 KB      B. 14 KB      C. 10 KB      D. 8 KB

**Answer key**

### 5.12.5 Memory Management: GATE CSE 2014 Set 2 | Question: 55 top



Consider the main memory system that consists of 8 memory modules attached to the system bus, which is one word wide. When a write request is made, the bus is occupied for 100 nanoseconds (ns) by the data, address, and control signals. During the same 100 ns, and for 500 ns thereafter, the addressed memory module executes one cycle accepting and storing the data. The (internal) operation of different memory modules may overlap in time, but only one request can be on the bus at any time. The maximum number of stores (of one word each) that can be initiated in 1 millisecond is \_\_\_\_\_

gatecse-2014-set2 operating-system memory-management numerical-answers normal

[Answer key](#)

### 5.12.6 Memory Management: GATE CSE 2015 Set 2 | Question: 30 top



Consider 6 memory partitions of sizes 200 KB, 400 KB, 600 KB, 500 KB, 300 KB and 250 KB, where KBrefers to kilobyte. These partitions need to be allotted to four processes of sizes 357 KB, 210 KB, 468 KB, 491 KBin that order. If the best-fit algorithm is used, which partitions are NOT allotted to any process?

- A. 200 KB and 300 KB
- B. 200 KB and 250 KB
- C. 250 KB and 300 KB
- D. 300 KB and 400 KB

gatecse-2015-set2 operating-system memory-management easy

[Answer key](#)

### 5.12.7 Memory Management: GATE CSE 2020 | Question: 11 top



Consider allocation of memory to a new process. Assume that none of the existing holes in the memory will exactly fit the process's memory requirement. Hence, a new hole of smaller size will be created if allocation is made in any of the existing holes. Which one of the following statement is TRUE?

- A. The hole created by first fit is always larger than the hole created by next fit.
- B. The hole created by worst fit is always larger than the hole created by first fit.
- C. The hole created by best fit is never larger than the hole created by first fit.
- D. The hole created by next fit is never larger than the hole created by best fit.

gatecse-2020 operating-system memory-management 1-mark

[Answer key](#)

### 5.12.8 Memory Management: GATE IT 2006 | Question: 56 top



For each of the four processes  $P_1, P_2, P_3$ , and  $P_4$ . The total size in kilobytes (KB) and the number of segments are given below.

Process	Total size (in KB)	Number of segments
$P_1$	195	4
$P_2$	254	5
$P_3$	45	3
$P_4$	364	8

The page size is 1 KB. The size of an entry in the page table is 4 bytes. The size of an entry in the segment table is 8 bytes. The maximum size of a segment is 256 KB. The paging method for memory management uses two-level paging, and its storage overhead is  $P$ . The storage overhead for the segmentation method is  $S$ . The storage overhead for the segmentation and paging method is  $T$ . What is the relation among the overheads for the different methods of memory management in the concurrent execution of the above four processes?

- A.  $P < S < T$
- B.  $S < P < T$
- C.  $S < T < P$
- D.  $T < S < P$

gateit-2006 operating-system memory-management difficult

[Answer key](#)

### 5.12.9 Memory Management: GATE IT 2007 | Question: 11 top



Let a memory have four free blocks of sizes  $4k$ ,  $8k$ ,  $20k$ ,  $2k$ . These blocks are allocated following the best-fit strategy. The allocation requests are stored in a queue as shown below.

Request No	J1	J2	J3	J4	J5	J6	J7	J8
Request Sizes	2k	14k	3k	6k	6k	10k	7k	20k
Usage Time	4	10	2	8	4	1	8	6

The time at which the request for  $J7$  will be completed will be

- A. 16      B. 19      C. 20      D. 37

gateit-2007 operating-system memory-management normal

[Answer key](#)

### 5.13

### Multilevel Paging (1) top



#### 5.13.1 Multilevel Paging: GATE CSE 2023 | Question: 48 top

Consider a computer system with 57-bit virtual addressing using multi-level tree-structured page tables with  $L$  levels for virtual to physical address translation. The page size is 4 KB ( $1 \text{ KB} = 1024 \text{ B}$ ) and a page table entry at any of the levels occupies 8 bytes.

The value of  $L$  is \_\_\_\_\_.

gatecse-2023 operating-system multilevel-paging numerical-answers 2-marks

[Answer key](#)

### 5.14

### Os Protection (3) top



#### 5.14.1 Os Protection: GATE CSE 1999 | Question: 1.11, UGCNET-Dec2015-II: 44 top

System calls are usually invoked by using

- A. a software interrupt      B. polling  
C. an indirect jump      D. a privileged instruction

gate1999 operating-system normal ugcnetcse-dec2015-paper2 os-protection

[Answer key](#)

#### 5.14.2 Os Protection: GATE CSE 2001 | Question: 1.13 top



A CPU has two modes -- privileged and non-privileged. In order to change the mode from privileged to non-privileged

- A. a hardware interrupt is needed  
B. a software interrupt is needed  
C. a privileged instruction (which does not generate an interrupt) is needed  
D. a non-privileged instruction (which does not generate an interrupt) is needed

gatecse-2001 operating-system normal os-protection

[Answer key](#)

#### 5.14.3 Os Protection: GATE IT 2005 | Question: 19, UGCNET-June2012-III: 57 top



A user level process in Unix traps the signal sent on a Ctrl-C input, and has a signal handling routine that saves appropriate files before terminating the process. When a Ctrl-C input is given to this process, what is the mode in which the signal handling routine executes?

- A. User mode      B. Kernel mode      C. Superuser mode      D. Privileged mode

gateit-2005 operating-system os-protection normal ugcnetcse-june2012-paper3

[Answer key](#)

**5.15.1 Page Replacement: GATE CSE 1993 | Question: 21** [top](#)

The following page addresses, in the given sequence, were generated by a program:

1 2 3 4 1 3 5 2 1 5 4 3 2 3

This program is run on a demand paged virtual memory system, with main memory size equal to 4 pages. Indicate the page references for which page faults occur for the following page replacement algorithms.

- A. LRU
- B. FIFO

Assume that the main memory is initially empty.

gate1993 operating-system page-replacement normal descriptive

[Answer key](#)

**5.15.2 Page Replacement: GATE CSE 1994 | Question: 1.13** [top](#)

A memory page containing a heavily used variable that was initialized very early and is in constant use is removed then

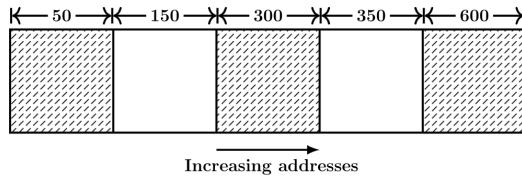
- A. LRU page replacement algorithm is used
- B. FIFO page replacement algorithm is used
- C. LFU page replacement algorithm is used
- D. None of the above

gate1994 operating-system page-replacement easy

[Answer key](#)

**5.15.3 Page Replacement: GATE CSE 1994 | Question: 1.24** [top](#)

Consider the following heap (figure) in which blank regions are not in use and hatched region are in use.



The sequence of requests for blocks of sizes 300, 25, 125, 50 can be satisfied if we use

- A. either first fit or best fit policy (any one)
- B. first fit but not best fit policy
- C. best fit but not first fit policy
- D. None of the above

gate1994 operating-system page-replacement normal

[Answer key](#)

**5.15.4 Page Replacement: GATE CSE 1995 | Question: 1.8** [top](#)

Which of the following page replacement algorithms suffers from Belady's anomaly?

- A. Optimal replacement
- B. LRU
- C. FIFO
- D. Both (A) and (C)

gate1995 operating-system page-replacement normal

[Answer key](#)

**5.15.5 Page Replacement: GATE CSE 1995 | Question: 2.7** [top](#)

The address sequence generated by tracing a particular program executing in a pure demand based paging system with 100 records per page with 1 free main memory frame is recorded as follows. What is the number of page faults?

0100, 0200, 0430, 0499, 0510, 0530, 0560, 0120, 0220, 0240, 0260, 0320, 0370

- A. 13
- B. 8
- C. 7
- D. 10

**Answer key****5.15.6 Page Replacement: GATE CSE 1997 | Question: 3.5**

Locality of reference implies that the page reference being made by a process

- A. will always be to the page used in the previous page reference
- B. is likely to be to one of the pages used in the last few page references
- C. will always be to one of the pages existing in memory
- D. will always lead to a page fault

**Answer key****5.15.7 Page Replacement: GATE CSE 1997 | Question: 3.9**

Thrashing

- A. reduces page I/O
- B. decreases the degree of multiprogramming
- C. implies excessive page I/O
- D. improve the system performance

**Answer key****5.15.8 Page Replacement: GATE CSE 2001 | Question: 1.21**

Consider a virtual memory system with FIFO page replacement policy. For an arbitrary page access pattern, increasing the number of page frames in main memory will

- A. always decrease the number of page faults
- B. always increase the number of page faults
- C. sometimes increase the number of page faults
- D. never affect the number of page faults

**Answer key****5.15.9 Page Replacement: GATE CSE 2002 | Question: 1.23**

The optimal page replacement algorithm will select the page that

- A. Has not been used for the longest time in the past
- B. Will not be used for the longest time in the future
- C. Has been used least number of times
- D. Has been used most number of times

**Answer key****5.15.10 Page Replacement: GATE CSE 2004 | Question: 21, ISRO2007-44**

The minimum number of page frames that must be allocated to a running process in a virtual memory environment is determined by

- A. the instruction set architecture
- B. page size
- C. number of processes in memory
- D. physical memory size

**Answer key**

### 5.15.11 Page Replacement: GATE CSE 2005 | Question: 22, ISRO2015-36 [top](#)



Increasing the RAM of a computer typically improves performance because:

- A. Virtual Memory increases
- B. Larger RAMs are faster
- C. Fewer page faults occur
- D. Fewer segmentation faults occur

gatecse-2005 operating-system page-replacement easy isro2015

[Answer key](#)



### 5.15.12 Page Replacement: GATE CSE 2007 | Question: 56 [top](#)



A virtual memory system uses First In First Out (FIFO) page replacement policy and allocates a fixed number of frames to a process. Consider the following statements:

**P:** Increasing the number of page frames allocated to a process sometimes increases the page fault rate.

**Q:** Some programs do not exhibit locality of reference.

Which one of the following is TRUE?

- A. Both P and Q are true, and Q is the reason for P
- B. Both P and Q are true, but Q is not the reason for P.
- C. P is false but Q is true
- D. Both P and Q are false.

gatecse-2007 operating-system page-replacement normal

[Answer key](#)



### 5.15.13 Page Replacement: GATE CSE 2007 | Question: 82 [top](#)



A process has been allocated 3 page frames. Assume that none of the pages of the process are available in the memory initially. The process makes the following sequence of page references (reference string):

**1, 2, 1, 3, 7, 4, 5, 6, 3, 1**

If optimal page replacement policy is used, how many page faults occur for the above reference string?

- A. 7
- B. 8
- C. 9
- D. 10

gatecse-2007 normal operating-system page-replacement

[Answer key](#)



### 5.15.14 Page Replacement: GATE CSE 2007 | Question: 83 [top](#)



A process, has been allocated 3 page frames. Assume that none of the pages of the process are available in the memory initially. The process makes the following sequence of page references (reference string):

**1, 2, 1, 3, 7, 4, 5, 6, 3, 1**

Least Recently Used (LRU) page replacement policy is a practical approximation to optimal page replacement. For the above reference string, how many more page faults occur with LRU than with the optimal page replacement policy?

- A. 0
- B. 1
- C. 2
- D. 3

gatecse-2007 normal operating-system page-replacement

[Answer key](#)



### 5.15.15 Page Replacement: GATE CSE 2009 | Question: 9, ISRO2016-52 [top](#)



In which one of the following page replacement policies, Belady's anomaly may occur?

- A. FIFO
- B. Optimal
- C. LRU
- D. MRU

gatecse-2009 normal operating-system page-replacement normal isro2016

[Answer key](#)



### 5.15.16 Page Replacement: GATE CSE 2010 | Question: 24 [top](#)



A system uses FIFO policy for system replacement. It has 4 page frames with no pages loaded to begin with. The system first accesses 100 distinct pages in some order and then accesses the same 100 pages but now in the reverse order. How many page faults will occur?

A. 196

B. 192

C. 197

D. 195

gatecse-2010 operating-system page-replacement normal

Answer key 

### 5.15.17 Page Replacement: GATE CSE 2012 | Question: 42 top



Consider the virtual page reference string

1, 2, 3, 2, 4, 1, 3, 2, 4, 1

on a demand paged virtual memory system running on a computer system that has main memory size of 3 page frames which are initially empty. Let LRU, FIFO and OPTIMAL denote the number of page faults under the corresponding page replacement policy. Then

- A. OPTIMAL < LRU < FIFO
- C. OPTIMAL = LRU

- B. OPTIMAL < FIFO < LRU
- D. OPTIMAL = FIFO

gatecse-2012 operating-system page-replacement normal

Answer key 

### 5.15.18 Page Replacement: GATE CSE 2014 Set 1 | Question: 33 top



Assume that there are 3 page frames which are initially empty. If the page reference string is 1, 2, 3, 4, 2, 1, 5, 3, 2, 4, 6 the number of page faults using the optimal replacement policy is \_\_\_\_\_.

gatecse-2014-set1 operating-system page-replacement numerical-answers

Answer key 

### 5.15.19 Page Replacement: GATE CSE 2014 Set 2 | Question: 33 top



A computer has twenty physical page frames which contain pages numbered 101 through 120. Now a program accesses the pages numbered 1, 2, ..., 100 in that order, and repeats the access sequence **THREE**. Which one of the following page replacement policies experiences the same number of page faults as the optimal page replacement policy for this program?

- A. Least-recently-used
- C. Last-in-first-out

- B. First-in-first-out
- D. Most-recently-used

gatecse-2014-set2 operating-system page-replacement ambiguous

Answer key 

### 5.15.20 Page Replacement: GATE CSE 2014 Set 3 | Question: 20 top



A system uses 3 page frames for storing process pages in main memory. It uses the Least Recently Used (**LRU**) page replacement policy. Assume that all the page frames are initially empty. What is the total number of page faults that will occur while processing the page reference string given below?

4, 7, 6, 1, 7, 6, 1, 2, 7, 2

gatecse-2014-set3 operating-system page-replacement numerical-answers normal

Answer key 

### 5.15.21 Page Replacement: GATE CSE 2015 Set 1 | Question: 47 top



Consider a main memory with five-page frames and the following sequence of page references: 3, 8, 2, 3, 9, 1, 6, 3, 8, 9, 3, 6, 2, 1, 3. Which one of the following is true with respect to page replacement policies First In First Out (FIFO) and Least Recently Used (LRU)?

- A. Both incur the same number of page faults
- B. FIFO incurs 2 more page faults than LRU
- C. LRU incurs 2 more page faults than FIFO
- D. FIFO incurs 1 more page faults than LRU

gatecse-2015-set1 operating-system page-replacement normal

[Answer key](#)

### 5.15.22 Page Replacement: GATE CSE 2016 Set 1 | Question: 49 [top](#)



Consider a computer system with ten physical page frames. The system is provided with an access sequence  $(a_1, a_2, \dots, a_{20}, a_1, a_2, \dots, a_{20})$ , where each  $a_i$  is a distinct virtual page number. The difference in the number of page faults between the last-in-first-out page replacement policy and the optimal page replacement policy is \_\_\_\_\_.

gatecse-2016-set1 operating-system page-replacement normal numerical-answers

[Answer key](#)

### 5.15.23 Page Replacement: GATE CSE 2016 Set 2 | Question: 20 [top](#)



In which one of the following page replacement algorithms it is possible for the page fault rate to increase even when the number of allocated frames increases?

- A. LRU (Least Recently Used)
- B. OPT (Optimal Page Replacement)
- C. MRU (Most Recently Used)
- D. FIFO (First In First Out)

gatecse-2016-set2 operating-system page-replacement easy

[Answer key](#)

### 5.15.24 Page Replacement: GATE CSE 2017 Set 1 | Question: 40 [top](#)



Recall that Belady's anomaly is that the page-fault rate may *increase* as the number of allocated frames increases. Now, consider the following statements:

- $S_1$ : Random page replacement algorithm (where a page chosen at random is replaced) suffers from Belady's anomaly.
- $S_2$ : LRU page replacement algorithm suffers from Belady's anomaly.

Which of the following is CORRECT?

- |                                  |                                   |
|----------------------------------|-----------------------------------|
| A. $S_1$ is true, $S_2$ is true  | B. $S_1$ is true, $S_2$ is false  |
| C. $S_1$ is false, $S_2$ is true | D. $S_1$ is false, $S_2$ is false |

gatecse-2017-set1 page-replacement operating-system normal

[Answer key](#)

### 5.15.25 Page Replacement: GATE CSE 2021 Set 1 | Question: 11 [top](#)



In the context of operating systems, which of the following statements is/are correct with respect to paging?

- A. Paging helps solve the issue of external fragmentation
- B. Page size has no impact on internal fragmentation
- C. Paging incurs memory overheads
- D. Multi-level paging is necessary to support pages of different sizes

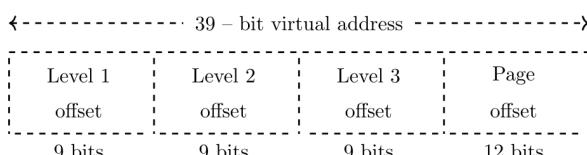
gatecse-2021-set1 multiple-selects operating-system page-replacement 1-mark

[Answer key](#)

### 5.15.26 Page Replacement: GATE CSE 2021 Set 2 | Question: 48 [top](#)



Consider a three-level page table to translate a 39-bit virtual address to a physical address as shown below:



The page size is 4 KB ( $1\text{KB} = 2^{10}$  bytes) and page table entry size at every level is 8 bytes. A process  $P$  is currently using 2GB ( $1\text{GB} = 2^{30}$  bytes) virtual memory which is mapped to 2GB of physical memory. The

minimum amount of memory required for the page table of  $P$  across all levels is \_\_\_\_\_ KB.

gatecse-2021-set2 numerical-answers operating-system memory-management page-replacement 2-marks

Answer key 

### 5.15.27 Page Replacement: GATE IT 2007 | Question: 12

The address sequence generated by tracing a particular program executing in a pure demand paging system with 100 bytes per page is

0100, 0200, 0430, 0499, 0510, 0530, 0560, 0120, 0220, 0240, 0260, 0320, 0410.



Suppose that the memory can store only one page and if  $x$  is the address which causes a page fault then the bytes from addresses  $x$  to  $x + 99$  are loaded on to the memory.

How many page faults will occur?

- A. 0      B. 4      C. 7      D. 8

gateit-2007 operating-system virtual-memory page-replacement normal

Answer key 

### 5.15.28 Page Replacement: GATE IT 2007 | Question: 58

A demand paging system takes 100 time units to service a page fault and 300 time units to replace a dirty page. Memory access time is 1 time unit. The probability of a page fault is  $p$ . In case of a page fault, the probability of page being dirty is also  $p$ . It is observed that the average access time is 3 time units. Then the value of  $p$  is

- A. 0.194      B. 0.233      C. 0.514      D. 0.981

gateit-2007 operating-system page-replacement probability normal

Answer key 

### 5.15.29 Page Replacement: GATE IT 2008 | Question: 41

Assume that a main memory with only 4 pages, each of 16 bytes, is initially empty. The CPU generates the following sequence of virtual addresses and uses the Least Recently Used (LRU) page replacement policy.

0, 4, 8, 20, 24, 36, 44, 12, 68, 72, 80, 84, 28, 32, 88, 92

How many page faults does this sequence cause? What are the page numbers of the pages present in the main memory at the end of the sequence?

- A. 6 and 1,2,3,4      B. 7 and 1,2,4,5      C. 8 and 1,2,4,5      D. 9 and 1,2,3,5

gateit-2008 operating-system page-replacement normal

Answer key 

## 5.16

### Paging (1)

#### 5.16.1 Paging: GATE CSE 1997 | Question: 3.10, ISRO2008-57, ISRO2015-64



Dirty bit for a page in a page table

- A. helps avoid unnecessary writes on a paging device  
B. helps maintain LRU information  
C. allows only read on a page  
D. None of the above

gate1997 operating-system paging easy isro2008 isro2015

Answer key 

## 5.17

### Precedence Graph (3)

#### 5.17.1 Precedence Graph: GATE CSE 1989 | Question: 11b



Consider the following precedence graph (Fig.6) of processes where a node denotes a process and a directed edge from node  $P_i$  to node  $P_j$  implies; that  $P_i$  must complete before  $P_j$  commences. Implement

the graph using FORK and JOIN constructs. The actual computation done by a process may be indicated by a comment line.

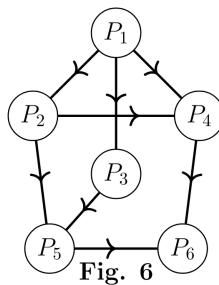


Fig. 6

gate1989 descriptive operating-system precedence-graph process-synchronization

Answer key

### 5.17.2 Precedence Graph: GATE CSE 1991 | Question: 01-xii



A given set of processes can be implemented by using only **parbegin/parend** statement, if the precedence graph of these processes is \_\_\_\_\_

gate1991 operating-system normal precedence-graph fill-in-the-blanks

Answer key

### 5.17.3 Precedence Graph: GATE CSE 1992 | Question: 12-a



Draw the precedence graph for the concurrent program given below

```
S1
parbegin
    begin
        S2:S4
    end;
    begin
        S3;
    parbegin
        S5;
        begin
            S6:S8
        end
    parend
    end;
    S7
parend;
S9
```

gate1992 operating-system normal concurrency precedence-graph descriptive

Answer key

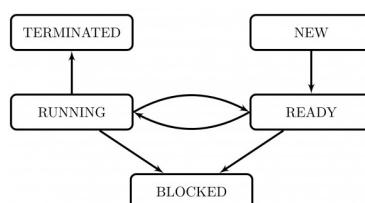
## 5.18

### Process (4)



### 5.18.1 Process: GATE CSE 1996 | Question: 1.18

The process state transition diagram in the below figure is representative of



- A. a batch operating system
- B. an operating system with a preemptive scheduler

- C. an operating system with a non-preemptive scheduler  
 D. a uni-programmed operating system

gate1996 operating-system normal process

[Answer key](#)

#### 5.18.2 Process: GATE CSE 2001 | Question: 2.20 [top](#)



Which of the following does not interrupt a running process?

- A. A device      B. Timer      C. Scheduler process    D. Power failure

gatecse-2001 operating-system easy process

[Answer key](#)

#### 5.18.3 Process: GATE CSE 2002 | Question: 2.21 [top](#)



Which combination of the following features will suffice to characterize an OS as a multi-programmed OS?

- a. More than one program may be loaded into main memory at the same time for execution  
 b. If a program waits for certain events such as I/O, another program is immediately scheduled for execution  
 c. If the execution of a program terminates, another program is immediately scheduled for execution.

- A. (a)      B. (a) and (b)      C. (a) and (c)      D. (a), (b) and (c)

gatecse-2002 operating-system normal process

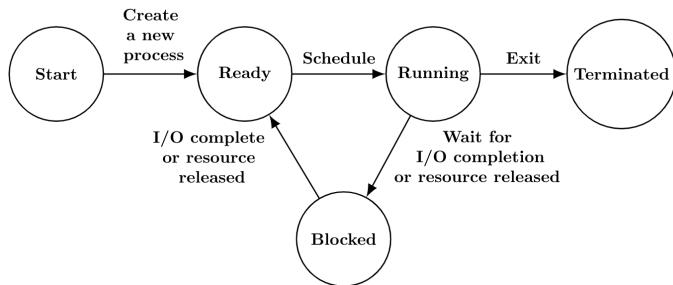
[Answer key](#)

#### 5.18.4 Process: GATE IT 2006 | Question: 13 [top](#)



The process state transition diagram of an operating system is as given below.

Which of the following must be FALSE about the above operating system?



- A. It is a multiprogrammed operating system  
 B. It uses preemptive scheduling  
 C. It uses non-preemptive scheduling  
 D. It is a multi-user operating system

gateit-2006 operating-system normal process

[Answer key](#)

### 5.19

#### Process And Threads (1) [top](#)



#### 5.19.1 Process And Threads: GATE CSE 2023 | Question: 12 [top](#)

Which one or more of the following need to be saved on a context switch from one thread ( $T_1$ ) of a process to another thread ( $T_2$ ) of the same process?

- A. Page table base register  
 B. Stack pointer  
 C. Program counter  
 D. General purpose registers

gatecse-2023 operating-system process-and-threads multiple-selects 1-mark

[Answer key](#)

### 5.20

#### Process Scheduling (44) [top](#)

### 5.20.1 Process Scheduling: GATE CSE 1988 | Question: 2xa top



State any undesirable characteristic of the following criteria for measuring performance of an operating system:

#### Turn around time

gate1988 normal descriptive operating-system process-scheduling

[Answer key](#)

### 5.20.2 Process Scheduling: GATE CSE 1988 | Question: 2xb top



State any undesirable characteristic of the following criteria for measuring performance of an operating system:

#### Waiting time

gate1988 normal descriptive operating-system process-scheduling

[Answer key](#)

### 5.20.3 Process Scheduling: GATE CSE 1990 | Question: 1-vi top



The highest-response ratio next scheduling policy favours \_\_\_\_\_ jobs, but it also limits the waiting time of \_\_\_\_\_ jobs.

gate1990 operating-system process-scheduling fill-in-the-blanks

[Answer key](#)

### 5.20.4 Process Scheduling: GATE CSE 1993 | Question: 7.10 top



Assume that the following jobs are to be executed on a single processor system

Job Id	CPU Burst Time
p	4
q	1
r	8
s	1
t	2

The jobs are assumed to have arrived at time  $0^+$  and in the order  $p, q, r, s, t$ . Calculate the departure time (completion time) for job  $p$  if scheduling is round robin with time slice 1

- A. 4      B. 10      C. 11      D. 12      E. None of the above

gate1993 operating-system process-scheduling normal

[Answer key](#)

### 5.20.5 Process Scheduling: GATE CSE 1995 | Question: 1.15 top



Which scheduling policy is most suitable for a time shared operating system?

- A. Shortest Job First      B. Round Robin  
C. First Come First Serve      D. Elevator

gate1995 operating-system process-scheduling easy

[Answer key](#)

### 5.20.6 Process Scheduling: GATE CSE 1995 | Question: 2.6 top



The sequence \_\_\_\_\_ is an optimal non-preemptive scheduling sequence for the following jobs which leaves the CPU idle for \_\_\_\_\_ unit(s) of time.

Job	Arrival Time	Burst Time
1	0.0	9
2	0.6	5
3	1.0	1

- A. {3,2,1},1      B. {2,1,3},0      C. {3,2,1},0      D. {1,2,3},5

gate1995 operating-system process-scheduling normal

[Answer key](#)

#### 5.20.7 Process Scheduling: GATE CSE 1996 | Question: 2.20, ISRO2008-15 [top](#)

Four jobs to be executed on a single processor system arrive at time 0 in the order  $A, B, C, D$ . Their burst CPU time requirements are 4, 1, 8, 1 time units respectively. The completion time of  $A$  under round robin scheduling with time slice of one time unit is

- A. 10      B. 4      C. 8      D. 9

gate1996 operating-system process-scheduling normal isro2008

[Answer key](#)

#### 5.20.8 Process Scheduling: GATE CSE 1998 | Question: 2.17, UGCNET-Dec2012-III: 43 [top](#)

Consider  $n$  processes sharing the CPU in a round-robin fashion. Assuming that each process switch takes  $s$  seconds, what must be the quantum size  $q$  such that the overhead resulting from process switching is minimized but at the same time each process is guaranteed to get its turn at the CPU at least every  $t$  seconds?

- A.  $q \leq \frac{t-ns}{n-1}$   
 C.  $q \leq \frac{t-ns}{n+1}$
- B.  $q \geq \frac{t-ns}{n-1}$   
 D.  $q \geq \frac{t-ns}{n+1}$

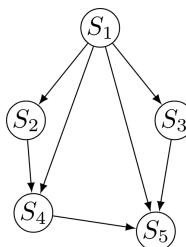
gate1998 operating-system process-scheduling normal ugcnetcse-dec2012-paper3

[Answer key](#)

#### 5.20.9 Process Scheduling: GATE CSE 1998 | Question: 24 [top](#)

a. Four jobs are waiting to be run. Their expected run times are 6, 3, 5 and  $x$ . In what order should they be run to minimize the average response time?

b. Write a concurrent program using `par begin-par end` to represent the precedence graph shown below.



gate1998 operating-system process-scheduling descriptive

[Answer key](#)

#### 5.20.10 Process Scheduling: GATE CSE 1998 | Question: 7-b [top](#)

In a computer system where the 'best-fit' algorithm is used for allocating 'jobs' to 'memory partitions', the following situation was encountered:

<b>Partitions size in KB</b>	4K 8K 20K 2K
<b>Job sizes in KB</b>	2K 14K 3K 6K 6K 10K 20K 2K
<b>Time for execution</b>	4 10 2 1 4 1 8 6

When will the  $20K$  job complete?

gate1998 operating-system process-scheduling normal

Answer key 

#### 5.20.11 Process Scheduling: GATE CSE 2002 | Question: 1.22

Which of the following scheduling algorithms is non-preemptive?

- A. Round Robin
- B. First-In First-Out
- C. Multilevel Queue Scheduling
- D. Multilevel Queue Scheduling with Feedback

gatecse-2002 operating-system process-scheduling easy

Answer key 

#### 5.20.12 Process Scheduling: GATE CSE 2003 | Question: 77

A uni-processor computer system only has two processes, both of which alternate  $10\text{ ms}$  CPU bursts with  $90\text{ ms}$  I/O bursts. Both the processes were created at nearly the same time. The I/O of both processes can proceed in parallel. Which of the following scheduling strategies will result in the *least* CPU utilization (over a long period of time) for this system?

- A. First come first served scheduling
- B. Shortest remaining time first scheduling
- C. Static priority scheduling with different priorities for the two processes
- D. Round robin scheduling with a time quantum of  $5\text{ ms}$

gatecse-2003 operating-system process-scheduling normal

Answer key 

#### 5.20.13 Process Scheduling: GATE CSE 2004 | Question: 46

Consider the following set of processes, with the arrival times and the CPU-burst times given in milliseconds.

Process	Arrival Time	Burst Time
P1	0	5
P2	1	3
P3	2	3
P4	4	1

What is the average turnaround time for these processes with the preemptive shortest remaining processing time first (SRPT) algorithm?

- A. 5.50
- B. 5.75
- C. 6.00
- D. 6.25

gatecse-2004 operating-system process-scheduling normal

Answer key 

#### 5.20.14 Process Scheduling: GATE CSE 2006 | Question: 06, ISRO2009-14

Consider three CPU-intensive processes, which require 10, 20 and 30 time units and arrive at times 0, 2 and 6, respectively. How many context switches are needed if the operating system implements a shortest remaining time first scheduling algorithm? Do not count the context switches at time zero and at the end.

- A. 1
- B. 2
- C. 3
- D. 4

gatecse-2006 operating-system process-scheduling normal isro2009

Answer key 

#### 5.20.15 Process Scheduling: GATE CSE 2006 | Question: 64

Consider three processes (process id 0, 1, 2 respectively) with compute time bursts 2, 4 and 8 time units. All

processes arrive at time zero. Consider the longest remaining time first (LRTF) scheduling algorithm. In LRTF ties are broken by giving priority to the process with the lowest process id. The average turn around time is:

- A. 13 units      B. 14 units      C. 15 units      D. 16 units

gatecse-2006 operating-system process-scheduling normal

Answer key 

#### 5.20.16 Process Scheduling: GATE CSE 2006 | Question: 65

Consider three processes, all arriving at time zero, with total execution time of 10, 20 and 30 units, respectively. Each process spends the first 20% of execution time doing I/O, the next 70% of time doing computation, and the last 10% of time doing I/O again. The operating system uses a shortest remaining compute time first scheduling algorithm and schedules a new process either when the running process gets blocked on I/O or when the running process finishes its compute burst. Assume that all I/O operations can be overlapped as much as possible. For what percentage of time does the CPU remain idle?

- A. 0%      B. 10.6%      C. 30.0%      D. 89.4%

gatecse-2006 operating-system process-scheduling normal

Answer key 

#### 5.20.17 Process Scheduling: GATE CSE 2007 | Question: 16

Group 1 contains some CPU scheduling algorithms and Group 2 contains some applications. Match entries in Group 1 to entries in Group 2.

Group I	Group II
(P) Gang Scheduling	(1) Guaranteed Scheduling
(Q) Rate Monotonic Scheduling	(2) Real-time Scheduling
(R) Fair Share Scheduling	(3) Thread Scheduling

- A. P – 3; Q – 2; R – B. P – 1; Q – 2; R – C. P – 2; Q – 3; R – D. P – 1; Q – 3; R – 2

gatecse-2007 operating-system process-scheduling normal

Answer key 

#### 5.20.18 Process Scheduling: GATE CSE 2007 | Question: 55

An operating system used Shortest Remaining System Time first (SRT) process scheduling algorithm. Consider the arrival times and execution times for the following processes:

Process	Execution Time	Arrival Time
P1	20	0
P2	25	15
P3	10	30
P4	15	45

What is the total waiting time for process P2 ?

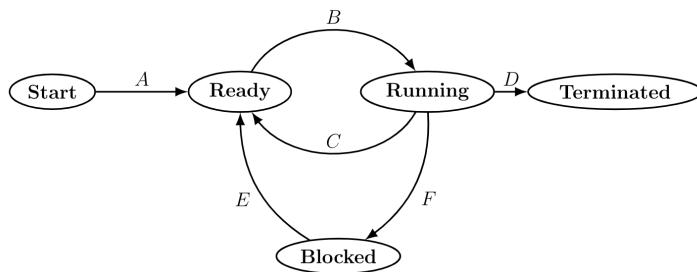
- A. 5      B. 15      C. 40      D. 55

gatecse-2007 operating-system process-scheduling normal

Answer key 

#### 5.20.19 Process Scheduling: GATE CSE 2009 | Question: 32

In the following process state transition diagram for a uniprocessor system, assume that there are always some processes in the ready state:



Now consider the following statements:

- I. If a process makes a transition  $D$ , it would result in another process making transition  $A$  immediately.
- II. A process  $P_2$  in blocked state can make transition  $E$  while another process  $P_1$  is in running state.
- III. The OS uses preemptive scheduling.
- IV. The OS uses non-preemptive scheduling.

Which of the above statements are TRUE?

- A. I and II      B. I and III      C. II and III      D. II and IV

gatecse-2009 operating-system process-scheduling normal

[Answer key](#)



#### 5.20.20 Process Scheduling: GATE CSE 2010 | Question: 25 top

Which of the following statements are true?

- I. Shortest remaining time first scheduling may cause starvation
  - II. Preemptive scheduling may cause starvation
  - III. Round robin is better than FCFS in terms of response time
- A. I only      B. I and III only      C. II and III only      D. I, II and III

gatecse-2010 operating-system process-scheduling easy

[Answer key](#)



#### 5.20.21 Process Scheduling: GATE CSE 2011 | Question: 35 top

Consider the following table of arrival time and burst time for three processes  $P_0$ ,  $P_1$  and  $P_2$ .

Process	Arrival Time	Burst Time
$P_0$	0 ms	9
$P_1$	1 ms	4
$P_2$	2 ms	9

The pre-emptive shortest job first scheduling algorithm is used. Scheduling is carried out only at arrival or completion of processes. What is the average waiting time for the three processes?

- A. 5.0 ms      B. 4.33 ms      C. 6.33 ms      D. 7.33 ms

gatecse-2011 operating-system process-scheduling normal

[Answer key](#)



#### 5.20.22 Process Scheduling: GATE CSE 2012 | Question: 31 top

Consider the 3 processes,  $P_1$ ,  $P_2$  and  $P_3$  shown in the table.

Process	Arrival Time	Time Units Required
$P_1$	0	5
$P_2$	1	7
$P_3$	3	4

The completion order of the 3 processes under the policies FCFS and RR2 (round robin scheduling with CPU quantum of 2 time units) are

- A. **FCFS:**  $P_1, P_2, P_3$  **RR2:**  $P_1, P_2, P_3$
- B. **FCFS:**  $P_1, P_3, P_2$  **RR2:**  $P_1, P_3, P_2$
- C. **FCFS:**  $P_1, P_2, P_3$  **RR2:**  $P_1, P_3, P_2$
- D. **FCFS:**  $P_1, P_3, P_2$  **RR2:**  $P_1, P_2, P_3$

gatecse-2012 operating-system process-scheduling normal

[Answer key](#)

#### 5.20.23 Process Scheduling: GATE CSE 2013 | Question: 10 [top](#)

A scheduling algorithm assigns priority proportional to the waiting time of a process. Every process starts with zero (the lowest priority). The scheduler re-evaluates the process priorities every  $T$  time units and decides the next process to schedule. Which one of the following is **TRUE** if the processes have no I/O operations and all arrive at time zero?

- A. This algorithm is equivalent to the first-come-first-serve algorithm.
- B. This algorithm is equivalent to the round-robin algorithm.
- C. This algorithm is equivalent to the shortest-job-first algorithm.
- D. This algorithm is equivalent to the shortest-remaining-time-first algorithm.

gatecse-2013 operating-system process-scheduling normal

[Answer key](#)

#### 5.20.24 Process Scheduling: GATE CSE 2014 Set 1 | Question: 32 [top](#)

Consider the following set of processes that need to be scheduled on a single CPU. All the times are given in milliseconds.

Process Name	Arrival Time	Execution Time
A	0	6
B	3	2
C	5	4
D	7	6
E	10	3

Using the *shortest remaining time first* scheduling algorithm, the average process turnaround time (in msec) is \_\_\_\_\_.

gatecse-2014-set1 operating-system process-scheduling numerical-answers normal

[Answer key](#)

#### 5.20.25 Process Scheduling: GATE CSE 2014 Set 2 | Question: 32 [top](#)

Three processes  $A$ ,  $B$  and  $C$  each execute a loop of 100 iterations. In each iteration of the loop, a process performs a single computation that requires  $t_c$  CPU milliseconds and then initiates a single I/O operation that lasts for  $t_{io}$  milliseconds. It is assumed that the computer where the processes execute has sufficient number of I/O devices and the OS of the computer assigns different I/O devices to each process. Also, the scheduling overhead of the OS is negligible. The processes have the following characteristics:

Process id	$t_c$	$t_{io}$
A	100 ms	500 ms
B	350 ms	500 ms
C	200 ms	500 ms

The processes  $A$ ,  $B$ , and  $C$  are started at times 0, 5 and 10 milliseconds respectively, in a pure time sharing

system (round robin scheduling) that uses a time slice of 50 milliseconds. The time in milliseconds at which process C would **complete** its first I/O operation is \_\_\_\_\_.

gatecse-2014-set2 operating-system process-scheduling numerical-answers normal

Answer key 

#### 5.20.26 Process Scheduling: GATE CSE 2014 Set 3 | Question: 32

An operating system uses *shortest remaining time first* scheduling algorithm for pre-emptive scheduling of processes. Consider the following set of processes with their arrival times and CPU burst times (in milliseconds):

Process	Arrival Time	Burst Time
P1	0	12
P2	2	4
P3	3	6
P4	8	5

The average waiting time (in milliseconds) of the processes is \_\_\_\_\_.

gatecse-2014-set3 operating-system process-scheduling numerical-answers normal

Answer key 

#### 5.20.27 Process Scheduling: GATE CSE 2015 Set 1 | Question: 46

Consider a uniprocessor system executing three tasks  $T_1, T_2$  and  $T_3$  each of which is composed of an infinite sequence of jobs (or instances) which arrive periodically at intervals of 3, 7 and 20 milliseconds, respectively. The priority of each task is the inverse of its period, and the available tasks are scheduled in order of priority, which is the highest priority task scheduled first. Each instance of  $T_1, T_2$  and  $T_3$  requires an execution time of 1, 2 and 4 milliseconds, respectively. Given that all tasks initially arrive at the beginning of the 1<sup>st</sup> millisecond and task preemptions are allowed, the first instance of  $T_3$  completes its execution at the end of \_\_\_\_\_ milliseconds.

gatecse-2015-set1 operating-system process-scheduling normal numerical-answers

Answer key 

#### 5.20.28 Process Scheduling: GATE CSE 2015 Set 3 | Question: 1

The maximum number of processes that can be in *Ready* state for a computer system with  $n$  CPUs is :

- A.  $n$       B.  $n^2$       C.  $2^n$       D. Independent of  $n$

gatecse-2015-set3 operating-system process-scheduling easy

Answer key 

#### 5.20.29 Process Scheduling: GATE CSE 2015 Set 3 | Question: 34

For the processes listed in the following table, which of the following scheduling schemes will give the lowest average turnaround time?

Process	Arrival Time	Process Time
A	0	3
B	1	6
C	4	4
D	6	2

- A. First Come First Serve  
C. Shortest Remaining Time  
B. Non-preemptive Shortest job first  
D. Round Robin with Quantum value two

gatecse-2015-set3 operating-system process-scheduling normal

[Answer key](#)

### 5.20.30 Process Scheduling: GATE CSE 2016 Set 1 | Question: 20 top



Consider an arbitrary set of CPU-bound processes with unequal CPU burst lengths submitted at the same time to a computer system. Which one of the following process scheduling algorithms would minimize the average waiting time in the ready queue?

- A. Shortest remaining time first
- B. Round-robin with the time quantum less than the shortest CPU burst
- C. Uniform random
- D. Highest priority first with priority proportional to CPU burst length

gatecse-2016-set1 operating-system process-scheduling normal

[Answer key](#)

### 5.20.31 Process Scheduling: GATE CSE 2016 Set 2 | Question: 47 top



Consider the following processes, with the arrival time and the length of the CPU burst given in milliseconds. The scheduling algorithm used is preemptive shortest remaining-time first.

Process	Arrival Time	Burst Time
$P_1$	0	10
$P_2$	3	6
$P_3$	7	1
$P_4$	8	3

The average turn around time of these processes is \_\_\_\_\_ milliseconds.

gatecse-2016-set2 operating-system process-scheduling normal numerical-answers

[Answer key](#)

### 5.20.32 Process Scheduling: GATE CSE 2017 Set 1 | Question: 24 top



Consider the following CPU processes with arrival times (in milliseconds) and length of CPU bursts (in milliseconds) as given below:

Process	Arrival Time	Burst Time
$P_1$	0	7
$P_2$	3	3
$P_3$	5	5
$P_4$	6	2

If the pre-emptive shortest remaining time first scheduling algorithm is used to schedule the processes, then the average waiting time across all processes is \_\_\_\_\_ milliseconds.

gatecse-2017-set1 operating-system process-scheduling numerical-answers

[Answer key](#)

### 5.20.33 Process Scheduling: GATE CSE 2017 Set 2 | Question: 51 top



Consider the set of process with arrival time (in milliseconds), CPU burst time (in milliseconds) and priority (0 is the highest priority) shown below. None of the process have I/O burst time

Process	Arrival Time	Burst Time	Priority
$P_1$	0	11	2
$P_2$	5	28	0
$P_3$	12	2	3
$P_4$	2	10	1
$P_5$	9	16	4

The average waiting time (in milli seconds) of all the process using preemptive priority scheduling algorithm is \_\_\_\_\_

gatecse-2017-set2 operating-system process-scheduling numerical-answers

Answer key 

#### 5.20.34 Process Scheduling: GATE CSE 2019 | Question: 41

Consider the following four processes with arrival times (in milliseconds) and their length of CPU bursts (in milliseconds) as shown below:

Process	P1	P2	P3	P4
Arrival Time	0	1	3	4
CPU burst time	3	1	3	Z

These processes are run on a single processor using preemptive Shortest Remaining Time First scheduling algorithm. If the average waiting time of the processes is 1 millisecond, then the value of Z is \_\_\_\_\_

gatecse-2019 numerical-answers operating-system process-scheduling 2-marks

Answer key 

#### 5.20.35 Process Scheduling: GATE CSE 2020 | Question: 12

Consider the following statements about process state transitions for a system using preemptive scheduling.

- I. A running process can move to ready state.
- II. A ready process can move to running state.
- III. A blocked process can move to running state.
- IV. A blocked process can move to ready state.

Which of the above statements are TRUE?

- A. I, II, and III only
- B. II and III only
- C. I, II, and IV only
- D. I, II, III and IV only

gatecse-2020 operating-system process-scheduling 1-mark

Answer key 

#### 5.20.36 Process Scheduling: GATE CSE 2020 | Question: 50

Consider the following set of processes, assumed to have arrived at time 0. Consider the CPU scheduling algorithms Shortest Job First (SJF) and Round Robin (RR). For RR, assume that the processes are scheduled in the order  $P_1, P_2, P_3, P_4$ .

Processes	P1	P2	P3	P4
Burst time (in ms)	8	7	2	4

If the time quantum for RR is 4 ms, then the absolute value of the difference between the average turnaround times (in ms) of SJF and RR (round off to 2 decimal places is \_\_\_\_\_)

gatecse-2020 numerical-answers operating-system process-scheduling 2-marks

Answer key 

#### 5.20.37 Process Scheduling: GATE CSE 2021 Set 1 | Question: 25

Three processes arrive at time zero with CPU bursts of 16, 20 and 10 milliseconds. If the scheduler has prior knowledge about the length of the CPU bursts, the minimum achievable average waiting time for these three processes in a non-preemptive scheduler (rounded to nearest integer) is \_\_\_\_\_ milliseconds.

gatecse-2021-set1 operating-system process-scheduling numerical-answers 1-mark

Answer key 

### 5.20.38 Process Scheduling: GATE CSE 2021 Set 2 | Question: 14 top



Which of the following statement(s) is/are correct in the context of CPU scheduling?

- A. Turnaround time includes waiting time
- B. The goal is to only maximize CPU utilization and minimize throughput
- C. Round-robin policy can be used even when the CPU time required by each of the processes is not known apriori
- D. Implementing preemptive scheduling needs hardware support

gatecse-2021-set2 multiple-selects operating-system process-scheduling 1-mark

Answer key

### 5.20.39 Process Scheduling: GATE CSE 2023 | Question: 17 top



Which one or more of the following CPU scheduling algorithms can potentially cause starvation?

- A. First-in First-Out
- B. Round Robin
- C. Priority Scheduling
- D. Shortest Job First

gatecse-2023 operating-system process-scheduling multiple-selects 1-mark

Answer key

### 5.20.40 Process Scheduling: GATE IT 2005 | Question: 60 top



We wish to schedule three processes  $P_1$ ,  $P_2$  and  $P_3$  on a uniprocessor system. The priorities, CPU time requirements and arrival times of the processes are as shown below.

Process	Priority	CPU time required	Arrival time (hh:mm:ss)
$P_1$	10 (highest)	20 sec	00 : 00 : 05
$P_2$	9	10 sec	00 : 00 : 03
$P_3$	8 (lowest)	15 sec	00 : 00 : 00

We have a choice of preemptive or non-preemptive scheduling. In preemptive scheduling, a late-arriving higher priority process can preempt a currently running process with lower priority. In non-preemptive scheduling, a late-arriving higher priority process must wait for the currently executing process to complete before it can be scheduled on the processor.

What are the turnaround times (time from arrival till completion) of  $P_2$  using preemptive and non-preemptive scheduling respectively?

- A. 30 sec, 30 sec
- B. 30 sec, 10 sec
- C. 42 sec, 42 sec
- D. 30 sec, 42 sec

gateit-2005 operating-system process-scheduling normal

Answer key

### 5.20.41 Process Scheduling: GATE IT 2006 | Question: 12 top



In the working-set strategy, which of the following is done by the operating system to prevent thrashing?

- I. It initiates another process if there are enough extra frames.
- II. It selects a process to suspend if the sum of the sizes of the working-sets exceeds the total number of available frames.

- A. I only
- B. II only
- C. Neither I nor II
- D. Both I and II

gateit-2006 operating-system process-scheduling normal

Answer key

### 5.20.42 Process Scheduling: GATE IT 2006 | Question: 54 top



The arrival time, priority, and duration of the CPU and I/O bursts for each of three processes  $P_1$ ,  $P_2$  and

$P_3$  are given in the table below. Each process has a CPU burst followed by an I/O burst followed by another CPU burst. Assume that each process has its own I/O resource.

Process	Arrival Time	Priority	Burst duration (CPU)	Burst duration (I/O)	Burst duration (CPU)
$P_1$	0	2	1	5	3
$P_2$	2	3 (lowest)	3	3	1
$P_3$	3	1 (highest)	2	3	1

The multi-programmed operating system uses preemptive priority scheduling. What are the finish times of the processes  $P_1$ ,  $P_2$  and  $P_3$ ?

- A. 11, 15, 9      B. 10, 15, 9      C. 11, 16, 10      D. 12, 17, 11

gateit-2006 operating-system process-scheduling normal

[Answer key](#)

#### 5.20.43 Process Scheduling: GATE IT 2007 | Question: 26 [top](#)

Consider  $n$  jobs  $J_1, J_2 \dots J_n$  such that job  $J_i$  has execution time  $t_i$  and a non-negative integer weight  $w_i$ . The weighted mean completion time of the jobs is defined to be  $\frac{\sum_{i=1}^n w_i T_i}{\sum_{i=1}^n w_i}$ , where  $T_i$  is the completion time of job  $J_i$ . Assuming that there is only one processor available, in what order must the jobs be executed in order to minimize the weighted mean completion time of the jobs?

- A. Non-decreasing order of  $t_i$   
 C. Non-increasing order of  $w_i t_i$   
 B. Non-increasing order of  $w_i$   
 D. Non-increasing order of  $w_i/t_i$

gateit-2007 operating-system process-scheduling normal

[Answer key](#)

#### 5.20.44 Process Scheduling: GATE IT 2008 | Question: 55 [top](#)

If the time-slice used in the round-robin scheduling policy is more than the maximum time required to execute any process, then the policy will

- A. degenerate to shortest job first  
 C. degenerate to first come first serve  
 B. degenerate to priority scheduling  
 D. none of the above

gateit-2008 operating-system process-scheduling easy

[Answer key](#)

### 5.21

#### Process Synchronization (52) [top](#)

##### 5.21.1 Process Synchronization: GATE CSE 1987 | Question: 1-xvi [top](#)

A critical region is

- A. One which is enclosed by a pair of  $P$  and  $V$  operations on semaphores.  
 B. A program segment that has not been proved bug-free.  
 C. A program segment that often causes unexpected system crashes.  
 D. A program segment where shared resources are accessed.

gate1987 operating-system process-synchronization

[Answer key](#)

##### 5.21.2 Process Synchronization: GATE CSE 1987 | Question: 8a [top](#)

Consider the following proposal to the "readers and writers problem."

Shared variables and semaphores:

```
aw, ar, rw, rr : integer;
mutex, reading, writing: semaphore;
initial values of variables and states of semaphores:
ar=rr=aw=rw=0
```

```

reading_value = writing_value = 0
mutex_value = 1.          Process writer;
Process reader;           begin
begin                      while true do
repeat                     begin
  P(mutex);
  ar := ar+1;
  grantread;
  V(mutex);
  P(reading);
  read;
  P(mutex);
  rr := rr - 1;
  ar := ar - 1;
  grantwrite;
  V(mutex);
  other-work;
until false               end
end.                      end.

Procedure grantread;
begin
  if aw = 0
  then while (rr < ar) do
    begin rr := rr + 1;
    V (reading)
    end
  end
end;
Procedure grantwrite;
begin
  if rr = 0
  then while (rw < aw) do
    begin rw := rw + 1;
    V (writing)
    end
  end
end;

```

- Give the value of the shared variables and the states of semaphores when 12 readers are reading and writers are writing.
- Can a group of readers make waiting writers starve? Can writers starve readers?
- Explain in two sentences why the solution is incorrect.

gate1987 operating-system process-synchronization descriptive

**Answer key**

### 5.21.3 Process Synchronization: GATE CSE 1988 | Question: 10iib



Given below is solution for the critical section problem of two processes  $P_0$  and  $P_1$  sharing the following variables:

```

var flag :array [0..1] of boolean; (initially false)
turn: 0 .. 1;

```

The program below is for process  $P_i$  ( $i = 0$  or  $1$ ) where process  $P_j$  ( $j = 1$  or  $0$ ) being the other one.

```

repeat
  flag[i]:= true;
  while turn != i
  do begin
    while flag [j] do skip
    turn:=i;
  end

  critical section

  flag[i]:=false;
until false

```

Determine of the above solution is correct. If it is incorrect, demonstrate with an example how it violates the conditions.

gate1988 descriptive operating-system process-synchronization

**Answer key**

#### 5.21.4 Process Synchronization: GATE CSE 1990 | Question: 2-iii



Match the pairs:

(a)	Critical region	(p)	Hoare's monitor
(b)	Wait/Signal	(q)	Mutual exclusion
(c)	Working Set	(r)	Principle of locality
(d)	Deadlock	(s)	Circular Wait

match-the-following gate1990 operating-system process-synchronization

Answer key

#### 5.21.5 Process Synchronization: GATE CSE 1991 | Question: 11,a



Consider the following scheme for implementing a critical section in a situation with three processes  $P_i, P_j$  and  $P_k$ .

```
Pi;
repeat
    flag[i] := true;
    while flag[j] or flag[k] do
        case turn of
            j: if flag [j] then
                begin
                    flag [i] := false;
                    while turn != i do skip;
                    flag [i] := true;
                end;
            k: if flag [k] then
                begin
                    flag [i] := false;
                    while turn != i do skip;
                    flag [i] := true
                end
        end
    critical section
    if turn = i then turn := j;
    flag [j] := false
non-critical section
until false;
```

- a. Does the scheme ensure mutual exclusion in the critical section? Briefly explain.

gate1991 process-synchronization normal operating-system descriptive

Answer key

#### 5.21.6 Process Synchronization: GATE CSE 1991 | Question: 11,b



Consider the following scheme for implementing a critical section in a situation with three processes  $P_i, P_j$  and  $P_k$ .

Pi;

```
repeat
    flag[i] := true;
    while flag[j] or flag[k] do
        case turn of
            j: if flag [j] then
                begin
                    flag [i] := false;
                    while turn != i do skip;
                    flag [i] := true;
                end;
            k: if flag [k] then
                begin
                    flag [i] := false;
                    while turn != i do skip;
                    flag [i] := true
                end
        end
    end
```

```

critical section
if turn = i then turn := j;
flag [i] := false
non-critical section
until false;

```

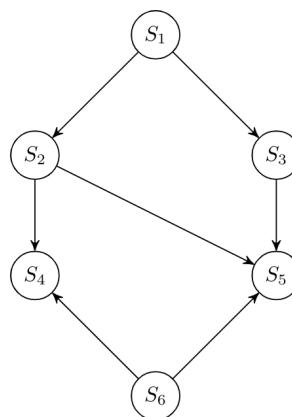
Is there a situation in which a waiting process can never enter the critical section? If so, explain and suggest modifications to the code to solve this problem

gate1991 process-synchronization normal operating-system descriptive

[Answer key](#)

### 5.21.7 Process Synchronization: GATE CSE 1993 | Question: 22 [top](#)

Write a concurrent program using parbegin-parend and semaphores to represent the precedence constraints of the statements  $S_1$  to  $S_6$ , as shown in figure below.



gate1993 operating-system process-synchronization normal descriptive

[Answer key](#)

### 5.21.8 Process Synchronization: GATE CSE 1994 | Question: 27 [top](#)

A. Draw a precedence graph for the following sequential code. The statements are numbered from  $S_1$  to  $S_6$

```

S1      read n
S2      i := 1
S3      if i > n next
S4      a(i) := i+1
S5      i := i+1
S6      next : write a(i)

```

B. Can this graph be converted to a concurrent program using parbegin-parend construct only?

gate1994 operating-system process-synchronization normal descriptive

[Answer key](#)

### 5.21.9 Process Synchronization: GATE CSE 1995 | Question: 19 [top](#)

Consider the following program segment for concurrent processing using semaphore operators  $P$  and  $V$  for synchronization. Draw the precedence graph for the statements  $S_1$  to  $S_9$ .

```

var
a,b,c,d,e,f,g,h,i,j,k : semaphore;
begin
cobegin
begin S1; V(b); V(b) end;
begin P(a); S2; V(c); V(d) end;
begin P(c); S4; V(e) end;
begin P(d); S5; V(f) end;
begin P(e); P(f); S7; V(k) end

```

```

begin P(b); S3; V(g); V(h) end;
begin P(g); S6; V(i) end;
begin P(h); P(i); S8; V(j) end;
begin P(j); P(k); S9 end;
coend
end;

```

gate1995 operating-system process-synchronization normal descriptive

[Answer key](#)

### 5.21.10 Process Synchronization: GATE CSE 1996 | Question: 1.19, ISRO2008-61 [top](#)



A critical section is a program segment

- A. which should run in a certain amount of time
- B. which avoids deadlocks
- C. where shared resources are accessed
- D. which must be enclosed by a pair of semaphore operations,  $P$  and  $V$

gate1996 operating-system process-synchronization easy isro2008

[Answer key](#)

### 5.21.11 Process Synchronization: GATE CSE 1996 | Question: 2.19 [top](#)



A solution to the Dining Philosophers Problem which avoids deadlock is to

- A. ensure that all philosophers pick up the left fork before the right fork
- B. ensure that all philosophers pick up the right fork before the left fork
- C. ensure that one particular philosopher picks up the left fork before the right fork, and that all other philosophers pick up the right fork before the left fork
- D. None of the above

gate1996 operating-system process-synchronization normal

[Answer key](#)

### 5.21.12 Process Synchronization: GATE CSE 1996 | Question: 21 [top](#)



The concurrent programming constructs fork and join are as below:

Fork <label> which creates a new process executing from the specified label

Join <variable> which decrements the specified synchronization variable (by 1) and terminates the process if the new value is not 0.

Show the precedence graph for  $S1, S2, S3, S4$ , and  $S5$  of the concurrent program below.

```

N = 2
M = 2
Fork L3
Fork L4
S1
L1 : join N
S3
L2 : join M
S5
L3 : S2
Goto L1
L4 : S4
Goto L2
Next:

```

**Answer key****5.21.13 Process Synchronization: GATE CSE 1997 | Question: 6.8**

Each Process  $P_i, i = 1 \dots 9$  is coded as follows

```
repeat
  P(mutex)
  {Critical section}
  V(mutex)
forever
```

The code for  $P_{10}$  is identical except it uses V(mutex) in place of P(mutex). What is the largest number of processes that can be inside the critical section at any moment?

- A. 1      B. 2      C. 3      D. None

**Answer key****5.21.14 Process Synchronization: GATE CSE 1997 | Question: 73**

A concurrent system consists of 3 processes using a shared resource  $R$  in a non-preemptible and mutually exclusive manner. The processes have unique priorities in the range  $1 \dots 3$ , 3 being the highest priority. It is required to synchronize the processes such that the resource is always allocated to the highest priority requester. The pseudo code for the system is as follows.

**Shared data**

```
mutex:semaphore = 1; /* initialized to 1*/
process[3]:semaphore = 0; /*all initialized to 0 */
R_requested [3]:boolean = false; /*all initialized to false */
busy: boolean = false; /*initialized to false */
```

**Code for processes**

```
begin process
my-priority:integer;
my-priority:=____; /*in the range 1..3*/
repeat
  request_R(my-priority);
  P (proceed [my-priority]);
  {use shared resource R}
  release_R (my-priority);
forever
end process;
```

**Procedures**

```
procedure request_R(priority);
P(mutex);
if busy = true then
  R_requested [priority]:=true;
else
begin
  V(proceed [priority]);
  busy:=true;
end
V(mutex)
```

Give the pseudo code for the procedure release\_R.

**Answer key**

### 5.21.15 Process Synchronization: GATE CSE 1998 | Question: 1.30 top



When the result of a computation depends on the speed of the processes involved, there is said to be

- A. cycle stealing
- B. race condition
- C. a time lock
- D. a deadlock

gate1998 operating-system easy process-synchronization

**Answer key**

### 5.21.16 Process Synchronization: GATE CSE 1999 | Question: 20-a top



A certain processor provides a 'test and set' instruction that is used as follows:

TSET register, flag

This instruction atomically copies flag to register and sets flag to 1. Give pseudo-code for implementing the entry and exit code to a critical region using this instruction.

gate1999 operating-system process-synchronization normal descriptive

**Answer key**

### 5.21.17 Process Synchronization: GATE CSE 1999 | Question: 20-b top



Consider the following solution to the producer-consumer problem using a buffer of size 1. Assume that the initial value of count is 0. Also assume that the testing of count and assignment to count are atomic operations.

Producer:

Repeat

```
    Produce an item;  
    if count = 1 then sleep;  
    place item in buffer.  
    count = 1;  
    Wakeup(Consumer);
```

Forever

Consumer:

Repeat

```
    if count = 0 then sleep;  
    Remove item from buffer;  
    count = 0;  
    Wakeup(Producer);  
    Consume item;
```

Forever;

Show that in this solution it is possible that both the processes are sleeping at the same time.

gate1999 operating-system process-synchronization normal descriptive

**Answer key**

### 5.21.18 Process Synchronization: GATE CSE 2000 | Question: 1.21 top



Let  $m[0] \dots m[4]$  be mutexes (binary semaphores) and  $P[0] \dots P[4]$  be processes.

Suppose each process  $P[i]$  executes the following:

```
wait (m[i]); wait (m(i+1) mod 4);  
.....  
release (m[i]); release (m(i+1) mod 4);
```

This could cause

- A. Thrashing
- B. Deadlock
- C. Starvation, but not deadlock
- D. None of the above

gatecse-2000 operating-system process-synchronization normal

**Answer key**

### 5.21.19 Process Synchronization: GATE CSE 2000 | Question: 20 top



- a. Fill in the boxes below to get a solution for the reader-writer problem, using a single binary semaphore, mutex (initialized to 1) and busy waiting. Write the box numbers (1, 2 and 3), and their contents in your answer book.

```
int R = 0, W = 0;

Reader () {
L1:  wait (mutex);
  if (W == 0) {
    R = R + 1;
    □ _____(1)
  }
  else {
    □ _____(2)
    goto L1;
  }
  ..../* do the read*/
  wait (mutex);
  R = R - 1;
  signal (mutex);
}
```

```
Writer () {
L2:  wait (mutex);
  if (R == 0) { _____(3)
    signal (mutex);
    goto L2;
  }
  W=1;
  signal (mutex);
  ..../*do the write*/
  wait( mutex);
  W=0;
  signal (mutex);
}
```

- b. Can the above solution lead to starvation of writers?

gatecse-2000 operating-system process-synchronization normal descriptive

Answer key

### 5.21.20 Process Synchronization: GATE CSE 2001 | Question: 2.22 top



Consider Peterson's algorithm for mutual exclusion between two concurrent processes i and j. The program executed by process is shown below.

```
repeat
  flag[i] = true;
  turn = j;
  while (P) do no-op;
  Enter critical section, perform actions, then
  exit critical section
  Flag[i] = false;
  Perform other non-critical section actions.
Until false;
```

For the program to guarantee mutual exclusion, the predicate P in the while loop should be

- A. flag[j] = true and turn = i
- B. flag[j] = true and turn = j
- C. flag[i] = true and turn = j
- D. flag[i] = true and turn = i

gatecse-2001 operating-system process-synchronization normal

Answer key

### 5.21.21 Process Synchronization: GATE CSE 2002 | Question: 18-a top



Draw the process state transition diagram of an OS in which (i) each process is in one of the five states: created, ready, running, blocked (i.e., sleep or wait), or terminated, and (ii) only non-preemptive scheduling is used by the OS. Label the transitions appropriately.

**Answer key****5.21.22 Process Synchronization: GATE CSE 2002 | Question: 18-b** 

The functionality of atomic TEST-AND-SET assembly language instruction is given by the following C function

```
int TEST-AND-SET (int *x)
{
    int y;
    A1: y=*x;
    A2: *x=1;
    A3: return y;
}
```

- i. Complete the following C functions for implementing code for entering and leaving critical sections on the above TEST-AND-SET instruction.

```
int mutex=0;
void enter-cs()
{
    while(.....);

}
void leave-cs()
{
    ....;
}
```

- ii. Is the above solution to the critical section problem deadlock free and starvation-free?  
 iii. For the above solution, show by an example that mutual exclusion is not ensured if TEST-AND-SET instruction is not atomic?

**Answer key****5.21.23 Process Synchronization: GATE CSE 2002 | Question: 20** 

The following solution to the single producer single consumer problem uses semaphores for synchronization.

```
#define BUFFSIZE 100
buffer buf[BUFFSIZE];
int first = last = 0;
semaphore b_full = 0;
semaphore b_empty = BUFFSIZE

void producer()
{
while(1) {
    produce an item;
    p1:....;
    put the item into buf (first);
    first = (first+1)%BUFFSIZE;
    p2:....;
}
}

void consumer()
{
while(1) {
    c1:.....
    take the item from buf[last];
    last = (last+1)%BUFFSIZE;
    c2:....;
    consume the item;
}
}
```

- A. Complete the dotted part of the above solution.  
 B. Using another semaphore variable, insert one line statement each immediately after *p1*, immediately before *p2*,

immediately after  $c1$  and immediately before  $c2$  so that the program works correctly for multiple producers and consumers.

gatecse-2002 operating-system process-synchronization normal descriptive

Answer key 

### 5.21.24 Process Synchronization: GATE CSE 2003 | Question: 80

Suppose we want to synchronize two concurrent processes  $P$  and  $Q$  using binary semaphores  $S$  and  $T$ . The code for the processes  $P$  and  $Q$  is shown below.

Process P:	Process Q:
<pre>while(1){ W:     print '0';     print '0'; X: }</pre>	<pre>while(1){ Y:     print '1';     print '1'; Z: }</pre>

Synchronization statements can be inserted only at points  $W$ ,  $X$ ,  $Y$ , and  $Z$

Which of the following will always lead to an output starting with '001100110011'?

- A.  $P(S)$  at  $W$ ,  $V(S)$  at  $X$ ,  $P(T)$  at  $Y$ ,  $V(T)$  at  $Z$ ,  $S$  and  $T$  initially 1
- B.  $P(S)$  at  $W$ ,  $V(T)$  at  $X$ ,  $P(T)$  at  $Y$ ,  $V(S)$  at  $Z$ ,  $S$  initially 1, and  $T$  initially 0
- C.  $P(S)$  at  $W$ ,  $V(T)$  at  $X$ ,  $P(T)$  at  $Y$ ,  $V(S)$  at  $Z$ ,  $S$  and  $T$  initially 1
- D.  $P(S)$  at  $W$ ,  $V(S)$  at  $X$ ,  $P(T)$  at  $Y$ ,  $V(T)$  at  $Z$ ,  $S$  initially 1, and  $T$  initially 0

gatecse-2003 operating-system process-synchronization normal

Answer key 

### 5.21.25 Process Synchronization: GATE CSE 2003 | Question: 81

Suppose we want to synchronize two concurrent processes  $P$  and  $Q$  using binary semaphores  $S$  and  $T$ . The code for the processes  $P$  and  $Q$  is shown below.

Process P:	Process Q:
<pre>while(1) { W:     print '0';     print '0'; X: }</pre>	<pre>while(1) { Y:     print '1';     print '1'; Z: }</pre>

Synchronization statements can be inserted only at points  $W$ ,  $X$ ,  $Y$ , and  $Z$

Which of the following will ensure that the output string never contains a substring of the form  $01^n0$  and  $10^n1$  where  $n$  is odd?

- A.  $P(S)$  at  $W$ ,  $V(S)$  at  $X$ ,  $P(T)$  at  $Y$ ,  $V(T)$  at  $Z$ ,  $S$  and  $T$  initially 1
- B.  $P(S)$  at  $W$ ,  $V(T)$  at  $X$ ,  $P(T)$  at  $Y$ ,  $V(S)$  at  $Z$ ,  $S$  and  $T$  initially 1
- C.  $P(S)$  at  $W$ ,  $V(S)$  at  $X$ ,  $P(S)$  at  $Y$ ,  $V(S)$  at  $Z$ ,  $S$  initially 1
- D.  $V(S)$  at  $W$ ,  $V(T)$  at  $X$ ,  $P(S)$  at  $Y$ ,  $P(T)$  at  $Z$ ,  $S$  and  $T$  initially 1

gatecse-2003 operating-system process-synchronization normal

Answer key 

### 5.21.26 Process Synchronization: GATE CSE 2004 | Question: 48 top



Consider two processes  $P_1$  and  $P_2$  accessing the shared variables  $X$  and  $Y$  protected by two binary semaphores  $S_X$  and  $S_Y$  respectively, both initialized to 1.  $P$  and  $V$  denote the usual semaphore operators, where  $P$  decrements the semaphore value, and  $V$  increments the semaphore value. The pseudo-code of  $P_1$  and  $P_2$  is as follows:

$P_1:$	$P_2:$
While true do {	While true do {
$L_1 : \dots$	$L_3 : \dots$
$L_2 : \dots$	$L_4 : \dots$
$X = X + 1;$	$Y = Y + 1;$
$Y = Y - 1;$	$X = X - 1;$
$V(S_X);$	$V(S_Y);$
$V(S_Y);$	$V(S_X);$
}	}

In order to avoid deadlock, the correct operators at  $L_1$ ,  $L_2$ ,  $L_3$  and  $L_4$  are respectively.

- A.  $P(S_Y), P(S_X); P(S_X), P(S_Y)$
- B.  $P(S_X), P(S_Y); P(S_Y), P(S_X)$
- C.  $P(S_X), P(S_X); P(S_Y), P(S_Y)$
- D.  $P(S_X), P(S_Y); P(S_X), P(S_Y)$

gatecse-2004 operating-system process-synchronization normal

[Answer key](#)

### 5.21.27 Process Synchronization: GATE CSE 2006 | Question: 61 top



The atomic *fetch-and-set*  $x, y$  instruction unconditionally sets the memory location  $x$  to 1 and fetches the old value of  $x$  in  $y$  without allowing any intervening access to the memory location  $x$ . Consider the following implementation of  $P$  and  $V$  functions on a binary semaphore  $S$ .

```
void P (binary_semaphore *s) {
    unsigned y;
    unsigned *x = &(s->value);
    do {
        fetch-and-set x, y;
    } while (y);
}

void V (binary_semaphore *s) {
    S->value = 0;
}
```

Which one of the following is true?

- A. The implementation may not work if context switching is disabled in  $P$
- B. Instead of using *fetch-and-set*, a pair of normal load/store can be used
- C. The implementation of  $V$  is wrong
- D. The code does not implement a binary semaphore

gatecse-2006 operating-system process-synchronization normal

[Answer key](#)

### 5.21.28 Process Synchronization: GATE CSE 2006 | Question: 78 top



Barrier is a synchronization construct where a set of processes synchronizes globally i.e., each process in the set arrives at the barrier and waits for all others to arrive and then all processes leave the barrier. Let the number of processes in the set be three and  $S$  be a binary semaphore with the usual  $P$  and  $V$  functions. Consider the following  $C$  implementation of a barrier with line numbers shown on left.

```
void barrier (void) {
```

```

1: P(S);
2: process_arrived++;
3: V(S);
4: while (process_arrived !=3);
5: P(S);
6: process_left++;
7: if (process_left==3) {
8:   process_arrived = 0;
9:   process_left = 0;
10: }
11: V(S);
}

```

The variables *process\_arrived* and *process\_left* are shared among all processes and are initialized to zero. In a concurrent program all the three processes call the barrier function when they need to synchronize globally.

The above implementation of barrier is incorrect. Which one of the following is true?

- A. The barrier implementation is wrong due to the use of binary semaphore  $S$
- B. The barrier implementation may lead to a deadlock if two barrier invocations are used in immediate succession.
- C. Lines 6 to 10 need not be inside a critical section
- D. The barrier implementation is correct if there are only two processes instead of three.

gatecse-2006 operating-system process-synchronization normal

[Answer key](#)

### 5.21.29 Process Synchronization: GATE CSE 2006 | Question: 79 [top](#)

Barrier is a synchronization construct where a set of processes synchronizes globally i.e., each process in the set arrives at the barrier and waits for all others to arrive and then all processes leave the barrier. Let the number of processes in the set be three and  $S$  be a binary semaphore with the usual  $P$  and  $V$  functions. Consider the following  $C$  implementation of a barrier with line numbers shown on left.

void barrier (void) {

```

1 P(S);
2 process_arrived++;
3 V(S);
4 while (process_arrived !=3);
5 P(S);
6 process_left++;
7 if (process_left==3) {
8   process_arrived = 0;
9   process_left = 0;
10 }
11 V(S);
}

```

The variables *process\_arrived* and *process\_left* are shared among all processes and are initialized to zero. In a concurrent program all the three processes call the barrier function when they need to synchronize globally.

Which one of the following rectifies the problem in the implementation?

- A. Lines 6 to 10 are simply replaced by *process\_arrived--*
- B. At the beginning of the barrier the first process to enter the barrier waits until *process\_arrived* becomes zero before proceeding to execute  $P(S)$ .
- C. Context switch is disabled at the beginning of the barrier and re-enabled at the end.
- D. The variable *process\_left* is made private instead of shared

gatecse-2006 operating-system process-synchronization normal

[Answer key](#)

### 5.21.30 Process Synchronization: GATE CSE 2007 | Question: 58 [top](#)

Two processes,  $P_1$  and  $P_2$ , need to access a critical section of code. Consider the following synchronization construct used by the processes:

```

/* P1 */
while (true) {
    wants1 = true;
    while (wants2 == true);
    /* Critical Section */
    wants1 = false;
}
/* Remainder section */

/* P2 */
while (true) {
    wants2 = true;
    while (wants1 == true);
    /* Critical Section */
    wants2=false;
}
/* Remainder section */

```

Here, `wants1` and `wants2` are shared variables, which are initialized to false.

Which one of the following statements is TRUE about the construct?

- A. It does not ensure mutual exclusion.
- B. It does not ensure bounded waiting.
- C. It requires that processes enter the critical section in strict alteration.
- D. It does not prevent deadlocks, but ensures mutual exclusion.

gatecse-2007 operating-system process-synchronization normal

[Answer key](#)

#### 5.21.31 Process Synchronization: GATE CSE 2009 | Question: 33 [top](#)

The `enter_CS()` and `leave_CS()` functions to implement critical section of a process are realized using test-and-set instruction as follows:

```

void enter_CS(X)
{
    while(test-and-set(X));
}

void leave_CS(X)
{
    X = 0;
}

```

In the above solution,  $X$  is a memory location associated with the  $CS$  and is initialized to 0. Now consider the following statements:

- I. The above solution to  $CS$  problem is deadlock-free
- II. The solution is starvation free
- III. The processes enter  $CS$  in FIFO order
- IV. More than one process can enter  $CS$  at the same time

Which of the above statements are TRUE?

- A. (I) only
- B. (I) and (II)
- C. (II) and (III)
- D. (IV) only

gatecse-2009 operating-system process-synchronization normal

[Answer key](#)

#### 5.21.32 Process Synchronization: GATE CSE 2010 | Question: 23 [top](#)

Consider the methods used by processes  $P_1$  and  $P_2$  for accessing their critical sections whenever needed, as given below. The initial values of shared boolean variables  $S1$  and  $S2$  are randomly assigned.

Method used by P1	Method used by P2
while ( $S_1 == S_2$ ); CriticalSection $S_1 = S_2$ ;	while ( $S_1 != S_2$ ); CriticalSection $S_2 = \text{not}(S_1)$ ;

Which one of the following statements describes the properties achieved?

- A. Mutual exclusion but not progress
- B. Progress but not mutual exclusion
- C. Neither mutual exclusion nor progress
- D. Both mutual exclusion and progress

gatecse-2010 operating-system process-synchronization normal

[Answer key](#)

#### 5.21.33 Process Synchronization: GATE CSE 2010 | Question: 45 [top](#)

The following program consists of 3 concurrent processes and 3 binary semaphores. The semaphores are initialized as  $S_0 = 1$ ,  $S_1 = 0$  and  $S_2 = 0$ .

Process P0	Process P1	Process P2
while (true) { wait ( $S_0$ ); print '0'; release ( $S_1$ ); release ( $S_2$ ); }	wait ( $S_1$ ); release ( $S_0$ );	wait ( $S_2$ ); release ( $S_0$ );

How many times will process  $P_0$  print '0'?

- A. At least twice
- B. Exactly twice
- C. Exactly thrice
- D. Exactly once

gatecse-2010 operating-system process-synchronization normal

[Answer key](#)

#### 5.21.34 Process Synchronization: GATE CSE 2012 | Question: 32 [top](#)

*Fetch\_And\_Add( $X, i$ )* is an atomic Read-Modify-Write instruction that reads the value of memory location  $X$ , increments it by the value  $i$ , and returns the old value of  $X$ . It is used in the pseudocode shown below to implement a busy-wait lock.  $L$  is an unsigned integer shared variable initialized to 0. The value of 0 corresponds to lock being available, while any non-zero value corresponds to the lock being not available.

```
AcquireLock(L){  
    while (Fetch_And_Add(L,1))  
        L = 1;  
}  
  
ReleaseLock(L){  
    L = 0;  
}
```

This implementation

- A. fails as  $L$  can overflow
- B. fails as  $L$  can take on a non-zero value when the lock is actually available
- C. works correctly but may starve some processes
- D. works correctly without starvation

gatecse-2012 operating-system process-synchronization normal

Answer key

### 5.21.35 Process Synchronization: GATE CSE 2013 | Question: 34 top



A shared variable  $x$ , initialized to zero, is operated on by four concurrent processes  $W, X, Y, Z$  as follows. Each of the processes  $W$  and  $X$  reads  $x$  from memory, increments by one, stores it to memory, and then terminates. Each of the processes  $Y$  and  $Z$  reads  $x$  from memory, decrements by two, stores it to memory, and then terminates. Each process before reading  $x$  invokes the  $P$  operation (i.e., wait) on a counting semaphore  $S$  and invokes the  $V$  operation (i.e., signal) on the semaphore  $S$  after storing  $x$  to memory. Semaphore  $S$  is initialized to two. What is the maximum possible value of  $x$  after all processes complete execution?

- A. -2      B. -1      C. 1      D. 2

gatecse-2013 operating-system process-synchronization normal

Answer key

### 5.21.36 Process Synchronization: GATE CSE 2013 | Question: 39 top



A certain computation generates two arrays  $a$  and  $b$  such that  $a[i] = f(i)$  for  $0 \leq i < n$  and  $b[i] = g(a[i])$  for  $0 \leq i < n$ . Suppose this computation is decomposed into two concurrent processes  $X$  and  $Y$  such that  $X$  computes the array  $a$  and  $Y$  computes the array  $b$ . The processes employ two binary semaphores  $R$  and  $S$ , both initialized to zero. The array  $a$  is shared by the two processes. The structures of the processes are shown below.

Process X:

```
private i;
for (i=0; i<n; i++) {
    a[i] = f(i);
    ExitX(R, S);
}
```

Process Y:

```
private i;
for (i=0; i<n; i++) {
    EntryY(R, S);
    b[i] = g(a[i]);
}
```

Which one of the following represents the **CORRECT** implementations of  $\text{ExitX}$  and  $\text{EntryY}$ ?

A. `ExitX(R, S) {  
 P(R);  
 V(S);  
}  
EntryY(R, S) {  
 P(S);  
 V(R);  
}`

B. `ExitX(R, S) {  
 V(R);  
 V(S);  
}  
EntryY(R, S) {  
 P(R);  
 P(S);  
}`

C. `ExitX(R, S) {  
 P(S);  
 V(R);  
}  
EntryY(R, S) {  
 V(S);  
 P(R);  
}`

D. `ExitX(R, S) {  
 V(R);  
 P(S);  
}  
EntryY(R, S) {  
 V(S);  
 P(R);  
}`

gatecse-2013 operating-system process-synchronization normal

Answer key

### 5.21.37 Process Synchronization: GATE CSE 2014 Set 2 | Question: 31 top



Consider the procedure below for the *Producer-Consumer* problem which uses semaphores:

```
semaphore n = 0;  
semaphore s = 1;
```

```

void producer()
{
    while(true)
    {
        produce();
        semWait(s);
        addToBuffer();
        semSignal(s);
        semSignal(n);
    }
}

```

```

void consumer()
{
    while(true)
    {
        semWait(s);
        semWait(n);
        removeFromBuffer();
        semSignal(s);
        consume();
    }
}

```

Which one of the following is **TRUE**?

- A. The producer will be able to add an item to the buffer, but the consumer can never consume it.
- B. The consumer will remove no more than one item from the buffer.
- C. Deadlock occurs if the consumer succeeds in acquiring semaphore  $s$  when the buffer is empty.
- D. The starting value for the semaphore  $n$  must be 1 and not 0 for deadlock-free operation.

gatecse-2014-set2 operating-system process-synchronization normal

[Answer key](#)

#### 5.21.38 Process Synchronization: GATE CSE 2015 Set 1 | Question: 9 [top](#)

The following two functions  $P1$  and  $P2$  that share a variable  $B$  with an initial value of 2 execute concurrently.

$P1() \{$ $C = B - 1;$ $B = 2 * C;$ }	$P2() \{$ $D = 2 * B;$ $B = D - 1;$ }
--	--

The number of distinct values that  $B$  can possibly take after the execution is \_\_\_\_\_.

gatecse-2015-set1 operating-system process-synchronization normal numerical-answers

[Answer key](#)

#### 5.21.39 Process Synchronization: GATE CSE 2015 Set 3 | Question: 10 [top](#)

Two processes  $X$  and  $Y$  need to access a critical section. Consider the following synchronization construct used by both the processes

Process X	Process Y
<pre>/* other code for process X*/ while (true) {     varP = true;     while (varQ == true)     {         /* Critical Section */         varP = false;     } } /* other code for process X */</pre>	<pre>/* other code for process Y*/ while (true) {     varQ = true;     while (varP == true)     {         /* Critical Section */         varQ = false;     } } /* other code for process Y */</pre>

Here *varP* and *varQ* are shared variables and both are initialized to false. Which one of the following statements is true?

- A. The proposed solution prevents deadlock but fails to guarantee mutual exclusion
- B. The proposed solution guarantees mutual exclusion but fails to prevent deadlock
- C. The proposed solution guarantees mutual exclusion and prevents deadlock
- D. The proposed solution fails to prevent deadlock and fails to guarantee mutual exclusion

gatecse-2015-set3 operating-system process-synchronization normal

[Answer key](#)

#### 5.21.40 Process Synchronization: GATE CSE 2016 Set 1 | Question: 50 [top](#)



Consider the following proposed solution for the critical section problem. There are  $n$  processes :  $P_0, \dots, P_{n-1}$ . In the code, function pmax returns an integer not smaller than any of its arguments .For all  $i, t[i]$  is initialized to zero.

Code for  $P_i$ :

```
do {
    c[i]=1; t[i]= pmax (t[0],...,t[n-1])+1; c[i]=0;
    for every j != i in {0,...,n-1} {
        while (c[j]);
        while (t[j] != 0 && t[j] <=t[i]);
    }
    Critical Section;
    t[i]=0;
    Remainder Section;
} while (true);
```

Which of the following is TRUE about the above solution?

- A. At most one process can be in the critical section at any time
- B. The bounded wait condition is satisfied
- C. The progress condition is satisfied
- D. It cannot cause a deadlock

gatecse-2016-set1 operating-system process-synchronization difficult ambiguous

[Answer key](#)

#### 5.21.41 Process Synchronization: GATE CSE 2016 Set 2 | Question: 48 [top](#)



Consider the following two-process synchronization solution.

PROCESS 0	Process 1
Entry: loop while (turn == 1); (critical section) Exit: turn = 1;	Entry: loop while (turn == 0); (critical section) Exit turn = 0;

The shared variable turn is initialized to zero. Which one of the following is TRUE?

- A. This is a correct two- process synchronization solution.
- B. This solution violates mutual exclusion requirement.
- C. This solution violates progress requirement.
- D. This solution violates bounded wait requirement.

gatecse-2016-set2 operating-system process-synchronization normal

[Answer key](#)

#### 5.21.42 Process Synchronization: GATE CSE 2017 Set 1 | Question: 27 [top](#)

A multithreaded program  $P$  executes with  $x$  number of threads and uses  $y$  number of locks for ensuring mutual exclusion while operating on shared memory locations. All locks in the program are *non-reentrant*, i.e., if a thread holds a lock  $l$ , then it cannot re-acquire lock  $l$  without releasing it. If a thread is unable to acquire a lock, it blocks until the lock becomes available. The *minimum* value of  $x$  and the *minimum* value of  $y$  together for which execution of  $P$  can result in a deadlock are:

- |                   |                   |
|-------------------|-------------------|
| A. $x = 1, y = 2$ | B. $x = 2, y = 1$ |
| C. $x = 2, y = 2$ | D. $x = 1, y = 1$ |

gatecse-2017-set1 operating-system process-synchronization normal

[Answer key](#)

#### 5.21.43 Process Synchronization: GATE CSE 2018 | Question: 40 [top](#)

Consider the following solution to the producer-consumer synchronization problem. The shared buffer size is  $N$ . Three semaphores *empty*, *full* and *mutex* are defined with respective initial values of 0,  $N$  and 1. Semaphore *empty* denotes the number of available slots in the buffer, for the consumer to read from. Semaphore *full* denotes the number of available slots in the buffer, for the producer to write to. The placeholder variables, denoted by  $P$ ,  $Q$ ,  $R$  and  $S$ , in the code below can be assigned either *empty* or *full*. The valid semaphore operations are: *wait()* and *signal()*.

Producer:	Consumer:
<pre>do {     wait (P);     wait (mutex);     //Add item to buffer     signal (mutex);     signal (Q); }while (1);</pre>	<pre>do {     wait (R);     wait (mutex);     //consume item from buffer     signal (mutex);     signal (S); }while (1);</pre>

Which one of the following assignments tp  $P$ ,  $Q$ ,  $R$  and  $S$  will yield the correct solution?

- A.  $P : full, Q : full, R : empty, S : empty$
- B.  $P : empty, Q : empty, R : full, S : full$
- C.  $P : full, Q : empty, R : empty, S : full$
- D.  $P : empty, Q : full, R : full, S : empty$

**Answer key****5.21.44 Process Synchronization: GATE CSE 2019 | Question: 23**

Consider three concurrent processes  $P_1, P_2$  and  $P_3$  as shown below, which access a shared variable  $D$  that has been initialized to 100.

$P_1$	$P_2$	$P_3$
:	:	:
:	:	:
$D = D + 20$	$D = D - 50$	$D = D + 10$
:	:	:
:	:	:

The processes are executed on a uniprocessor system running a time-shared operating system. If the minimum and maximum possible values of  $D$  after the three processes have completed execution are  $X$  and  $Y$  respectively, then the value of  $Y - X$  is \_\_\_\_\_

**Answer key****5.21.45 Process Synchronization: GATE CSE 2019 | Question: 39**

Consider the following snapshot of a system running  $n$  concurrent processes. Process  $i$  is holding  $X_i$  instances of a resource  $R$ ,  $1 \leq i \leq n$ . Assume that all instances of  $R$  are currently in use. Further, for all  $i$ , process  $i$  can place a request for at most  $Y_i$  additional instances of  $R$  while holding the  $X_i$  instances it already has. Of the  $n$  processes, there are exactly two processes  $p$  and  $q$  such that  $Y_p = Y_q = 0$ . Which one of the following conditions guarantees that no other process apart from  $p$  and  $q$  can complete execution?

- A.  $X_p + X_q < \text{Min}\{Y_k \mid 1 \leq k \leq n, k \neq p, k \neq q\}$
- B.  $X_p + X_q < \text{Max}\{Y_k \mid 1 \leq k \leq n, k \neq p, k \neq q\}$
- C.  $\text{Min}(X_p, X_q) \geq \text{Min}\{Y_k \mid 1 \leq k \leq n, k \neq p, k \neq q\}$
- D.  $\text{Min}(X_p, X_q) \leq \text{Max}\{Y_k \mid 1 \leq k \leq n, k \neq p, k \neq q\}$

**Answer key****5.21.46 Process Synchronization: GATE IT 2004 | Question: 65**

The semaphore variables full, empty and mutex are initialized to 0,  $n$  and 1, respectively. Process  $P_1$  repeatedly adds one item at a time to a buffer of size  $n$ , and process  $P_2$  repeatedly removes one item at a time from the same buffer using the programs given below. In the programs,  $K, L, M$  and  $N$  are unspecified statements.

$P_1$

```
while (1) {
    K;
    P(mutex);
    Add an item to the buffer;
    V(mutex);
    L;
}
```

$P_2$

```
while (1) {
    M;
    P(mutex);
    Remove an item from the buffer;
    V(mutex);
    N;
}
```

The statements  $K$ ,  $L$ ,  $M$  and  $N$  are respectively

- A. P(full), V(empty), P(full), V(empty)  
C. P(empty), V(full), P(empty), V(full)
- B. P(full), V(empty), P(empty), V(full)  
D. P(empty), V(full), P(full), V(empty)

gateit-2004 operating-system process-synchronization normal

Answer key 

#### 5.21.47 Process Synchronization: GATE IT 2005 | Question: 41



Given below is a program which when executed spawns two concurrent processes :

semaphore  $X := 0;$

/\* Process now forks into concurrent processes  $P1$  &  $P2$  \*/

$P1$	$P2$
repeat forever $V(X);$ Compute; $P(X);$	repeat forever $P(X);$ Compute; $V(X);$

Consider the following statements about processes  $P1$  and  $P2$  :

- I. It is possible for process  $P1$  to starve.  
II. It is possible for process  $P2$  to starve.

Which of the following holds?

- A. Both (I) and (II) are true.  
C. (II) is true but (I) is false
- B. (I) is true but (II) is false.  
D. Both (I) and (II) are false

gateit-2005 operating-system process-synchronization normal

Answer key 

#### 5.21.48 Process Synchronization: GATE IT 2005 | Question: 42



Two concurrent processes  $P1$  and  $P2$  use four shared resources  $R1$ ,  $R2$ ,  $R3$  and  $R4$ , as shown below.

$P1$	$P2$
Compute;	Compute;
Use R1;	Use R1;
Use R2;	Use R2;
Use R3;	Use R3;
Use R4;	Use R4;

Both processes are started at the same time, and each resource can be accessed by only one process at a time. The following scheduling constraints exist between the access of resources by the processes:

- $P2$  must complete use of  $R1$  before  $P1$  gets access to  $R1$ .
- $P1$  must complete use of  $R2$  before  $P2$  gets access to  $R2$ .
- $P2$  must complete use of  $R3$  before  $P1$  gets access to  $R3$ .
- $P1$  must complete use of  $R4$  before  $P2$  gets access to  $R4$ .

There are no other scheduling constraints between the processes. If only binary semaphores are used to enforce the above scheduling constraints, what is the minimum number of binary semaphores needed?

- A. 1      B. 2      C. 3      D. 4

gateit-2005 operating-system process-synchronization normal

Answer key 

5.21.49 Process Synchronization: GATE IT 2006 | Question: 55 top

Consider the solution to the bounded buffer producer/consumer problem by using general semaphores  $S$ ,  $F$ , and  $E$ . The semaphore  $S$  is the mutual exclusion semaphore initialized to 1. The semaphore  $F$  corresponds to the number of free slots in the buffer and is initialized to  $N$ . The semaphore  $E$  corresponds to the number of elements in the buffer and is initialized to 0.

Producer Process	Consumer Process
Produce an item;	Wait(E);
Wait(F);	Wait(S);
Wait(S);	Remove an item from the buffer;
Append the item to the buffer;	Signal(S);
Signal(S);	Signal(F);
Signal(E);	Consume the item;

Which of the following interchange operations may result in a deadlock?

- I. Interchanging Wait ( $F$ ) and Wait ( $S$ ) in the Producer process
  - II. Interchanging Signal ( $S$ ) and Signal ( $F$ ) in the Consumer process  
  - A. (I) only
  - B. (II) only
  - C. Neither (I) nor (II)
  - D. Both (I) and (II)

gateit-2006 operating-system process-synchronization normal

Answer key

5.21.50 Process Synchronization: GATE IT 2007 | Question: 10 [top](#)

Processes  $P_1$  and  $P_2$  use critical\_flag in the following routine to achieve mutual exclusion. Assume that critical\_flag is initialized to FALSE in the main program.

```
get_exclusive_access ()  
{  
    if (critical_flag == FALSE) {  
        critical_flag = TRUE ;  
        critical_region () ;  
        critical_flag = FALSE;  
    }  
}
```

Consider the following statements.

- i. It is possible for both  $P1$  and  $P2$  to access critical\_region concurrently.
  - ii. This may lead to a deadlock.

Which of the following holds?

- A. (i) is false (ii) is true      B. Both (i) and (ii) are false  
C. (i) is true (ii) is false      D. Both (i) and (ii) are true

gateit-2007 operating-system process-synchronization normal

Answer key

5.21.51 Process Synchronization: GATE IT 2007 | Question: 56 [top](#)

Synchronization in the classical readers and writers problem can be achieved through use of semaphores. In the following incomplete code for readers-writers problem, two binary semaphores mutex and wrt are used to obtain synchronization

```
wait (wrt)  
writing is performed  
signal (wrt)  
wait (mutex)  
readcount = readcount + 1  
if readcount = 1 then S1
```

```

S2
reading is performed
S3
readcount = readcount - 1
if readcount = 0 then S4
signal (mutex)

```

The values of  $S_1, S_2, S_3, S_4$ , (in that order) are

- A. signal (mutex), wait (wrt), signal (wrt), wait (mutex)
- B. signal (wrt), signal (mutex), wait (mutex), wait (wrt)
- C. wait (wrt), signal (mutex), wait (mutex), signal (wrt)
- D. signal (mutex), wait (mutex), signal (mutex), wait (mutex)

gateit-2007 operating-system process-synchronization normal

[Answer key](#)

### 5.21.52 Process Synchronization: GATE IT 2008 | Question: 53 [top](#)

The following is a code with two threads, producer and consumer, that can run in parallel. Further,  $S$  and  $Q$  are binary semaphores quipped with the standard  $P$  and  $V$  operations.

```

semaphore S = 1, Q = 0;
integer x;

producer:           consumer:
while (true) do    while (true) do
  P(S);            P(Q);
  x = produce ();  consume (x);
  V(Q);            V(S);
done               done

```

Which of the following is TRUE about the program above?

- A. The process can deadlock
- B. One of the threads can starve
- C. Some of the items produced by the producer may be lost
- D. Values generated and stored in ' $x$ ' by the producer will always be consumed before the producer can generate a new value

gateit-2008 operating-system process-synchronization normal

[Answer key](#)

## 5.22

### Resource Allocation (27) [top](#)

#### 5.22.1 Resource Allocation: GATE CSE 1988 | Question: 11 [top](#)

A number of processes could be in a deadlock state if none of them can execute due to non-availability of sufficient resources. Let  $P_i, 0 \leq i \leq 4$  represent five processes and let there be four resources types  $r_j, 0 \leq j \leq 3$ . Suppose the following data structures have been used.

**Available:** A vector of length 4 such that if  $\text{Available}[i] = k$ , there are  $k$  instances of resource type  $r_j$  available in the system.

**Allocation.** A  $5 \times 4$  matrix defining the number of each type currently allocated to each process. If  $\text{Allocation}[i, j] = k$  then process  $p_i$  is currently allocated  $k$  instances of resource type  $r_j$ .

**Max.** A  $5 \times 4$  matrix indicating the maximum resource need of each process. If  $\text{Max}[i, j] = k$  then process  $p_i$ , may need a maximum of  $k$  instances of resource type  $r_j$  in order to complete the task.

Assume that system allocated resources only when it does not lead into an unsafe state such that resource requirements in future never cause a deadlock state. Now consider the following snapshot of the system.

	Allocation				Max				Available
	$r_0$	$r_1$	$r_2$	$r_3$	$r_0$	$r_1$	$r_2$	$r_3$	
$p_0$	0	0	1	2	0	0	1	2	
$p_1$	1	0	0	0	1	7	5	0	
$p_2$	1	3	5	4	2	3	5	6	1 5 2 0
$p_3$	0	6	3	2	0	6	5	2	
$p_4$	0	0	1	4	0	6	5	6	

Is the system currently in a safe state? If yes, explain why.

gate1988 normal descriptive operating-system resource-allocation

Answer key 

### 5.22.2 Resource Allocation: GATE CSE 1989 | Question: 11a top

- i. A system of four concurrent processes,  $P, Q, R$  and  $S$ , use shared resources  $A, B$  and  $C$ . The sequences in which processes,  $P, Q, R$  and  $S$  request and release resources are as follows:

- |            |                 |
|------------|-----------------|
| Process P: | 1. P requests A |
|            | 2. P requests B |
|            | 3. P releases A |
|            | 4. P releases B |
| Process Q: | 1. Q requests C |
|            | 2. Q requests A |
|            | 3. Q releases C |
|            | 4. Q releases A |
| Process R: | 1. R requests B |
|            | 2. R requests C |
|            | 3. R releases B |
|            | 4. R releases C |
| Process S: | 1. S requests A |
|            | 2. S requests C |
|            | 3. S releases A |
|            | 4. S releases C |

If a resource is free, it is granted to a requesting process immediately. There is no preemption of granted resources. A resource is taken back from a process only when the process explicitly releases it.

Can the system of four processes get into a deadlock? If yes, give a sequence (ordering) of operations (for requesting and releasing resources) of these processes which leads to a deadlock.

- ii. Will the processes always get into a deadlock? If your answer is no, give a sequence of these operations which leads to completion of all processes.
- iii. What strategies can be used to prevent deadlocks in a system of concurrent processes using shared resources if preemption of granted resources is not allowed?

descriptive gate1989 operating-system resource-allocation

Answer key 

### 5.22.3 Resource Allocation: GATE CSE 1992 | Question: 02-xi top

A computer system has 6 tape devices, with  $n$  processes competing for them. Each process may need 3 tape drives. The maximum value of  $n$  for which the system is guaranteed to be deadlock-free is:

A. 2

B. 3

C. 4

D. 1

gate1992 operating-system resource-allocation normal multiple-selects

Answer key 

#### 5.22.4 Resource Allocation: GATE CSE 1993 | Question: 7.9, UGCNET-Dec2012-III: 41

Consider a system having  $m$  resources of the same type. These resources are shared by 3 processes  $A, B$ , and  $C$  which have peak demands of 3, 4, and 6 respectively. For what value of  $m$  deadlock will not occur?

A. 7

B. 9

C. 10

D. 13

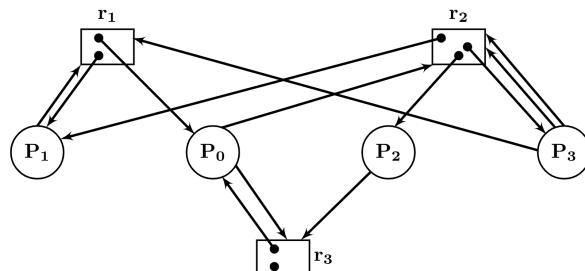
E. 15

gate1993 operating-system resource-allocation normal ugcnetcse-dec2012-paper3 multiple-selects

Answer key 

#### 5.22.5 Resource Allocation: GATE CSE 1994 | Question: 28

Consider the resource allocation graph in the figure.



A. Find if the system is in a deadlock state

B. Otherwise, find a safe sequence

gate1994 operating-system resource-allocation normal descriptive

Answer key 

#### 5.22.6 Resource Allocation: GATE CSE 1996 | Question: 22

A computer system uses the Banker's Algorithm to deal with deadlocks. Its current state is shown in the table below, where  $P_0, P_1, P_2$  are processes, and  $R_0, R_1, R_2$  are resources types.

	Maximum Need			Current Allocation			Available			
	R0	R1	R2	P0	R0	R1	R2	P0	R1	R2
P0	4	1	2	P0	1	0	2	2	2	0
P1	1	5	1	P1	0	3	1			
P2	1	2	3	P2	1	0	2			

A. Show that the system can be in this state

B. What will the system do on a request by process  $P_0$  for one unit of resource type  $R_1$ ?

gate1996 operating-system resource-allocation normal descriptive

Answer key 

#### 5.22.7 Resource Allocation: GATE CSE 1997 | Question: 6.7

An operating system contains 3 user processes each requiring 2 units of resource  $R$ . The minimum number of units of  $R$  such that no deadlocks will ever arise is

A. 3

B. 5

C. 4

D. 6

**Answer key****5.22.8 Resource Allocation: GATE CSE 1997 | Question: 75**

An operating system handles requests to resources as follows.

A process (which asks for some resources, uses them for some time and then exits the system) is assigned a unique timestamp when it starts. The timestamps are monotonically increasing with time. Let us denote the timestamp of a process  $P$  by  $TS(P)$ .

When a process  $P$  requests for a resource the  $OS$  does the following:

- If no other process is currently holding the resource, the  $OS$  awards the resource to  $P$ .
- If some process  $Q$  with  $TS(Q) < TS(P)$  is holding the resource, the  $OS$  makes  $P$  wait for the resources.
- If some process  $Q$  with  $TS(Q) > TS(P)$  is holding the resource, the  $OS$  restarts  $Q$  and awards the resources to  $P$ . (Restarting means taking back the resources held by a process, killing it and starting it again with the same timestamp)

When a process releases a resource, the process with the smallest timestamp (if any) amongst those waiting for the resource is awarded the resource.

- Can a deadlock ever arise? If yes, show how. If not prove it.
- Can a process  $P$  ever starve? If yes, show how. If not prove it.

**Answer key****5.22.9 Resource Allocation: GATE CSE 1998 | Question: 1.32**

A computer has six tape drives, with  $n$  processes competing for them. Each process may need two drives. What is the maximum value of  $n$  for the system to be deadlock free?

- A. 6      B. 5      C. 4      D. 3

**Answer key****5.22.10 Resource Allocation: GATE CSE 2000 | Question: 2.23**

Which of the following is not a valid deadlock prevention scheme?

- Release all resources before requesting a new resource.
- Number the resources uniquely and never request a lower numbered resource than the last one requested.
- Never request a resource after releasing any resource.
- Request and all required resources be allocated before execution.

**Answer key****5.22.11 Resource Allocation: GATE CSE 2001 | Question: 19**

Two concurrent processes  $P_1$  and  $P_2$  want to use resources  $R_1$  and  $R_2$  in a mutually exclusive manner. Initially,  $R_1$  and  $R_2$  are free. The programs executed by the two processes are given below.

Program for P1:	Program for P2:
S1: While ( $R_1$ is busy) do no-op;	Q1: While ( $R_1$ is busy) do no-op;
S2: Set $R_1 \leftarrow$ busy;	Q2: Set $R_1 \leftarrow$ busy;
S3: While ( $R_2$ is busy) do no-op;	Q3: While ( $R_2$ is busy) do no-op;
S4: Set $R_2 \leftarrow$ busy;	Q4: Set $R_2 \leftarrow$ busy;
S5: Use $R_1$ and $R_2$ ;	Q5: Use $R_1$ and $R_2$ ;
S6: Set $R_1 \leftarrow$ free;	Q6: Set $R_2 \leftarrow$ free;
S7: Set $R_2 \leftarrow$ free;	Q7: Set $R_1 \leftarrow$ free;

- A. Is mutual exclusion guaranteed for  $R_1$  and  $R_2$ ? If not show a possible interleaving of the statements of  $P1$  and  $P2$  such mutual exclusion is violated (i.e., both  $P1$  and  $P2$  use  $R_1$  and  $R_2$  at the same time).
- B. Can deadlock occur in the above program? If yes, show a possible interleaving of the statements of  $P1$  and  $P2$  leading to deadlock.
- C. Exchange the statements  $Q1$  and  $Q3$  and statements  $Q2$  and  $Q4$ . Is mutual exclusion guaranteed now? Can deadlock occur?

gatecse-2001 operating-system resource-allocation normal descriptive

Answer key 

#### 5.22.12 Resource Allocation: GATE CSE 2005 | Question: 71 top



Suppose  $n$  processes,  $P_1, \dots, P_n$  share  $m$  identical resource units, which can be reserved and released one at a time. The maximum resource requirement of process  $P_i$  is  $s_i$ , where  $s_i > 0$ . Which one of the following is a sufficient condition for ensuring that deadlock does not occur?

- A.  $\forall i, s_i < m$
- B.  $\forall i, s_i < n$
- C.  $\sum_{i=1}^n s_i < (m + n)$
- D.  $\sum_{i=1}^n s_i < (m \times n)$

gatecse-2005 operating-system resource-allocation normal

Answer key 

#### 5.22.13 Resource Allocation: GATE CSE 2006 | Question: 66 top



Consider the following snapshot of a system running  $n$  processes. Process  $i$  is holding  $x_i$  instances of a resource  $R$ ,  $1 \leq i \leq n$ . Currently, all instances of  $R$  are occupied. Further, for all  $i$ , process  $i$  has placed a request for an additional  $y_i$  instances while holding the  $x_i$  instances it already has. There are exactly two processes  $p$  and  $q$  and such that  $y_p = y_q = 0$ . Which one of the following can serve as a necessary condition to guarantee that the system is not approaching a deadlock?

- A.  $\min(x_p, x_q) < \max_{k \neq p, q} y_k$
- B.  $x_p + x_q \geq \min_{k \neq p, q} y_k$
- C.  $\max(x_p, x_q) > 1$
- D.  $\min(x_p, x_q) > 1$

gatecse-2006 operating-system resource-allocation normal

Answer key 

#### 5.22.14 Resource Allocation: GATE CSE 2007 | Question: 57 top



A single processor system has three resource types  $X$ ,  $Y$  and  $Z$ , which are shared by three processes. There are 5 units of each resource type. Consider the following scenario, where the column **alloc** denotes the number of units of each resource type allocated to each process, and the column **request** denotes the number of units of each resource type requested by a process in order to complete execution. Which of these processes will finish **LAST**?

	alloc			request		
	X	Y	Z	X	Y	Z
P0	1	2	1	1	0	3
P1	2	0	1	0	1	2
P2	2	2	1	1	2	0

- A.  $P_0$   
 C.  $P_2$   
 D. None of the above, since the system is in a deadlock

gatecse-2007 operating-system resource-allocation normal

Answer key 

#### 5.22.15 Resource Allocation: GATE CSE 2008 | Question: 65 top

Which of the following is NOT true of deadlock prevention and deadlock avoidance schemes?

- A. In deadlock prevention, the request for resources is always granted if the resulting state is safe  
 B. In deadlock avoidance, the request for resources is always granted if the resulting state is safe  
 C. Deadlock avoidance is less restrictive than deadlock prevention  
 D. Deadlock avoidance requires knowledge of resource requirements *a priori*..

gatecse-2008 operating-system easy resource-allocation

Answer key 

#### 5.22.16 Resource Allocation: GATE CSE 2009 | Question: 30 top

Consider a system with 4 types of resources  $R_1$  (3 units),  $R_2$  (2 units),  $R_3$  (3 units),  $R_4$  (2 units). A non-preemptive resource allocation policy is used. At any given instance, a request is not entertained if it cannot be completely satisfied. Three processes  $P_1$ ,  $P_2$ ,  $P_3$  request the resources as follows if executed independently.

Process P1:	Process P2:	Process P3:
$t = 0$ : requests 2 units of $R_2$	$t = 0$ : requests 2 units of $R_3$	$t = 0$ : requests 1 unit of $R_4$
$t = 1$ : requests 1 unit of $R_3$	$t = 2$ : requests 1 unit of $R_4$	$t = 2$ : requests 2 units of $R_1$
$t = 3$ : requests 2 units of $R_1$	$t = 4$ : requests 1 unit of $R_1$	$t = 5$ : releases 2 units of $R_1$
$t = 5$ : releases 1 unit of $R_2$ and 1 unit of $R_1$	$t = 6$ : releases 1 unit of $R_3$	$t = 7$ : requests 1 unit of $R_2$
$t = 7$ : releases 1 unit of $R_3$	$t = 8$ : Finishes	$t = 8$ : requests 1 unit of $R_3$
$t = 8$ : requests 2 units of $R_4$		$t = 9$ : Finishes
$t = 10$ : Finishes		

Which one of the following statements is TRUE if all three processes run concurrently starting at time  $t = 0$ ?

- A. All processes will finish without any deadlock  
 C. Only  $P_1$  and  $P_3$  will be in deadlock  
 B. Only  $P_1$  and  $P_2$  will be in deadlock  
 D. All three processes will be in deadlock

gatecse-2009 operating-system resource-allocation normal

Answer key 

#### 5.22.17 Resource Allocation: GATE CSE 2010 | Question: 46 top

A system has  $n$  resources  $R_0, \dots, R_{n-1}$ , and  $k$  processes  $P_0, \dots, P_{k-1}$ . The implementation of the resource request logic of each process  $P_i$  is as follows:

```
if(i%2 == 0){
    if(i < n) request  $R_i$ ;
```

```

if( $i + 2 < n$ ) request  $R_{i+2};\}$ 
else{
    if( $i < n$ ) request  $R_{n-i};$ 
    if( $i + 2 < n$ ) request  $R_{n-i-2};\}$ 

```

In which of the following situations is a deadlock possible?

- A.  $n = 40, k = 26$     B.  $n = 21, k = 12$     C.  $n = 20, k = 10$     D.  $n = 41, k = 19$

gatecse-2010 operating-system resource-allocation normal

[Answer key](#)

### 5.22.18 Resource Allocation: GATE CSE 2013 | Question: 16 [top](#)

Three concurrent processes  $X$ ,  $Y$ , and  $Z$  execute three different code segments that access and update certain shared variables. Process  $X$  executes the  $P$  operation (i.e., *wait*) on semaphores  $a$ ,  $b$ , and  $c$ ; process  $Y$  executes the  $P$  operation on semaphores  $b$ ,  $c$ , and  $d$ ; process  $Z$  executes the  $P$  operation on semaphores  $c$ ,  $d$ , and  $a$  before entering the respective code segments. After completing the execution of its code segment, each process invokes the  $V$  operation (i.e., *signal*) on its three semaphores. All semaphores are binary semaphores initialized to one. Which one of the following represents a deadlock-free order of invoking the  $P$  operations by the processes?

- A.  $X : P(a)P(b)P(c) Y : P(b)P(c)P(d) Z : P(c)P(d)P(a)$   
 B.  $X : P(b)P(a)P(c) Y : P(b)P(c)P(d) Z : P(a)P(c)P(d)$   
 C.  $X : P(b)P(a)P(c) Y : P(c)P(b)P(d) Z : P(a)P(c)P(d)$   
 D.  $X : P(a)P(b)P(c) Y : P(c)P(b)P(d) Z : P(c)P(d)P(a)$

gatecse-2013 operating-system resource-allocation normal

[Answer key](#)

### 5.22.19 Resource Allocation: GATE CSE 2014 Set 1 | Question: 31 [top](#)

An operating system uses the *Banker's algorithm* for deadlock avoidance when managing the allocation of three resource types  $X$ ,  $Y$ , and  $Z$  to three processes  $P_0$ ,  $P_1$ , and  $P_2$ . The table given below presents the current system state. Here, the *Allocation matrix* shows the current number of resources of each type allocated to each process and the *Max matrix* shows the maximum number of resources of each type required by each process during its execution.

	Allocation			Max		
	X	Y	Z	X	Y	Z
<b>P0</b>	0	0	1	8	4	3
<b>P1</b>	3	2	0	6	2	0
<b>P2</b>	2	1	1	3	3	3

There are 3 units of type  $X$ , 2 units of type  $Y$  and 2 units of type  $Z$  still available. The system is currently in a **safe** state. Consider the following independent requests for additional resources in the current state:

**REQ1:**  $P_0$  requests 0 units of  $X$ , 0 units of  $Y$  and 2 units of  $Z$

**REQ2:**  $P_1$  requests 2 units of  $X$ , 0 units of  $Y$  and 0 units of  $Z$

Which one of the following is **TRUE**?

- A. Only REQ1 can be permitted.  
 C. Both REQ1 and REQ2 can be permitted.  
 B. Only REQ2 can be permitted.  
 D. Neither REQ1 nor REQ2 can be permitted.

gatecse-2014-set1 operating-system resource-allocation normal

[Answer key](#)

### 5.22.20 Resource Allocation: GATE CSE 2014 Set 3 | Question: 31 top



A system contains three programs and each requires three tape units for its operation. The minimum number of tape units which the system must have such that deadlocks never arise is \_\_\_\_\_.

gatecse-2014-set3 operating-system resource-allocation numerical-answers easy

[Answer key](#)

### 5.22.21 Resource Allocation: GATE CSE 2015 Set 2 | Question: 23 top



A system has 6 identical resources and  $N$  processes competing for them. Each process can request at most 2 requests. Which one of the following values of  $N$  could lead to a deadlock?

- A. 1      B. 2      C. 3      D. 4

gatecse-2015-set2 operating-system resource-allocation easy

[Answer key](#)

### 5.22.22 Resource Allocation: GATE CSE 2015 Set 3 | Question: 52 top



Consider the following policies for preventing deadlock in a system with mutually exclusive resources.

- Process should acquire all their resources at the beginning of execution. If any resource is not available, all resources acquired so far are released.
- The resources are numbered uniquely, and processes are allowed to request for resources only in increasing resource numbers
- The resources are numbered uniquely, and processes are allowed to request for resources only in decreasing resource numbers
- The resources are numbered uniquely. A processes is allowed to request for resources only for a resource with resource number larger than its currently held resources

Which of the above policies can be used for preventing deadlock?

- |   |   |
|---|---|
| A. Any one of (I) and (III) but not (II)<br>or (IV) | B. Any one of (I), (III) and (IV) but not<br>(II) |
| C. Any one of (II) and (III) but not (I)<br>or (IV) | D. Any one of (I), (II), (III) and (IV)           |

gatecse-2015-set3 operating-system resource-allocation normal

[Answer key](#)

### 5.22.23 Resource Allocation: GATE CSE 2017 Set 2 | Question: 33 top



A system shares 9 tape drives. The current allocation and maximum requirement of tape drives for that processes are shown below:

Process	Current Allocation	Maximum Requirement
P1	3	7
P2	1	6
P3	3	5

Which of the following best describes current state of the system?

- |                         |                             |
|-------------------------|-----------------------------|
| A. Safe, Deadlocked     | B. Safe, Not Deadlocked     |
| C. Not Safe, Deadlocked | D. Not Safe, Not Deadlocked |

gatecse-2017-set2 operating-system resource-allocation normal

[Answer key](#)

### 5.22.24 Resource Allocation: GATE CSE 2017 Set 2 | Question: 33 (MSQ Version) top



**\*\* MSQ \*\***

A system shares 9 tape drives. The current allocation and maximum requirement of tape drives for that processes are shown below:

Process	Current Allocation	Maximum Requirement
P1	3	7
P2	1	6
P3	3	5

Which of the following best describes the system?

1. Safe state  $P_3 \rightarrow P_2 \rightarrow P_1$  and  $P_3 \rightarrow P_1 \rightarrow P_2$  exists
2. Currently not in a deadlock
3. Deadlock never possible as safe states are present
4. Deadlock is possible in future, even though we have safe state as of now

gatecse-2017-set2 operating-system resource-allocation normal multiple-selects

[Answer key](#)

#### 5.22.25 Resource Allocation: GATE CSE 2022 | Question: 16 top ↗



Which of the following statements is/are TRUE with respect to deadlocks?

- A. Circular wait is a necessary condition for the formation of deadlock.
- B. In a system where each resource has more than one instance, a cycle in its wait-for graph indicates the presence of a deadlock.
- C. If the current allocation of resources to processes leads the system to unsafe state, then deadlock will necessarily occur.
- D. In the resource-allocation graph of a system, if every edge is an assignment edge, then the system is not in deadlock state.

gatecse-2022 operating-system resource-allocation multiple-selects 1-mark

[Answer key](#)

#### 5.22.26 Resource Allocation: GATE IT 2005 | Question: 62 top ↗



Two shared resources  $R_1$  and  $R_2$  are used by processes  $P_1$  and  $P_2$ . Each process has a certain priority for accessing each resource. Let  $T_{ij}$  denote the priority of  $P_i$  for accessing  $R_j$ . A process  $P_i$  can snatch a resource  $R_k$  from process  $P_j$  if  $T_{ik}$  is greater than  $T_{jk}$ .

Given the following :

- I.  $T_{11} > T_{21}$
- II.  $T_{12} > T_{22}$
- III.  $T_{11} < T_{21}$
- IV.  $T_{12} < T_{22}$

Which of the following conditions ensures that  $P_1$  and  $P_2$  can never deadlock?

- A. (I) and (IV)
- B. (II) and (III)
- C. (I) and (II)
- D. None of the above

gateit-2005 operating-system resource-allocation normal

[Answer key](#)

#### 5.22.27 Resource Allocation: GATE IT 2008 | Question: 54 top ↗



An operating system implements a policy that requires a process to release all resources before making a request for another resource. Select the TRUE statement from the following:

- A. Both starvation and deadlock can occur
- B. Starvation can occur but deadlock cannot occur
- C. Starvation cannot occur but deadlock can occur

- D. Neither starvation nor deadlock can occur

gateit-2008 operating-system resource-allocation normal

Answer key 

5.23

### Round Robin Scheduling (1)

#### 5.23.1 Round Robin Scheduling: GATE CSE 2022 | Question: 32



Consider four processes P, Q, R, and S scheduled on a CPU as per round robin algorithm with a time quantum of 4 units. The processes arrive in the order P, Q, R, S, all at time  $t = 0$ . There is exactly one context switch from S to Q, exactly one context switch from R to Q, and exactly two context switches from Q to R. There is no context switch from S to P. Switching to a ready process after the termination of another process is also considered a context switch. Which one of the following is NOT possible as CPU burst time (in time units) of these processes?

- A.  $P = 4, Q = 10, R = 6, S = 2$   
B.  $P = 2, Q = 9, R = 5, S = 1$   
C.  $P = 4, Q = 12, R = 5, S = 4$   
D.  $P = 3, Q = 7, R = 7, S = 3$

gatecse-2022 operating-system process-scheduling round-robin-scheduling 2-marks

Answer key 

5.24

### Runtime Environment (3)

#### 5.24.1 Runtime Environment: GATE CSE 1991 | Question: 02-iii



Match the pairs in the following questions by writing the corresponding letters only.

(a)	Buddy system	(p)	Run time type specification
(b)	Interpretation	(q)	Segmentation
(c)	Pointer type	(r)	Memory allocation
(d)	Virtual memory	(s)	Garbage collection

gate1991 operating-system normal match-the-following runtime-environment

Answer key 

#### 5.24.2 Runtime Environment: GATE CSE 1996 | Question: 2.17



The correct matching for the following pairs is

(A)	Activation record	(1)	Linking loader
(B)	Location counter	(2)	Garbage collection
(C)	Reference counts	(3)	Subroutine call
(D)	Address relocation	(4)	Assembler

- A. A-3 B-4 C-1 D-2   B. A-4 B-3 C-1 D-2   C. A-4 B-3 C-2 D-1   D. A-3 B-4 C-2 D-1

gate1996 operating-system easy runtime-environment

Answer key 

#### 5.24.3 Runtime Environment: GATE CSE 2002 | Question: 2.20



Dynamic linking can cause security concerns because

- A. Security is dynamic  
B. The path for searching dynamic libraries is not known till runtime  
C. Linking is insecure  
D. Cryptographic procedures are not available for dynamic linking

**Answer key****5.25****Semaphore (10)****5.25.1 Semaphore: GATE CSE 1990 | Question: 1-vii**

Semaphore operations are atomic because they are implemented within the OS \_\_\_\_\_.

**Answer key****5.25.2 Semaphore: GATE CSE 1992 | Question: 02,x, ISRO2015-35**

At a particular time of computation, the value of a counting semaphore is 7. Then 20 P operations and 15 V operations were completed on this semaphore. The resulting value of the semaphore is :

- A. 42      B. 2      C. 7      D. 12

**Answer key****5.25.3 Semaphore: GATE CSE 1998 | Question: 1.31**

A counting semaphore was initialized to 10. Then 6P (wait) operations and 4V (signal) operations were completed on this semaphore. The resulting value of the semaphore is

- A. 0      B. 8      C. 10      D. 12

**Answer key****5.25.4 Semaphore: GATE CSE 2008 | Question: 63**

The P and V operations on counting semaphores, where s is a counting semaphore, are defined as follows:

$s = s - 1;$   
 $P(s) : \text{if } s < 0 \text{ then wait;}$

$s = s + 1;$   
 $V(s) : \text{if } s \leq 0 \text{ then wake up process waiting on s;}$

Assume that  $P_b$  and  $V_b$  the wait and signal operations on binary semaphores are provided. Two binary semaphores  $x_b$  and  $y_b$  are used to implement the semaphore operations  $P(s)$  and  $V(s)$  as follows:

$P(s) :$   
 $P_b(x_b);$   
 $s = s - 1;$   
 $\text{if } (s < 0)$   
 $\quad \{$   
 $\quad \quad V_b(x_b);$   
 $\quad \quad P_b(y_b);$   
 $\quad \}$   
 $\text{else } V_b(x_b);$

$V(s) :$   
 $P_b(x_b);$   
 $s = s + 1;$   
 $\text{if } (s \leq 0) V_b(y_b);$   
 $V_b(x_b);$

The initial values of  $x_b$  and  $y_b$  are respectively

- A. 0 and 0      B. 0 and 1      C. 1 and 0      D. 1 and 1

**Answer key**

### 5.25.5 Semaphore: GATE CSE 2016 Set 2 | Question: 49 top



Consider a non-negative counting semaphore  $S$ . The operation  $P(S)$  decrements  $S$ , and  $V(S)$  increments  $S$ . During an execution, 20  $P(S)$  operations and 12  $V(S)$  operations are issued in some order. The largest initial value of  $S$  for which at least one  $P(S)$  operation will remain blocked is \_\_\_\_\_

gatecse-2016-set2 operating-system semaphore normal numerical-answers

Answer key

### 5.25.6 Semaphore: GATE CSE 2020 | Question: 34 top



Each of a set of  $n$  processes executes the following code using two semaphores  $a$  and  $b$  initialized to 1 and 0, respectively. Assume that `count` is a shared variable initialized to 0 and not used in CODE SECTION P.

#### CODE SECTION P

```
wait(a); count=count+1;  
if (count==n) signal (b);  
signal (a); wait (b) ; signal (b);
```

#### CODE SECTION Q

What does the code achieve?

- A. It ensures that no process executes CODE SECTION Q before every process has finished CODE SECTION P.
- B. It ensures that two processes are in CODE SECTION Q at any time.
- C. It ensures that all processes execute CODE SECTION P mutually exclusively.
- D. It ensures that at most  $n - 1$  processes are in CODE SECTION P at any time.

gatecse-2020 operating-system semaphore 2-marks

Answer key

### 5.25.7 Semaphore: GATE CSE 2021 Set 1 | Question: 46 top



Consider the following pseudocode, where  $S$  is a semaphore initialized to 5 in line #2 and `counter` is a shared variable initialized to 0 in line #1. Assume that the increment operation in line #7 is *not* atomic.

```
1. int counter = 0;  
2. Semaphore S = init(5);  
3. void parop(void)  
4. {  
5.     wait(S);  
6.     wait(S);  
7.     counter++;  
8.     signal(S);  
9.     signal(S);  
10. }
```

If five threads execute the function `parop` concurrently, which of the following program behavior(s) is/are possible?

- A. The value of `counter` is 5 after all the threads successfully complete the execution of `parop`
- B. The value of `counter` is 1 after all the threads successfully complete the execution of `parop`
- C. The value of `counter` is 0 after all the threads successfully complete the execution of `parop`
- D. There is a deadlock involving all the threads

gatecse-2021-set1 multiple-selects operating-system process-synchronization semaphore 2-marks

Answer key

### 5.25.8 Semaphore: GATE CSE 2022 | Question: 9 top



Consider the following threads,  $T_1$ ,  $T_2$ , and  $T_3$  executing on a single processor, synchronized using three binary semaphore variables,  $S_1$ ,  $S_2$ , and  $S_3$ , operated upon using standard `wait()` and `signal()`. The threads can be context switched in any order and at any time.

T <sub>1</sub>	T <sub>2</sub>	T <sub>3</sub>
while(true){ wait(S <sub>3</sub> ); print("C"); signal(S <sub>2</sub> ); }	while(true){ wait(S <sub>1</sub> ); print("B"); signal(S <sub>3</sub> ); }	while(true){ wait(S <sub>2</sub> ); print("A"); signal(S <sub>1</sub> ); }

Which initialization of the semaphores would print the sequence BCABCABC...?

- A. S<sub>1</sub> = 1; S<sub>2</sub> = 1; S<sub>3</sub> = 1  
 C. S<sub>1</sub> = 1; S<sub>2</sub> = 0; S<sub>3</sub> = 0  
 B. S<sub>1</sub> = 1; S<sub>2</sub> = 1; S<sub>3</sub> = 0  
 D. S<sub>1</sub> = 0; S<sub>2</sub> = 1; S<sub>3</sub> = 1

gatecse-2022 operating-system process-synchronization semaphore 1-mark

Answer key 



### 5.25.9 Semaphore: GATE CSE 2023 | Question: 28

Consider the two functions **incr** and **decr** shown below.

```
incr(){      decr(){  
    wait(s);    wait(s);  
    X = X+1;    X = X-1;  
    signal(s);  signal(s);  
}
```

There are 5 threads each invoking **incr** once, and 3 threads each invoking **decr** once, on the same shared variable X. The initial value of X is 10.

Suppose there are two implementations of the semaphore s, as follows:

**I-1:** s is a binary semaphore initialized to 1.

**I-2:** s is a counting semaphore initialized to 2.

Let V<sub>1</sub>, V<sub>2</sub> be the values of X at the end of execution of all the threads with implementations **I-1**, **I-2**, respectively.

Which one of the following choices corresponds to the minimum possible values of V<sub>1</sub>, V<sub>2</sub>, respectively?

- A. 15,7                  B. 7,7                  C. 12,7                  D. 12,8

gatecse-2023 operating-system semaphore 2-marks

Answer key 



### 5.25.10 Semaphore: GATE IT 2006 | Question: 57

The wait and signal operations of a monitor are implemented using semaphores as follows. In the following,

- x is a condition variable,
- mutex is a semaphore initialized to 1,
- x\_sem is a semaphore initialized to 0,
- x\_count is the number of processes waiting on semaphore x\_sem, initially 0,
- next is a semaphore initialized to 0,
- next\_count is the number of processes waiting on semaphore next, initially 0.

The body of each procedure that is visible outside the monitor is replaced with the following:

```
P(mutex);  
...  
body of procedure  
...  
if (next_count > 0)  
    V(next);  
else  
    V(mutex);
```

Each occurrence of x.wait is replaced with the following:

```

x_count = x_count + 1;
if (next_count > 0)
    V(next);
else
    V(mutex);
----- E1;
x_count = x_count - 1;

```

Each occurrence of  $x.signal$  is replaced with the following:

```

if (x_count > 0)
{
    next_count = next_count + 1;
    ----- E2;
    P(next);
    next_count = next_count - 1;
}

```

For correct implementation of the monitor, statements  $E1$  and  $E2$  are, respectively,

- |                         |                           |
|-------------------------|---------------------------|
| A. $P(x\_sem), V(next)$ | B. $V(next), P(x\_sem)$   |
| C. $P(next), V(x\_sem)$ | D. $P(x\_sem), V(x\_sem)$ |

gateit-2006 operating-system process-synchronization semaphore normal

[Answer key](#)

5.26

System Call (1) [top](#)

#### 5.26.1 System Call: GATE CSE 2021 Set 1 | Question: 14 [top](#)



Which of the following standard  $C$  library functions will always invoke a system call when executed from a single-threaded process in a UNIX/Linux operating system?

- |                      |                        |                       |                        |
|----------------------|------------------------|-----------------------|------------------------|
| A. <code>exit</code> | B. <code>malloc</code> | C. <code>sleep</code> | D. <code>strlen</code> |
|----------------------|------------------------|-----------------------|------------------------|

gatecse-2021-set1 multiple-selects operating-system system-call 1-mark

[Answer key](#)

5.27

Threads (8) [top](#)

#### 5.27.1 Threads: GATE CSE 2004 | Question: 11 [top](#)



Consider the following statements with respect to user-level threads and kernel-supported threads

- context switch is faster with kernel-supported threads
- for user-level threads, a system call can block the entire process
- Kernel supported threads can be scheduled independently
- User level threads are transparent to the kernel

Which of the above statements are true?

- |                              |                        |
|------------------------------|------------------------|
| A. (II), (III) and (IV) only | B. (II) and (III) only |
| C. (I) and (III) only        | D. (I) and (II) only   |

gatecse-2004 operating-system threads normal

[Answer key](#)

#### 5.27.2 Threads: GATE CSE 2007 | Question: 17 [top](#)



Consider the following statements about user level threads and kernel level threads. Which one of the following statements is FALSE?

- Context switch time is longer for kernel level threads than for user level threads.
- User level threads do not need any hardware support.
- Related kernel level threads can be scheduled on different processors in a multi-processor system.

D. Blocking one kernel level thread blocks all related threads.

gatecse-2007 operating-system threads normal

Answer key

### 5.27.3 Threads: GATE CSE 2011 | Question: 16, UGCNET-June2013-III: 65 top



A thread is usually defined as a light weight process because an Operating System (OS) maintains smaller data structure for a thread than for a process. In relation to this, which of the following statement is correct?

- A. OS maintains only scheduling and accounting information for each thread
- B. OS maintains only CPU registers for each thread
- C. OS does not maintain virtual memory state for each thread
- D. OS does not maintain a separate stack for each thread

gatecse-2011 operating-system threads normal ugcnetcse-june2013-paper3

Answer key

### 5.27.4 Threads: GATE CSE 2014 Set 1 | Question: 20 top



Which one of the following is **FALSE**?

- A. User level threads are not scheduled by the kernel.
- B. When a user level thread is blocked, all other threads of its process are blocked.
- C. Context switching between user level threads is faster than context switching between kernel level threads.
- D. Kernel level threads cannot share the code segment.

gatecse-2014-set1 operating-system threads normal

Answer key

### 5.27.5 Threads: GATE CSE 2017 Set 1 | Question: 18 top



Threads of a process share

- A. global variables but not heap
- C. neither global variables nor heap
- B. heap but not global variables
- D. both heap and global variables

gatecse-2017-set1 operating-system threads

Answer key

### 5.27.6 Threads: GATE CSE 2017 Set 2 | Question: 07 top



Which of the following is/are shared by all the threads in a process?

- I. Program counter
  - II. Stack
  - III. Address space
  - IV. Registers
- 
- A. (I) and (II) only
  - B. (III) only
  - C. (IV) only
  - D. (III) and (IV) only

gatecse-2017-set2 operating-system threads

Answer key

### 5.27.7 Threads: GATE CSE 2021 Set 2 | Question: 42 top



Consider the following multi-threaded code segment (in a mix of C and pseudo-code), invoked by two processes  $P_1$  and  $P_2$ , and each of the processes spawns two threads  $T_1$  and  $T_2$ :

```
int x = 0; // global
Lock L1; // global
main () {
    create a thread to execute foo(); // Thread T1
    create a thread to execute foo(); // Thread T2
    wait for the two threads to finish execution;
```

```
print(x);}
```

```
foo() {  
    int y = 0;  
    Acquire L1;  
    x = x + 1;  
    y = y + 1;  
    Release L1;  
    print (y);}
```

Which of the following statement(s) is/are correct?

- A. Both  $P_1$  and  $P_2$  will print the value of  $x$  as 2.
- B. At least of  $P_1$  and  $P_2$  will print the value of  $x$  as 4.
- C. At least one of the threads will print the value of  $y$  as 2.
- D. Both  $T_1$  and  $T_2$ , in both the processes, will print the value of  $y$  as 1.

gatecse-2021-set2 multiple-selects operating-system threads 2-marks

[Answer key](#)



#### 5.27.8 Threads: GATE IT 2004 | Question: 14 [top](#)

Which one of the following is NOT shared by the threads of the same process ?

- A. Stack
- B. Address Space
- C. File Descriptor Table
- D. Message Queue

gateit-2004 operating-system easy threads

[Answer key](#)

#### 5.28

#### Translation Lookaside Buffer (1) [top](#)



#### 5.28.1 Translation Lookaside Buffer: GATE CSE 2022 | Question: 28 [top](#)

Which one of the following statements is FALSE?

- A. The TLB performs an associative search in parallel on all its valid entries using page number of incoming virtual address.
- B. If the virtual address of a word given by CPU has a TLB hit, but the subsequent search for the word results in a cache miss, then the word will always be present in the main memory.
- C. The memory access time using a given inverted page table is always same for all incoming virtual addresses.
- D. In a system that uses hashed page tables, if two distinct virtual addresses  $V_1$  and  $V_2$  map to the same value while hashing, then the memory access time of these addresses will not be the same.

gatecse-2022 operating-system memory-management translation-lookaside-buffer 2-marks

[Answer key](#)

#### 5.29

#### Virtual Memory (39) [top](#)



#### 5.29.1 Virtual Memory: GATE CSE 1989 | Question: 2-iv [top](#)

Match the pairs in the following:

(A)	Virtual memory	(p)	Temporal Locality
(B)	Shared memory	(q)	Spatial Locality
(C)	Look-ahead buffer	(r)	Address Translation
(D)	Look-aside buffer	(s)	Mutual Exclusion

match-the-following gate1989 operating-system virtual-memory

[Answer key](#)

### 5.29.2 Virtual Memory: GATE CSE 1990 | Question: 1-V [top](#)

Under paged memory management scheme, simple lock and key memory protection arrangement may still be required if the \_\_\_\_\_ processors do not have address mapping hardware.

gate1990 operating-system virtual-memory fill-in-the-blanks

[Answer key](#)

### 5.29.3 Virtual Memory: GATE CSE 1990 | Question: 7-b [top](#)

In a two-level virtual memory, the memory access time for main memory,  $t_M = 10^{-8}$  sec, and the memory access time for the secondary memory,  $t_D = 10^{-3}$  sec. What must be the hit ratio,  $H$  such that the access efficiency is within 80 percent of its maximum value?

gate1990 descriptive operating-system virtual-memory

[Answer key](#)

### 5.29.4 Virtual Memory: GATE CSE 1991 | Question: 03-xi [top](#)

Indicate all the false statements from the statements given below:

- A. The amount of virtual memory available is limited by the availability of the secondary memory
- B. Any implementation of a critical section requires the use of an indivisible machine- instruction ,such as test-and-set.
- C. The use of monitors ensure that no dead-locks will be caused .
- D. The LRU page-replacement policy may cause thrashing for some type of programs.
- E. The best fit techniques for memory allocation ensures that memory will never be fragmented.

gate1991 operating-system virtual-memory normal multiple-selects

[Answer key](#)

### 5.29.5 Virtual Memory: GATE CSE 1994 | Question: 1.21 [top](#)

Which one of the following statements is true?

- A. Macro definitions cannot appear within other macro definitions in assembly language programs
- B. Overlaying is used to run a program which is longer than the address space of a computer
- C. Virtual memory can be used to accommodate a program which is longer than the address space of a computer
- D. It is not possible to write interrupt service routines in a high level language

gate1994 operating-system normal virtual-memory

[Answer key](#)

### 5.29.6 Virtual Memory: GATE CSE 1995 | Question: 1.7 [top](#)

In a paged segmented scheme of memory management, the segment table itself must have a page table because

- A. The segment table is often too large to fit in one page
- B. Each segment is spread over a number of pages
- C. Segment tables point to page tables and not to the physical locations of the segment
- D. The processor's description base register points to a page table

gate1995 operating-system virtual-memory normal

[Answer key](#)

### 5.29.7 Virtual Memory: GATE CSE 1995 | Question: 2.16 [top](#)

In a virtual memory system the address space specified by the address lines of the CPU must be \_\_\_\_\_ than the physical memory size and \_\_\_\_\_ than the secondary storage size.

- A. smaller, smaller  
C. larger, smaller

- B. smaller, larger  
D. larger, larger

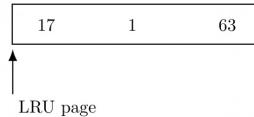
gate1995 operating-system virtual-memory normal

Answer key

#### 5.29.8 Virtual Memory: GATE CSE 1996 | Question: 7



A demand paged virtual memory system uses 16 bit virtual address, page size of 256 bytes, and has 1 Kbyte of main memory. LRU page replacement is implemented using the list, whose current status (page number is decimal) is



For each hexadecimal address in the address sequence given below,

00FF, 010D, 10FF, 11B0

indicate

- the new status of the list
- page faults, if any, and
- page replacements, if any.

gate1996 operating-system virtual-memory normal descriptive

Answer key

#### 5.29.9 Virtual Memory: GATE CSE 1998 | Question: 2.18, UGCNET-June2012-III: 48



If an instruction takes  $i$  microseconds and a page fault takes an additional  $j$  microseconds, the effective instruction time if on the average a page fault occurs every  $k$  instruction is:

- A.  $i + \frac{j}{k}$       B.  $i + (j \times k)$       C.  $\frac{i+j}{k}$       D.  $(i+j) \times k$

gate1998 operating-system virtual-memory easy ugcnetcse-june2012-paper3

Answer key

#### 5.29.10 Virtual Memory: GATE CSE 1999 | Question: 19



A certain computer system has the segmented paging architecture for virtual memory. The memory is byte addressable. Both virtual and physical address spaces contain  $2^{16}$  bytes each. The virtual address space is divided into 8 non-overlapping equal size segments. The memory management unit (MMU) has a hardware segment table, each entry of which contains the physical address of the page table for the segment. Page tables are stored in the main memory and consists of 2 byte page table entries.

- What is the minimum page size in bytes so that the page table for a segment requires at most one page to store it? Assume that the page size can only be a power of 2.
- Now suppose that the pages size is 512 bytes. It is proposed to provide a TLB (Transaction look-aside buffer) for speeding up address translation. The proposed TLB will be capable of storing page table entries for 16 recently referenced virtual pages, in a fast cache that will use the direct mapping scheme. What is the number of tag bits that will need to be associated with each cache entry?
- Assume that each page table entry contains (besides other information) 1 valid bit, 3 bits for page protection and 1 dirty bit. How many bits are available in page table entry for storing the aging information for the page? Assume that the page size is 512 bytes.

gate1999 operating-system virtual-memory normal descriptive

Answer key

### 5.29.11 Virtual Memory: GATE CSE 1999 | Question: 2.10 top



A multi-user, multi-processing operating system cannot be implemented on hardware that does not support

- A. Address translation
- B. DMA for disk transfer
- C. At least two modes of CPU execution (privileged and non-privileged)
- D. Demand paging

gate1999 operating-system normal virtual-memory

[Answer key](#)

### 5.29.12 Virtual Memory: GATE CSE 1999 | Question: 2.11 top



Which of the following is/are advantage(s) of virtual memory?

- A. Faster access to memory on an average.
- B. Processes can be given protected address spaces.
- C. Linker can assign addresses independent of where the program will be loaded in physical memory.
- D. Program larger than the physical memory size can be run.

gate1999 operating-system virtual-memory easy

[Answer key](#)

### 5.29.13 Virtual Memory: GATE CSE 2000 | Question: 2.22 top



Suppose the time to service a page fault is on the average 10 milliseconds, while a memory access takes 1 microsecond. Then a 99.99% hit ratio results in average memory access time of

- |                        |                        |
|------------------------|------------------------|
| A. 1.9999 milliseconds | B. 1 millisecond       |
| C. 9.999 microseconds  | D. 1.9999 microseconds |

gatecse-2000 operating-system easy virtual-memory

[Answer key](#)

### 5.29.14 Virtual Memory: GATE CSE 2001 | Question: 1.20 top



Where does the swap space reside?

- A. RAM
- B. Disk
- C. ROM
- D. On-chip cache

gatecse-2001 operating-system easy virtual-memory

[Answer key](#)

### 5.29.15 Virtual Memory: GATE CSE 2001 | Question: 1.8 top



Which of the following statements is false?

- A. Virtual memory implements the translation of a program's address space into physical memory address space
- B. Virtual memory allows each program to exceed the size of the primary memory
- C. Virtual memory increases the degree of multiprogramming
- D. Virtual memory reduces the context switching overhead

gatecse-2001 operating-system virtual-memory normal

[Answer key](#)

### 5.29.16 Virtual Memory: GATE CSE 2001 | Question: 2.21 top



Consider a machine with 64 MB physical memory and a 32-bit virtual address space. If the page size is 4 KB, what is the approximate size of the page table?

- A. 16 MB
- B. 8 MB
- C. 2 MB
- D. 24 MB

gatecse-2001 operating-system virtual-memory normal

Answer key 

### 5.29.17 Virtual Memory: GATE CSE 2002 | Question: 19 top

A computer uses  $32 - bit$  virtual address, and  $32 - bit$  physical address. The physical memory is byte addressable, and the page size is 4 Kbytes. It is decided to use two level page tables to translate from virtual address to physical address. Equal number of bits should be used for indexing first level and second level page table, and the size of each table entry is 4 bytes.

- A. Give a diagram showing how a virtual address would be translated to a physical address.
- B. What is the number of page table entries that can be contained in each page?
- C. How many bits are available for storing protection and other information in each page table entry?

gatecse-2002 operating-system virtual-memory normal descriptive

Answer key 

### 5.29.18 Virtual Memory: GATE CSE 2003 | Question: 26 top

In a system with 32 bit virtual addresses and 1 KB page size, use of one-level page tables for virtual to physical address translation is not practical because of

- A. the large amount of internal fragmentation
- B. the large amount of external fragmentation
- C. the large memory overhead in maintaining page tables
- D. the large computation overhead in the translation process

gatecse-2003 operating-system virtual-memory normal

Answer key 

### 5.29.19 Virtual Memory: GATE CSE 2003 | Question: 78 top

A processor uses  $2 - level$  page tables for virtual to physical address translation. Page tables for both levels are stored in the main memory. Virtual and physical addresses are both 32 bits wide. The memory is byte addressable. For virtual to physical address translation, the 10 most significant bits of the virtual address are used as index into the first level page table while the next 10 bits are used as index into the second level page table. The 12 least significant bits of the virtual address are used as offset within the page. Assume that the page table entries in both levels of page tables are 4 bytes wide. Further, the processor has a translation look-aside buffer (TLB), with a hit rate of 96%. The TLB caches recently used virtual page numbers and the corresponding physical page numbers. The processor also has a physically addressed cache with a hit rate of 90%. Main memory access time is 10 ns, cache access time is 1 ns, and TLB access time is also 1 ns.

Assuming that no page faults occur, the average time taken to access a virtual address is approximately (to the nearest 0.5 ns)

- A. 1.5 ns
- B. 2 ns
- C. 3 ns
- D. 4 ns

gatecse-2003 operating-system normal virtual-memory

Answer key 

### 5.29.20 Virtual Memory: GATE CSE 2003 | Question: 79 top

A processor uses 2-level page tables for virtual to physical address translation. Page tables for both levels are stored in the main memory. Virtual and physical addresses are both 32 bits wide. The memory is byte addressable. For virtual to physical address translation, the 10 most significant bits of the virtual address are used as index into the first level page table while the next 10 bits are used as index into the second level page table. The 12 least significant bits of the virtual address are used as offset within the page. Assume that the page table entries in both levels of page tables are 4 bytes wide. Further, the processor has a translation look-aside buffer (TLB), with a hit rate of 96%. The TLB caches recently used virtual page numbers and the corresponding physical page numbers. The processor also has a physically addressed cache with a hit rate of 90%. Main memory access time is 10 ns, cache access time is 1 ns, and TLB access time is also 1 ns.

Suppose a process has only the following pages in its virtual address space: two contiguous code pages starting at virtual address  $0x00000000$ , two contiguous data pages starting at virtual address  $0x00400000$ , and a stack

page starting at virtual address  $0xFFFFF000$ . The amount of memory required for storing the page tables of this process is

- A. 8 KB      B. 12 KB      C. 16 KB      D. 20 KB

gatecse-2003 operating-system normal virtual-memory

Answer key 

#### 5.29.21 Virtual Memory: GATE CSE 2006 | Question: 62, ISRO2016-50

A CPU generates 32-bit virtual addresses. The page size is 4 KB. The processor has a translation look-aside buffer (TLB) which can hold a total of 128 page table entries and is 4-way set associative. The minimum size of the TLB tag is:

- A. 11 bits      B. 13 bits      C. 15 bits      D. 20 bits

gatecse-2006 operating-system virtual-memory normal isro2016

Answer key 

#### 5.29.22 Virtual Memory: GATE CSE 2006 | Question: 63, UGCNET-June2012-III: 45

A computer system supports 32-bit virtual addresses as well as 32-bit physical addresses. Since the virtual address space is of the same size as the physical address space, the operating system designers decide to get rid of the virtual memory entirely. Which one of the following is true?

- A. Efficient implementation of multi-user support is no longer possible
- B. The processor cache organization can be made more efficient now
- C. Hardware support for memory management is no longer needed
- D. CPU scheduling can be made more efficient now

gatecse-2006 operating-system virtual-memory normal ugcnetcse-june2012-paper3

Answer key 

#### 5.29.23 Virtual Memory: GATE CSE 2008 | Question: 67

A processor uses 36 bit physical address and 32 bit virtual addresses, with a page frame size of 4 Kbytes. Each page table entry is of size 4 bytes. A three level page table is used for virtual to physical address translation, where the virtual address is used as follows:

- Bits 30 – 31 are used to index into the first level page table.
- Bits 21 – 29 are used to index into the 2nd level page table.
- Bits 12 – 20 are used to index into the 3rd level page table.
- Bits 0 – 11 are used as offset within the page.

The number of bits required for addressing the next level page table(or page frame) in the page table entry of the first, second and third level page tables are respectively

- A. 20,20,20      B. 24,24,24      C. 24,24,20      D. 25,25,24

gatecse-2008 operating-system virtual-memory normal

Answer key 

#### 5.29.24 Virtual Memory: GATE CSE 2009 | Question: 10

The essential content(s) in each entry of a page table is / are

- A. Virtual page number
- B. Page frame number
- C. Both virtual page number and page frame number
- D. Access right information

gatecse-2009 operating-system virtual-memory easy

Answer key 

### 5.29.25 Virtual Memory: GATE CSE 2009 | Question: 34 top



A multilevel page table is preferred in comparison to a single level page table for translating virtual address to physical address because

- A. It reduces the memory access time to read or write a memory location.
- B. It helps to reduce the size of page table needed to implement the virtual address space of a process
- C. It is required by the translation lookaside buffer.
- D. It helps to reduce the number of page faults in page replacement algorithms.

gatecse-2009 operating-system virtual-memory easy

[Answer key](#)

### 5.29.26 Virtual Memory: GATE CSE 2011 | Question: 20, UGCNET-June2013-II: 48 top



Let the page fault service time be 10 milliseconds(ms) in a computer with average memory access time being 20 nanoseconds (ns). If one page fault is generated every  $10^6$  memory accesses, what is the effective access time for memory?

- A. 21 ns
- B. 30 ns
- C. 23 ns
- D. 35 ns

gatecse-2011 operating-system virtual-memory normal ugcnetcse-june2013-paper2

[Answer key](#)

### 5.29.27 Virtual Memory: GATE CSE 2013 | Question: 52 top



A computer uses 46-bit virtual address, 32-bit physical address, and a three-level paged page table organization. The page table base register stores the base address of the first-level table (T1), which occupies exactly one page. Each entry of T1 stores the base address of a page of the second-level table (T2). Each entry of T2 stores the base address of a page of the third-level table (T3). Each entry of T3 stores a page table entry (PTE). The PTE is 32 bits in size. The processor used in the computer has a 1 MB 16 way set associative virtually indexed physically tagged cache. The cache block size is 64 bytes.

What is the size of a page in KB in this computer?

- A. 2
- B. 4
- C. 8
- D. 16

gatecse-2013 operating-system virtual-memory normal

[Answer key](#)

### 5.29.28 Virtual Memory: GATE CSE 2013 | Question: 53 top



A computer uses 46-bit virtual address, 32-bit physical address, and a three-level paged page table organization. The page table base register stores the base address of the first-level table (T1), which occupies exactly one page. Each entry of T1 stores the base address of a page of the second-level table (T2). Each entry of T2 stores the base address of a page of the third-level table (T3). Each entry of T3 stores a page table entry (PTE). The PTE is 32 bits in size. The processor used in the computer has a 1 MB 16 way set associative virtually indexed physically tagged cache. The cache block size is 64 bytes.

What is the minimum number of page colours needed to guarantee that no two synonyms map to different sets in the processor cache of this computer?

- A. 2
- B. 4
- C. 8
- D. 16

gatecse-2013 normal operating-system virtual-memory

[Answer key](#)

### 5.29.29 Virtual Memory: GATE CSE 2014 Set 3 | Question: 33 top



Consider a paging hardware with a  $TLB$ . Assume that the entire page table and all the pages are in the physical memory. It takes 10 milliseconds to search the  $TLB$  and 80 milliseconds to access the physical

memory. If the  $TLB$  hit ratio is 0.6, the effective memory access time (in milliseconds) is \_\_\_\_\_.

gatecse-2014-set3 operating-system virtual-memory numerical-answers normal

Answer key 

#### 5.29.30 Virtual Memory: GATE CSE 2015 Set 1 | Question: 12

Consider a system with byte-addressable memory, 32-bit logical addresses, 4 kilobyte page size and page table entries of 4 bytes each. The size of the page table in the system in megabytes is \_\_\_\_\_.

gatecse-2015-set1 operating-system virtual-memory easy numerical-answers

Answer key 

#### 5.29.31 Virtual Memory: GATE CSE 2015 Set 2 | Question: 25

A computer system implements a 40-bit virtual address, page size of 8 kilobytes, and a 128-entry translation look-aside buffer (TLB) organized into 32 sets each having 4 ways. Assume that the TLB tag does not store any process id. The minimum length of the TLB tag in bits is \_\_\_\_\_.

gatecse-2015-set2 operating-system virtual-memory easy numerical-answers

Answer key 

#### 5.29.32 Virtual Memory: GATE CSE 2015 Set 2 | Question: 47

A computer system implements 8 kilobyte pages and a 32-bit physical address space. Each page table entry contains a valid bit, a dirty bit, three permission bits, and the translation. If the maximum size of the page table of a process is 24 megabytes, the length of the virtual address supported by the system is \_\_\_\_\_ bits.

gatecse-2015-set2 operating-system virtual-memory normal numerical-answers

Answer key 

#### 5.29.33 Virtual Memory: GATE CSE 2016 Set 1 | Question: 47

Consider a computer system with 40-bit virtual addressing and page size of sixteen kilobytes. If the computer system has a one-level page table per process and each page table entry requires 48 bits, then the size of the per-process page table is \_\_\_\_\_ megabytes.

gatecse-2016-set1 operating-system virtual-memory easy numerical-answers

Answer key 

#### 5.29.34 Virtual Memory: GATE CSE 2018 | Question: 10

Consider a process executing on an operating system that uses demand paging. The average time for a memory access in the system is  $M$  units if the corresponding memory page is available in memory, and  $D$  units if the memory access causes a page fault. It has been experimentally measured that the average time taken for a memory access in the process is  $X$  units.

Which one of the following is the correct expression for the page fault rate experienced by the process.

- A.  $(D - M)/(X - M)$  B.  $(X - M)/D - M)$  C.  $(D - X)/D - M)$  D.  $(X - M)/D - X)$

gatecse-2018 operating-system virtual-memory normal 1-mark

Answer key 

#### 5.29.35 Virtual Memory: GATE CSE 2019 | Question: 33

Assume that in a certain computer, the virtual addresses are 64 bits long and the physical addresses are 48 bits long. The memory is word addressable. The page size is 8 kB and the word size is 4 bytes. The Translation Look-aside Buffer (TLB) in the address translation path has 128 valid entries. At most how many distinct virtual addresses can be translated without any TLB miss?

- A.  $16 \times 2^{10}$  B.  $256 \times 2^{10}$   
C.  $4 \times 2^{20}$  D.  $8 \times 2^{20}$

**Answer key****5.29.36 Virtual Memory: GATE CSE 2020 | Question: 53**

Consider a paging system that uses 1-level page table residing in main memory and a TLB for address translation. Each main memory access takes 100 ns and TLB lookup takes 20 ns. Each page transfer to/from the disk takes 5000 ns. Assume that the TLB hit ratio is 95%, page fault rate is 10%. Assume that for 20% of the total page faults, a dirty page has to be written back to disk before the required page is read from disk. TLB update time is negligible. The average memory access time in ns (round off to 1 decimal places) is

**Answer key****5.29.37 Virtual Memory: GATE IT 2004 | Question: 66**

In a virtual memory system, size of the virtual address is 32-bit, size of the physical address is 30-bit, page size is 4 Kbyte and size of each page table entry is 32-bit. The main memory is byte addressable. Which one of the following is the maximum number of bits that can be used for storing protection and other information in each page table entry?

- A. 2      B. 10      C. 12      D. 14

**Answer key****5.29.38 Virtual Memory: GATE IT 2008 | Question: 16**

A paging scheme uses a Translation Look-aside Buffer (TLB). A TLB-access takes 10 ns and the main memory access takes 50 ns. What is the effective access time(in ns) if the TLB hit ratio is 90% and there is no page-fault?

- A. 54      B. 60      C. 65      D. 75

**Answer key****5.29.39 Virtual Memory: GATE IT 2008 | Question: 56**

Match the following flag bits used in the context of virtual memory management on the left side with the different purposes on the right side of the table below.

Name of the bit	Purpose
I. Dirty	a. Page initialization
II. R/W	b. Write-back policy
III. Reference	c. Page protection
IV. Valid	d. Page replacement policy

- A. I-d, II-a, III-b, IV-c  
B. I-b, II-c, III-a, IV-d  
C. I-c, II-d, III-a, IV-b  
D. I-b, II-c, III-d, IV-a

**Answer key****Answer Keys**

5.1.1	C
5.2.4	A
5.4.4	N/A

5.1.2	B
5.3.1	0.6
5.4.5	9.006

5.2.1	2
5.4.1	N/A
5.4.6	D

5.2.2	A
5.4.2	N/A
5.4.7	N/A

5.2.3	A;B;C
5.4.3	B
5.4.8	N/A

5.4.9	D	5.4.10	D	5.4.11	A	5.4.12	800	5.4.13	A
5.4.14	C	5.4.15	B	5.4.16	A	5.4.17	B	5.4.18	C
5.4.19	C	5.4.20	B	5.4.21	B	5.4.23	14020	5.4.24	6.1 : 6.2
5.4.25	85	5.4.26	C	5.4.27	D	5.4.28	B	5.4.29	D
5.5.1	N/A	5.5.2	N/A	5.5.3	N/A	5.5.4	C	5.5.5	B
5.5.6	D	5.5.7	B	5.5.8	3	5.5.9	10	5.5.11	B
5.5.12	C	5.5.13	B	5.5.14	C	5.6.1	N/A	5.6.2	C
5.6.3	D	5.6.4	99.55 : 99.65	5.6.5	D	5.6.6	4.0 : 4.1	5.6.7	A;C
5.6.8	153	5.6.9	B	5.7.1	C	5.7.2	B	5.7.3	C
5.7.4	31	5.7.5	C;D	5.7.6	C	5.8.1	B	5.9.1	90.00
5.9.2	D	5.9.3	A	5.9.4	C	5.9.5	C	5.9.6	D
5.9.7	A	5.10.1	A	5.10.2	B	5.10.3	C	5.10.4	A
5.10.5	B	5.10.6	C	5.11.1	4096	5.12.1	3.2	5.12.2	N/A
5.12.3	B	5.12.4	B	5.12.5	10000	5.12.6	A	5.12.7	C
5.12.8	B	5.12.9	B	5.13.1	5	5.14.1	A	5.14.2	D
5.14.3	B	5.15.1	N/A	5.15.2	B	5.15.3	B	5.15.4	C
5.15.5	C	5.15.6	B	5.15.7	C	5.15.8	C	5.15.9	B
5.15.10	A	5.15.11	C	5.15.12	B	5.15.13	A	5.15.14	C
5.15.15	A	5.15.16	A	5.15.17	B	5.15.18	7	5.15.19	D
5.15.20	6	5.15.21	A	5.15.22	1	5.15.23	D	5.15.24	B
5.15.25	A;C	5.15.26	4108 : 4108	5.15.27	C	5.15.28	A	5.15.29	B
5.16.1	A	5.17.1	N/A	5.17.2	N/A	5.17.3	N/A	5.18.1	B
5.18.2	C	5.18.3	B	5.18.4	B	5.19.1	B;C;D	5.20.1	N/A
5.20.2	N/A	5.20.3	N/A	5.20.4	C	5.20.5	B	5.20.6	A
5.20.7	D	5.20.8	A	5.20.9	N/A	5.20.10	19	5.20.11	B
5.20.12	D	5.20.13	A	5.20.14	B	5.20.15	A	5.20.16	B
5.20.17	A	5.20.18	B	5.20.19	C	5.20.20	D	5.20.21	A
5.20.22	C	5.20.23	B	5.20.24	7.2	5.20.25	1000	5.20.26	5.5
5.20.27	12	5.20.28	D	5.20.29	C	5.20.30	A	5.20.31	8.25
5.20.32	3	5.20.33	29	5.20.34	2	5.20.35	C	5.20.36	5.25:5.26
5.20.37	12 : 12	5.20.38	A;C;D	5.20.39	C;D	5.20.40	D	5.20.41	D
5.20.42	B	5.20.43	D	5.20.44	C	5.21.1	D	5.21.2	N/A
5.21.3	N/A	5.21.4	N/A	5.21.5	N/A	5.21.6	N/A	5.21.7	N/A
5.21.8	N/A	5.21.9	N/A	5.21.10	C	5.21.11	C	5.21.12	N/A
5.21.13	D	5.21.14	N/A	5.21.15	B	5.21.16	N/A	5.21.17	N/A
5.21.18	B	5.21.19	N/A	5.21.20	B	5.21.21	N/A	5.21.22	N/A
5.21.23	N/A	5.21.24	B	5.21.25	C	5.21.26	D	5.21.28	B
5.21.29	B	5.21.30	D	5.21.31	A	5.21.32	A	5.21.33	A
5.21.34	B	5.21.35	D	5.21.36	C	5.21.37	C	5.21.38	3
5.21.39	A	5.21.41	C	5.21.42	D	5.21.43	C	5.21.44	80

5.21.45	A	5.21.46	D	5.21.47	A	5.21.48	B	5.21.49	A
5.21.50	C	5.21.51	C	5.21.52	D	5.22.1	N/A	5.22.2	N/A
5.22.4	D;E	5.22.5	N/A	5.22.6	N/A	5.22.7	C	5.22.8	N/A
5.22.9	B	5.22.10	C	5.22.11	N/A	5.22.12	C	5.22.13	B
5.22.14	C	5.22.15	A	5.22.16	A	5.22.17	B	5.22.18	B
5.22.19	B	5.22.21	D	5.22.22	D	5.22.23	B	5.22.24	Q-Q
5.22.26	C	5.22.27	B	5.23.1	D	5.24.1	N/A	5.24.2	D
5.24.3	B	5.25.1	N/A	5.25.2	B	5.25.3	B	5.25.4	C
5.25.5	7	5.25.6	A	5.25.7	A;B;D	5.25.8	C	5.25.9	C
5.25.10	D	5.26.1	A;C	5.27.2	D	5.27.3	C	5.27.4	D
5.27.5	D	5.27.6	B	5.27.7	A;D	5.27.8	A	5.28.1	C
5.29.1	N/A	5.29.2	N/A	5.29.3	99.99	5.29.4	B;C;E	5.29.5	A
5.29.6	A	5.29.7	C	5.29.8	N/A	5.29.9	A	5.29.10	N/A
5.29.11	A;C	5.29.12	B;D	5.29.13	D	5.29.14	B	5.29.15	D
5.29.16	C	5.29.17	N/A	5.29.18	C	5.29.19	D	5.29.20	C
5.29.21	C	5.29.22	C	5.29.23	D	5.29.24	B	5.29.25	B
5.29.26	B	5.29.28	C	5.29.29	122	5.29.30	4	5.29.31	22
5.29.32	36	5.29.33	384	5.29.34	B	5.29.35	B	5.29.37	D
5.29.38	C	5.29.39	D						