INDRAPRASTHA INSTITUTE *of*
INFORMATION TECHNOLOGY
DELHI

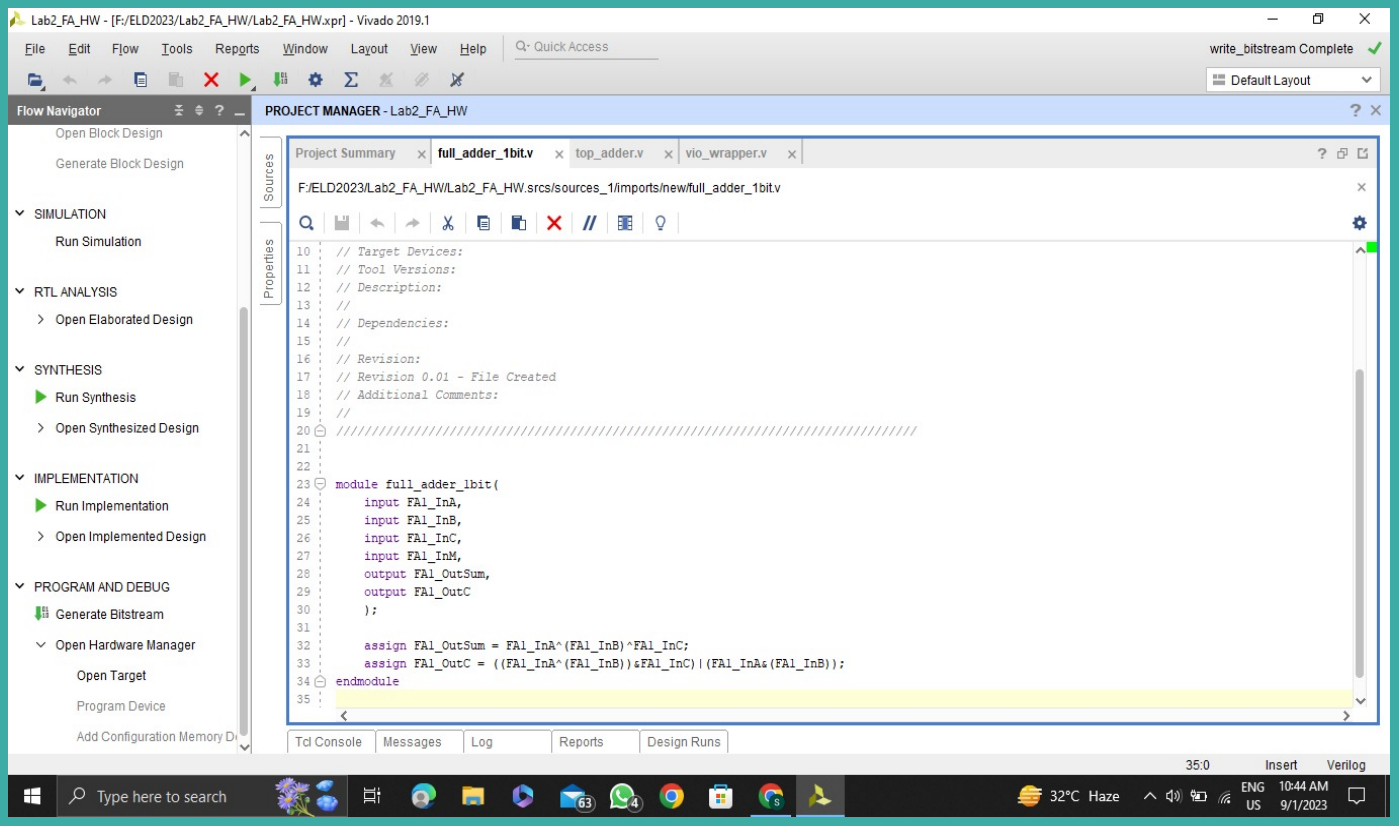
Department
of
Electronics & Communication Engineering

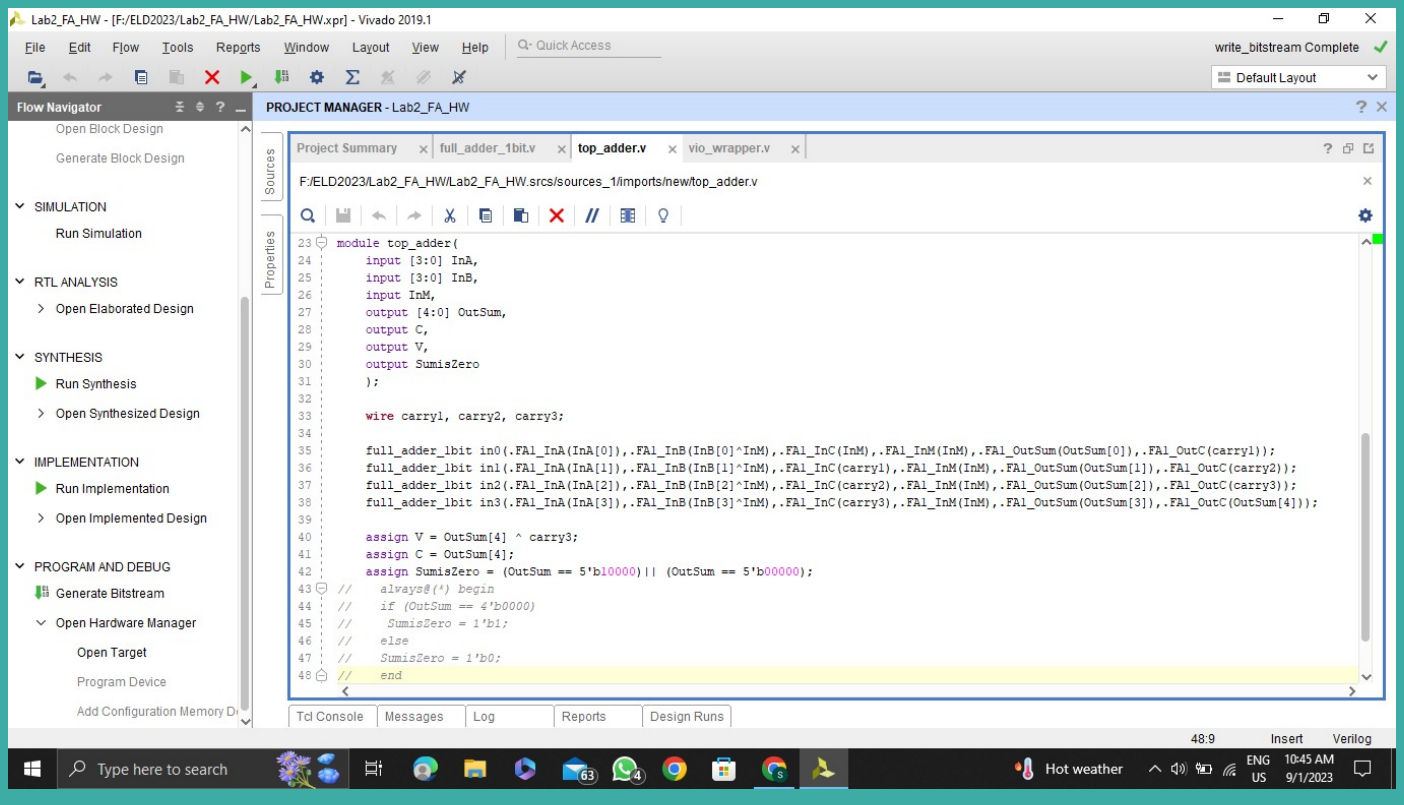
Embedded Logic Design

Lab 2 Submission

SHIVAM SHUKLA
2022478

Source Code


Lab2_FA_HW - [F:/ELD2023/Lab2_FA_HW/Lab2_FA_HW.xpr] - Vivado 2019.1
File Edit Flow Tools Reports Window Layout View Help
write_bitstream Complete
Default Layout
Flow Navigator
PROJECT MANAGER - Lab2_FA_HW
Project Summary
full_adder_1bit.v
top_adder.v
vio_wrapper.v
F:/ELD2023/Lab2_FA_HW/Lab2_FA_HW.srcs/sources_1/imports/new/full_adder_1bit.v
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
Open Target
Program Device
Add Configuration Memory Device
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
module full_adder_1bit(
input FAl_InA,
input FAl_InB,
input FAl_InC,
input FAl_InM,
output FAl_OutSum,
output FAl_OutC
);
assign FAl_OutSum = FAl_InA^(FAl_InB)^FAl_InC;
assign FAl_OutC = ((FAl_InA^(FAl_InB))&FAl_InC)|(FAl_InA&(FAl_InB));
endmodule
Tcl Console
Messages
Log
Reports
Design Runs
35:0
Insert
Verilog
Type here to search
32°C Haze
ENG US
10:44 AM
9/1/2023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top_adder.v
vio_wrapper.v
F:/ELD2023/Lab2_FA_HW/Lab2_FA_HW.srcs/sources_1/imports/new/top_adder.v
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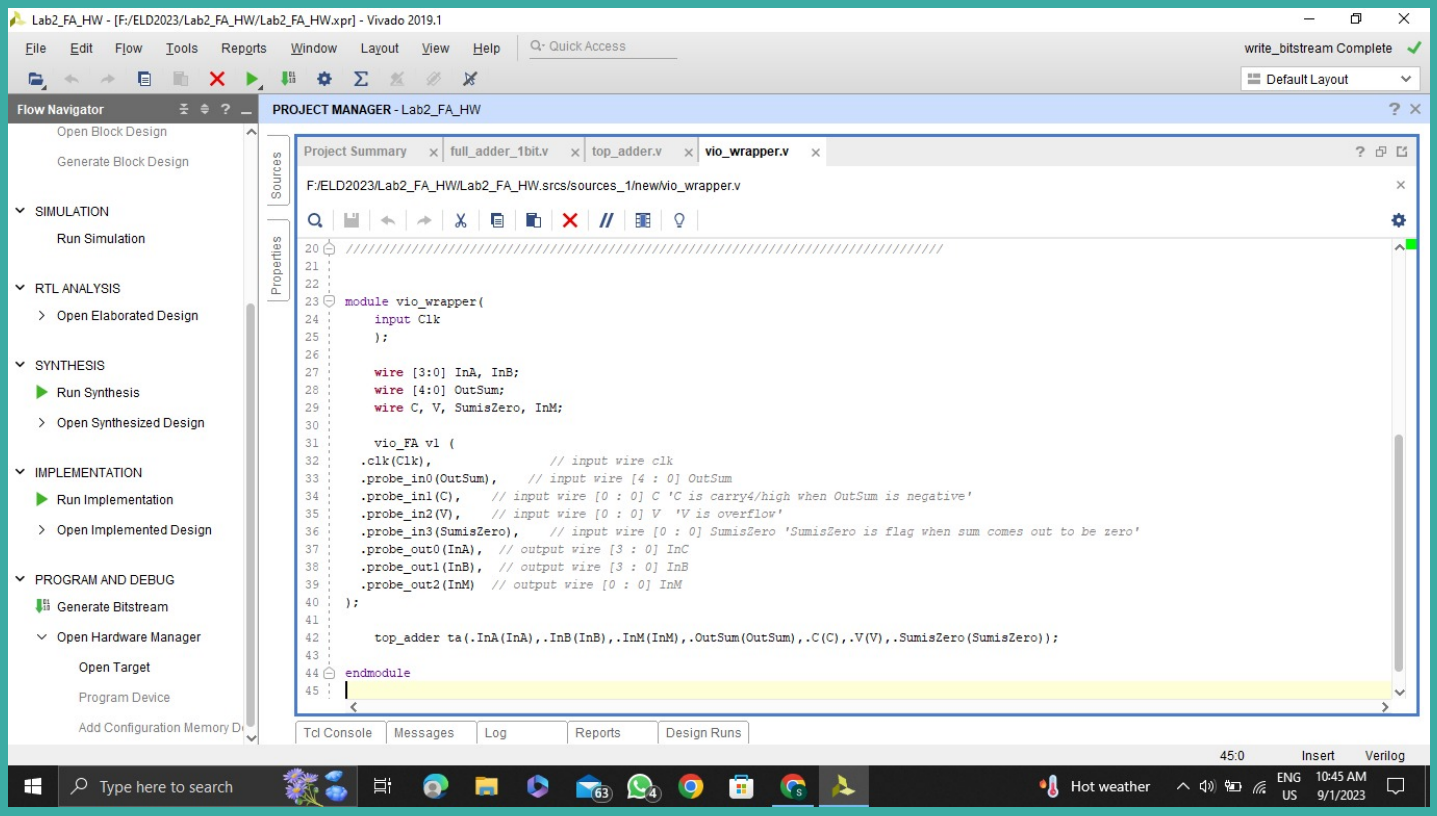
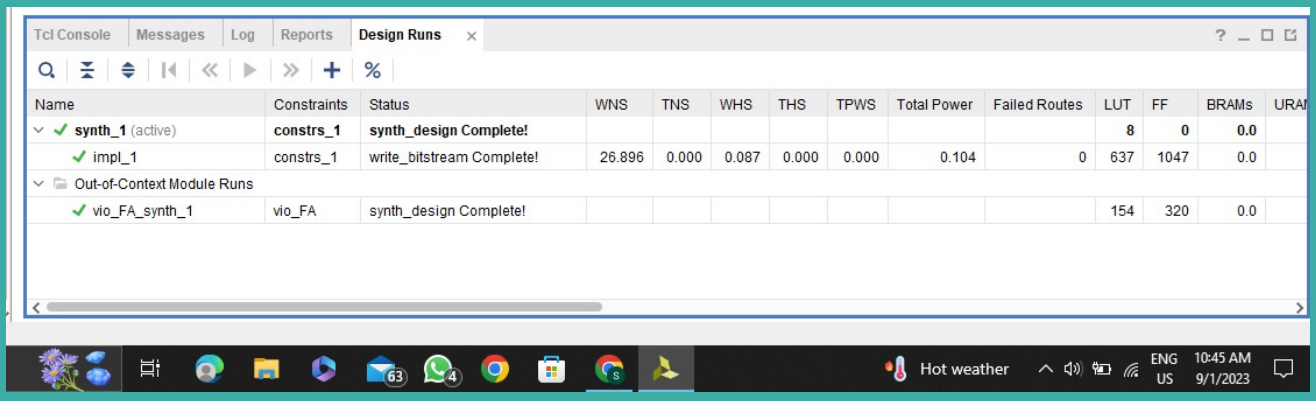
module top_adder(
input [3:0] InA,
input [3:0] InB,
input InM,
output [4:0] OutSum,
output C,
output V,
output SumisZero
);
wire carry1, carry2, carry3;
full_adder_1bit in0(.FAl_InA(InA[0]),.FAl_InB(InB[0]^InM),.FAl_InC(InM),.FAl_InM(InM),.FAl_OutSum(OutSum[0]),.FAl_OutC(carry1));
full_adder_1bit in1(.FAl_InA(InA[1]),.FAl_InB(InB[1]^InM),.FAl_InC(carry1),.FAl_InM(InM),.FAl_OutSum(OutSum[1]),.FAl_OutC(carry2));
full_adder_1bit in2(.FAl_InA(InA[2]),.FAl_InB(InB[2]^InM),.FAl_InC(carry2),.FAl_InM(InM),.FAl_OutSum(OutSum[2]),.FAl_OutC(carry3));
full_adder_1bit in3(.FAl_InA(InA[3]),.FAl_InB(InB[3]^InM),.FAl_InC(carry3),.FAl_InM(InM),.FAl_OutSum(OutSum[3]),.FAl_OutC(OutSum[4]));
assign V = OutSum[4] ^ carry3;
assign C = OutSum[4];
assign SumisZero = (OutSum == 5'b10000)|| (OutSum == 5'b00000);
// always@(*) begin
// if (OutSum == 4'b0000)
// SumisZero = 1'b1;
// else
// SumisZero = 1'b0;
// end
Tcl Console
Messages
Log
Reports
Design Runs
48:9
Insert
Verilog
Type here to search
Hot weather
ENG US
10:45 AM
9/1/2023

VIO WRAPPER FILE:

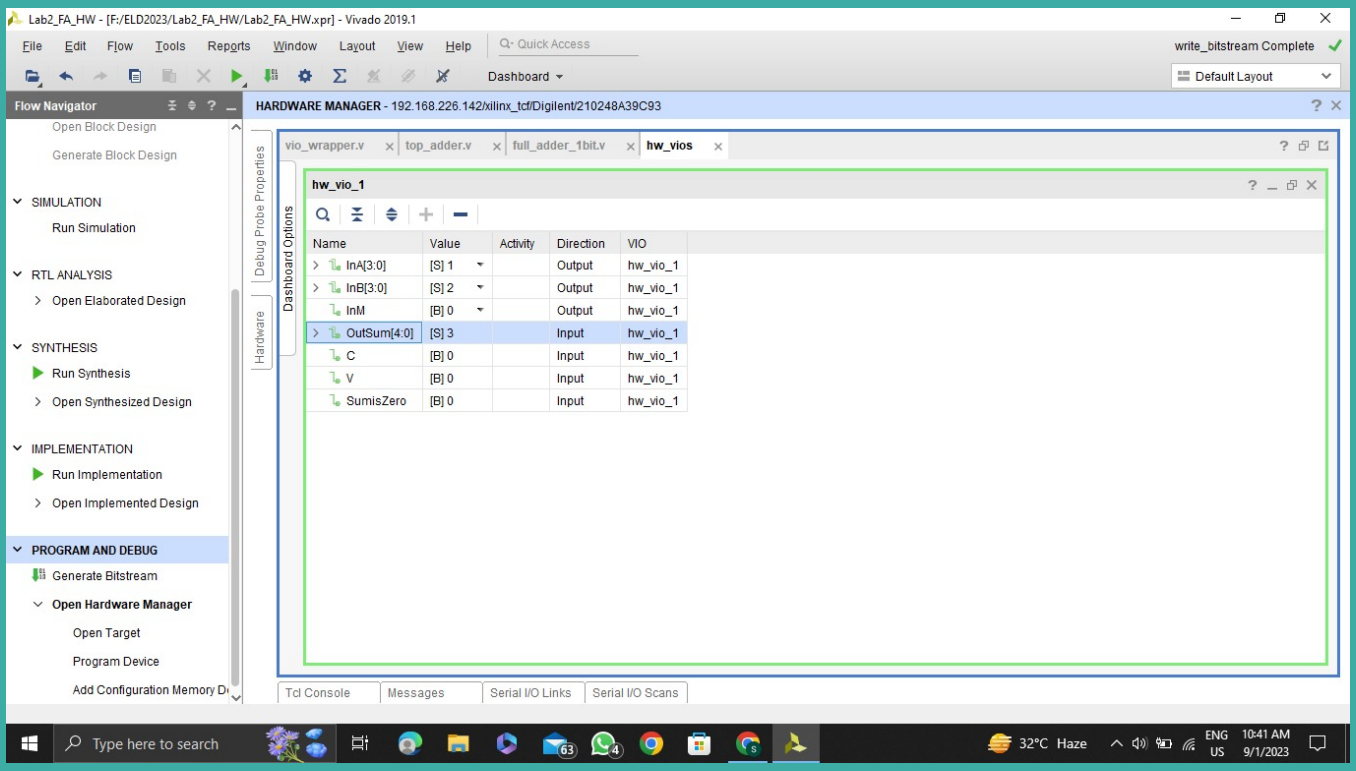


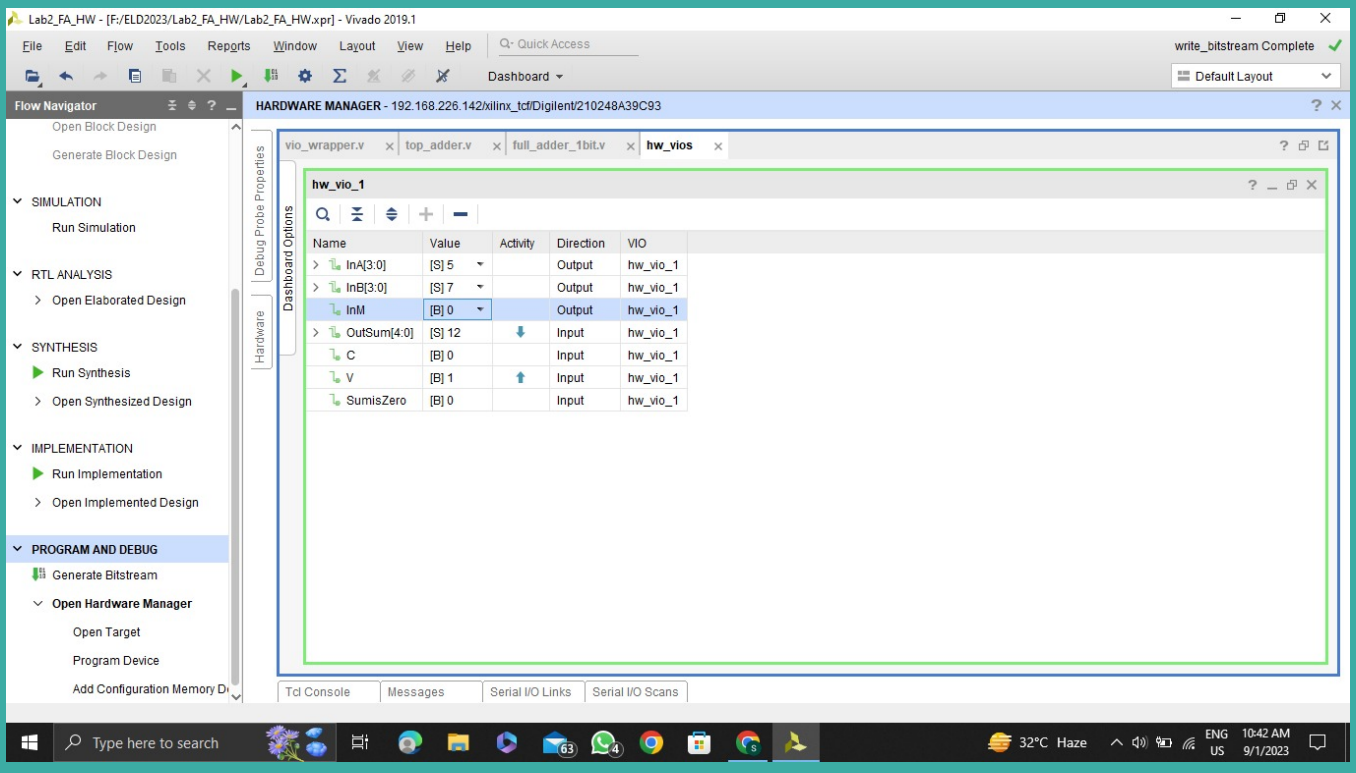
BITSTREAM GENERATION :



VIO OUTPUT

M = 0 , Adder :

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Quick Access
write_bitstream Complete
Dashboard
Default Layout
Flow Navigator
HARDWARE MANAGER - 192.168.226.142/xilinx_tcf/Digilent/210248A39C93
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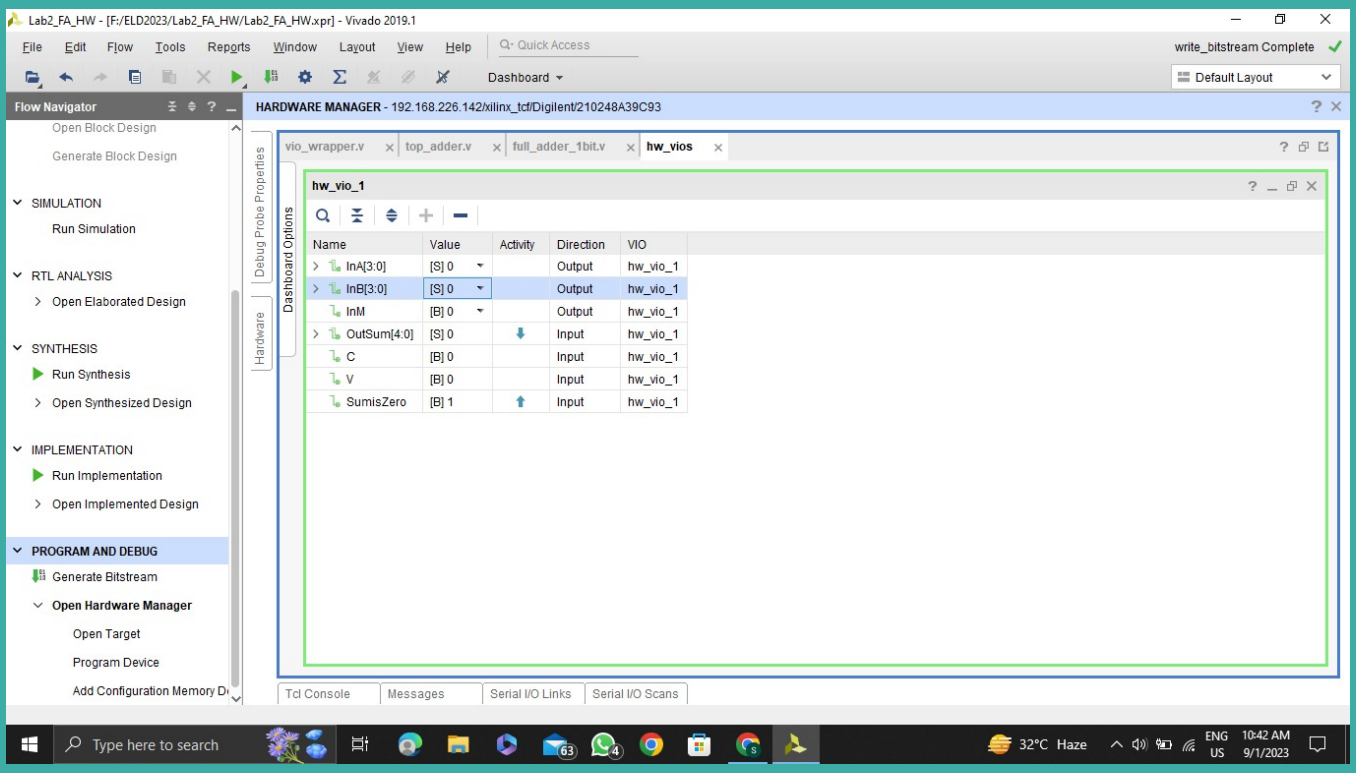
vio_wrapper.v
top_adder.v
full_adder_1bit.v
hw_vios
hw_vio_1
Debug Probe Properties
Dashboard Options
Hardware
Name Value Activity Direction VIO
InA[3:0] [S] 5 Output hw_vio_1
InB[3:0] [S] 7 Output hw_vio_1
InM [B] 0 Output hw_vio_1
OutSum[4:0] [S] 12 Input hw_vio_1
C [B] 0 Input hw_vio_1
V [B] 1 Input hw_vio_1
SumisZero [B] 0 Input hw_vio_1
Tcl Console
Messages
Serial I/O Links
Serial I/O Scans
Type here to search
32°C Haze
ENG US
10:42 AM 9/1/2023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InM [B] 0 Output hw_vio_1
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C [B] 0 Input hw_vio_1
V [B] 0 Input hw_vio_1
SumisZero [B] 1 Input hw_vio_1
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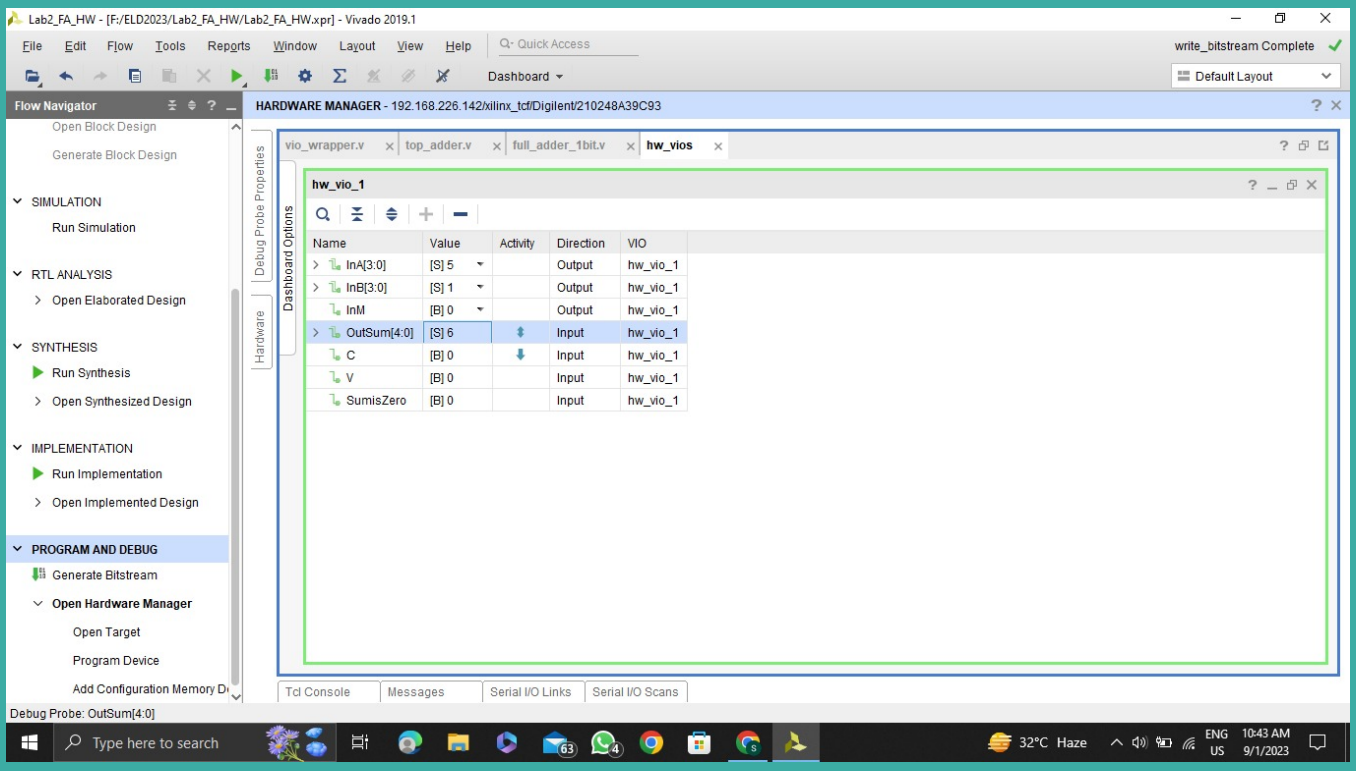
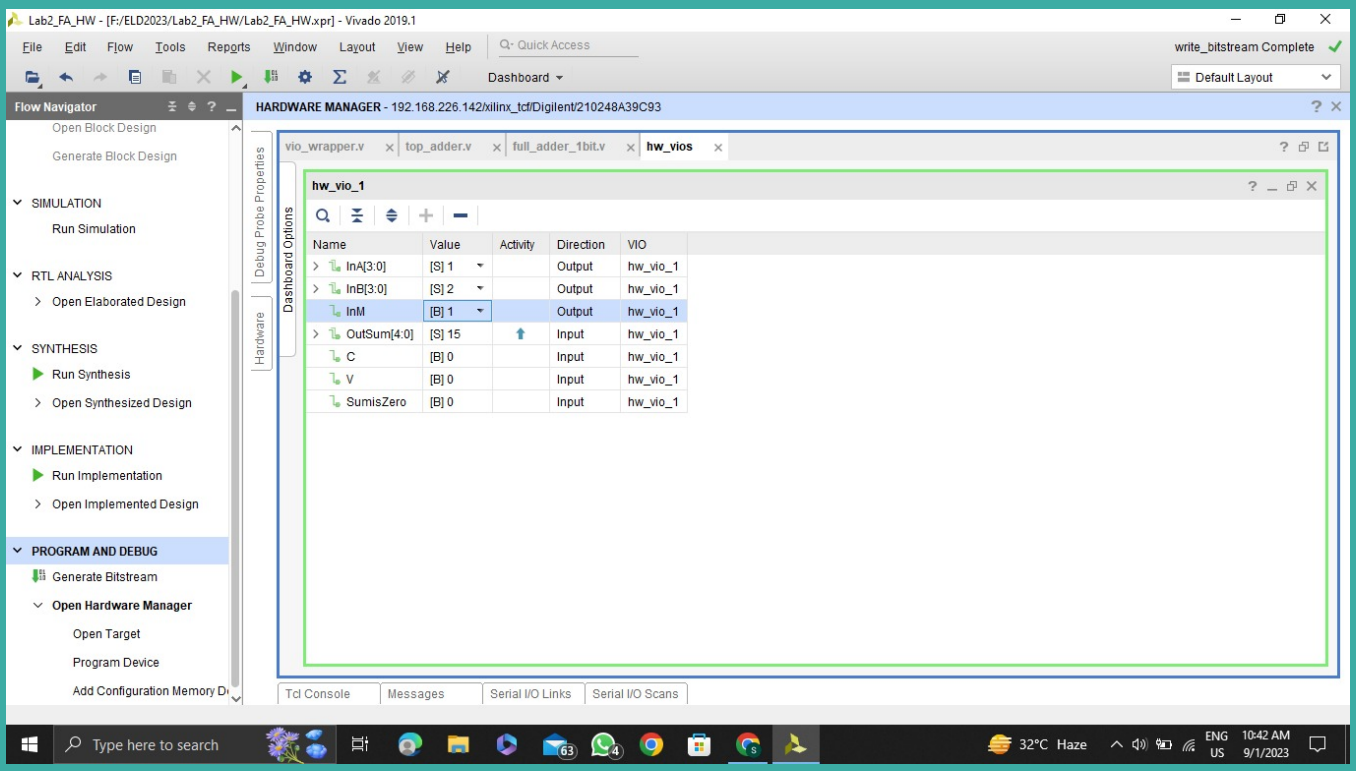
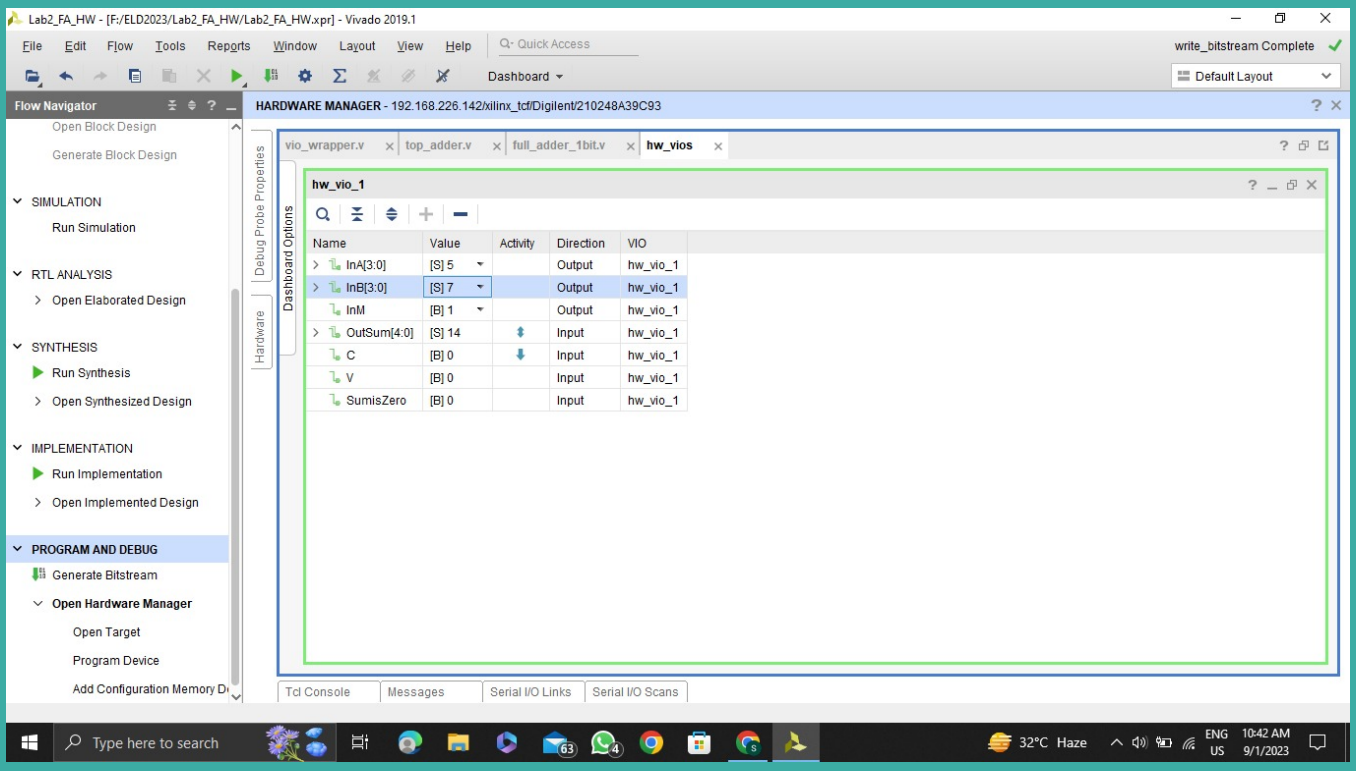


M = 1 , Subtractor :

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InM [B] 1 Output hw_vio_1
OutSum[4:0] [S] 14 Input hw_vio_1
C [B] 0 Input hw_vio_1
V [B] 0 Input hw_vio_1
SumisZero [B] 0 Input hw_vio_1
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Messages
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Serial I/O Scans
Type here to search
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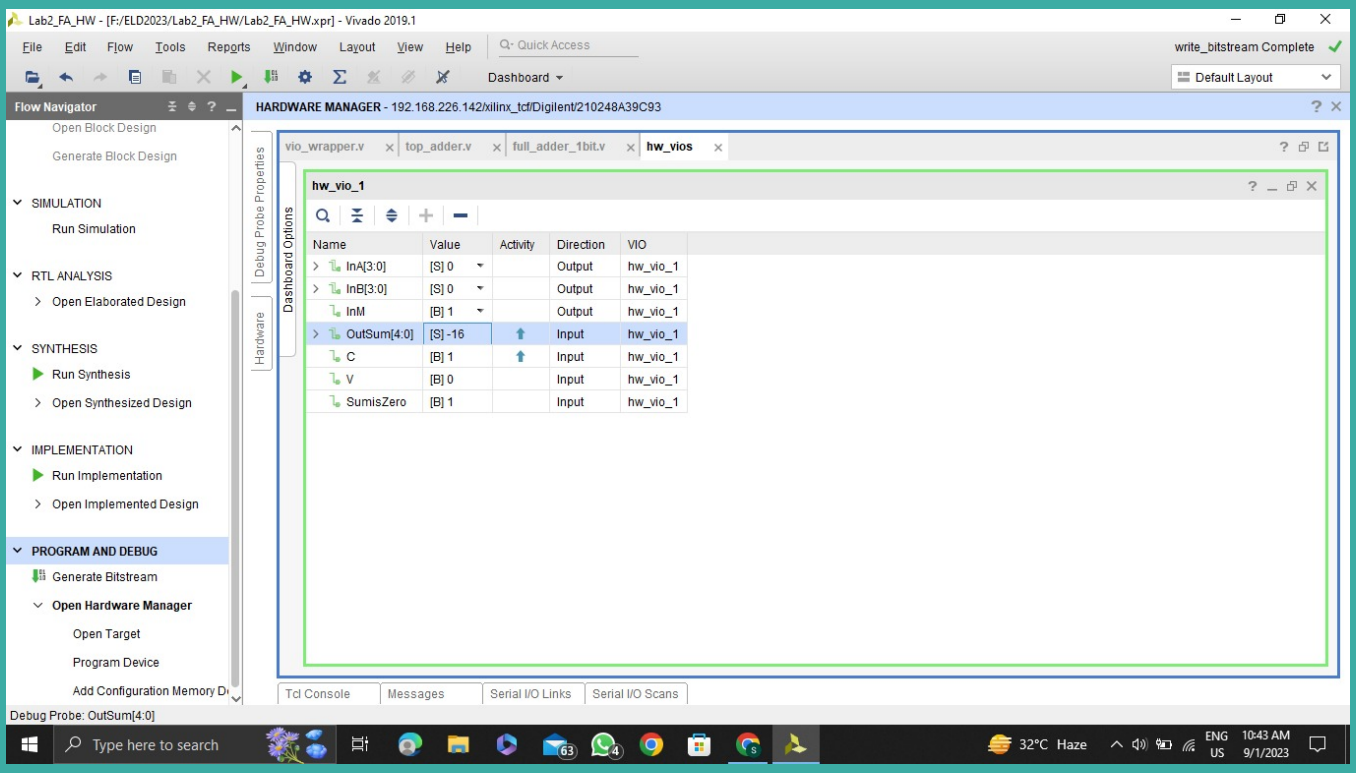
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InB[3:0] [S] 0 Output hw_vio_1
InM [B] 1 Output hw_vio_1
OutSum[4:0] [S] -16 Input hw_vio_1
C [B] 1 Input hw_vio_1
V [B] 0 Input hw_vio_1
SumisZero [B] 1 Input hw_vio_1
Tcl Console
Messages
Serial I/O Links
Serial I/O Scans
Debug Probe: OutSum[4:0]
Type here to search
32°C Haze
ENG US
10:43 AM
9/1/2023

Thank You