



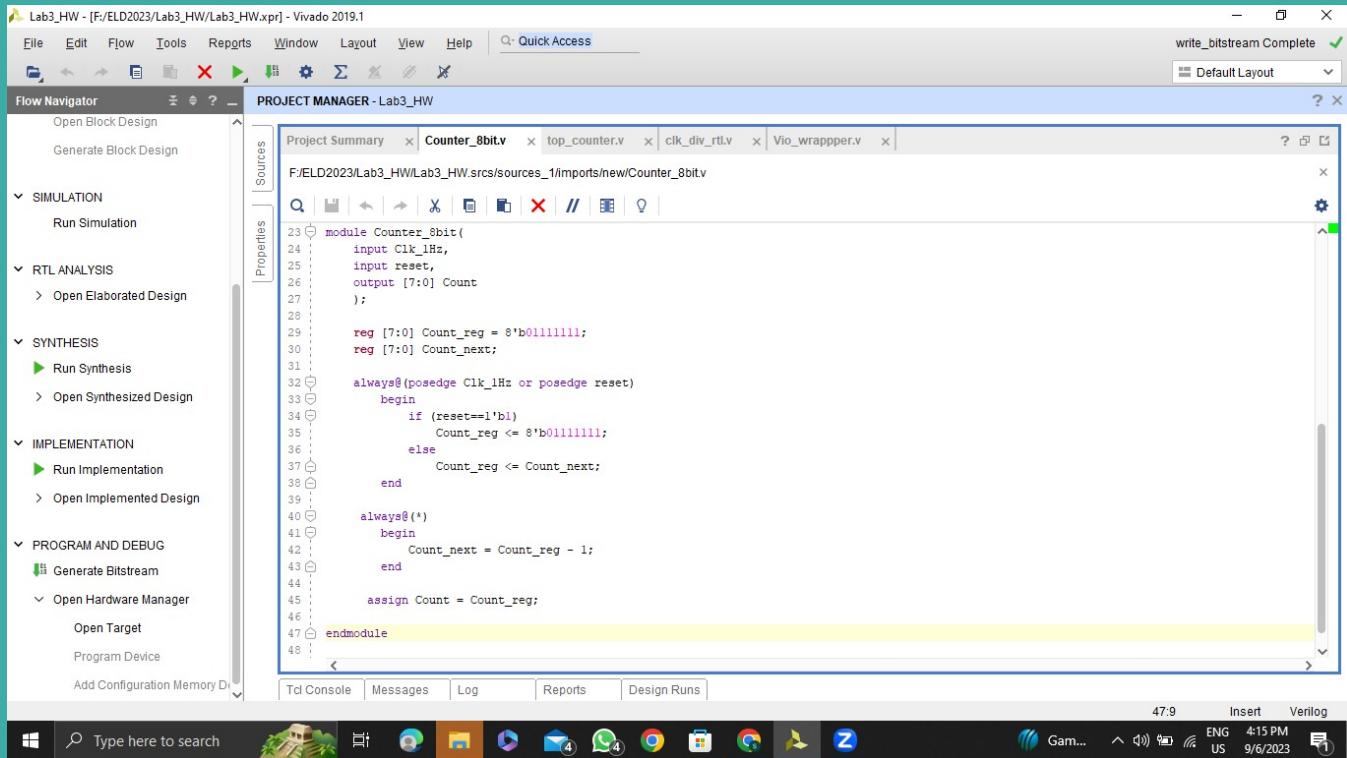
INDRAPRASTHA INSTITUTE *of*
INFORMATION TECHNOLOGY
DELHI

Department
of
Electronics & Communication Engineering

Embedded Logic Design
Lab 3 Submission

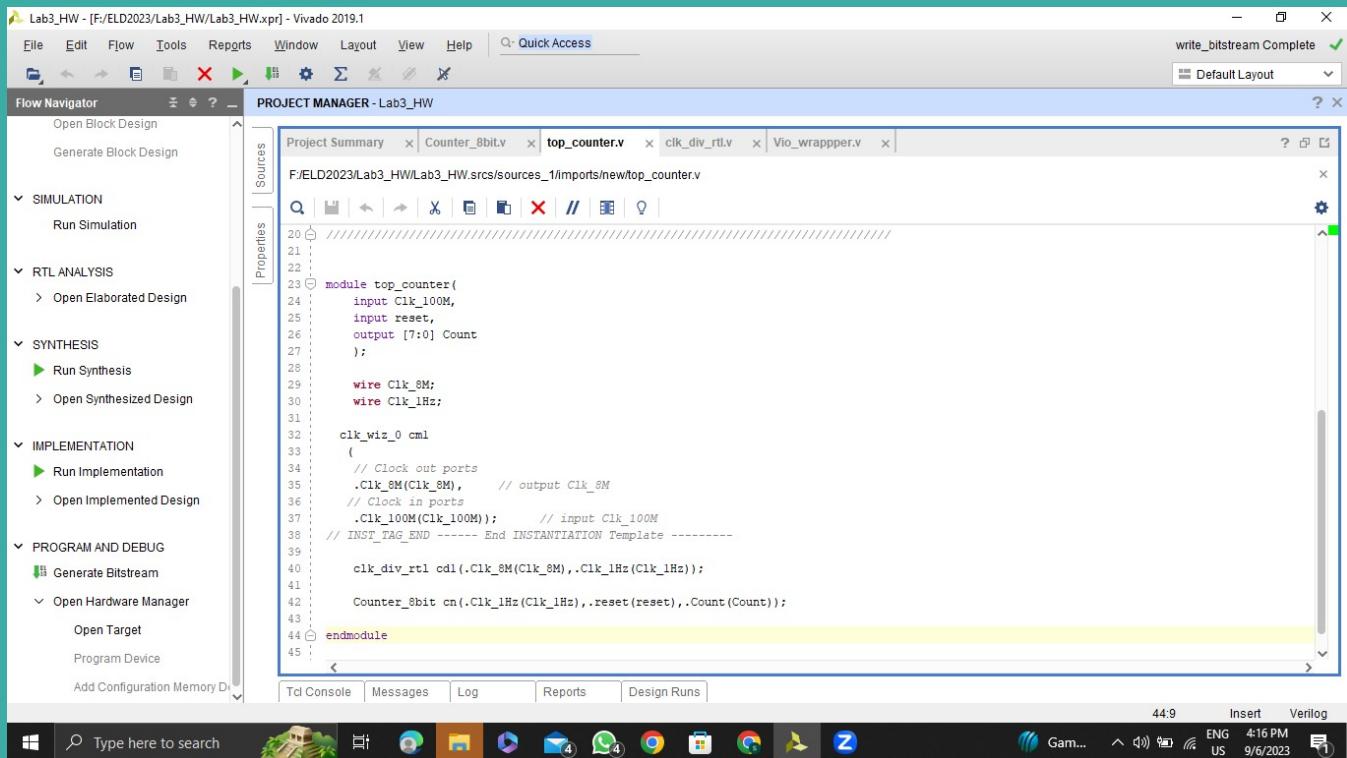
SHIVAM SHUKLA
2022478

Source Code



The screenshot shows the Vivado 2019.1 interface with the project "Lab3_HW" open. The "PROJECT MANAGER - Lab3_HW" window is active, displaying the "Sources" tab. The code editor shows the "Counter_8bit.v" file. The code defines a module Counter_8bit with an input Clk_1Hz, an input reset, and an output Count [7:0]. It uses a register Count_reg initialized to 8'b01111111. The logic updates Count_reg on the rising edge of Clk_1Hz or on the falling edge of reset. A comment indicates that Count_reg is updated to Count_next. The code ends with an endmodule statement.

```
23 module Counter_8bit(
24   input Clk_1Hz,
25   input reset,
26   output [7:0] Count
27 );
28
29   reg [7:0] Count_reg = 8'b01111111;
30   reg [7:0] Count_next;
31
32   always@(posedge Clk_1Hz or posedge reset)
33   begin
34     if (reset==1'b1)
35       Count_reg <= 8'b01111111;
36     else
37       Count_reg <= Count_next;
38   end
39
40   always@(*)
41   begin
42     Count_next = Count_reg - 1;
43   end
44
45   assign Count = Count_reg;
46
47 endmodule
48
```



The screenshot shows the Vivado 2019.1 interface with the project "Lab3_HW" open. The "PROJECT MANAGER - Lab3_HW" window is active, displaying the "Sources" tab. The code editor shows the "top_counter.v" file. The code defines a module top_counter with inputs Clk_100M, reset, and outputs Count [7:0]. It includes a wire declaration for Clk_8M and Clk_1Hz. The instantiation section uses the clk_wiz_0 template for Clk_8M and the clk_100m template for Clk_100M. The instantiation section ends with an INST_TAG_END marker. The code then instantiates a Counter_8bit module with Clk_1Hz and reset as inputs, and Count as the output. The code ends with an endmodule statement.

```
20 //////////////////////////////////////////////////////////////////
21
22
23 module top_counter(
24   input Clk_100M,
25   input reset,
26   output [7:0] Count
27 );
28
29   wire Clk_8M;
30   wire Clk_1Hz;
31
32   clk_wiz_0 cml
33   (
34     // Clock out ports
35     .Clk_8M(Clk_8M),    // output Clk_8M
36     // Clock in ports
37     .Clk_100M(Clk_100M); // input Clk_100M
38   // INST_TAG_END ----- End INSTANTIATION Template -----
39
40   clk_div_rtl1 cd1(.Clk_8M(Clk_8M),.Clk_1Hz(Clk_1Hz));
41
42   Counter_8bit cn(.Clk_1Hz(Clk_1Hz),.reset(reset),.Count(Count));
43
44 endmodule
45
```

Lab3_HW - [F:/ELD2023/Lab3_HW/Lab3_HW.xpr] - Vivado 2019.1

File Edit Flow Tools Reports Window Layout View Help Quick Access

PROJECT MANAGER - Lab3_HW

Flow Navigator Sources Properties

PROJECT SUMMARY Counter_Bbit.v top_counter.v clk_div_rtl.v Vio_wrappper.v

F:/ELD2023/Lab3_HW/Lab3_HW.srscs_1imports/new/clk_div_rtl.v

```
19 //////////////////////////////////////////////////////////////////
20 module clk_div_rtl(
21   input Clk_8M,
22   output Clk_1Hz
23 );
24
25   reg [22:0] Count_Reg = 23'b00000000000000000000000000000000;
26
27   always@(posedge Clk_8M)
28     begin
29       Count_Reg <= Count_Next;
30     end
31
32   always@(*)
33     begin
34       Count_Next = Count_Reg - 1;
35     end
36
37   assign Clk_1Hz = Count_Reg[22];
38
39 endmodule
```

Tcl Console Messages Log Reports Design Runs

43.9 Insert Verilog

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Lab3_HW - [F:/ELD2023/Lab3_HW/Lab3_HW.xpr] - Vivado 2019.1

File Edit Flow Tools Reports Window Layout View Help Quick Access

PROJECT MANAGER - Lab3_HW

Flow Navigator Sources Properties

PROJECT SUMMARY Counter_Bbit.v top_counter.v clk_div_rtl.v Vio_wrappper.v

F:/ELD2023/Lab3_HW/Lab3_HW.srscs_1imports/new/Vio_wrappper.v

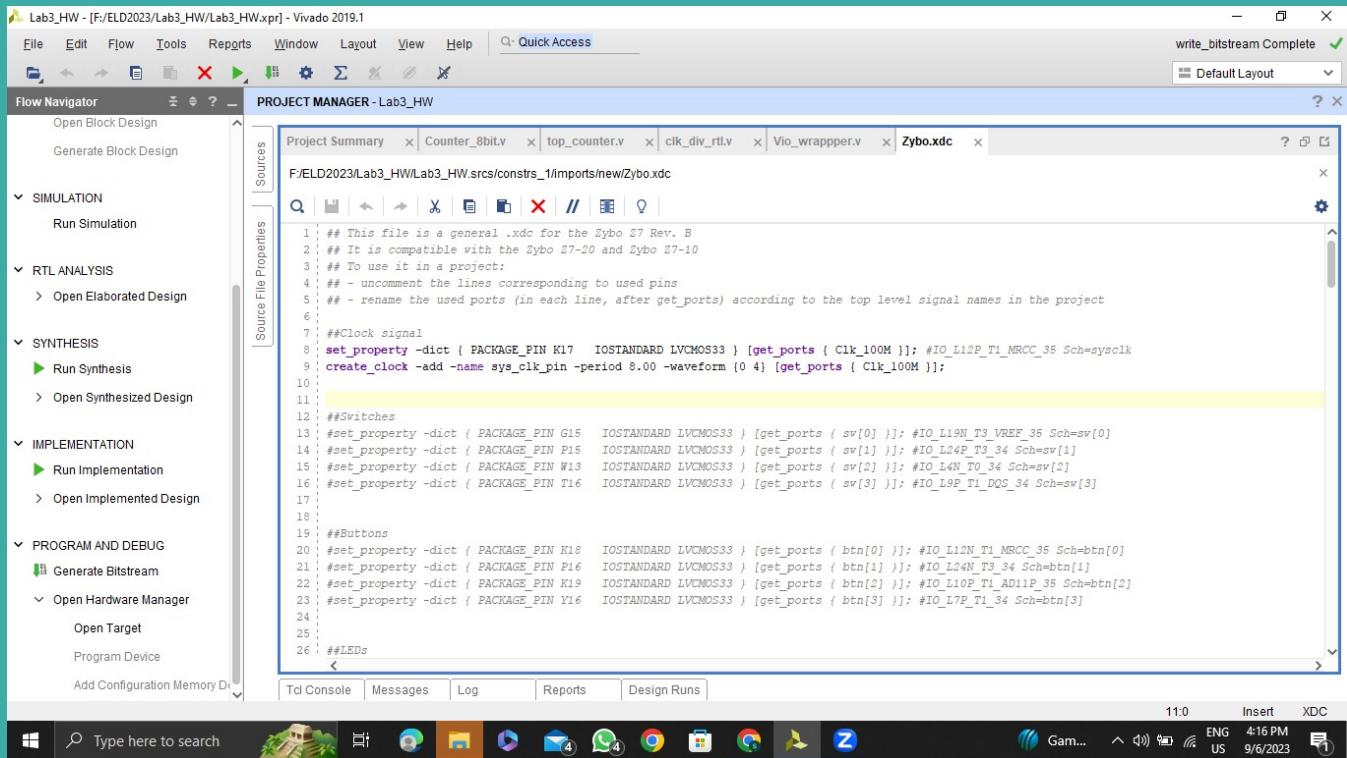
```
13 // Dependencies:
14 // Revision:
15 // Revision 0.01 - File Created
16 // Additional Comments:
17 //////////////////////////////////////////////////////////////////
18
19 module Vio_wrapper(
20   input Clk_100M
21 );
22   wire reset;
23   wire [7:0] Count;
24
25   vio_count v1 (
26     .clk(Clk_100M),           // input wire clk
27     .probe_in0(Count),        // input wire [7 : 0] Count
28     .probe_out0(reset)        // output wire [0 : 0] reset
29   );
30
31   top_counter tc(.Clk_100M(Clk_100M),.reset(reset),.Count(Count));
32
33 endmodule
```

Tcl Console Messages Log Reports Design Runs

37.9 Insert Verilog

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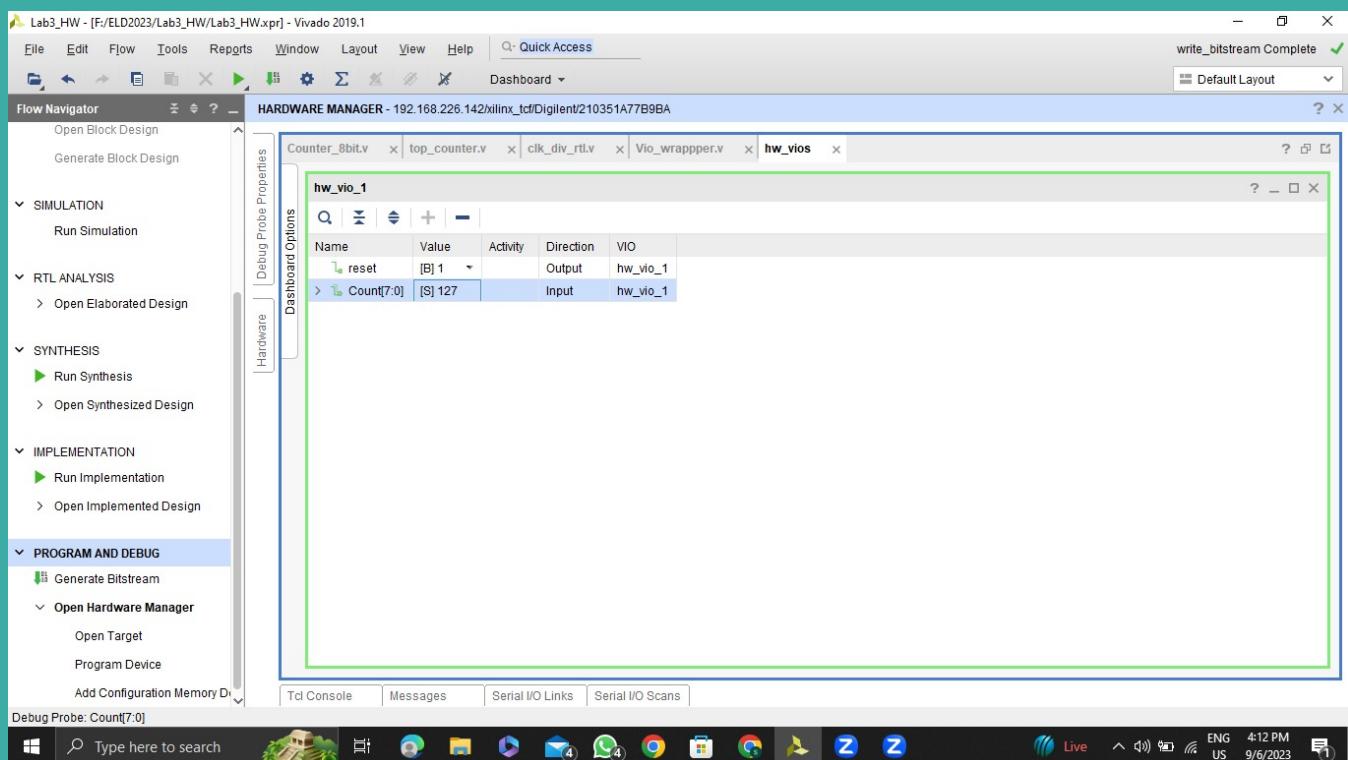
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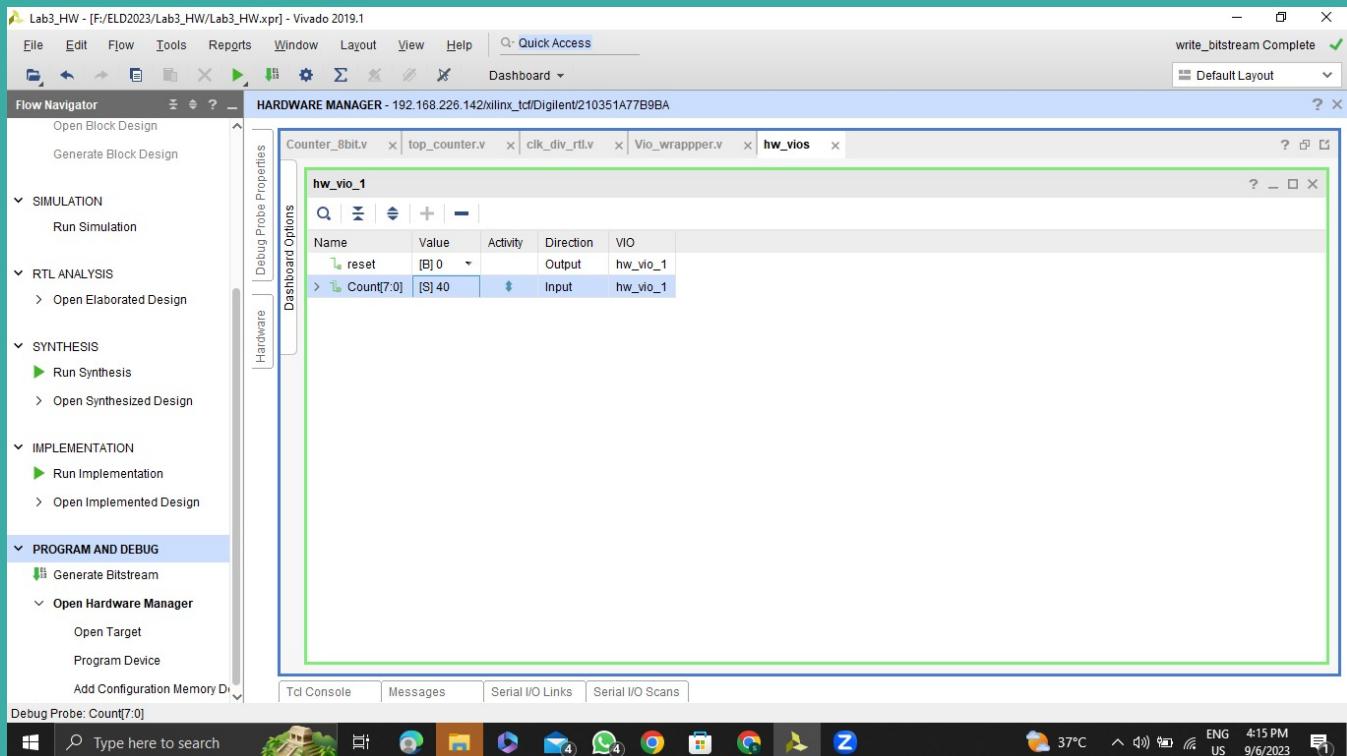
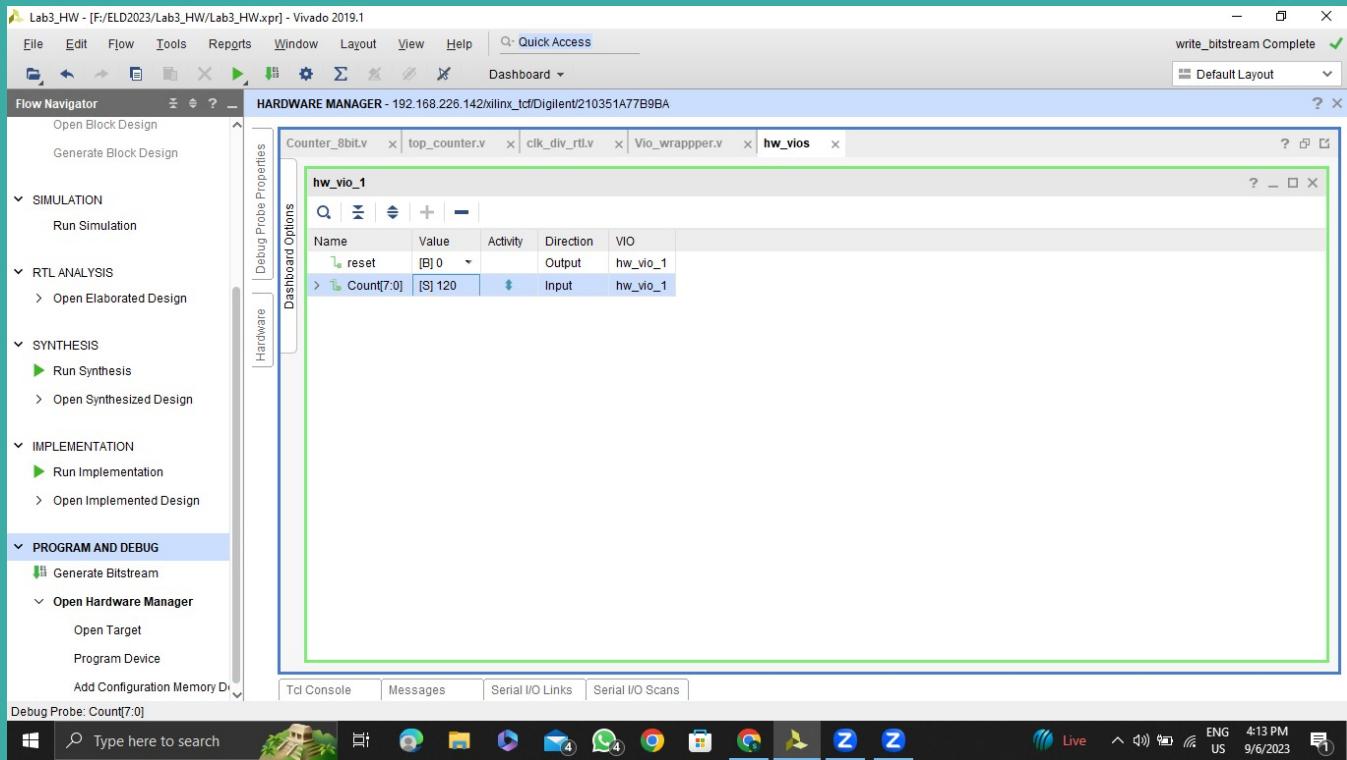


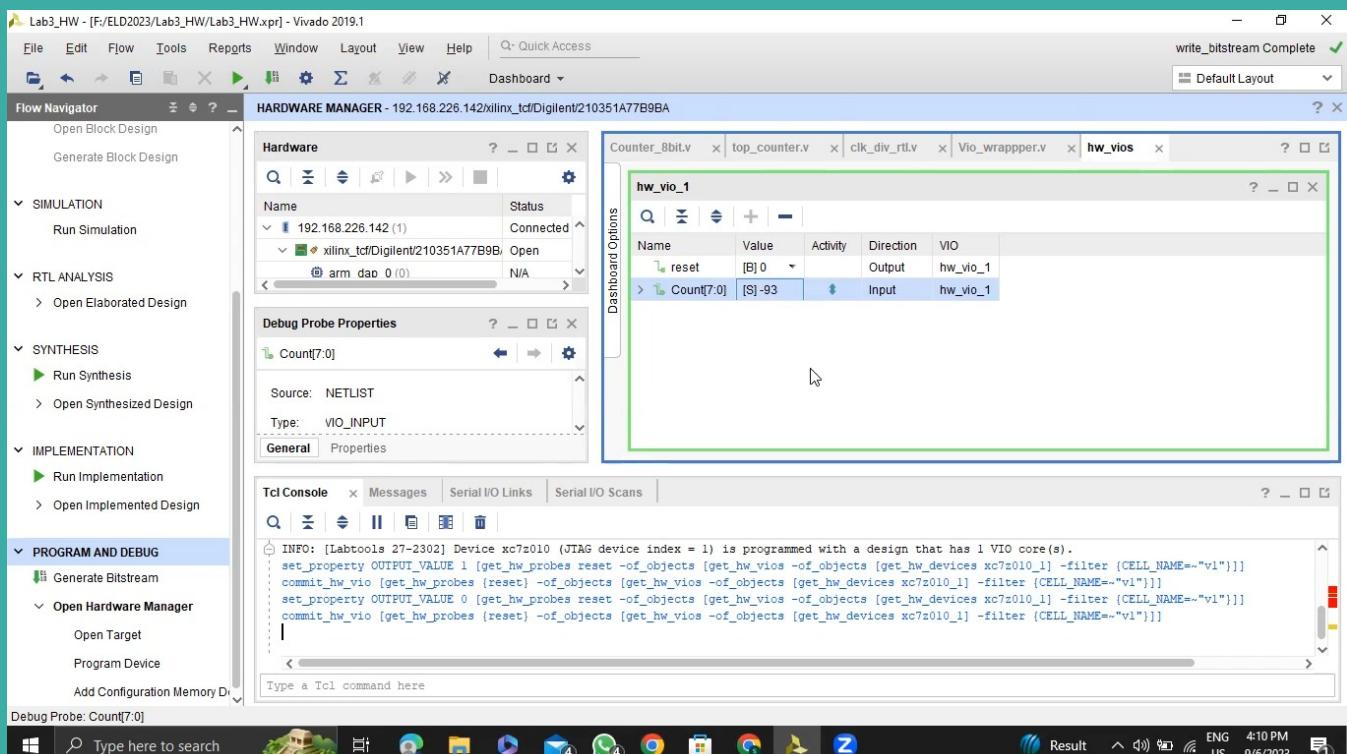
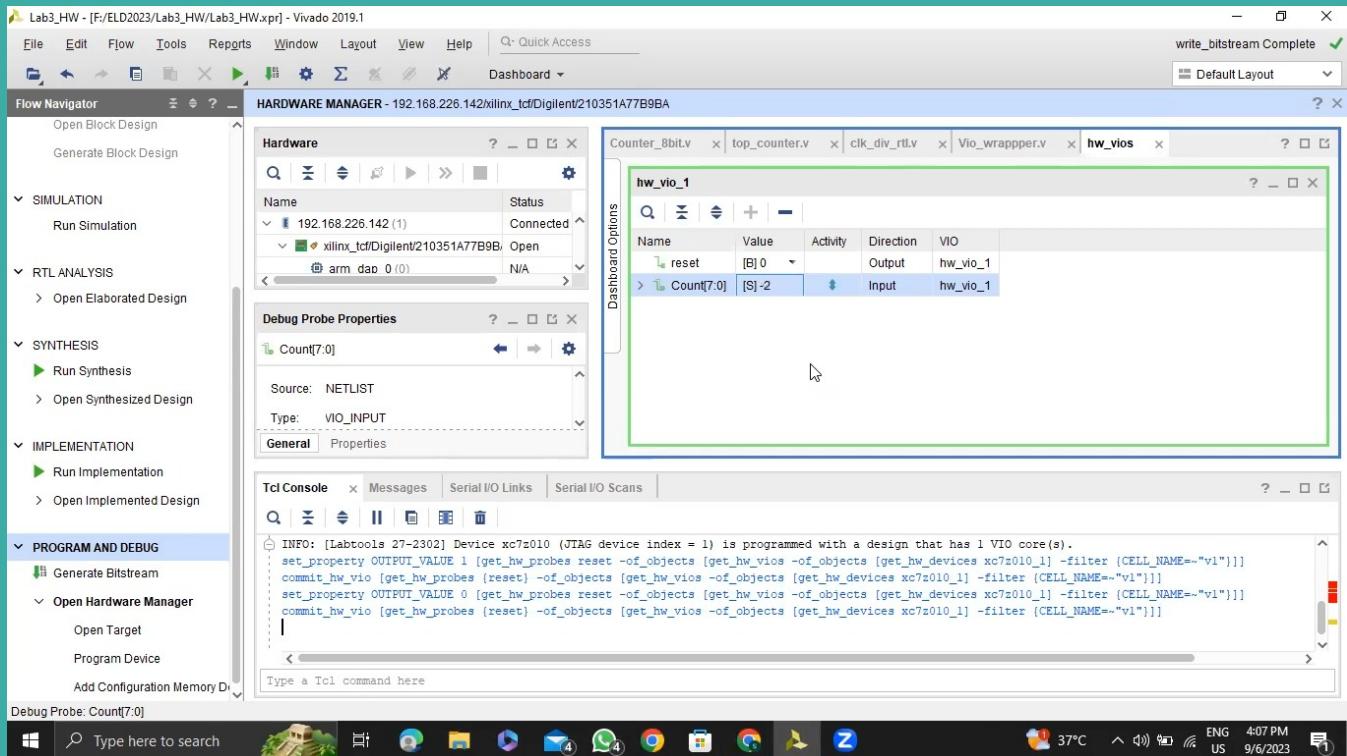
VIO OUTPUT

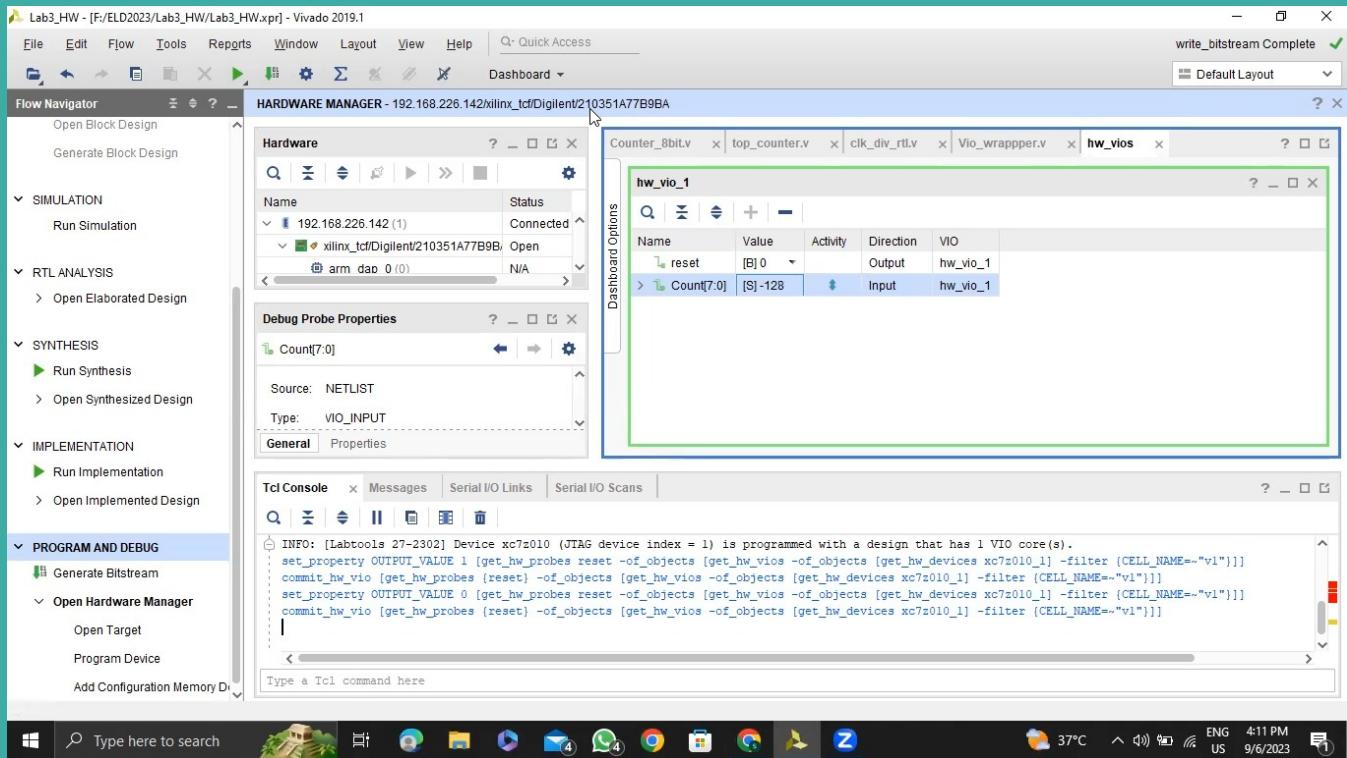
Reset = 1 , Counter = 127

This is a counter which counts downwards from 127 to -128.









Thank You