INDRAPRASTHA INSTITUTE *of*
INFORMATION TECHNOLOGY
DELHI

Department
of
Electronics & Communication Engineering

Embedded Logic Design
Lab 5 Submission

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Source Code

FSM_moore_1101.v

F:/ELD2023/Lab5_HW_FSM/Lab5_HW_FSM.srcs/sources_1/imports/sources_1/imports/new/FSM_moore_1101.v

```
20  //////////////////////////////////////////////////////////////////////////////////


21
22
23  module FSM_moore_1101(
24      input Clk_pb,
25      input Clear,
26      output [3:0] FSM_state
27      );
28
29      parameter S0 = 4'b0100, S1 = 4'b0110, S2 = 4'b1000;
30      reg[3:0] present_state = S0;
31      reg[3:0] next_state;
32
33      always@(posedge Clk_pb or posedge Clear)
34          begin
35              if (Clear)
36                  present_state <= S0;
37              else
38                  present_state <= next_state;
39          end
40
41      always@(*)
42          begin
43              case(present_state)
44                  S0: next_state = S1;
45                  S1: next_state = S2;
46                  S2: next_state = S0;
47                  default next_state = S0;
48               endcase
49           end
50
51       assign FSM_state = present_state;
52
53  endmodule
54
```

clk_div_rtl.v

F:/ELD2023/Lab5_HW_FSM/Lab5_HW_FSM.srcs/sources_1/imports/sources_1/imports/new/clk_div_rtl.v

```
10  // Target Devices:
11  // Tool Versions:
12  // Description:
13  //
14  // Dependencies:
15  //
16  // Revision:
17  // Revision 0.01 - File Created
18  // Additional Comments:
19  //
20  //////////////////////////////////////////////////////////////////////////////////
21
22
23  module clk_div_rtl(
24      input Clk_8M,
25      output Clk_1Hz
26      );
27
28
29      reg [22:0] Count_reg = 0;
30      reg [22:0] Count_next;
31
32      always@(posedge Clk_8M)
33          begin
34              Count_reg <= Count_next;
35          end
36
37       always@(*)
38          begin
39              Count_next = Count_reg + 1;
40          end
41
42        assign Clk_1Hz = Count_reg[22];
43  endmodule
44
```

top_counter.v

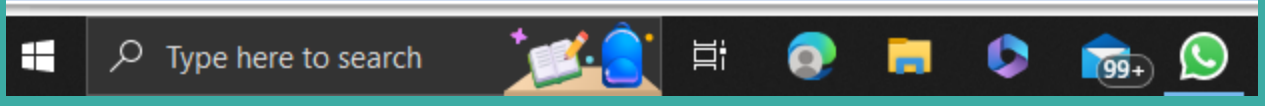
F:/ELD2023/Lab5_HW_FSM/Lab5_HW_FSM.srcs/sources_1/imports/sources_1/imports/new/top_counter.v

```
11  // Tool Versions:
12  // Description:
13  //
14  // Dependencies:
15  //
16  // Revision:
17  // Revision 0.01 - File Created
18  // Additional Comments:
19  //
20  //////////////////////////////////////////////////////////////////////////////////
21
22
23  module top_counter(
24      input Clk_100M,
25      input Clr,
26      output [3:0] FSM_state
27      );
28
29      wire Clk_8M;
30      wire Clk_1Hz;
31
32    clk_wiz_0 cm1
33     (
34      // Clock out ports
35      .Clk_8M(Clk_8M),     // output Clk_8M
36     // Clock in ports
37      .Clk_100M(Clk_100M));      // input Clk_100M
38  // INST_TAG_END ------ End INSTANTIATION Template ---------
39
40      clk_div_rtl cdl(.Clk_8M(Clk_8M),.Clk_1Hz(Clk_1Hz));
41
42      FSM_moore_1101 f1(.Clk_pb(Clk_1Hz),.Clear(Clr),.FSM_state(FSM_state));
43
44  endmodule
45
```

Vio_wrappper.v

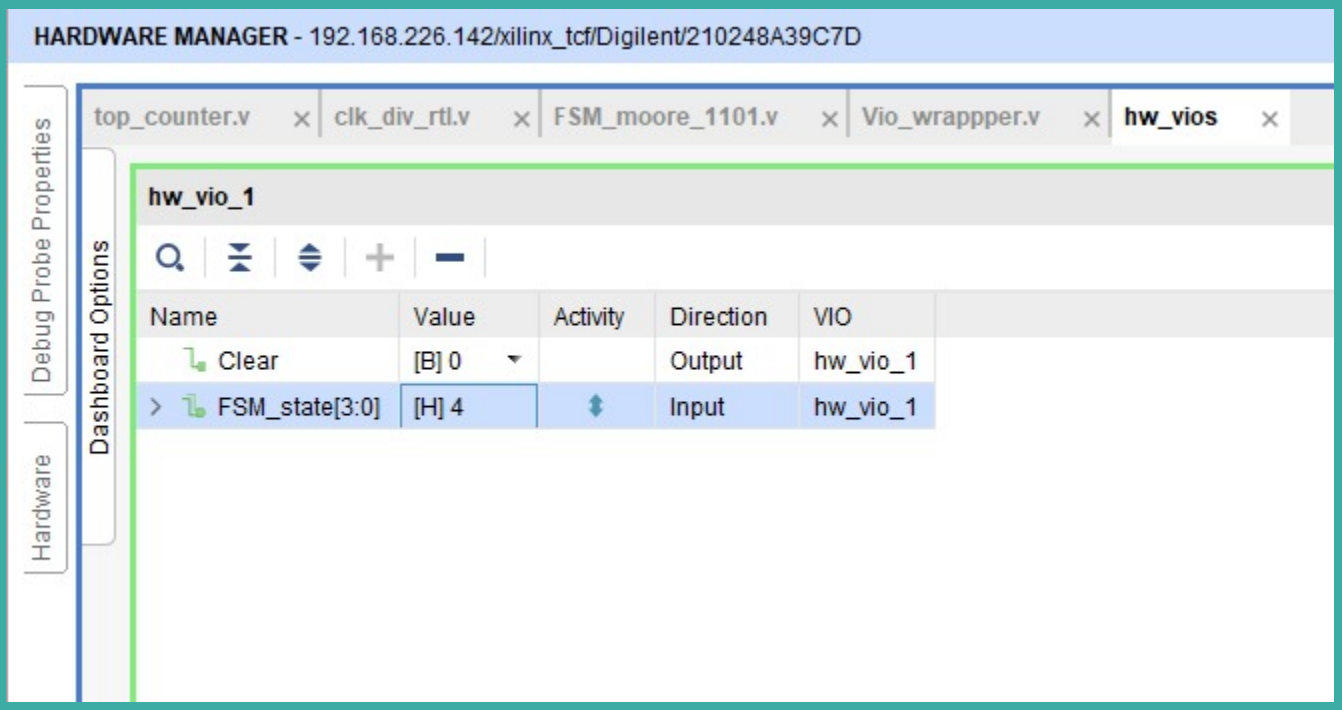
F:/ELD2023/Lab5_HW_FSM/Lab5_HW_FSM.srcs/sources_1/imports/sources_1/imports/new/Vio_wrappper.v

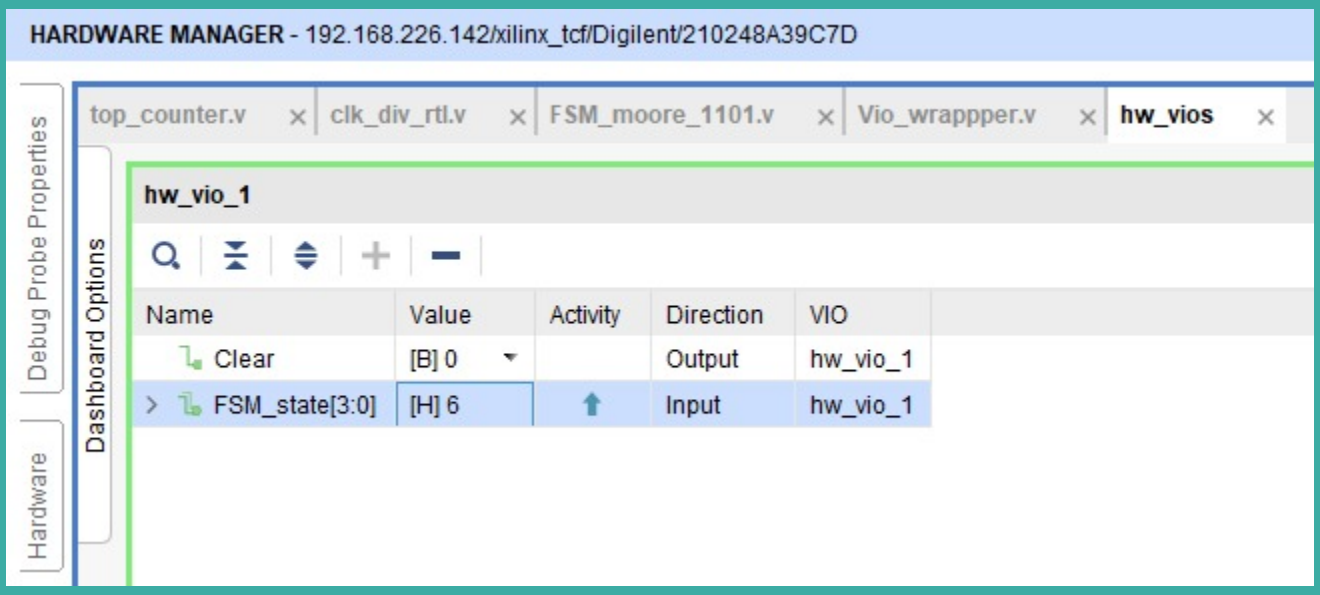
```
5  //
6  // Create Date: 09/05/2023 09:53:15 AM
7  // Design Name:
8  // Module Name: Vio_wrappper
9  // Project Name:
10 // Target Devices:
11 // Tool Versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //////////////////////////////////////////////////////////////////////////////////
21
22
23 module Vio_wrappper(
24     input Clk_100M
25     );
26
27     wire Clear;
28     wire [3:0]FSM_state;
29
30     vio_0 v1 (
31   .clk(Clk_100M),                // input wire clk
32   .probe_in0(FSM_state),     // input wire [2 : 0] probe_in1
33   .probe_out0(Clear)  // output wire [0 : 0] probe_out0
34 );
35
36     top_counter f1(.Clk_100M(Clk_100M), .Clr(Clear),.FSM_state(FSM_state));
37
38 endmodule
39
```

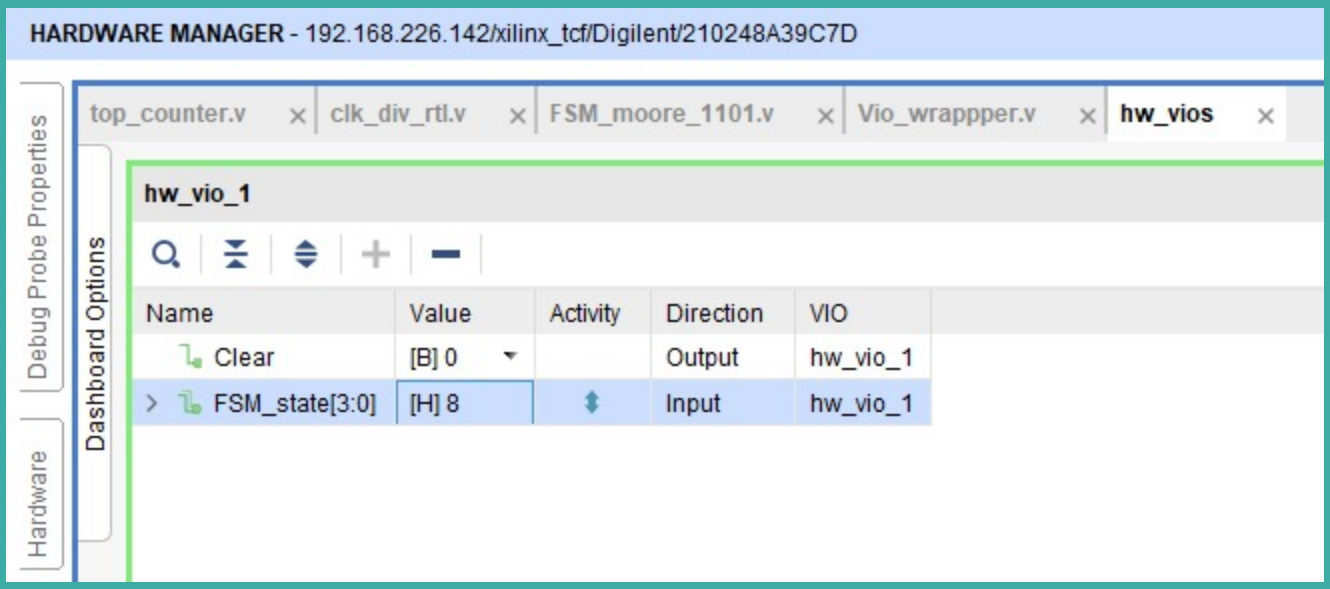


VIO Output

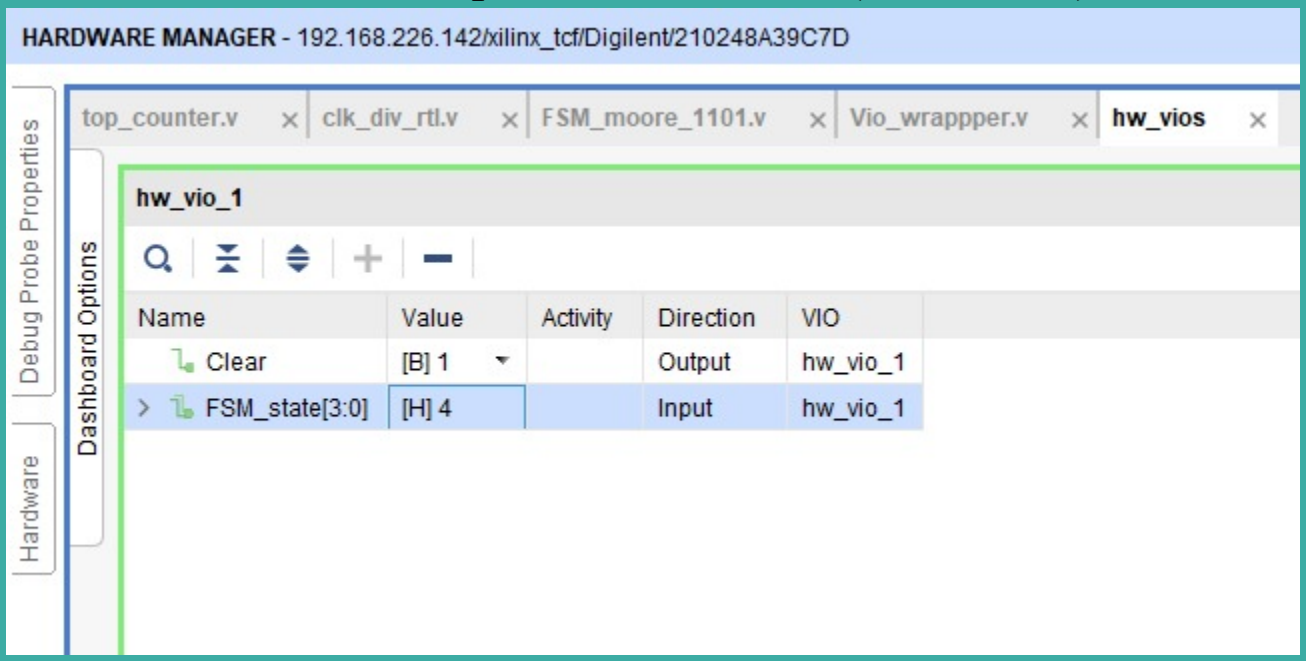
- **If clear == 0 we can see output as a counter having sequence 4 => 6 => 8 => 4 => 6 and so on.**







- **Else if clear == 1 the output will be S0 i.e. 4 (initial state)**



Thank You