INDRAPRASTHA INSTITUTE *of*
INFORMATION TECHNOLOGY
DELHI

Department
of
Electronics & Communication Engineering

Embedded Logic Design

Lab 1 Submission

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Source Code

full_adder_1bit.v

F:/ELD2023/Lab1_FA_HW/Lab1_FA_HW.srcs/sources_1/new/full_adder_1bit.v

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 08/24/2023 08:54:40 PM
// Design Name:
// Module Name: full_adder_1bit
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module full_adder_1bit(
    input FA1_InA,
    input FA1_InB,
    input FA1_InC,
    input FA1_InM,
    output FA1_OutSum,
    output FA1_OutC
    );

    assign FA1_OutSum = FA1_InA^(FA1_InB)^FA1_InC;
    assign FA1_OutC = ((FA1_InA^(FA1_InB))&FA1_InC)|(FA1_InA&(FA1_InB));
endmodule
```

top_adder.v

F:/ELD2023/Lab1_FA_HW/Lab1_FA_HW.srcs/sources_1/new/top_adder.v

```
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module top_adder(
    input [3:0] InA,
    input [3:0] InB,
    input InM,
    output [3:0] OutSum,
    output C,
    output V,
    output SumisZero
    );

    full_adder_1bit in0(.FA1_InA(InA[0]),.FA1_InB(InB[0]^InM),.FA1_InC(InM),.FA1_InM(InM),.FA1_OutSum(OutSum[0]),.FA1_OutC(carry1));
    full_adder_1bit in1(.FA1_InA(InA[1]),.FA1_InB(InB[1]^InM),.FA1_InC(carry1),.FA1_InM(InM),.FA1_OutSum(OutSum[1]),.FA1_OutC(carry2));
    full_adder_1bit in2(.FA1_InA(InA[2]),.FA1_InB(InB[2]^InM),.FA1_InC(carry2),.FA1_InM(InM),.FA1_OutSum(OutSum[2]),.FA1_OutC(carry3));
    full_adder_1bit in3(.FA1_InA(InA[3]),.FA1_InB(InB[3]^InM),.FA1_InC(carry3),.FA1_InM(InM),.FA1_OutSum(OutSum[3]),.FA1_OutC(carry4));

    assign V = carry4 ^ carry3;
    assign C = carry4;
    assign SumisZero = (OutSum == 4'b0000);
//    always@(*) begin
//    if (OutSum == 4'b0000)
//     SumisZero = 1'b1;
//    else
//    SumisZero = 1'b0;
//    end
endmodule
```

TESTBENCH

adder_sub_tb.v

F:/ELD2023/Lab1_FA_HW/Lab1_FA_HW.srcs/sim_1/new/adder_sub_tb.v

```
15      //
16      // Revision:
17      // Revision 0.01 - File Created
18      // Additional Comments:
19      //
20      //////////////////////////////////////////////////////////////////////////////////
21
22
23      module adder_sub_tb(
24
25          );
26          reg [3:0] InA, InB;
27          wire [3:0] OutSum;
28          wire C;
29          reg InM;
30          wire V;
31          wire SumisZero;
32
33          top_adder tb0(.InA(InA), .InB(InB), .OutSum(OutSum),.InM(InM),.V(V),.C(C),.SumisZero(SumisZero));
34
35          initial begin
36
37              // Test cases for subtraction (M = 1)
38              InA = 4'b0000; InB = 4'b0000; InM = 1'b1;
39              #5 InA = 4'b0100; InB = 4'b0110; InM = 1'b1;
40              #5 InA = 4'b0101; InB = 4'b0111; InM = 1'b1;
41
42              // Test cases for addition (M = 0)
43              #5 InA = 4'b0000; InB = 4'b0000; InM = 1'b0;
44              #5 InA = 4'b1111; InB = 4'b0000;  InM = 1'b0;
45              #5 InA = 4'b0111; InB = 4'b0001;  InM = 1'b0;
46
47          end
48      endmodule
49
```

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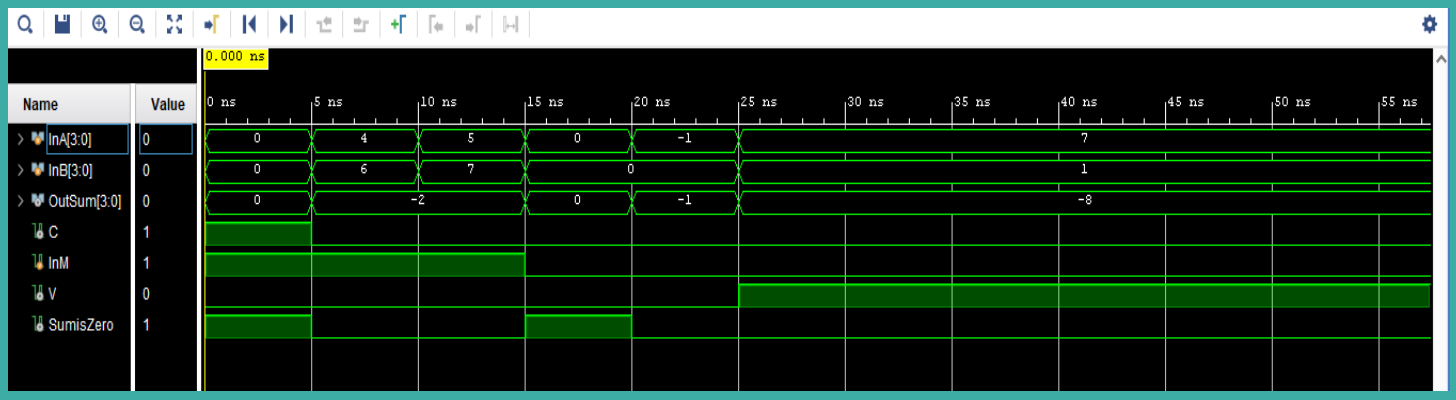
SIMULATION OF WAVEFORM



Thank you