Assignment - 4

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Course: VDF

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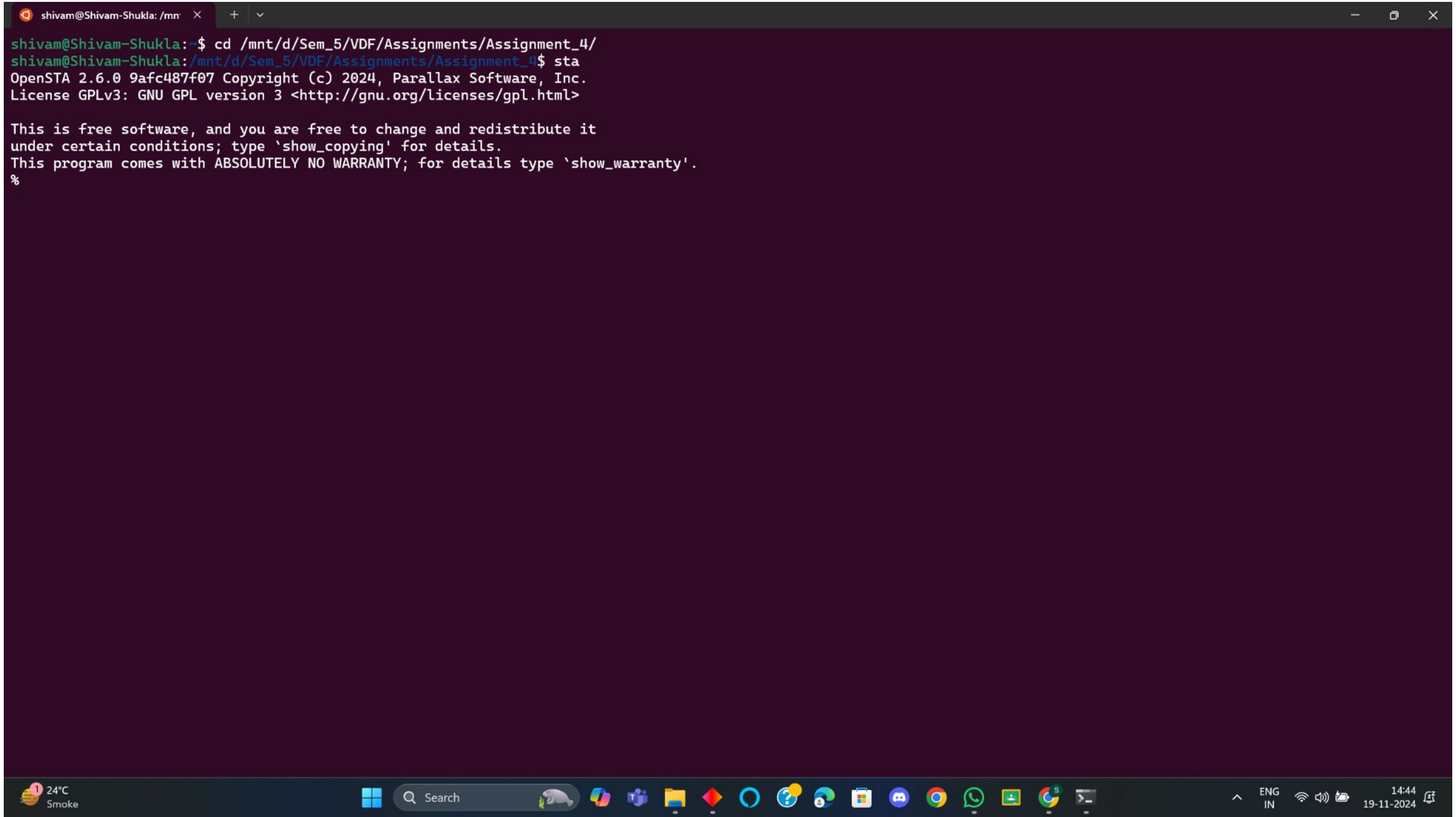
Q1) Snippet of the log files to prove that I have indeed run the tools



```
shivam@Shivam-Shukla:~$ cd /mnt/d/Sem_5/VDF/Assignments/Assignment_4/
shivam@Shivam-Shukla:/mnt/d/Sem_5/VDF/Assignments/Assignment_4$ sta
OpenSTA 2.6.0 9afc487f07 Copyright (c) 2024, Parallax Software, Inc.
License GPLv3: GNU GPL version 3 <http://gnu.org/licenses/gpl.html>

This is free software, and you are free to change and redistribute it
under certain conditions; type `show_copying' for details.
This program comes with ABSOLUTELY NO WARRANTY; for details type `show_warranty'.
%
```

Q2 Verilog netlist

```
module circuit1 (
   input A, B, C, D, E, CLK,
   output OUT
);
   wire and1_out, nand1_out, f1_out,
f2_out, nand2_out, f3_out, final_out;

   // Instantiating gates and flip-flops
   AND2_X1 u1 (.A1(D), .A2(E),
.ZN(and1_out)); // AND Gate

   DFF_X1 f1 (.D(and1_out), .CK(CLK),
.Q(f1_out)); // D Flip-Flop F1

   NAND2_X1 u2 (.A1(C), .A2(f1_out),
.ZN(nand1_out)); // NAND Gate

   DFF_X1 f2 (.D(nand1_out),
.CK(CLK), .Q(f2_out)); // D Flip-Flop F2

   NAND2_X1 u3 (.A1(B), .A2(f2_out),
.ZN(nand2_out)); // NAND Gate

   DFF_X1 f3 (.D(nand2_out),
.CK(CLK), .Q(f3_out)); // D Flip-Flop F3

   NAND2_X1 u4 (.A1(A), .A2(f3_out),
.ZN(final_out)); // NAND Gate

   assign OUT = final_out;

endmodule
```

PS: I've combined the code snippets in sequence, with each section following after the white rectangles. Can also find the code here

Q2 SDC file

```
# clock period 200 ps
create_clock -name CLK -period 200 [get_ports CLK]

# clock uncertainty of 50 ps
set_clock_uncertainty 50 [get_clocks CLK]

set_input_delay 20 -clock [get_clocks CLK] [get_ports {A B C D E}]
set_output_delay 20 -clock [get_clocks CLK] [get_ports OUT]
```

PS: Can also find the code here

Q2 worst slack

a. Late path between F1 and F2

```
Setup Path Analysis:
Startpoint: f1 (rising edge-triggered flip-flop clocked by CLK)
Endpoint: f2 (rising edge-triggered flip-flop clocked by CLK)
Path Group: CLK
Path Type: max

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock CLK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 ^ f1/CK (DFF_X1)
   0.09    0.09 ^ f1/Q (DFF_X1)
   0.01    0.10 v u2/ZN (NAND2_X1)
   0.00    0.10 v f2/D (DFF_X1)
           0.10   data arrival time

 200.00  200.00   clock CLK (rise edge)
   0.00  200.00   clock network delay (ideal)
 -50.00  150.00   clock uncertainty
   0.00  150.00   clock reconvergence pessimism
         150.00 ^ f2/CK (DFF_X1)
  -0.04  149.96   library setup time
         149.96   data required time
---------------------------------------------------------
         149.96   data required time
          -0.10   data arrival time
---------------------------------------------------------
         149.86   slack (MET)
```

b. Early path between F1 and F2

```
Hold Path Analysis:
Startpoint: f1 (rising edge-triggered flip-flop clocked by CLK)
Endpoint: f2 (rising edge-triggered flip-flop clocked by CLK)
Path Group: CLK
Path Type: min

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock CLK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 ^ f1/CK (DFF_X1)
   0.08    0.08 v f1/Q (DFF_X1)
   0.01    0.09 ^ u2/ZN (NAND2_X1)
   0.00    0.09 ^ f2/D (DFF_X1)
           0.09   data arrival time

   0.00    0.00   clock CLK (rise edge)
   0.00    0.00   clock network delay (ideal)
  50.00   50.00   clock uncertainty
   0.00   50.00   clock reconvergence pessimism
          50.00 ^ f2/CK (DFF_X1)
   0.01   50.01   library hold time
          50.01   data required time
---------------------------------------------------------
          50.01   data required time
          -0.09   data arrival time
---------------------------------------------------------
         -49.91   slack (VIOLATED)
```

Q3 Verilog netlist

```
module circuit2 (
   input A, B, C, D, E, CLK, SI, SE,
   output OUT, SO
);
   wire and1_out, nand1_out, f1_out,
f2_out, nand2_out, f3_out, final_out;

   // Instantiating gates and flip-flops
   AND2_X1 u1 (.A1(D), .A2(E),
.ZN(and1_out)); // AND Gate

   SDFF_X1 f1 (.D(and1_out), .SE(SE),
.SI(S1), .CK(CLK), .Q(f1_out)); // D
Flip-Flop F1

   NAND2_X1 u2 (.A1(C), .A2(f1_out),
.ZN(nand1_out)); // NAND Gate
```

```
   SDFF_X1 f2 (.D(nand1_out), .SE(SE),
.SI(f1_out), .CK(CLK), .Q(f2_out)); // D
Flip-Flop F2

   NAND2_X1 u3 (.A1(B), .A2(f2_out),
.ZN(nand2_out)); // NAND Gate

   SDFF_X1 f3 (.D(nand2_out), .SE(SE),
.SI(f2_out), .CK(CLK), .Q(f3_out)); // D
Flip-Flop F3

   NAND2_X1 u4 (.A1(A), .A2(f3_out),
.ZN(final_out)); // NAND Gate

   assign OUT = final_out;
   assign SO = f3_out; // Scan-out
endmodule
```

PS: I've combined the code snippets in sequence, with each section following after the white rectangles. Can also find the code here

Q4 SDC file for the functional mode for netlist

```
# clock period 200 ps
create_clock -name CLK -period 200 [get_ports CLK]

# clock uncertainty of 50 ps
set_clock_uncertainty 50 [get_clocks CLK]

# Set functional mode
set_case_analysis 0 [get_ports SE]

set_input_delay 20 -clock [get_clocks CLK] [get_ports {A B C D E SI}]
set_output_delay 20 -clock [get_clocks CLK] [get_ports {OUT SO}]
```

PS: Can also find the code here

Q4 worst slack

a. Late path between F1 and F2

```
Setup Path Analysis:
Startpoint: f1 (rising edge-triggered flip-flop clocked by CLK)
Endpoint: f2 (rising edge-triggered flip-flop clocked by CLK)
Path Group: CLK
Path Type: max

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock CLK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 ^ f1/CK (SDFF_X1)
   0.06    0.06 v f1/Q (SDFF_X1)
   0.02    0.08 ^ u2/ZN (NAND2_X1)
   0.00    0.08 ^ f2/D (SDFF_X1)
           0.08   data arrival time

 200.00  200.00   clock CLK (rise edge)
   0.00  200.00   clock network delay (ideal)
 -50.00  150.00   clock uncertainty
   0.00  150.00   clock reconvergence pessimism
         150.00 ^ f2/CK (SDFF_X1)
  -0.07  149.93   library setup time
         149.93   data required time
---------------------------------------------------------
         149.93   data required time
          -0.08   data arrival time
---------------------------------------------------------
         149.85   slack (MET)
```

b. Early path between F1 and F2

```
Hold Path Analysis:
Startpoint: f1 (rising edge-triggered flip-flop clocked by CLK)
Endpoint: f2 (rising edge-triggered flip-flop clocked by CLK)
Path Group: CLK
Path Type: min

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock CLK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 ^ f1/CK (SDFF_X1)
   0.06    0.06 v f1/Q (SDFF_X1)
   0.02    0.08 ^ u2/ZN (NAND2_X1)
   0.00    0.08 ^ f2/D (SDFF_X1)
           0.08   data arrival time

   0.00    0.00   clock CLK (rise edge)
   0.00    0.00   clock network delay (ideal)
  50.00   50.00   clock uncertainty
   0.00   50.00   clock reconvergence pessimism
          50.00 ^ f2/CK (SDFF_X1)
  -0.01   49.99   library hold time
          49.99   data required time
---------------------------------------------------------
          49.99   data required time
          -0.08   data arrival time
---------------------------------------------------------
         -49.91   slack (VIOLATED)
```

Q4 Comparisons & Explanations

Q2:

- **Setup Path:**
  - Data Arrival Time: **0.10 ps**
  - Data Required Time: **149.96 ps**
  - Slack: **149.86 ps** (MET)
- **Hold Path:**
  - Data Arrival Time: **0.09 ps**
  - Data Required Time: **50.01 ps**
  - Slack: **-49.91 ps** (VIOLATED)

Observations

Q4:

- **Setup Path:**
  - Data Arrival Time: **0.08 ps**
  - Data Required Time: **149.93 ps**
  - Slack: **149.85 ps** (MET)
- **Hold Path:**
  - Data Arrival Time: **0.08 ps**
  - Data Required Time: **49.99 ps**
  - Slack: **-49.91 ps** (VIOLATED)

Key Comparisons and Explanations

Setup Path (Late Path) Comparison:

- **Q2: Slack = 149.86 ps**
- **Q4: Slack = 149.85 ps**

Reason for Slack Decrease in Q4:

1. In Q4, SDFF flip-flops are used instead of DFF. The SDFF has a slightly lower **clock-to-Q delay** (0.06 ps in Q4 vs. 0.09 ps in Q2).
2. The slight improvement in flip-flop delay decreases the **data arrival time** by 0.02 ps in Q4. However, the **library setup time** for SDFF is marginally higher (-0.07 ps in Q4 vs. -0.04 ps in Q2).
3. The combined effect results in a small reduction in slack by **0.01 ps**.

Q4 Comparisons & Explanations

Key Comparisons and Explanations

Hold Path (Early Path) Comparison:

- **Q2: Slack = -49.91 ns**
- **Q4: Slack = -49.91 ns**

Why Does the Slack Change?

1. **Setup Slack Decrease Q4:**
   - The use of SDFF reduces propagation delays but increases setup timing constraints. This trade-off leads to a slight reduction in slack.
2. **Hold Slack Change:**
   - The dominant factor in hold analysis is the **clock uncertainty**. As this remains constant at 50 ns in both circuits, the slack violation is the approximately the same.

Reason for Change in Slack in Both Circuits:

1. The hold timing violations in both circuits are influenced by the same factors:
   - **Clock uncertainty**: Both circuits experience a **50 ns uncertainty** that significantly impacts the hold margin.
   - **Propagation delays**: While SDFF reduces the **clock-to-Q delay** slightly (0.06 ns in Q4 vs. 0.08 ns in Q2), the difference is small and does not mitigate the hold violation caused by the large uncertainty.
2. The changes in **data arrival time** (0.09 ns in Q2 vs. 0.08 ns in Q4) are not sufficient to affect the hold slack significantly.

Q5 SDC file for the shift mode for netlist

```
# clock period 200 ps
create_clock -name CLK -period 200 [get_ports CLK]

# clock uncertainty of 50 ps
set_clock_uncertainty 50 [get_clocks CLK]

set_input_delay 20 -clock [get_clocks CLK] [get_ports {A B C D E SI}]
set_output_delay 20 -clock [get_clocks CLK] [get_ports {OUT SO}]

# Set shift mode
set_case_analysis 1 [get_ports SE]
```

PS: Can also find the code here

Q5 worst slack

a. Late path between F1 and F2

```
Setup Path Analysis:
Startpoint: f1 (rising edge-triggered flip-flop clocked by CLK)
Endpoint: f2 (rising edge-triggered flip-flop clocked by CLK)
Path Group: CLK
Path Type: max

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock CLK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 ^ f1/CK (SDFF_X1)
   0.06    0.06 v f1/Q (SDFF_X1)
   0.00    0.06 v f2/SI (SDFF_X1)
           0.06   data arrival time

 200.00  200.00   clock CLK (rise edge)
   0.00  200.00   clock network delay (ideal)
 -50.00  150.00   clock uncertainty
   0.00  150.00   clock reconvergence pessimism
         150.00 ^ f2/CK (SDFF_X1)
  -0.09  149.91   library setup time
         149.91   data required time
---------------------------------------------------------
         149.91   data required time
          -0.06   data arrival time
---------------------------------------------------------
         149.85   slack (MET)
```

b. Early path between F1 and F2

```
Hold Path Analysis:
Startpoint: f1 (rising edge-triggered flip-flop clocked by CLK)
Endpoint: f2 (rising edge-triggered flip-flop clocked by CLK)
Path Group: CLK
Path Type: min

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock CLK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 ^ f1/CK (SDFF_X1)
   0.06    0.06 ^ f1/Q (SDFF_X1)
   0.00    0.06 ^ f2/SI (SDFF_X1)
           0.06   data arrival time

   0.00    0.00   clock CLK (rise edge)
   0.00    0.00   clock network delay (ideal)
  50.00   50.00   clock uncertainty
   0.00   50.00   clock reconvergence pessimism
          50.00 ^ f2/CK (SDFF_X1)
  -0.01   49.99   library hold time
          49.99   data required time
---------------------------------------------------------
          49.99   data required time
          -0.06   data arrival time
---------------------------------------------------------
         -49.92   slack (VIOLATED)
```

Q5 Comparisons & Explanations

Q4:

- **Setup Path:**
  - Data Arrival Time: **0.08 ps**
  - Data Required Time: **149.93 ps**
  - Slack: **149.85 ps** (MET)
- **Hold Path:**
  - Data Arrival Time: **0.08 ps**
  - Data Required Time: **49.99 ps**
  - Slack: **-49.91 ps** (VIOLATED)

Observations

Q5:

- **Setup Path:**
  - Data Arrival Time: **0.06 ps**
  - Data Required Time: **149.91 ps**
  - Slack: **149.85 ps** (MET)
- **Hold Path:**
  - Data Arrival Time: **0.06 ps**
  - Data Required Time: **49.99 ps**
  - Slack: **-49.92 ps** (VIOLATED)

Key Comparisons and Explanations

Setup Path (Late Path) Comparison:

- **Q4: Slack = 149.85 ps**
- **Q5: Slack = 149.85 ps**

- **Functional Mode:** The data travels through the path F1 → NAND2 → F2/D. The inclusion of the NAND2 gate increases the data arrival time to 0.08 ns.
- **Shift Mode:** The data travels directly from F1 → F2/SI without passing through the NAND2 gate, resulting in a reduced data arrival time of 0.06 ns.

Reason for Path Change: In shift mode (Q5), the flip-flops are connected in a scan chain for serial data shifting. This skips the NAND2 gate used in functional mode, making the data path simpler. As a result, the data arrives faster, but the slack stays the same because the clock does not change.

Q5 Comparisons & Explanations

Key Comparisons and Explanations

Hold Path (Early Path) Comparison:

- **Q4: Slack = -49.91 ns**
- **Q5: Slack = -49.92 ns**

- **Functional Mode:** The data path includes the NAND2_X1 gate, resulting in a data arrival time of 0.08 ns. This slightly reduces the risk of hold violations compared to shift mode.
- **Shift Mode:** The direct connection F1 → F2/SI reduces the data arrival time to 0.06 ns. While this shortens the data propagation delay, it exacerbates the hold time violation.

Reason for Path Change: In shift mode, the removal of the NAND2 gate reduces the delay in the data path. Although this optimization is beneficial for setup timing, it worsens hold timing issues as the early arrival of data increases the likelihood of hold violations.

Conclusion:

The transition from functional mode (Q4) to shift mode (Q5) alters the data paths between flip-flops F1 and F2:

- **Setup Path:** In shift mode, the direct connection bypasses the NAND2 gate, reducing the data arrival time but keeping slack unchanged.
- **Hold Path:** The same direct connection shortens the delay further, aggravating the hold violation due to an earlier data arrival.

This change reflects the design intent of shift mode, prioritizing efficient data shifting over timing robustness. To address the hold violations, additional circuit modifications, such as adding hold buffers, may be required.

PS: All the codes can be found here .

Thank You

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