VDF Assignment-4

Objective

The objective of this assignment is to gain a hands-on experience on the impact of scan insertion on timing.

Instructions

- The assignment needs to be done individually
- Each student will submit only one PDF file containing all the answers [no ZIP file or other format accepted.]
- The focus should not only be on running of the tool, but also on analysis/interpretation of the results.
- **Copying/Plagiarism is strictly prohibited. Institute copying/plagiarism policy will apply with no exception.**

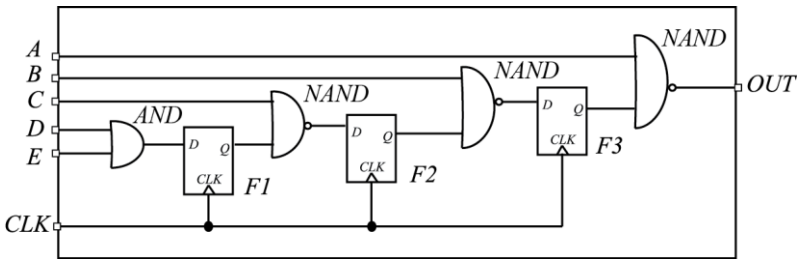
Choice of Tools

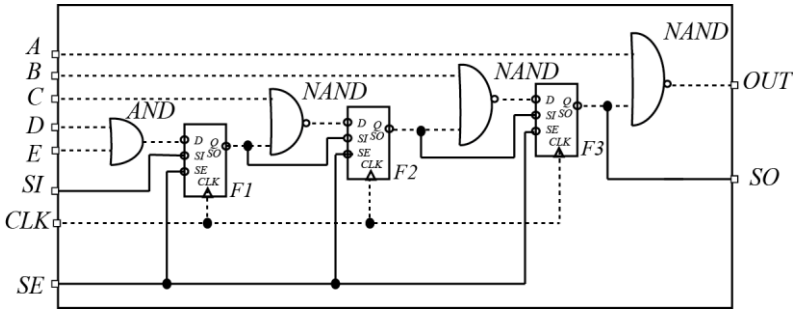
- You need to use the following tool

  Name of the tool: OpenSTA
  How to download and install and run? See Assignment 3

  You may use **Tempus** or **Primetime**, if you want (OpenSTA is preferable).

- You can use any technology library that has scan cells for D flip-flops.





Questions

1. Show screenshot or snippet of log file to prove that you have indeed run the tool [**If this is not given then your assignment will not be evaluated**].

2. Write a Verilog netlist for the circuit shown in (a). Show the Verilog netlist in the report. **[1 Mark]**

   Write an SDC file with clock period 200 ps and clock uncertainty of 50 ps. Choose other SDC commands as appropriate. **[1 Mark]**
   Run STA on the above netlist.
   Report the worst slack for the following cases:

   a. Late path between F1 and F2
   b. Early path between F1 and F2

   [2 Marks]

3. Write a Verilog netlist for the circuit shown in (b). Show the Verilog netlist in the report. F1, F2, F3 are scan cells. (Note that scan insertion is done in (b). In this assignment you are doing it manually to understand the concept. In practice (b) will be generated by a scan synthesis tool). **[2 Mark]**

4. Write SDC file for the functional mode for netlist of (b) (same as Q. 3. However, add the command set_case_analysis to distinguish the mode). **[1 Mark]**
   Run STA on the netlist for (b) using above SDC.
   Report the worst slack for the following cases:
   a. Late path between F1 and F2. Compare with the report of Q. 3a and explain why does the slack decrease. **[1+1+1 Mark]**
   b. Early path between F1 and F2. Compare with the report of Q. 3b and explain why does the slack change. **[1+1+1 Mark]**

5. Write SDC file for the shift mode for netlist of (b) (same as Q. 3. However, add the command set_case_analysis to distinguish the mode). **[1 Mark]**
   Run STA on the netlist for (b) using above SDC.
   Report the worst slack for the following cases:
   a. Late path between F1 and F2. Compare with the report of Q. 4a and explain why does the path change compared to the previous question. **[1+2 Mark]**
   b. Early path between F1 and F2. Compare with the report of Q. 4b and explain why does the path change compared to the previous question. **[1+2 Mark]**