VDF Assignment-1

Objective

The objective of this assignment is to gain hands-on experience on UNIX and TCL.

You can go through the following tutorials to get a heads start on UNIX and TCL:

UNIX:

https://www.google.com/url?q=https://www.youtube.com/watch?v%3DztPFMRfpPfk&sa=D&source=editors&ust=1724175316641209&usg=AOvVaw1H8lQA2q1MW999rL_VGOnl

TCL:

https://www.google.com/url?q=https://www.youtube.com/watch?v%3D1fPNZstiL4o&sa=D&source=editors&ust=1724175316641507&usg=AOvVaw0MdImLBNTi10UF98-kp_s6

Instructions

- These assignments need to be done individually
- Each student will submit a ZIP file containing TCL (.tcl) and Shell (.sh) files.
- Write comments in the code and also explain them wherever applicable.
- Do not copy code/explanation from others or the internet, not only in terms of **content** but also in terms of **presentation**.
- **Copying/Plagiarism is strictly prohibited. Institute copying/plagiarism policy will apply with no exception.**

Questions

1. Write a **TCL** script designed to analyze a given Verilog file and ascertain the count of occurrences for specific Verilog keywords:

a. always
b. initial
c. begin
d. end

If a line is a comment (starts with //), then you should not count these keywords contained in this line. Example following lines should not be counted:

// always do your homework

// initialize your design

// ending …..

Do not use any system calls (such as grep etc.) in this code.

Words not matching exactly (example initialize, beginning, bend etc.) should not be counted.

2. Write a **Shell** script designed to analyze a given Verilog file and ascertain the count of occurrences for specific Verilog keywords:

a. task
b. function
c. module
d. endmodule

If a line is a comment (starts with //), then you should not count these keywords contained in this line. Example following lines should not be counted:

// function is easy to implement

// starting the module

// ending …..

Use the shell commands only in the code. Do not use any other program (such as TCL script) inside your code.

Words not matching exactly (example multitask, functioning, etc.) should not be counted.

You will not be evaluated based on the Test Files' output. There will be a separate Verilog File for the evaluation. The Test Files are just for your reference.

Test File 1:

Expected output for TCL script:

Number of "**always**" statements is 1

Number of "**initial**" statements is 1

Number of "**begin**" statements is 4

Number of "**end**" statements is 4

Expected output for Shell script:

Number of "**task**" statements is 0

Number of "**function**" statements is 0

Number of "**module**" statements is 1

Number of "**endmodule**" statements is 1

Test File 2:

Expected output for TCL script:

Number of "**always**" statements is 3

Number of "**initial**" statements is 1

Number of "**begin**" statements is 8

Number of "**end**" statements is 8

Expected output for Shell script:

Number of "**task**" statements is 1

Number of "**function**" statements is 0

Number of "**module**" statements is 1

Number of "**endmodule**" statements is 1