Krishnendu Guha (Curriculum Vitae)

Current Position: Assistant Professor (Temporary Faculty) in National Institute of Technology (NIT), Jamshedpur
Previous Positions:
>   INSPIRE PhD Fellow *(Department of Science and Technology, Government of India)*
>   Intel India Research Fellow *from Intel Corporations, India*
>   Visiting Scientist in *Indian Statistical Institute (ISI), Kolkata*

Date of Birth: March 16, 1988
Nationality: Indian
e-mail: mail2krishnendu@gmail.com, krishnendu.ca@nitjsr.ac.in
Address: Uttarayan, Kaikhali Main Road, P.O.: R-Gopalpur, Kolkata- 700136, West Bengal, India
Contact no.: +91-9748333727, +91-7980657535

ORCID ID: https://orcid.org/0000-0003-1139-9582
Research Gate: https://www.researchgate.net/profile/Krishnendu_Guha3
Google Scholar: https://scholar.google.co.in/citations?user=qufeeP8AAAAJ&hl=en
DBLP Link: https://dblp.uni-trier.de/pers/hd/g/Guha:Krishnendu

EDUCATION AND ACHIEVEMENTS:

➢ **Post PhD Submission** (3rd December 2019- 30th November 2020): **Intel India Research Fellow**
>   **Topic:** *Security as a Cost based Model for Reconfigurable Hardware based Cloud Environment*
>   **Supervisors:** Dr. Krishna Paul, Mr. Biswadeep Chatterjee (Intel Corporations, India),
>   Prof. Amlan Chakrabarti (University of Calcutta)

➢ **Doctor of Philosophy (PhD)** (15th March 2015- 2nd Dec 2019):
>   Information Technology, University of Calcutta
>   **Thesis Title:** *Self Aware Nature Inspired Approaches Ensuring Embedded Security*
>   **Date of Thesis Submission:** 2nd December 2019
>   **Date of Defence:** 13th February, 2021 (Defence delayed due to CoVID19 lockdown)
>   **Supervisors:** Prof. (Dr.) Amlan Chakrabarti, Dr. Debasri Saha

➢ **Master of Technology (M. Tech.)** - (1st August 2012- 31st July 2014), University of Calcutta
>   **Achievement:** 1st Class 1st Position **(Gold Medallist)**

➢ **Master of Computer Applications (MCA)** (1st August 2009- 31st July 2012), University of Calcutta
>   **Achievement:** 1st Class 2nd Position

➢ **Bachelor of Science (B. Sc.)** (1st August 2006- 31st July 2009) – Physics Honours,
>   Scottish Church College under University of Calcutta

➢ **ISC (Class XII)** (1st May 2004- 1st April 2006), The Frank Anthony Public School, Kolkata
>   **Achievement:** 100% in ISC Mathematics

➢ **ICSE (Class X)** (April 2004), The Frank Anthony Public School, Kolkata

AWARDS AND RECOGNITIONS

- **University Gold Medal** (MTech (IT) 2014) – University of Calcutta
- **INSPIRE Fellowship Award** (2016) - Department of Science and Technology, Government of India
- **Intel India Final Year PhD Fellowship Award** (2019) – Intel Corporations, India
- **University of Calcutta Research Fellowship Award** (2014)- University of Calcutta
- **GATE Scholarship Award** (2012)- (Ministry of Human Resource Development, Government of India)
- **PhD Forum Award** (2nd Runners Up) (2018) - 31st International Conference in VLSI Design, (Pune, India), 2018
- **University Travel Endowment Award** (2018) – University of Calcutta for travelling to Prague, Czech Republic
- **Conference Fellowships/ Grants** (Design Automation Conference (DAC) 2020, Design, Automation and Test in Europe (DATE) 2020, Asian Test Symposium (ATS) 2019, VLSI Design and Embedded Systems (VLSID) 2020, 2018, 2017, 2016, VLSI Design and Test (VDAT) 2015)

PROFESSIONAL RESEARCH EXPERIENCE

- **VISITING SCIENTIST in Indian Statistical Institute (ISI), Kolkata** (1st December 2020- 1st March 2021)
    Domain: Statistical Cost Analysis for Hardware Security Techniques

- **INTEL INDIA RESEARCH FELLOW** (3rd December 2019- 30th November, 2020)
    Supported by Intel India
    Domain: Security for Reconfigurable Hardware based Cloud Platforms

- **INSPIRE PhD Fellow** (16th June 2016- 2nd December 2019)
    Supported by Department of Science and Technology, Government of India
    Domain: Hardware Security, Self Awareness, Nature Inspired Approaches

- **UNIVERSITY RESEARCH FELLOW** (26th September 2014- 15th June 2016)
    Supported by University of Calcutta under University Grants Commission, Government of India
    Domain: Artificial Intelligence, Hardware Security

- **GATE Scholar** (1st August 2012- 31st July 2014)
    Supported by Ministry of Human Resource Development (MHRD), Government of India for Studies and Research during MTech
    Domain: On-chip Power Distribution Networks

PROFFESSIONAL MEMBERSHIPS
- Association of Computing Machinery (ACM) Student Member: Membership No.: 9552484
- Institute of Electrical and Electronics Engineers (IEEE) Student Member: Membership No.: 93406088
- International Association of Engineers (IAENG): Membership No.: 157962
- Thompson Reuters Researcher ID: B-8501-2016

TECHNICAL SKILLS
- Associated with the forming and development of VLSI Design Laboratory and Embedded System Laboratory in A.K.Choudhury School of IT, University of Calcutta.
- Experience in Hardware Designing- Field Programmable Gate Arrays (FPGA) and Application Specific Integrated Circuits (ASIC) platforms.
- Tools: Xilinx, Mentor Graphics, Matlab, etc.
- Programming in Verilog, VHDL, C, Java, etc.

NATIONAL LEVEL QUALIFICATIONS:
- University Grants Commission (UGC) National Eligibility Test (**NET**) June **2013**
    (Recognition for Lectureship in Computer Science and Applications)
- University Grants Commission (UGC) National Eligibility Test (**NET**) June **2012**
    (Recognition for Lectureship in Computer Science and Applications)
- Graduate Aptitude Test in Engineering (**GATE**) **2012**
    (Subject: Computer Science and Engineering)

TEACHING EXPERIENCE

- **Assistant Professor in National Institute of Technology (NIT), Jamshedpur (February 2021- Present)**
- **Springer IVARSITY Program (Online Course) "*Cybersecurity for Critical Infrastructures*"**
  (Starting April 2021)
- **Guest Lecturer in University of Calcutta:**
  C and Data Structures (BTech) (Session 2019-2020)
- **Teaching Assistant in University of Calcutta:**
- **As a Research Scholar**
  Embedded Systems (BTech IT) (Session 2017-2018)
  Computer Architecture, Cryptography, Security and Privacy, VLSI Design (MTech IT & CSA)
    (Sessions 2017-18, 2016-17, 2015-16, 2014-15)
  Database Management Systems- SQL (MCA)
    (Sessions 2018-19, 2017-18, 2016-17, 2015-16, 2014-15)
- **As a GATE Scholar**
  SQL Classes (MCA) (Session 2013-14 and Session 2012-13)
  UNIX Classes (MCA) (Session 2013-14 and Session 2012-13)

REVIEWER
- **Journals:**
  IEEE Transactions on Semiconductor Manufacturing
  Springer Journal on Supercomputing
- **Conferences:**
  Several IEEE and Springer Conferences (like IEEE TENCON 2020, IEEE RTDPCC 2020, Springer
  IEMIS 2018, etc.)

- **Assistant Mentor** for MTech and BTech Students

CO-CURRICULAR ACTIVITIES:

- Organizing Team Member in 29th VLSI Design Conference, Kolkata, 2016.
- Anchor and Organizing Team Member in various Tech Events in University of Calcutta
- Two Days Workshop on Waging War against Cyber Crime, 2016.
- A Three Day Workshop in Embedded System Design: recent trends and techniques, March 2013 (University of Calcutta)
- All-Go-Rhythm Technical Seminar, 2012, 2013, 2017, 2018 (AKCSIT, University of Calcutta)

LIST OF REFERENCES:

1. Prof. (Dr.) Amlan Chakrabarti
Email: acakcs@caluniv.ac.in
Professor and Director,
A.K.Choudhury School of Information Technology,
University of Calcutta, India

2. Dr. Debasri Saha
Email: debasri_cu@yahoo.in
Assistant Professor
A. K. Choudhury School of I.T.,
University of Calcutta, India

3. Mr. Biswadeep Chatterjee
Email: biswadeep.chatterjee@intel.com
Director of Engineering
Intel Corporations, India

4. Dr. Sangeet Saha
Email: sangeet.saha@essex.ac.uk
Senior Research Officer,
University of Essex (School of CS and EE), UK

5. Prof. Subhamoy Maitra
Email: subho@isical.ac.in
Professor and Head,
Applied Statistics Unit,
Indian Statistical Institute (ISI), Kolkata

PUBLICATIONS AND PRESENTATIONS (till date)

PUBLICATIONS
(LINK IN GOOGLE SCHOLAR: https://scholar.google.co.in/citations?user=qufeeP8AAAAJ&hl=en)
(DBLP Link: https://dblp.uni-trier.de/pers/hd/g/Guha:Krishnendu)

Journals

- [j1] K. Guha, D. Saha and A. Chakrabarti, "Stigmergy based Security for SoC Operations from Runtime Performance Degradation of SoC Components," *ACM Transactions on Embedded Computing Systems,* vol. 18, no. 2, Article 14, March 2019

- [j2] K. Guha, D. Saha and A. Chakrabarti, "Real Time SoC Security against Passive Threats using Crypsis Behavior of Geckos," *ACM Journal of Emerging Topics in Computing*, vol. 13, no. 3, Article 41, March 2017

- [j3] K. Guha, A. Majumder, D. Saha and A. Chakrabarti, "Criticality based Reliability against Hardware Trojan Attacks for Processing of Tasks on Reconfigurable Hardware," *Elsevier Microprocessor and Microsystems,* vol. 71, pp. 102865, 2019

- [j4] K. Guha, A. Majumder, D. Saha and A. Chakrabarti, "Dynamic Power Aware Scheduling of Real Time Tasks for FPGA based Cyber Physical Systems against Power Draining Hardware Trojan Attacks," *Springer Journal of Supercomputing*, vol. 76, pp. 8972-9009, 2020, https://doi.org/10.1007/s11227-020-03184-3

- [j5] M. Chakraborty, K. Guha, D. Saha, P. Mitra and A. Chakrabarti, "Pre-Layout Decoupling Capacitance Estimation and Allocation for Noise-Aware Crypto-System on Chip Applications", *Journal of Low Power Electronics (JOLPE),* vol.11, no.3, 2015, pp. 333-339

Conferences

- [c1] K. Guha, D. Saha and A. Chakrabarti, "Blockchain Technology Enabled Pay Per Use Licensing Approach for Hardware IPs," *Design, Automation and Test in Europe Conference (DATE 2020),* Grenoble, France, 2020, pp. 1618-1621

- [c2] K. Guha, A. Majumder, D. Saha and A. Chakrabarti, "Reliability Driven Mixed Critical Tasks Processing on FPGAs against Hardware Trojan Attacks," *2018 21st Euromicro Conference on Digital System Design (DSD 2018),* Prague, Czech Republic, 2018, pp. 537-544

- [c3] K. Guha, A. Majumder, D. Saha and A. Chakrabarti: "Ensuring Green Computing in Reconfigurable Hardware Based Cloud Platforms from Hardware Trojan Attacks", *2020 IEEE Region 10 Conference (TENCON 2020),* Osaka, Japan, 2020, pp. 1380-1385

- [c4] K. Guha, D. Saha and A. Chakrabarti, "Zero Knowledge Authentication for Reuse of IPs in Reconfigurable Platforms," *2019 IEEE Region 10 Conference (TENCON)*, Kochi, India, 2019, pp. 2040-2045.

- [c5] K. Guha, D. Saha and A. Chakrabarti, "A Multi-Agent Co-operative Model to Facilitate Criticality based Reliability for Mixed Critical Task Execution on FPGA based Cloud Environment," *2020 33rd International Conference on VLSI Design and 2020 19th International Conference on Embedded Systems (VLSID 2020)*, Bangalore, India, 2020, pp. 137-142

- [c6] K. Guha, S. Saha and A. Chakrabarti, "SHIRT (Self Healing Intelligent Real Time) Scheduling for Secure Embedded Task Processing," *2018 31th International Conference on VLSI Design and 2018 17th International Conference on Embedded Systems (VLSID 2018),* Pune, 2018, pp. 463-464

- [c7] K. Guha, D. Saha and A. Chakrabarti, "Self Aware SoC Security to Counteract Delay Inducing Hardware Trojans at Runtime," *2017 30th International Conference on VLSI Design and 2017 16th International Conference on Embedded Systems (VLSID 2017),* Hyderabad, 2017, pp. 417-422

- [c8] K. Guha, D. Saha and A. Chakrabarti, "SARP: Self Aware Runtime Protection against Integrity Attacks of Hardware Trojans," *22nd International Symposium on VLSI Design and Test (VDAT 2018)*, Madurai, India, 2018, pp. 198-209

- [c9] K. Guha, D. Saha and A. Chakrabarti, "RTNA: Securing SOC Architectures from Confidentiality Attacks at Runtime using ART1 Neural Networks," *2015 19th International Symposium on VLSI Design and Test (VDAT 2015)*, Ahmedabad, 2015, pp. 1-6

- [c10] K. Guha, R.R. Sahani, M. Chakraborty, A. Chakrabarti and D. Saha, "Analysis of Secret Key Revealing Trojan Using Path Delay Analysis for Some Cryptocores*", 2014 3rd International Conference on Frontiers in Intelligent Computing Theory and Applications (FICTA 2014),* Springer AISC vol. 328, 2014, pp. 13-20

- [c11] M. Chakraborty, A. Chakrabarti, P. Mitra, D. Saha and K. Guha, "Pre-Layout Module wise Decap Allocation for Noise Suppresion and Accurate Delay Estimation for SoC", *20th International Symposium on VLSI Design and Test (VDAT 2016)*, Guwahati, 2016 ,pp.1-6

- [c12] M. Chakraborty, K. Guha, A. Chakrabarti and D. Saha, "Analysis of Power Distribution Network for Some Cryptocores," *2014 International Conference on Advances in Computing, Communications and Informatics (ICACCI 2014),* Delhi, 2014, pp. 2618-2622

- [c13] A. Mazumdar, M. Chakraborty, K. Guha and A. Chakrabarti: "CAD Based Analysis of Power Distribution Network for SOC Design", *2015 2nd International Doctoral Symposium on Applied Computation and Security Systems (ACSS 2015),* Springer AISC vol. 396, 2015, pp. 189-198

- [c14] A. Majumder, K. Guha, S. Saha and A. Chakrabarti: "Auction based Power Aware Real Time Scheduler for Heterogeneous FPGA Cloud Platform", *2019 IEEE International Symposium on Smart Electronic Systems (iSES 2019),* pp. 81-86

- [c15] K. Guha, K. Paul, B. Chatterjee and A. Chakrabarti, "Criticality based Reduction of Security Costs in a FPGA based Cloud Computing Farm," *2021 34th International Conference on VLSI Design and 2021 20th International Conference on Embedded Systems (VLSID 2021)*, Guwahati, India, 2021 *[Accepted]*

Newsletter/ Magazines

- K. Guha, D. Saha and A. Chakrabarti, "Hardware Trojan Horses: The New Face of Cyber-Terrorism," IEEE India Council Newsletter, vol. 13, no. 4, Oct-Dec 2018,
  Link: http://sites.ieee.org/indiacouncil/files/2019/01/p48-p52.pdf

- K. Guha, D. Saha and A. Chakrabarti, "Hardware Trojan Threat to Robotic Control Systems," Industrial Automation Magazine India, August 2020,
  Link: https://www.industrialautomationindia.in/articleitm/10403/Hardware-Trojan-Threat-to-Robotic-Control-Systems/articles

Books
- [b1] K. Guha, S. Saha and A. Chakrabarti, "Self Aware Security for Real Time Task Schedules in Reconfigurable Hardware Platforms," (Accepted and to be published by Springer Nature in 2021)

PhD FORUM PRESENTATIONS
PhD Thesis Topic: Self Aware Nature Inspired Approaches Ensuring Embedded Security
   Krishnendu Guha, Supervisors: Prof. (Dr.) Amlan Chakrabarti and Dr. Debasri Saha

- [p1] DAC 2020: Design, Automation Conference (San Francisco, USA)
- [p2] DATE 2020: Design, Automation and Test in Europe Conference (Grenoble, France)
- [p3] ATS 2019: Asian Test Symposium (Kolkata, India)
- [p4] VLSID 2018: 31st International Conference on VLSI Design [PhD Forum on Ongoing Work] (Pune, India)