Iteration-2 → for stage 1 to get gain ≈ 80dB.

→ providing $V_{ds5} = V_{ds6} = 0.15V$

→ providing $V_{ds9} = V_{ds15} = 0.2V$

→ providing $V_{ds7} = V_{ds11} = V_{ds12} = V_{ds17} = 0.18V$.

from V_{ds} and current in the transistor, we get (W/L) of all transistor.

gain of stage 1 ≈ 80 dB.

Design flow of 2nd Stage (class AB Stage)

→ We get common output of Ist stage. which is V_g of M_{19} and M_{20}.

→ V_{gs} of M_{19} and M_{20} is calculated.

$V_g M_{19} = 1.19V$

$V_g M_{20} = 0.625V$

$V_{sg} M_{19} = 1.8 - 1.19V = 0.61$

$V_{gs} M_{20} = 0.625 - 0$

$= 0.625V$

→ Assume current in M_{19} & M_{20} (I_{oss})

$$I_{oss} = I_{bias}\left(1 + \frac{C_L}{C_C}\right)$$

where $C_C = 0.65pF$

$C_L = 5pF$

$I_{bias} = 40\mu A$.

$$\boxed{I_{oss} = 0.347mA}$$

→ Calculate $(W/L)_{19\&20}$ using formula.

$$(W/L) = \frac{2I_D}{\mu_{Con}(V_{gsT})^2}$$

$(W/L)_{19} = 262$

$(W/L)_{20} = 40$ [Ist iteration]

→ Range C_C :-

$$\frac{g_{m1}}{C_C} > 4GF$$

$$\frac{g_{m1}}{4GF} > C_C$$

$$C_C < \frac{0.369 \times 10^{-3}}{2\pi X} \doteq 2.34pF$$

$$C_c > \frac{g_{m1}}{g_{m19}} \times C_L$$

$$C_c > \frac{0.369 \times 10^{-3}}{3.64 \times 10^{-3}} \times 5 \times 10^{-12}$$

$C_c > 0.5pF$

$$\boxed{0.5pF < C_c < 2.3pF}$$

→ Calculation of R_z.

- first we get poles from the simulation.

$$\frac{g_{m19}}{C_L} = 10.33MHz.$$

- for pole zero cancellation.

$$\text{Zero} = \text{pole}.$$

$$\frac{g_{m19}}{2\pi C_c (1 - g_{m19} R_z)} = 10.33MHz.$$

$$\boxed{R_z = 24.7K}$$

→ with above R_z p.m was not meeting specification.

→ so we used.

$$R_z > \frac{1}{g_{m19}} \left(1 + \frac{C_L}{C_c}\right)$$

$$\boxed{R_z > 2.387K}$$