EE618 Course Project, IIT Bombay

Operational Amplifier Design

Total Marks: 50

Deadline : Friday, 4th December 2020, 8:00 PM

The report submission is through the link provided on EE618 Moodle webpage.

- In this project you will design an Op-Amp inspired from TI OPA344/345.
- Reference for the Op-Amp internal circuit configuration: OPA344/345 data sheet uploaded on Moodle with highlights, also available from TI website (https://www.ti.com/product/OPA344)
- Use PTM 180nm CMOS technology model file. V_{DD}= 1.8 V, V_{SS} = 0 V.
  PTM model file can be accessed using this link
- **Notice:** Use the following relations (λ: Grid size = 90 nm).
  AS = 4λ×W (for single-finger transistor)
  PD = PS = 2× (4λ + W) (for single-finger transistor)
  AD = 2λ×W (for multi-finger transistor)
  PD = PS = 4λ + W (for multi-finger transistor)
- Maximum transistor length in the design should not be more than 2μm.
- In case, the transistor bulk connection is not mentioned :
  Bulk of NMOS transistor should be connected to V_{SS}.
  Bulk of the PMOS transistor should be connected to the source of same transistor.
- **Note:** ngSPICE netlist for Op-amp is provided to you on Page 6 of this Project PDF. You can modify the template for your design. You have to mention the work contribution from each member of your group at the end of your report. The template for which is given on Page 5.

Target requirements and specifications

Note : These are different from data sheet specifications.

- Single ended output
- Open loop small signal low-frequency voltage gain > 100 dB
- Unity gain bandwidth > 10 MHz
- Input CM voltage range: 100 mV to 1.7 V
- Output voltage range: 100 mV to 1.7 V
- Phase margin > 60º (Load capacitance = 5 pF)
- Slew rate > 2 V/μs (Load capacitance = 5 pF)

Op-amp Architecture

The purpose of this course project is to design a rail-to-rail, two folded cascode stages Op-amp with Class-AB output stage. The circuit diagram of the same is shown in Fig 1.

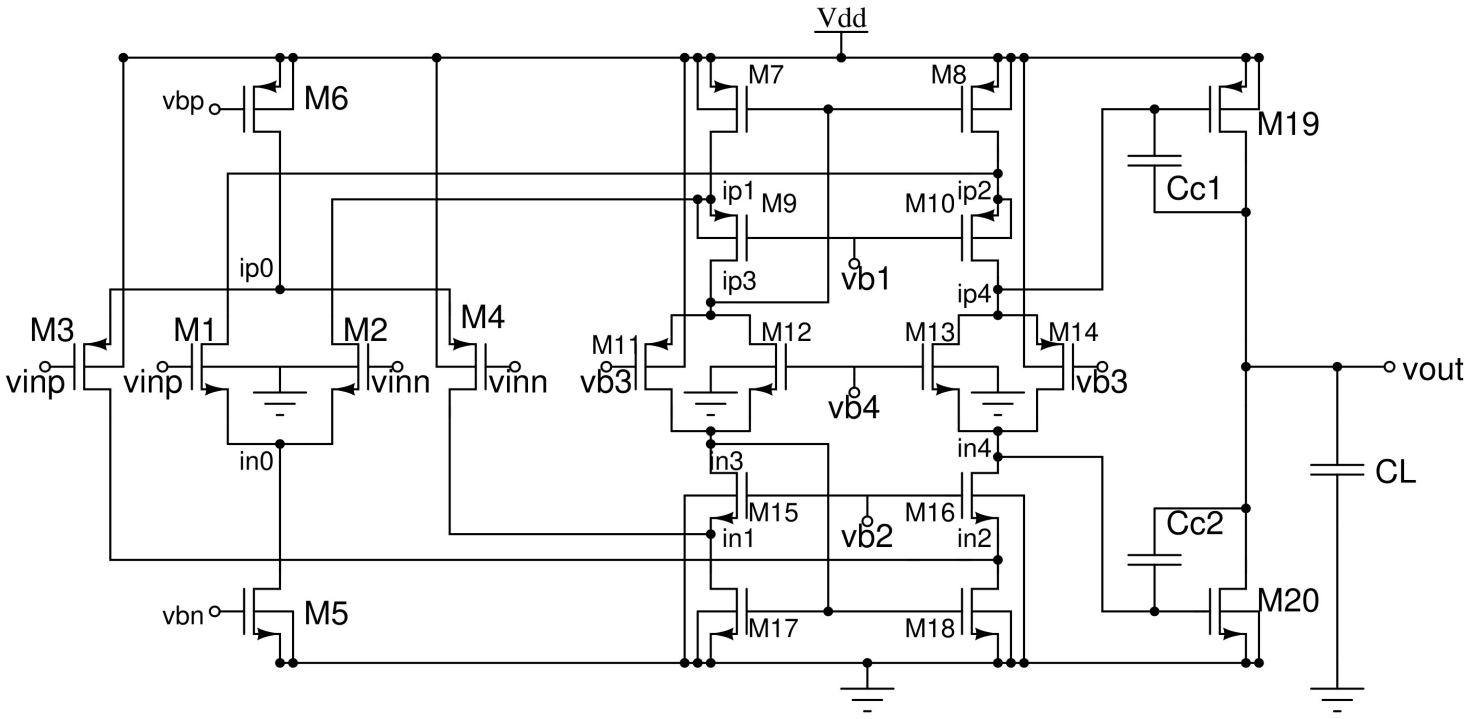

Figure 1: Two stage rail-to-rail folded cascode Op-amp with Class AB output stage

1- Op-amp Design flow (Total 6 + 1 Marks)

1.1 Report the design flow of the op-amp in the form of step by step procedure. Design flow involves determining bias currents, voltages and size of transistors compatible with section 2 of this project using the information from Assignment 2. [3 marks]

1.2 The design procedure may not succeed in one step. So simply show how you repeated the design to finally achieve the target specifications. [2 marks]

1.3 Clearly show bias currents and voltages on the schematic. [0.5 marks]

1.4 Write size of transistors in a table. [0.5 marks]

2- Reference Generator Circuit Design (Total 5 + 1 Marks)

In this section of the project, you will design a reference generator circuit of your choice. Reference generator circuit includes generating reference current (I_{ref}) first and then use current mirroring to generate bias voltages : V_{bn}, V_{bp} and V_{b1} to V_{b4}, .

2.1 Draw the reference generator circuit which includes generating reference current (I_{ref}) and use current mirroring to generate other bias voltages for Op-amp. [2 marks]

2.2 Report the step by step design procedure for reference generator circuit. [2 marks]

2.3 Tabulate the size of transistors used in the circuit. [1 mark]

3- DC Simulations (Total 5 + 1 Marks)

3.1 Connect the Op-amp in closed loop mode with voltage gain of -1 and apply DC common mode voltage (V_{CM}) at positive terminal of Op-amp. [1 mark]

3.2 Run DC simulations on Op-amp including reference generator and find DC operating points. -[2 marks]

3.3 DC operating points should clearly show all the node voltages and currents. [2 marks]

4- AC Simulations (Total 5 + 1 Marks)

4.1 Plot the open loop differential voltage gain (in dB) as a function of frequency. Highlight the approximate location of poles and zeros. (Use common mode voltage : 0.9 V) [1.5 marks]

4.2 Compare the results from simulation with estimated pole-zero locations from hand calculations (C_L = 5 pF) [1 mark]

4.3 Plot phase of open loop voltage gain as a function of frequency and specify the phase margin. -[1.5 marks]

4.4 Calculate the roll-off at 1 octave above unity gain frequency. [1 mark]

5- Slew rate Simulation (Total 5 + 1 Marks)

5.1 Connect the Op-amp in closed loop mode with voltage gain of -1. (Use common mode voltage : 0.9 V). [1 mark]

5.2 Simulate step response to +450 mV and -450 mV differential input step voltage and calculate slew rate. [4 marks]

6- Transient Simulation (Total 5 + 1 Marks)

6.1 Connect the Op-amp in closed loop mode with voltage gain of -1. (Use common mode voltage : 0.9 V). [1 mark]

6.2 Run transient simulation for maximum output voltage swing. [4 marks]

7- Common-mode (CM) DC Simulation (Total 5 + 1 Marks)

7.1 Connect the Op-amp in closed loop mode with voltage gain of -1. [0.5 marks]

7.2 Sweep the common-mode DC input voltage from V_{CM_min} to V_{CM_max} (total range better than 50% of the VDD). Plot output CM DC voltage as a function of input CM DC voltage. [2 marks]

7.3 Calculate the non-linearity of Op-amp by marking the values of slope at V_{CM} = 100 mV, 0.9 V and 1.6 V . [2 marks]

7.4 Report the maximum and minimum values of the slope calculated in 7.3 part. [0.5 marks]

Marking scheme :

- Section 1 of the report carries 7 marks, rest each section has 6 marks (Total: 43 marks).
- 1 mark for clarity of the plots, annotations and explanation of each graph for each section (Total: 7 marks).

Total : 50 Marks

All the best.

Work contribution template

- You have to write work contribution from each member of your group at the end of project report using this template.
- Write the names of your group members in place of Member 1 and Member 2. For each question number, put a checkmark (✓) in Member 1 column or Member 2 column to specify whether the question is solved by Member 1 or Member 2 respectively.
- You may add any comments if you have in the same columns corresponding to every question.

Example to fill up the table :

Question number	**Harry**	**Ron**
1.1	(✓) Comment 1	
1.2		(✓) Comment 2
1.3		(✓)
1.4	(✓)	

Table 1: Example table

Question number	**Member 1**	**Member 2**
1.1		
1.2		
1.3		
1.4		
2.1		
2.2		
2.3		
3.1		
3.2		
3.3		
4.1		
4.2		
4.3		
4.4		
5.1		
5.2		
6.1		
6.2		
7.1		
7.2		
7.3		
7.4		

Table 2: Table to be filled up

OTA subcircuit netlist

```
*OTA symbol
*Defining the OTA schematic here 'Opamp_under_test'
.subckt Opamp_under_test vinn vinp vout VDD VSS

.param lambda = 90n

***OTA parameters (to be modified)***
.param W1 = 1u
.param W2 = 1u
.param W3 = 1u
.param W4 = 1u
.param W5 = 1u
.param W6 = 1u
.param W7 = 1u
.param W8 = 1u
.param W9 = 1u
.param W10 = 1u
.param W11 = 1u
.param W12 = 1u
.param W13 = 1u
.param W14 = 1u
.param W15 = 1u
.param W16 = 1u
.param W17 = 1u
.param W18 = 1u
.param W19 = 1u
.param W20 = 1u
.param L = 1u
***/OTA parameters (to be modified)***

***OTA schematic (Do not change this)***
M1 ip2 vinp in0 VSS nmos L=L W=W1 AS={4*lambda*W1} PS={2*W1+8*lambda} AD={4*lambda*W1} PD={2*W1+8*lambda}
M2 ip1 vinn in0 VSS nmos L=L W=W2 AS={4*lambda*W2} PS={2*W2+8*lambda} AD={4*lambda*W2} PD={2*W2+8*lambda}
M3 in2 vinp ip0 VDD pmos L=L W=W3 AS={4*lambda*W3} PS={2*W3+8*lambda} AD={4*lambda*W3} PD={2*W3+8*lambda}
M4 in1 vinn ip0 VDD pmos L=L W=W4 AS={4*lambda*W4} PS={2*W4+8*lambda} AD={4*lambda*W4} PD={2*W4+8*lambda}
M5 in0 vbn VSS VSS nmos L=L W=W5 AS={4*lambda*W5} PS={2*W5+8*lambda} AD={4*lambda*W5} PD={2*W5+8*lambda}
M6 ip0 vbp VDD VDD pmos L=L W=W6 AS={4*lambda*W6} PS={2*W6+8*lambda} AD={4*lambda*W6} PD={2*W6+8*lambda}
M7 ip1 ip3 VDD VDD pmos L=L W=W7 AS={4*lambda*W7} PS={2*W7+8*lambda} AD={4*lambda*W7} PD={2*W7+8*lambda}
M8 ip2 ip3 VDD VDD pmos L=L W=W8 AS={4*lambda*W8} PS={2*W8+8*lambda} AD={4*lambda*W8} PD={2*W8+8*lambda}
M9 ip3 vb1 ip1 ip1 pmos L=L W=W9 AS={4*lambda*W9} PS={2*W9+8*lambda} AD={4*lambda*W9} PD={2*W9+8*lambda}
M10 ip4 vb1 ip2 ip2 pmos L=L W=W10 AS={4*lambda*W10} PS={2*W10+8*lambda} AD={4*lambda*W10} PD={2*W10+8*lambda}
M11 in3 vb3 ip3 VDD pmos L=L W=W11 AS={4*lambda*W11} PS={2*W11+8*lambda} AD={4*lambda*W11} PD={2*W11+8*lambda}
M12 ip3 vb4 in3 VSS nmos L=L W=W12 AS={4*lambda*W12} PS={2*W12+8*lambda} AD={4*lambda*W12} PD={2*W12+8*lambda}
M13 ip4 vb4 in4 VSS nmos L=L W=W13 AS={4*lambda*W13} PS={2*W13+8*lambda} AD={4*lambda*W13} PD={2*W13+8*lambda}
M14 in4 vb3 ip4 VDD pmos L=L W=W14 AS={4*lambda*W14} PS={2*W14+8*lambda} AD={4*lambda*W14} PD={2*W14+8*lambda}
M15 in3 vb2 in1 VSS nmos L=L W=W15 AS={4*lambda*W15} PS={2*W15+8*lambda} AD={4*lambda*W15} PD={2*W15+8*lambda}
M16 in4 vb2 in2 VSS nmos L=L W=W16 AS={4*lambda*W16} PS={2*W16+8*lambda} AD={4*lambda*W16} PD={2*W16+8*lambda}
M17 in1 in3 VSS VSS nmos L=L W=W17 AS={4*lambda*W17} PS={2*W17+8*lambda} AD={4*lambda*W17} PD={2*W17+8*lambda}
M18 in2 in3 VSS VSS nmos L=L W=W18 AS={4*lambda*W18} PS={2*W18+8*lambda} AD={4*lambda*W18} PD={2*W18+8*lambda}
M19 vout ip4 VDD VDD pmos L=L W=W19 AS={4*lambda*W19} PS={2*W19+8*lambda} AD={4*lambda*W19} PD={2*W19+8*lambda}
M20 vout in4 VSS VSS nmos L=L W=W20 AS={4*lambda*W20} PS={2*W20+8*lambda} AD={4*lambda*W20} PD={2*W20+8*lambda}

Cc1 ip4 vout 4p
Cc2 in4 vout 4p

***/OTA schematic (Do not change this)***

.ends
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