CMOS Analog Design

Project :- Rail-to-Rail opamp.

Design flow :-

Requirement :- gain of 2 stages >100 dB.

We want to get around 60dB gain from stage 1. and Rest from the class AB stage.

$V_{thn} = 0.399V$
$V_{thp} = 0.42V$ [given in the model file - PTM_180nm]

Gain of stage 1 is given by

$$A_{V1} \approx g_{m1}(g_{m10} r_{o10} r_{o8})$$

Assuming $g_{m1} = 0.25ms = g_{m2} = g_{m3} = g_{m4}$
$I_{no} = I_{po} = 50uA$
$I_{p3} = I_{p4} = 50uA$.

from g_{m1} (we can get (W/L) of $M_1 M_2 M_3 M_4$)

using formula

$$g_m = \sqrt{2 I_D \mu_n C_{ox} (W/L)}$$

→ providing $V_{dss} = V_{ds8} = 0.15V$ to the tail current sources. (M_5 and M_6)

→ $V_{dd} = 1.8V$ (given)

→ dividing V_{dd} among $M_7 M_8, M_9, M_{10}, M_{11}, M_{12}, M_{13}, M_{14} M_{15} M_{16} M_{17}$.

V_{ds} for $M_7, M_8, M_{17} M_{18}, M_{11} M_{12} M_{13} M_{14} = 0.3V$

V_{ds} for $M_9, M_{10}, M_{15} M_{16} = 0.40V$ (these may go in triode region first)

→ from V_{ds} and current in the transistor we can calculate the (W/L) of all transistors.

→ for finding bias voltages –

$$V_{b3} - V_{gsm11} - V_{gs17} - V_{dd} = 0$$

$$V_{b4} - V_{gs14} - V_{gs17} = 0$$

$$-V_{b2} + V_{gs15} + V_{ds17} = 0$$

$$-V_{dd} + V_{sd7} + V_{sg15} + V_{b1} = 0$$

→ r_o can be calculategd using formula.

$$r_o = \frac{1}{\lambda I_D}$$

$\lambda_n = 0.05$, $\lambda_p = 0.1$ } given.

→ according to above assumption,

Hand Calculation gain is –

$$A_{V_1} = 2380.$$

$$\boxed{A_{V_1} \approx 67.5 \text{ dB}}$$

→ with Simulation

Stage 1 gain. $\boxed{A_{V_1} = 68.20 \text{ dB}}$