



Indian Institute of Technology Bombay

Electrical Engineering Department

CMOS ANALOG VLSI DESIGN  
SELF PROJECT: DECEMBER 2021

Submitted at: <https://github.com/Shivam1164/Rail-2-Rail-Op-Amp>

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**Task:**

- In this project designed an Op-Amp inspired from TI OPA344/345.
- Reference for the Op-Amp internal circuit configuration: OPA344/345 data sheet uploaded on Moodle with highlights, also available from TI website (<https://www.ti.com/product/OPA344>)
  - Use PTM 180nm CMOS technology model file. VDD = 1.8 V, VSS = 0 V.
  - Notice: Use the following relations (W: Grid size = 90 nm).
    - $AS = 4 \text{ W}$  (for single-negger transistor)
    - $PD = PS = 2 \text{ W} (4 \text{ W})$  (for single-negger transistor)
    - $AD = 2 \text{ W}$  (for multi-negger transistor)
    - $PD = PS = 4 \text{ W} + W$  (for multi-negger transistor)

**Target requirements and specifications**

- Single ended output
- Open loop small signal low-frequency voltage gain > 100 dB
- Unity gain bandwidth > 10 MHz
- Input CM voltage range: 100 mV to 1.7 V
- Output voltage range: 100 mV to 1.7 V
- Phase margin > 60° (Load capacitance = 5 pF)
- Slew rate > 2 V/μs (Load capacitance = 5 pF).

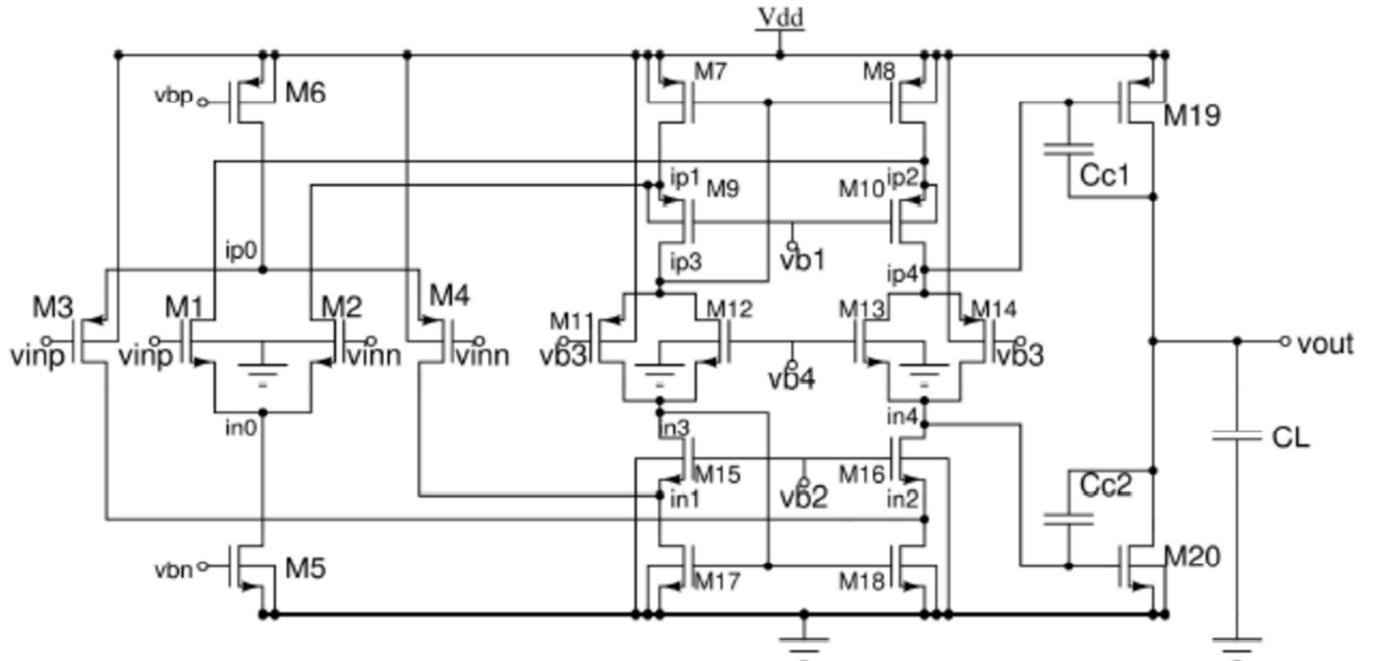
**Op-amp Architecture:**

Figure 1: Op-amp architecture.

## 1 OPAMP design flow

1.1, 1.2 Design flow of the op-amp in the form of step by step procedure which involves determining bias currents, voltages, and size of transistors to meet target specifications

CMOS Analog Design

Project :- Rail-to-Rail opamp.

Design Flow :-

Requirements :- gain of 2 stages  $> 100 \text{ dB}$ .  
We want to get around  $60 \text{ dB}$  gain from stage 1. and Rest from the class AB stage.

$V_{thn} = 0.399 \text{ V}$   
 $V_{thp} = 0.42 \text{ V}$  [given in the model file - PRM\_180nm]

Gain of stage 1 is given by  

$$|A_{v1} \approx g_{m1} / g_{m10} V_{o10} V_{o2}|$$

Assuming  $g_{m1} = 0.25 \text{ mS} = g_{m2} = g_{m3} = g_{m4}$   
 $I_{no} = I_{po} = 50 \mu\text{A}$   
 $I_{ps} = I_{p4} = 50 \mu\text{A}$ .

from  $g_{m1}$ , we can get ( $w/l$ ) of  $M_1, M_2, M_3, M_4$   
using formula  

$$|g_m = \sqrt{2 I_{ds} \mu n C_{ox} (w/l)}|$$

→ providing  $V_{dss} = V_{ds8} = 0.15 \text{ V}$  to the tail current sources.  
 $(M_5 \text{ and } M_6)$

→  $V_{dd} = 1.8 \text{ V}$  (given)

→ dividing  $V_{dd}$  among  $M_7, M_8, M_9, M_{10}, M_{11}, M_{12}, M_{13}, M_{14}, M_{15}, M_{16}, M_{17}$   
 $V_{ds}$  for  $M_7, M_8, M_{17}, M_{18}, M_{11}, M_{12}, M_{13}, M_{14} = 0.8 \text{ V}$   
 $V_{ds}$  for  $M_9, M_{10}, M_{15}, M_{16} = 0.4 \text{ V}$  (these may go in triode region first)

→ from  $V_{ds}$  and current in the transistor we can calculate the  $(W/L)$  of all transistors.

→ for finding bias voltages -

$$V_{b3} - V_{gsm11} - V_{gs17} - V_{dd} = 0$$

$$V_{b4} - V_{gsm14} - V_{gs17} = 0$$

$$-V_{b2} + V_{gs15} + V_{ds17} = 0$$

$$-V_{dd} + V_{sd17} + V_{sg15} + V_{b1} = 0$$

→  $r_o$  can be calculated using formula.

$$r_o = \frac{1}{250} \quad d_m = 0.05 \quad \left. \begin{array}{l} d_m = 0.05 \\ d_p = 0.1 \end{array} \right\} \text{given}$$

→ according to the above assumption,

Hand calculation gain is -

$$A_{v1} = 2380$$

$$\boxed{|A_{v1} \approx 67.5 \text{ dB}|}$$

→ with simulation

$$\boxed{\text{Stage 1 gain } |A_{v2} = 68.20 \text{ dB}|}$$

Iteration - 2 → for stage 1 to get gain  $\approx$  80dB.

→ providing  $v_{ds3} = v_{ds5} = 0.15V$

→ providing  $v_{dsq} = v_{ds15} = 0.2V$

→ providing  $v_{ds7} = v_{ds11} = v_{ds12} = v_{ds17} = 0.18V$

from  $v_{ds}$  and current in the Transistor, we get

(w/l) of all Transistor.

[gain of stage 1  $\approx$  80 dB.]

## Design flow of 2nd Stage (class AB Stage)

→ We get common output of 1st stage. Which is  $V_g$  of  $M_{19}$  and  $M_{20}$ .

→  $V_{gs}$  of  $M_{19}$  and  $M_{20}$  is calculated.

$$V_{gM_{19}} = 1.8 - 1.19V = 0.61V$$

$$V_{gM_{20}} = 0.625V \quad V_{gsM_{20}} = 0.625 - 0 \\ = 0.625V$$

→ Assume current in  $M_{19}$  &  $M_{20}$  ( $I_{oss}$ )

$$I_{oss} = I_{bias} \left( 1 + \frac{C_L}{C_E} \right)$$

$$\text{where } C_E = 0.65\text{ pF}$$

$$C_L = 5\text{ pF}$$

$$I_{bias} = 40\text{ mA}$$

$$I_{oss} = 40 \times 1.047 = 0.347 \text{ mA}$$

→ Calculate  $(w/l)_{19 \& 20}$  using formula.

$$(w/l) = \frac{\alpha I_D}{\mu_{n(on)} (V_{gsT})^2}$$

$$(w/l)_{19} = 26.2 \quad [1st \ iteration]$$

$$(w/l)_{20} = 40$$

→ Range  $C_C$  :-

$$\frac{q_{M1}}{C_C} > uGF$$

$$\frac{q_{M1}}{uGF} > C_C$$

$$C_C < \frac{0.364 \times 10^{-3}}{2\pi X} \doteq 2.34 \text{ pF}$$

$$C_C > \frac{g_{m1}}{g_{m1q}} \times C_L$$

$$C_C > \frac{0.369 \times 10^{-3}}{3.64 \times 10^{-3}} \times 5 \times 10^{-12}$$

$$C_C > 0.5 \text{ pF}$$

$$\boxed{0.5 \text{ pF} < C_C < 2.3 \text{ pF}}$$

→ Calculation of  $R_Z$ .

- first we get pole from the simulation.

$$\frac{g_{m2q}}{C_L} = 10.83 \text{ MHz.}$$

- for pole zero cancellation.

$$\text{Zero} = \text{pole.}$$

$$\frac{g_{m1q}}{2\pi C_C(1-g_{m1q}R_Z)} = 10.83 \text{ MHz.}$$

$$\boxed{R_Z = 24.7 \text{ K}}$$

→ With above  $R_Z$  p.i.m was not meeting specification.

→ so we used.

$$R_Z > \frac{1}{g_{m1q}} \left( 1 + \frac{C_L}{C_C} \right)$$

$$\boxed{R_Z > 2.387 \text{ K}}$$

$$C_2 < 2.03 \text{ pF}$$

for minimum value of  $C_2$ .

$$C_2 > \frac{g_{m1}}{g_{m10}} C_L$$

$$C_2 > \frac{12.83}{5.36} \times 0.5$$

$$\boxed{C_2 > 1.19 \text{ pF}}$$

Range of  $R_2$

$$\boxed{1.19 \text{ pF} < C_2 < 2.03 \text{ pF}}$$

Range of  $R_2$  :-

$$R_2 > \frac{1}{g_{m10}} \left( 1 + \frac{C_L}{C_2} \right)$$

$$R_2 > \frac{1}{5.36} \left( 1 + \frac{0.5}{1.2} \right)$$

$$\boxed{R_2 > 264.3 \text{ ohm}}$$

→ The value of  $R_2$  and  $C_2$  are adjusted to get the desired specification of phase margin and unity gain frequency.

Gain of 1st stage from iteration 1- Gian = 68.8db

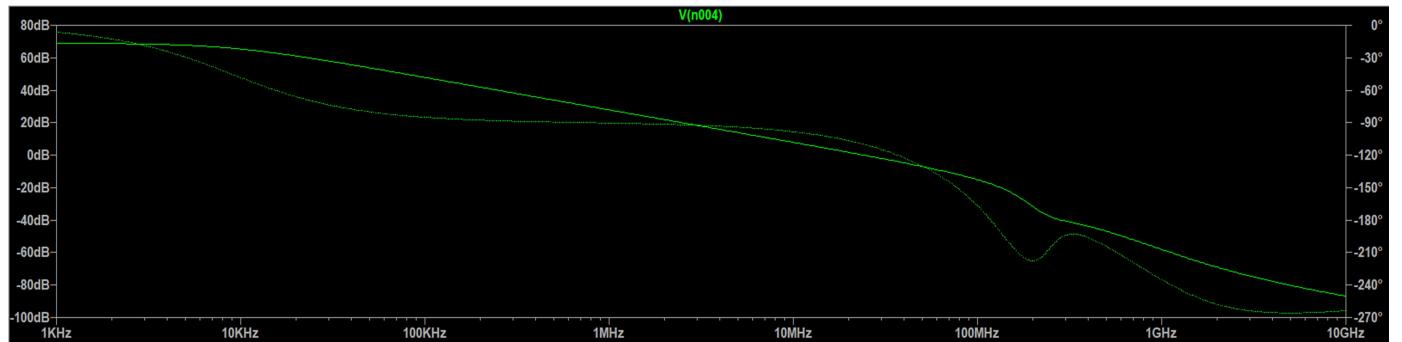


Figure 2: Gain of 1st stage from iteration 1- Gian = 68.8db

Gain of 1st stage from iteration 2- Gain=77.7db

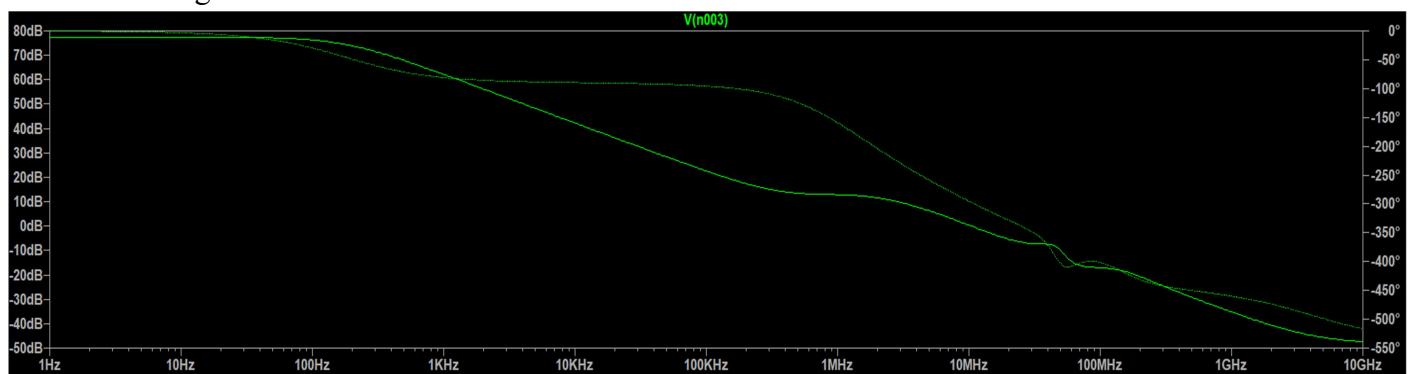


Figure 3: Gain of 1st stage from iteration 2- Gain=77.7db.

### 1.3, 1.4 Table for size of transistors of op-amp architecture

#### Stage 1

Transistor	W/L(um/um)	Drain Current(uA)
M1-M2	27/1	<b>24.6</b>
M3-M4	72.8/1	19.4
M5	20/1	49.1
M6	110/1	38.8
M7-M8	36/1	24.9
M9-M10	15/1	0.32
M11-M14	9/1	0.16
M12-M13	2/1	0.15
M15-M16	3.5/1	0.32
M17-M18	4.1	19.7
M19	65/0.25	348
M20	28.7/0.25	348

## Components Value

Component	Value
CL	5pF
Cz	0.65pF
RZ	10.5kohm

## Table of Bias Voltages

Bias voltage	Value (Volt)
Vb1	1
Vb2	0.78
Vb3	0.6
Vb4	1.16
Vbn	0.55
Vbp	1.23

## 2. Reference Generator Circuit Design

**2.1** Reference current source for ( $I_{ref} = 50 \mu A$ ), and current mirrors that you use to generate bias voltages for main class AB amplifiers as well as auxiliary circuit.

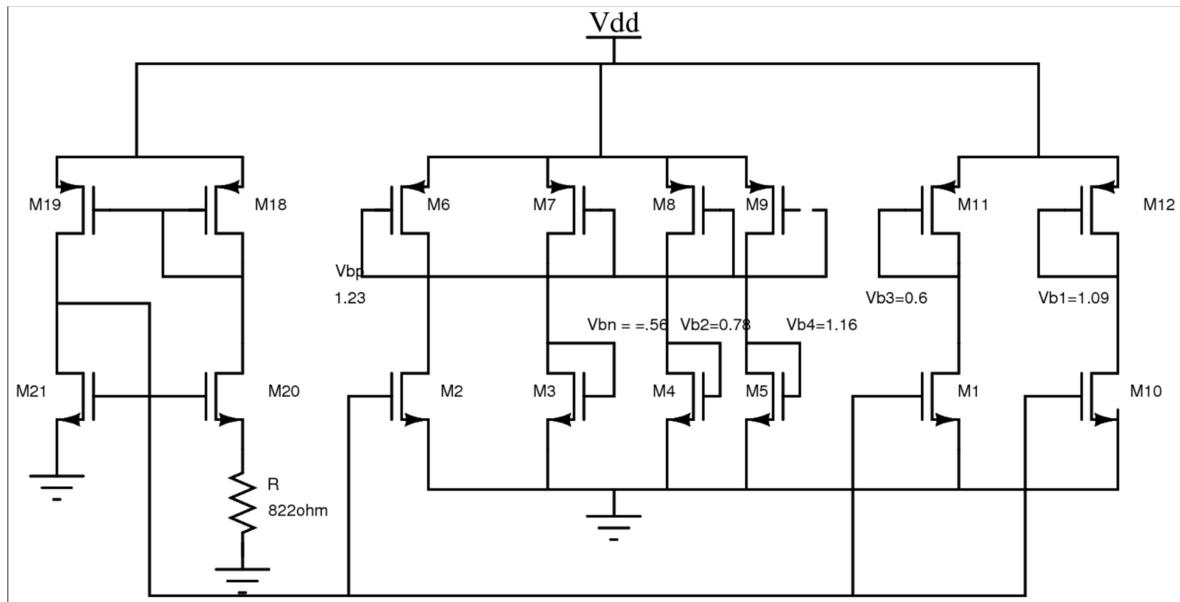


Figure 4: Reference generator circuit for generating bias voltages.

- Current Reference Generator Circuit Design (50uA)

Transistor	W/L(um/um)	Drain Current(uA)
M21	400/1	50
M20	850/1	50
M19-M18	400/1	50

Component	Value
Rs	822ohm

Table for transistor size of voltage generator

Voltage	Transistor	W/L(um/um)
Vb1	M1	400/1
	M11	2.32/1
Vb2	M10	101/1
	M12	10/1
Vb3	M4	23.4/1
	M8	120/1
Vb4	M5	5/1
	M9	91.8/1
Vbn	M3	55.5/1
	M7	50/1
Vbp	M2	37.3/1
	M6	2/1

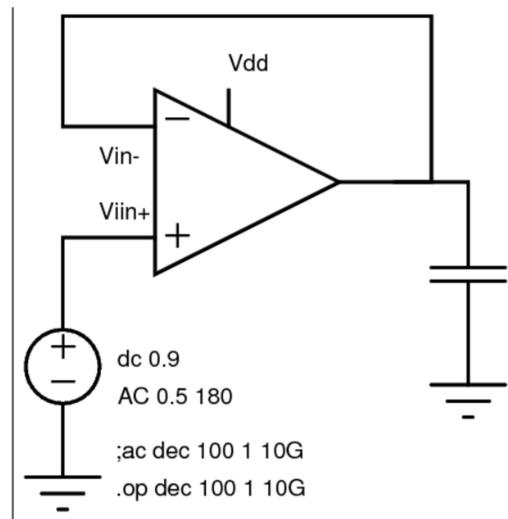
## Design Procedure:

1. A reference current of 50u Amp is chosen.
2. Taking a start value for W/L for M1.
3. Using the property of the current mirror that it replicates i.e  $\frac{Id_2}{Id_1} = \frac{(W/L)_2}{(W/L)_1}$  ignoring lambda so W/L for M1 will be approximately the same as W/L.
4. Using the mobility ratio of the n and pmos transistor we find the W/L for pmos (nmos mobility can be considered twice that of pmos).
5. In the same way W/L for M4 and M5 are taken.
6. We then check the voltage at node and according to the required bias voltage we adjust Width of n and pmos transistors.
7. If the Voltage generated is more than required voltage then we make the nmos transistor stronger by increasing its width.
8. If the voltage generated is less than the required voltage then we make the pmos transistor stronger by increasing the width

“ Current source generation circuit used is also called the constant gm circuit. The idea of a constant transconductance circuit is to generate bias current( $I_{ref}$ ) which is a function of resistor and inversely proportional to  $unCox(W/L)$  . If we pass this current into a transistor whose gm is  $\sqrt{2 * unCox(W/L) * I_{ref}}$  the only variable left is a resistor with some constant.  $I_{ref} = 2 / (unCox(W/L)n) * 1 / (Rs^2) * (1 - 1/\sqrt{K})^2$  “

### 3. DC Operating point simulations

**3.1** Connect the Op-amp in closed loop mode with voltage gain of +1 and apply DC common mode voltage (VCM) at positive terminal of Op-amp.



*Figure 5:Op-amp in closed loop mode with voltage gain of 1.*

### 3.2 Run DC simulations on Op-amp including reference generator and DC operating points.

Semiconductor Device Operating Points:									
--- BSIM3 MOSFETs ---									
Name:	Name:	m:x1:9	m:x1:7	m:x1:8	m:x1:10	m:x1:11			
Name:	m:x1:12	m:x1:17	m:x1:15	m:x1:16	m:x1:18				
Mode:	x1:nmos	x1:nmos	x1:nmos	x1:nmos	x1:nmos	3.21e-07	2.49e-05	2.49e-05	3.21e-07
Id:	1.55e-07	1.97e-05	3.21e-07	3.21e-07	1.97e-05	-8.27e-02	-3.50e-01	-3.50e-01	-8.32e-02
Vgs:	Vgs:	5.38e-01	6.25e-01	4.66e-01	4.66e-01	6.25e-01	3.50e-01	2.70e-01	2.70e-01
Vds:	Vds:	5.56e-01	3.14e-01	3.11e-01	3.11e-01	3.14e-01	3.50e-01	2.70e-01	2.70e-01
Vth:	Vth:	-6.25e-01	0.00e+00	-3.14e-01	-3.14e-01	0.00e+00	-4.46e-01	-4.46e-01	-4.46e-01
Vdsat:	Vdsat:	6.12e-01	4.46e-01	5.35e-01	5.35e-01	4.46e-01	-4.22e-02	-1.30e-01	-1.30e-01
Gm:	Gm:	4.91e-02	1.74e-01	4.97e-02	4.97e-02	1.74e-01	7.64e-06	2.96e-04	2.96e-04
Gds:	Gds:	3.59e-06	1.77e-04	7.30e-06	7.30e-06	1.77e-04	5.36e-08	4.82e-06	4.82e-06
Gcb:	Gcb:	2.06e-08	2.89e-06	4.84e-08	4.83e-08	2.89e-06	2.16e-06	8.03e-05	8.03e-05
Gmb:	Gmb:	8.86e-07	5.62e-05	1.99e-06	1.99e-06	5.62e-05	5.17e-14	1.23e-13	1.23e-13
Cbd:	Cbd:	4.56e-15	1.10e-14	8.66e-15	8.66e-15	1.10e-14	4.38e-14	9.29e-08	9.29e-08
Cbs:	Cbs:	5.15e-15	1.24e-14	9.49e-15	9.49e-15	1.24e-14	v:	8.12e-15	1.96e-14
Cgso:	Cgso:	1.09e-15	2.24e-15	1.91e-15	1.91e-15	2.24e-15	v:	8.16e-15	1.96e-14
Cgdo:	Cgdo:	1.08e-15	2.23e-15	1.90e-15	1.90e-15	2.23e-15	v:	0.00e+00	0.00e+00
Cgb:	Cgb:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	Vgb:	7.11e-14	2.70e-13
dQgdVgb:	dQgdVgb:	5.92e-15	3.05e-14	1.12e-14	1.12e-14	3.05e-14	Vdb:	-8.17e-15	-2.08e-14
dQgdVdb:	dQgdVdb:	-1.08e-15	-2.36e-15	-1.90e-15	-1.90e-15	-2.36e-15	Vsb:	-4.42e-14	-2.36e-13
dQgdVdv:	dQgdVdv:	-1.99e-15	-2.63e-14	-3.88e-15	-3.88e-15	-2.63e-14	Vgb:	-8.30e-15	-2.34e-14
dQddVgb:	dQddVgb:	-1.08e-15	-2.62e-15	-1.91e-15	-1.91e-15	-2.62e-15	Vdb:	5.99e-14	1.46e-13
dQddVdb:	dQddVdb:	5.63e-15	1.36e-14	1.06e-14	1.06e-14	1.36e-14	Vsb:	1.49e-16	1.47e-15
dQdbVsb:	dQdbVsb:	1.64e-18	1.95e-16	1.02e-17	1.02e-17	1.95e-16	Vgb:	-2.41e-14	-4.56e-14
dQdbVdb:	dQdbVdb:	-2.93e-15	-4.27e-15	-5.60e-15	-5.60e-15	-4.27e-15	Vdb:	-5.17e-14	-1.24e-13
dQdbVdv:	dQdbVdv:	-4.56e-15	-1.11e-14	-8.66e-15	-8.66e-15	-1.11e-14	Vsb:	-4.78e-14	-9.29e-08
dQdbVsb:	dQdbVsb:	-5.27e-15	-1.65e-14	-9.79e-15	-9.79e-15	-1.65e-14		-1.29e-13	-4.78e-14
Name:	Name:	m:x1:5	m:x1:2	m:x1:1	:	m:x1:6	m:x1:4	m:x1:20	m:x1:13
Mode:	Model:	x1:nmos	x1:nmos	x1:nmos	l:	x1:pmos	x1:pmos	x1:nmos	x1:nmos
Vgs:	Id:	4.91e-05	2.46e-05	2.46e-05	1:	3.88e-05	1.94e-05	1.94e-05	3.48e-04
Vds:	Vgs:	5.61e-01	5.78e-01	5.78e-01	2:	-2.88e-01	5.86e-01	5.86e-01	6.26e-01
Vth:	Vth:	0.00e+00	-3.22e-01	-3.22e-01	2:	2.82e-01	1.20e+00	1.20e+00	9.00e-01
Vdsat:	Vdsat:	4.46e-01	5.37e-01	5.37e-01	2:	2.82e-01	1.49e+00	1.49e+00	0.00e+00
Gm:	Gm:	1.30e-01	8.76e-02	8.76e-02	t:	-4.46e-01	-5.23e-01	5.23e-01	6.12e-01
Gds:	Gds:	5.94e-04	4.08e-04	4.08e-04	t:	-9.80e-02	-8.62e-02	-8.62e-02	1.19e-01
Gmb:	Gmb:	6.61e-06	2.74e-06	2.74e-06	t:	6.04e-04	3.43e-04	3.43e-04	4.14e-03
Cbd:	Cbd:	1.86e-04	1.12e-04	1.12e-04	t:	6.78e-06	2.54e-06	2.54e-06	1.44e-04
Cbs:	Cbs:	5.16e-14	5.27e-14	5.27e-14	t:	1.64e-04	8.43e-05	8.43e-05	1.04e-03
Cgso:	Cgso:	5.84e-14	6.95e-14	6.95e-14	t:	3.72e-13	2.15e-13	2.15e-13	8.71e-07
Cgdo:	Cgdo:	1.09e-14	1.47e-14	1.47e-14	t:	3.25e-13	1.52e-13	1.52e-13	7.24e-14
Cgb:	Cgb:	1.09e-14	1.36e-14	1.36e-14	t:				5.15e-15

#### 4. AC simulations

4.1 Plot of open loop fully differential voltage gain (in dB) and phase (in degrees) as a function of frequency (Bode plot).

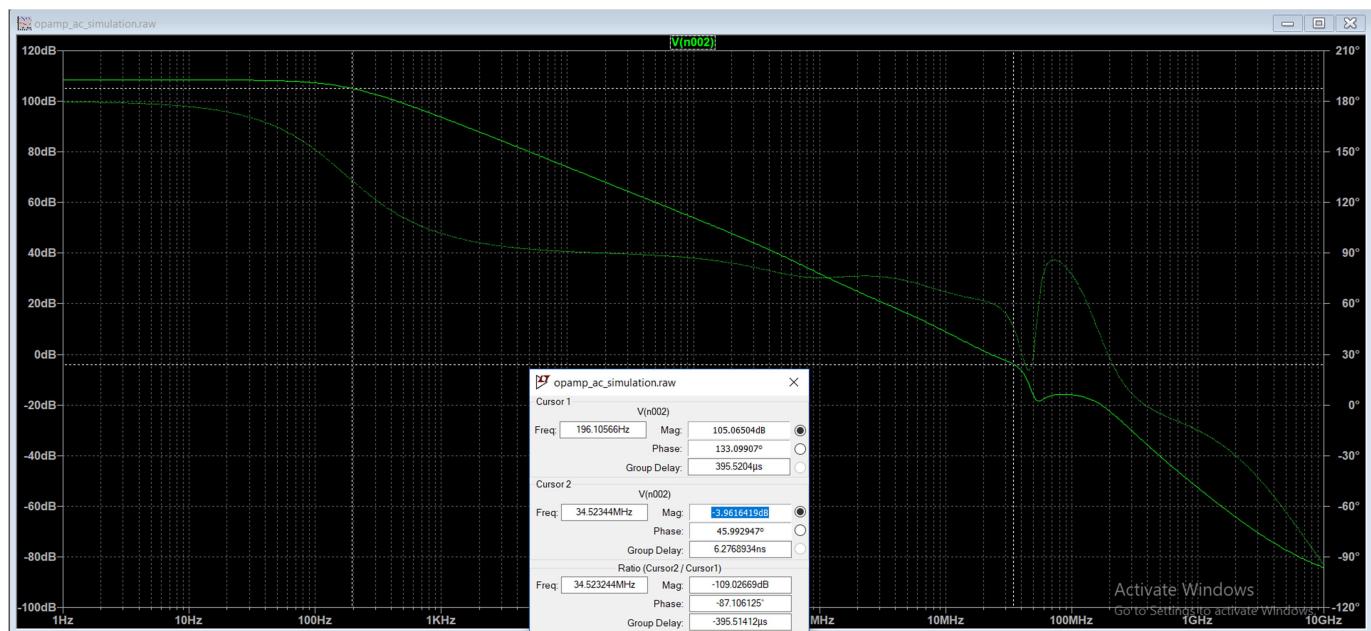
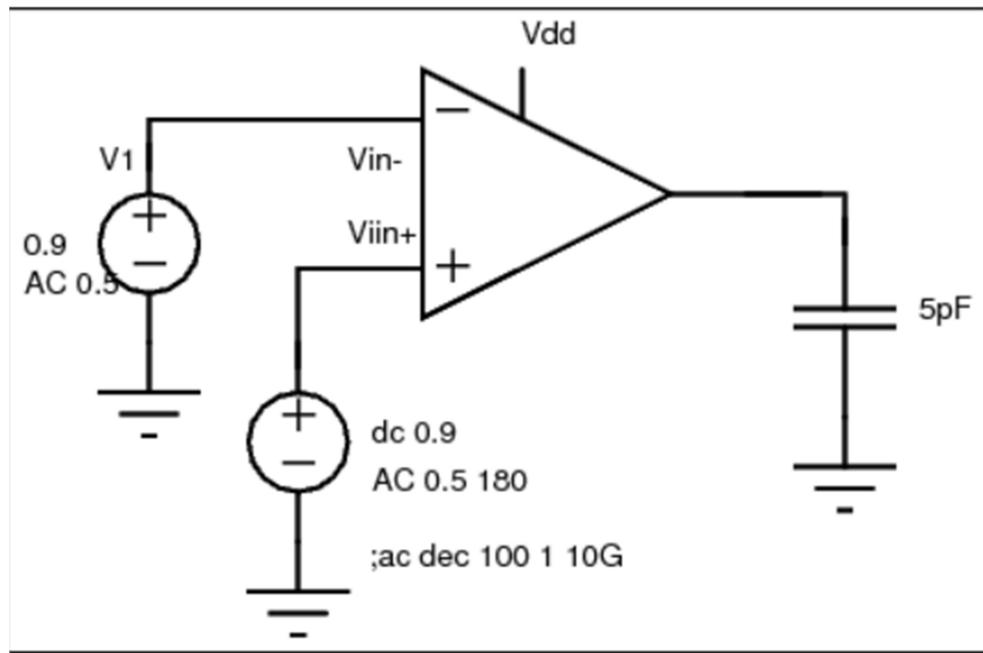


Figure 6.4.1 Plot of open loop fully differential voltage gain (in dB) and phase (in degrees).

### Table for specification:

<b>Gain (in dB)</b>	108.46 dB
<b>Phase Margin</b>	60.5 degree
<b>UGB</b>	22.77 MHz
<b>P1</b>	196 Hz
<b>P2</b>	34.5 MHz
<b>Z1</b>	32.12 MHz
<b>Roll off @1octave above UGB</b>	-12dB/Octave

## 5. Slew rate simulation

**5.1** Connect the Op-amp in closed loop mode with voltage gain of -1. (Use common mode voltage 0.9 V).

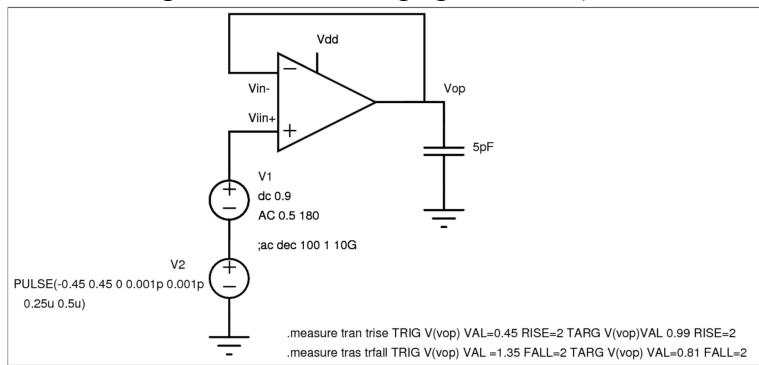


Figure 7:the Op-amp in closed loop mode with voltage gain of 1.

## 5.2 Simulate step response to +450 mV and -450 mV differential input step voltage and calculate slew rate

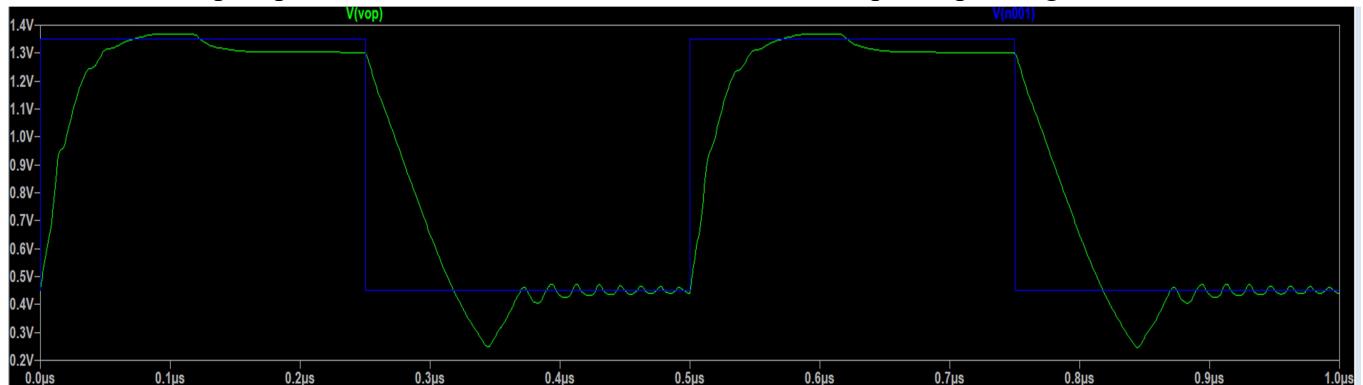


Figure 8:step response to +450 mV and -450 mV differential input step voltage.

```

Python 3.7.2 Shell
File Edit Shell Debug Options Window Help
Python 3.7.2 (tags/v3.7.2:9a3ffc0492, Dec 23 2018, 22:20:52) [MSC v.1916 32 bit
(Intel)] on win32
Type "help", "copyright", "credits" or "license()" for more information.
>>>
==> RESTART: E:\IIT Bombay\M.Tech Sem 1\Analog IC\Project\Slew_calc_sr.py ===
3.4385865610091377
>>>
==> RESTART: E:\IIT Bombay\M.Tech Sem 1\Analog IC\Project\Slew_calc_sr.py ===
3.4385865610091377V/us
>>>

```

```

Slew_calc_sr.py - E:\IIT Bombay\M.Tech Sem 1\Analog IC\Project\Slew_calc_sr.py (3.7.2)
File Edit Format Run Options Window Help
trise = 0.149
tfall = 0.166
sr_n = (0.54)/(tfall)
sr_p =(0.54)/(trise)
sr_avg = (sr_n +sr_p)/2
print (str(sr_avg)+"V/us")

```

Figure 9: Calculated Slew rate for the op-amp architecture.

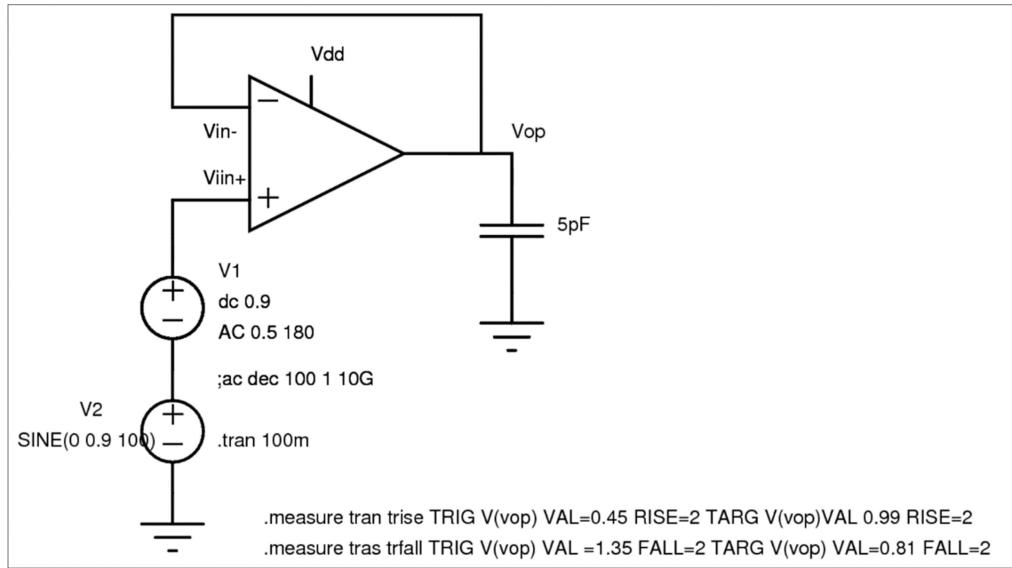
**Observation:** The Op-amp is designed for a slew rate of greater than 2 V/ $\mu$ -sec, and For the Op-amp connected in closed loop with a gain of +1, provides a slew rate of 3.43 V/ $\mu$ -sec as shown in Figure 9.

- The input applied to the circuit is  $V_{in} = 0.9 \text{ V} \pm 450 \text{ mV} \rightarrow V_{in-\text{max}} = 1.35 \text{ V}$  and  $V_{in-\text{min}} = 0.45 \text{ V}$ .
- For  $V_{in-\text{max}}$  transistor M2 will be on and M1 will be turned off and vice versa for  $V_{in-\text{min}}$ , this causes the entire  $I_{bias}$  current to flow through only one input transistor. So, the total current flowing through the capacitor CC will be  $I_{bias}$  which leads to rate of change of voltage across capacitor CC by  $I_{bias}/CC$  which results in a slope for the output waveform as shown in Figure 14 and Figure 15, this slope defines the slew rate of the Op-amp.

Slew Rate +ve	3.6241
Slew Rate -ve	3.253
Slew Rate Average	3.4385

## 6. Transient Simulation

**6.1** Connect the Op-amp in closed loop mode with voltage gain of 1. (Use common mode voltage 0.9 V).



*Figure 10 Circuit Setup for Transient Simulation*

## 6.2 Run transient simulation for maximum output voltage swing.

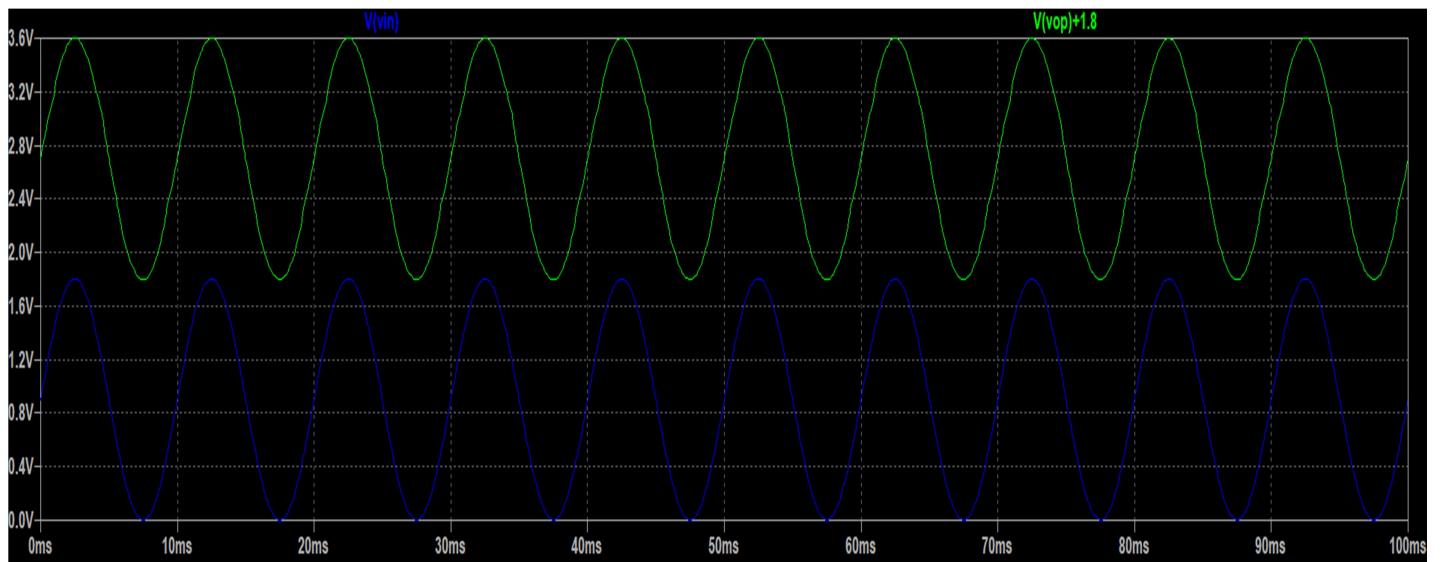


Figure 11. Transient Simulation Output,  $V_{in}$ (Blue),  $V_{out}+1.8V$ (green)

## 7. Common-mode (CM) DC Simulation

**7.1** Connect the Op-amp in closed loop mode with voltage gain of +1.

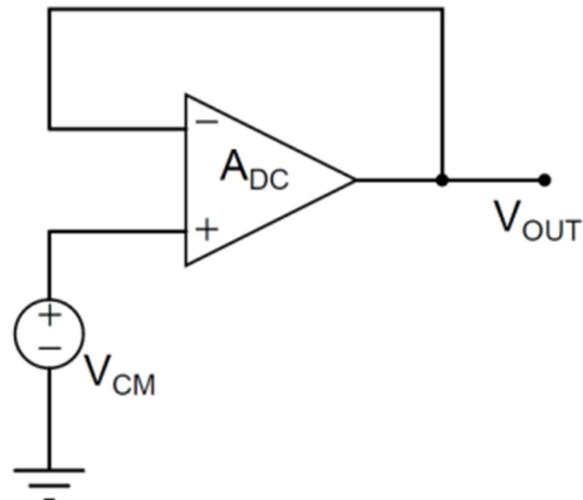


Figure 12 Circuit Setup for CM Analysis

**7.2** Sweep the common-mode DC input voltage from  $V_{CM}$  min to  $V_{CM}$  max (total range better than 50% of the VDD). Plot output CM DC voltage as a function of input CM DC voltage.



Figure 13  $V_{out\_CM}$  v/s  $V_{in\_CM}$

**7.3** Calculate the non-linearity of Op-amp by marking the values of slope at  $V_{CM} = 100 \text{ mV}$ ,  $0.9 \text{ V}$  and  $1.6 \text{ V}$ .

**Slope at given points:**

V_CM Voltage	Slope
0.1 V	0.999986
0.9 V	0.999997
1.6 V	0.999980

Slope at all specified points is approximately equal to 1, which implies that the op-amp behaves as a linear circuit in rail-to-rail input common mode voltage. This linear behavior is due to the presence of complementary combination of NMOS and PMOS differential input pair.

**7.4** Report the maximum and minimum values of the slope calculated in 7.3 part.

- Maximum slope = 0.999997
- Minimum slope = 0.999980