Team – MazeProcessor
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PROGRESS REPORT

Introduction:

For our MP3, we will design a 5-staged pipeline processor that supports the LC3-b Instruction Set Architecture. The processor will have a cache hierarchy consisting of a split L1 cache and a unified L2 cache. It will also include data forwarding and hazard detection for proper functionality. Lastly, we will also implement advanced features to improve the performance of our processor further like static branch prediction, evict write buffer, software visible performance counters and 4-way set associative L2 cache.

Completed Work:

Checkpoint0: We completed the paper design for the complete datapath of our pipelined processor. We included all components and modules required for the complete ISA support and discussed our datapath with our mentor TA. We also started thinking about what advanced features we would like to add to our processor and if we need to modify our datapath accordingly.

Checkpoint1: On the basis of the designed datapath, we implemented the SystemVerilog code for our processor. We were supposed to support the LC3-bα ISA, but we also wrote code for all instructions except STI and LDI. We tested the provided test code as well as our own test cases, and they worked as expected. We also discussed and designed the cache hierarchy for the processor and how it works with the shared wishbone even though the L1 cache has separate wishbone master ports. We decided to implement the 4-way set associative L2 cache with LRU policy.

Checkpoint2: We completed the coding for supporting the full LC3-b ISA, while also implementing the instruction cache as well as cache hierarchy with a functional 2-way set associative cache. We modified our datapath design to support data-forwarding and hazard detection. We also completed our planning for the implementation of the L2 cache as well as made progress on our advanced design features discussion.

Checkpoint3: We completely integrated our two-level cache hierarchy to the pipelined CPU along with implementing structural, control and data hazard detections to ensure proper functioning of our processor. We also implemented static branch prediction in this checkpoint itself. Out L2 cache is 4-way set associative with a pseudo-LRU.

Checkpoint4: We completed our implementation of the eviction write buffer (4-way, fully associative) as well as the performance counters to keep track of branches, memory hits and pipeline stalls. We also finished implementing some advanced features like a 4-way BTB, local branch history table, a global history table as well as a tournament predictor.

Road Map:

Checkpoint5: We have implemented most of the advanced features required. We will attempt to increase our performance further by increasing our frequency by shortening our critical path as well as attempt to do an early branch resolution in the EX stage.