Team – MazeProcessor
Arnav Agarwal, agarwl13
Shivam Bharuka, bharuka2
Arvind Arunasalam, arunasa2

PROGRESS REPORT

Introduction:

For our MP3, we will design a 5-staged pipeline processor that supports the LC3-b Instruction Set Architecture. The processor will have a cache hierarchy consisting of a split L1 cache and a unified L2 cache. It will also include data forwarding and hazard detection for proper functionality. Lastly, we will also implement advanced features to improve the performance of our processor further like static branch prediction, evict write buffer, software visible performance counters and 4-way set associative L2 cache.

Completed Work:

Checkpoint0: We completed the paper design for the complete datapath of our pipelined processor. We included all components and modules required for the complete ISA support and discussed our datapath with our mentor TA. We also started thinking about what advanced features we would like to add to our processor and if we need to modify our datapath accordingly.

Checkpoint1: On the basis of the designed datapath, we implemented the SystemVerilog code for our processor. We were supposed to support the LC3-bα ISA, but we also wrote code for all instructions except STI and LDI. We tested the provided test code as well as our own test cases, and they worked as expected. We also discussed and designed the cache hierarchy for the processor and how it works with the shared wishbone even though the L1 cache has separate wishbone master ports. We decided to implement the 4-way set associative L2 cache with LRU policy.

Checkpoint2: We completed the coding for supporting the full LC3-b ISA, while also implementing the instruction cache as well as cache hierarchy with a functional 2-way set associative cache. We modified our datapath design to support data-forwarding and hazard detection. We also completed our planning for the implementation of the L2 cache as well as made progress on our advanced design features discussion.

Road Map:

Checkpoint3: We plan on modifying our coded datapath for functioning hazard detection and data forwarding as well as ensuring a completely integrated cache hierarchy including the unified L2 cache. Also, we plan on starting on our required advanced design features and modifying our paper design according to the our finally decided optional advanced features.

Checkpoint4: We plan on completing our required advanced design options as well as a couple of the optional ones to ensure enough time to completely test our design and performance.

Checkpoint5: We plan on having our final processor design complete and fully functional after including all advanced features to be able to compete in the competition.