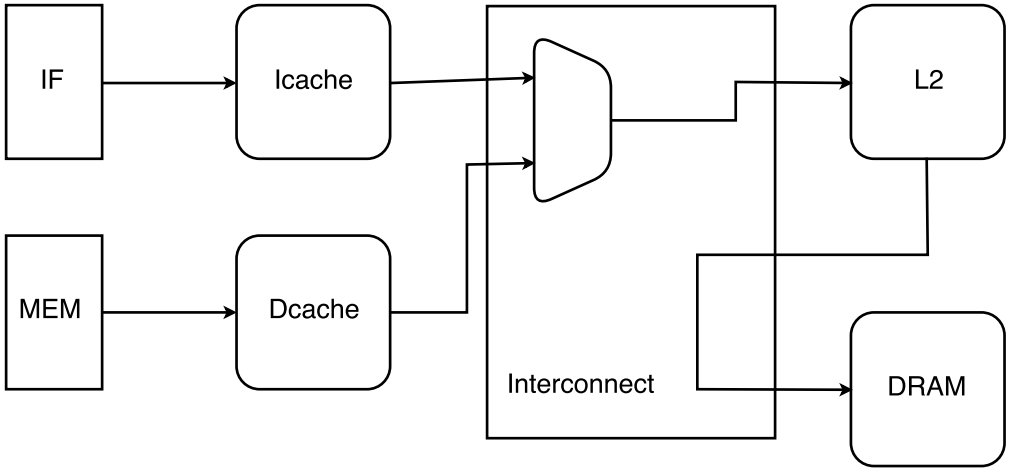

Cache Hierarchy

The interconnect receives the master inputs from Icache, Dcache and the L2 while it connects to the slave ports of L2 and DRAM. The interconnect looks at the CYC, STB and WE signals from the Icache and Dcache to determine which one is connected to the L2 cache slave port first. If only one of them is attempting a read or a write, that cache's master port is connected to L2 cache slave port. If both of them are attempting a read or a write, Icache is given preference. The L2 master port is always directly connected to the DRAM slave port.