ECE111|Digital Circuits
Dr. Vish Visweswaran
Lab_5:
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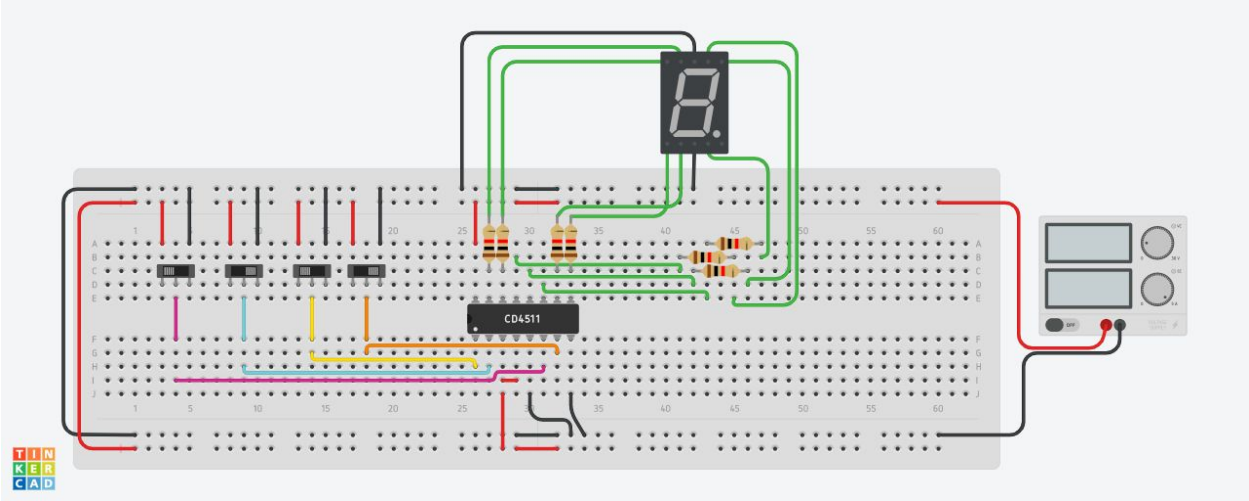
Roll No. : 2020123
Date : 07/3/2021

Aim 1 : Implement a 7 segment decoder using CD 4511 IC

Components / ICs used : 1 power supply , 4 slide switches , 1 7-Segment Decoder , 1 Cathode 7-Segment Display , 7 1kohm resistors

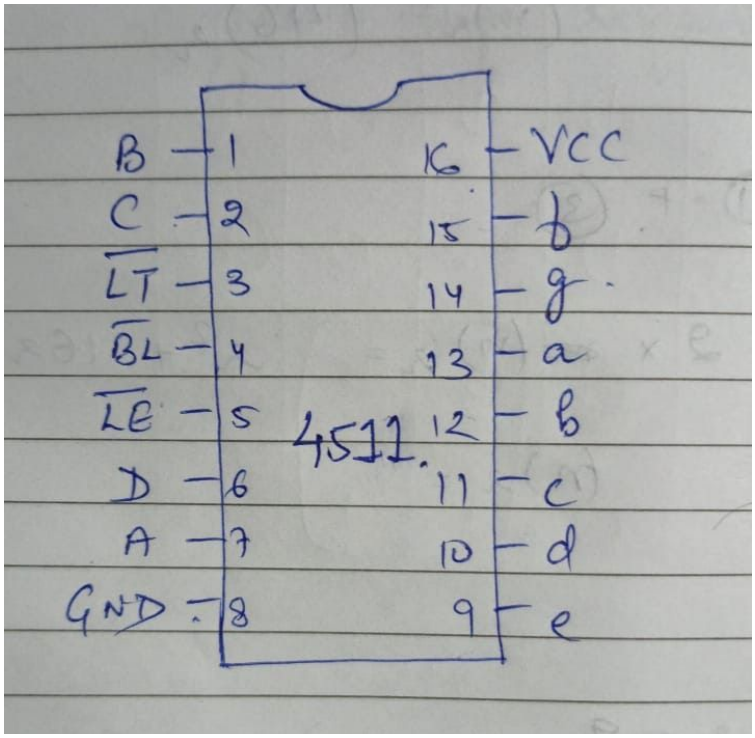
Circuit Diagram :



Link of Tinkercad workspace :

https://www.tinkercad.com/things/k45AkXYK62F-7-segment-display/editel?sharecode=StUUVZafPzcsKaoZ-3_-e_pY52O1MAJ_64170ajtwDQ

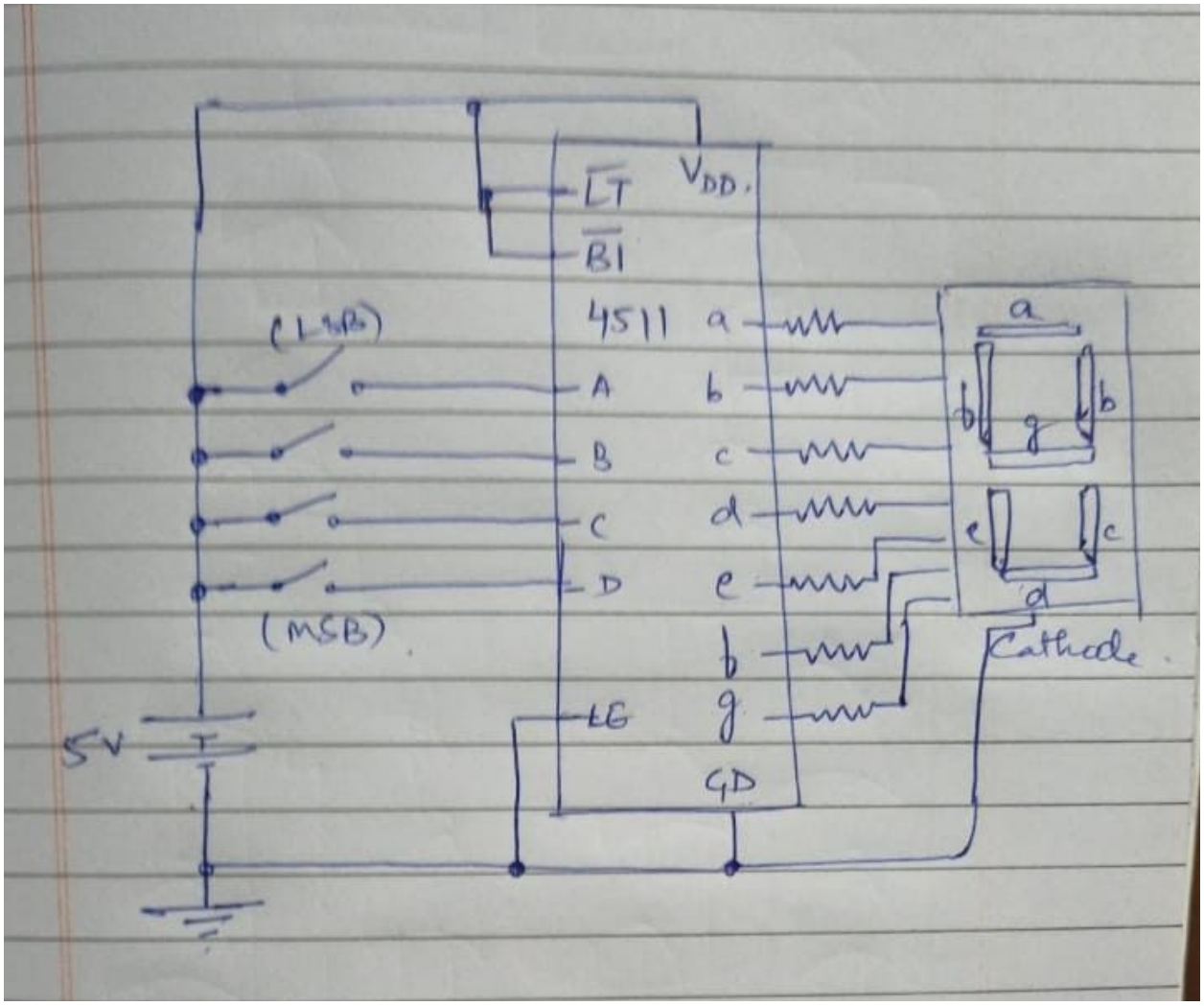
IC - CD4511



Truth Table :

DE	D	C	B	A	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	0	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1

Logic Circuit Diagram :



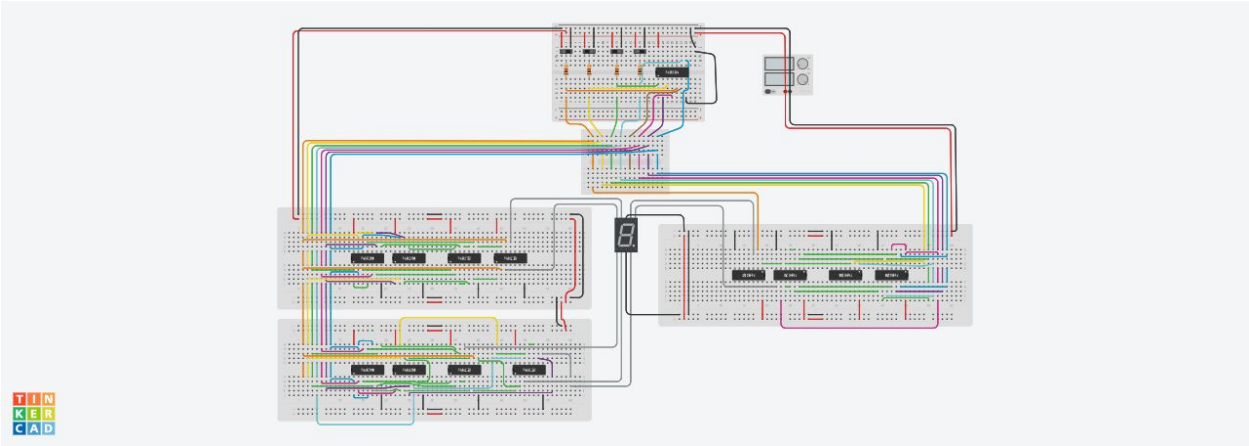
Observations :

The 7 segment display displays the decimal equivalent of the input DCBA which is in the form of BCD(Binary Coded Decimal)

Aim 1 : Implement a 7 segment decoder by only using basic gates

Components / ICs used : 1 power supply , 4 slide switches , 1hex inverter , 1 Cathode 7-Segment Display , 4 1kohm resistors, 6 Quad and gate , 6 Quad or gate

Circuit Diagram :

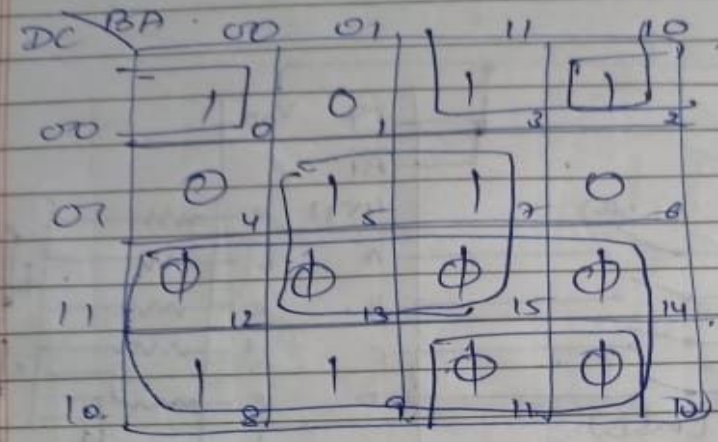


Link of Tinkercad workspace :

https://www.tinkercad.com/things/0fbMpDMM4Hk-copy-of-7-segment-display-using-basic-gates/editel?sharecode=bvCDWbC7m2I6mlkypnQW3X_t9El5AGLmyJj01OHVaKs

K maps :

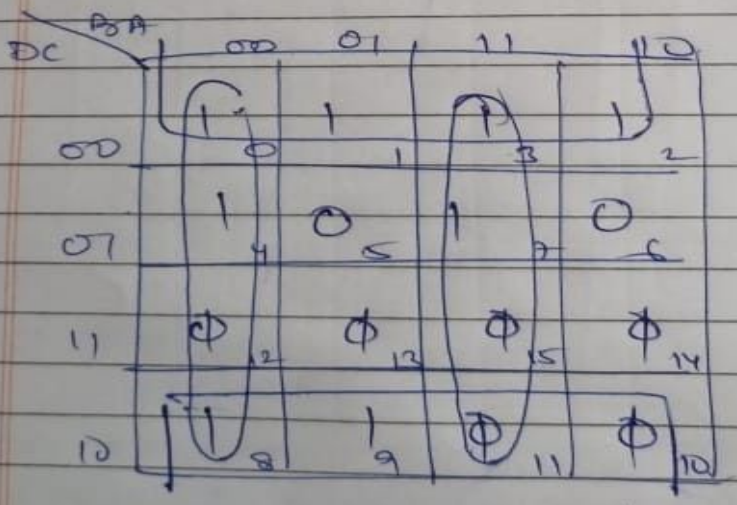
KMap for a.



$a = D + \bar{C}B + AC + \bar{D}\bar{C}\bar{A}$

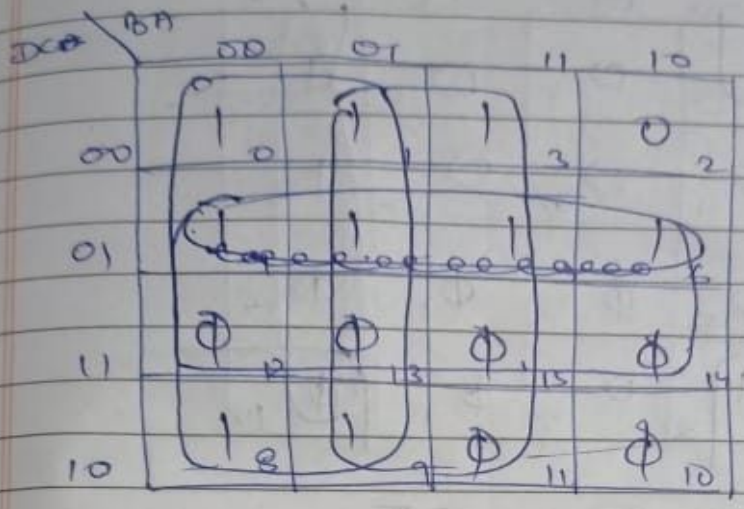
$= D + B\bar{C} + AC + \bar{C}\bar{A}$.

KMap for b.



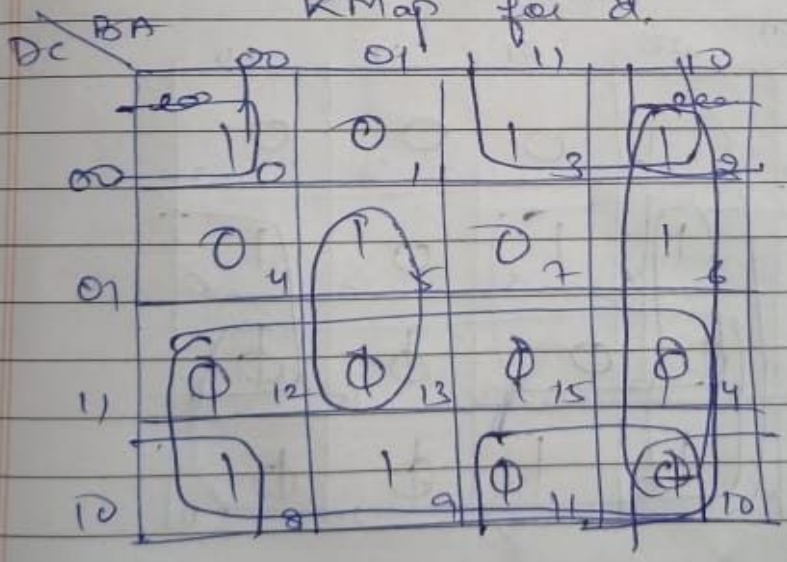
$b = \bar{C} + \bar{A}B + A\bar{B}$

KMap for c



$c = \bar{B} + A + C$.

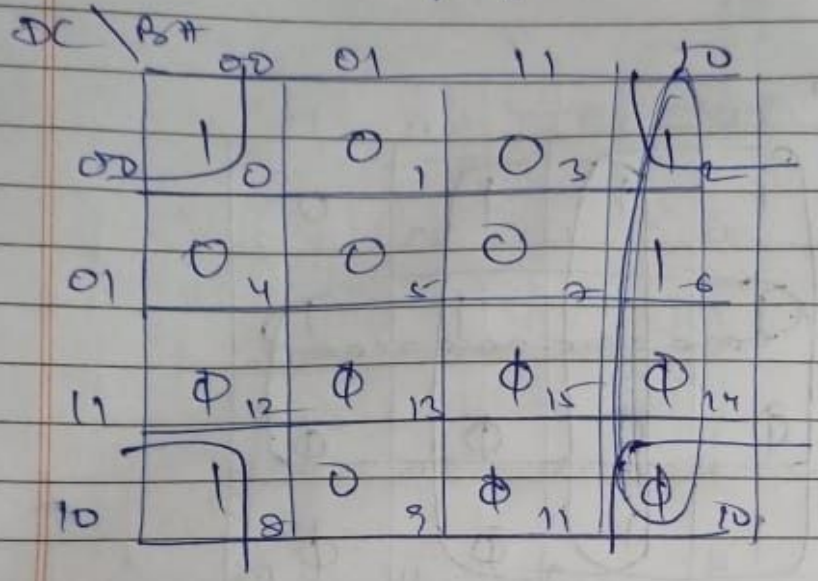
KMap for d.



$d = D + B\bar{A} + \bar{C}.B + \bar{B}\bar{C}.\bar{A} + C.\bar{B}A.$

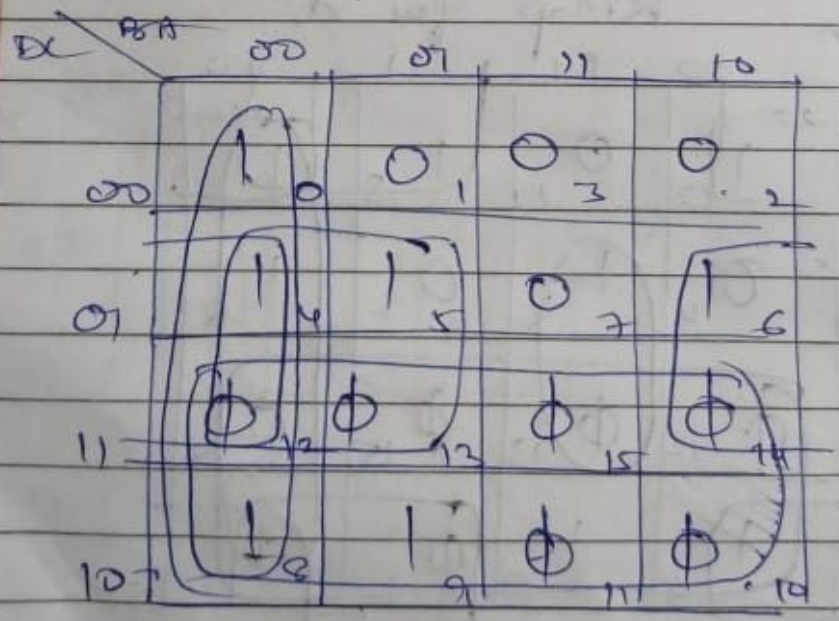
$= D + B\bar{A} + \bar{C}B + \bar{C}\bar{A} + A\bar{B}C.$

Kmap for e :



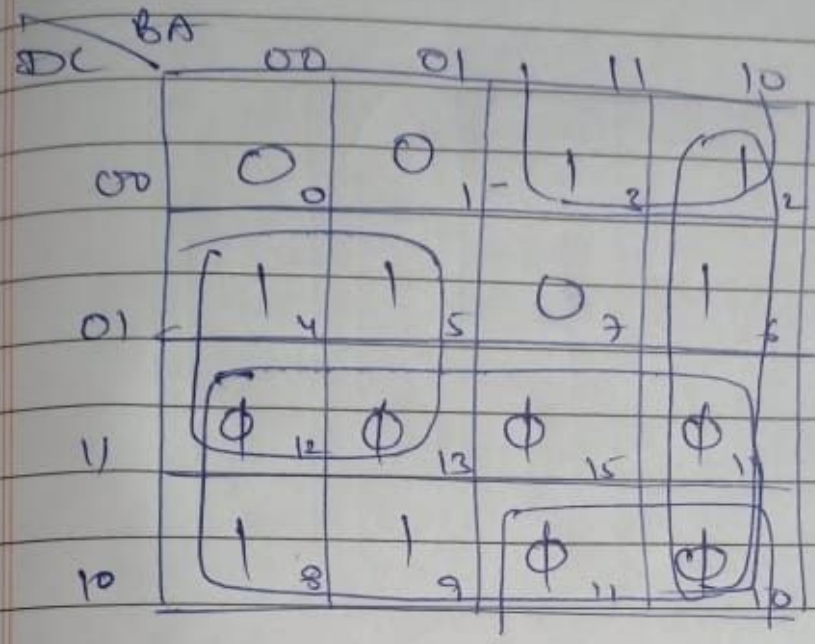
$\bar{e} = \bar{A}B + \bar{A}\bar{C}$

Kmap for f :



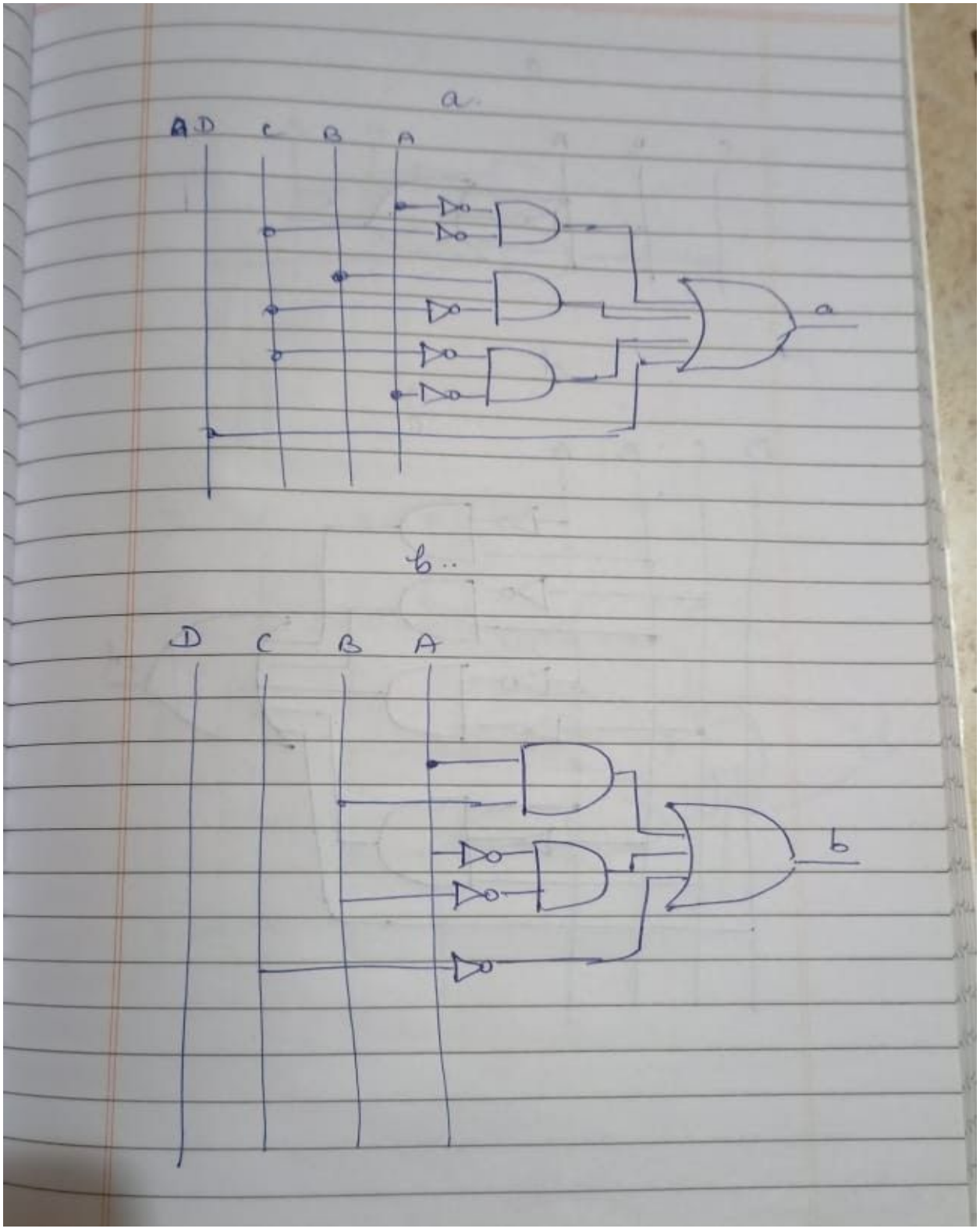
$f = D + C\bar{A} + C\bar{B} + \bar{A}\bar{B}$

Kmap for g.

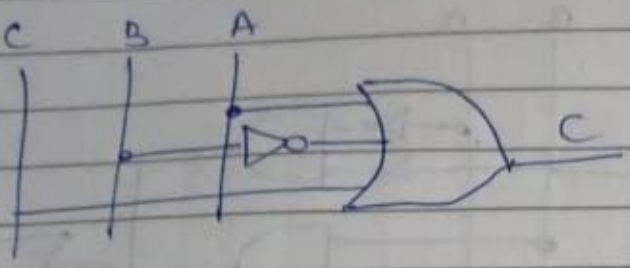


$g = D + C\cdot\overline{B} + \overline{C}\cdot B + \overline{A}B$

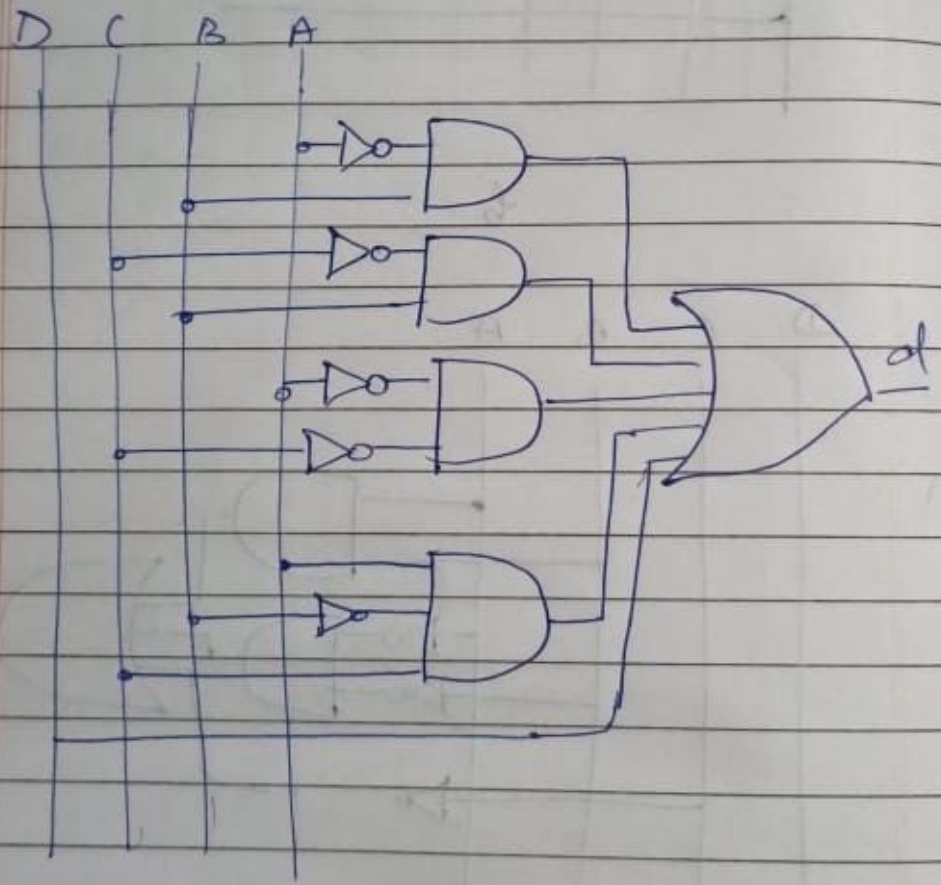
Logic Circuit Diagrams :



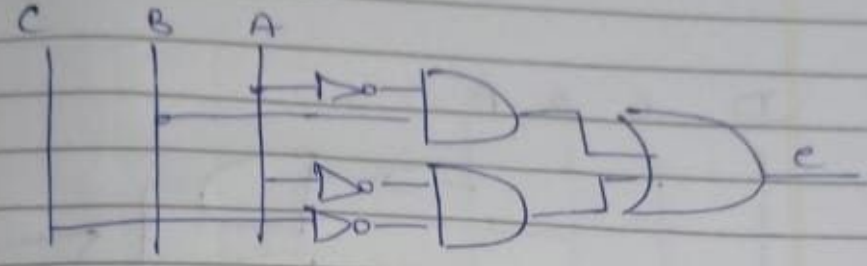
c



d.

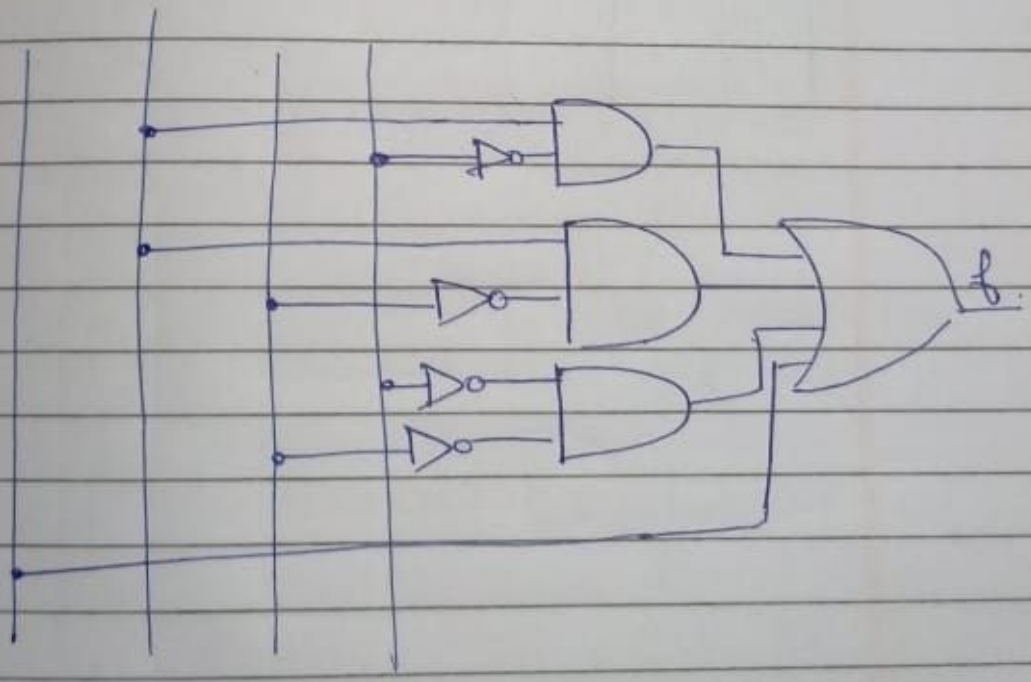


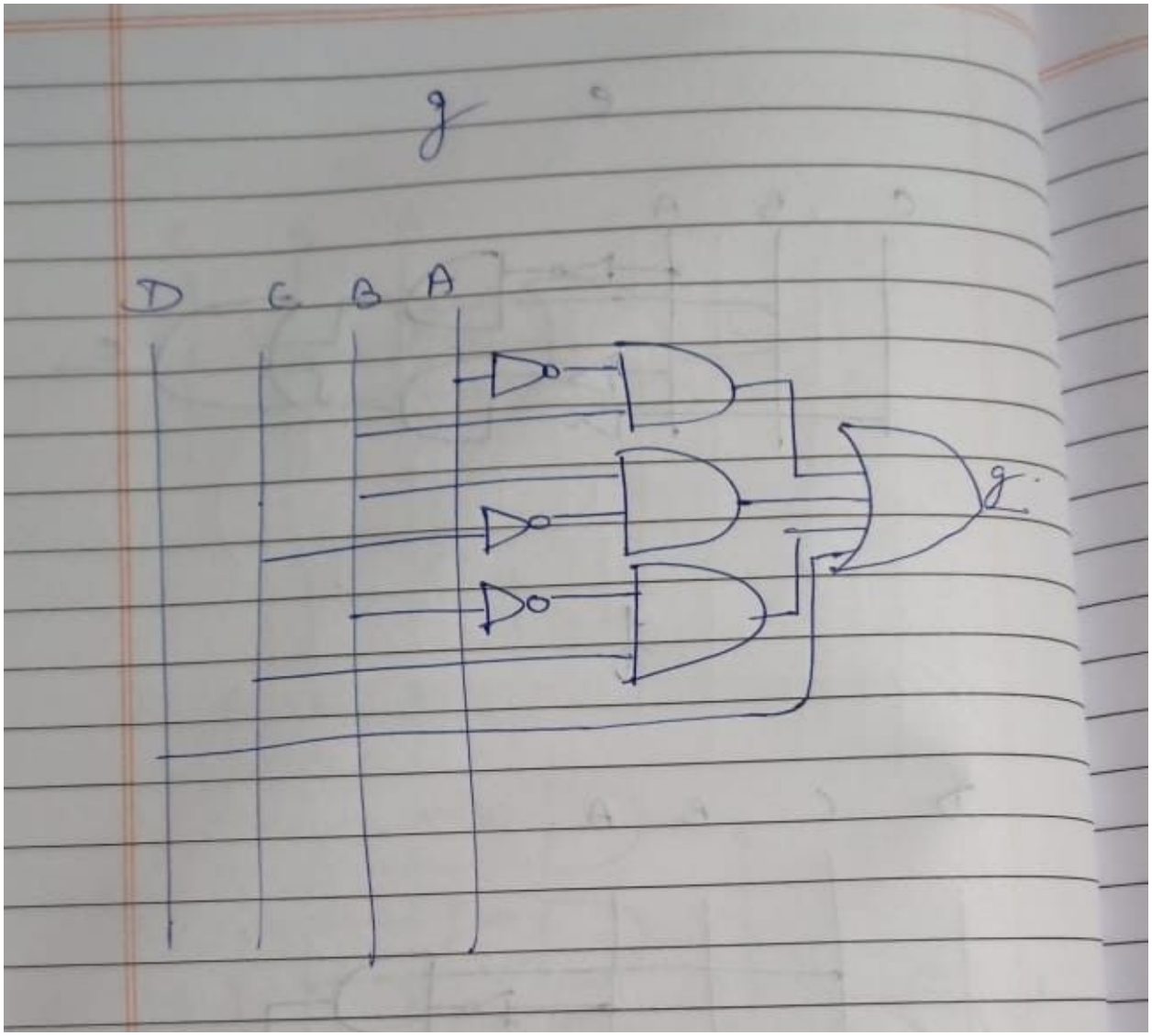
e



f.

D C B A.





Truth Table :

DE	D	C	B	A	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1

5	**0**	**1**	**0**	**1**	**1**	**0**	**1**	**1**	**0**	**1**	**1**
6	**0**	**1**	**1**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**
7	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**0**
8	**1**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
9	**1**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**0**	**1**	**1**

Observations :

The above experiment depicts how to make a seven segment display by using only AND,OR,NOT gates.
From this we can assume that the above circuit shows the inner workings of a 7 Segment decoder.