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(A)

Q1

Ans

* step ① : convert the binary number to decimal.

$$A = 10_{10} = 1010_2$$

$$B = 12_{10} = 1100_2$$

* step 2 = Ensure both number have the same bit width.

$$* A = 01010_2$$

$$B = 01100_2$$

* ③ Perform operation

① Addition: $A + B$

$$\begin{array}{r} 01010 \\ + 01100 \\ \hline 10110 \end{array} \quad (\text{Result in binary})$$

$$\text{Result } 10110_2 = 22_{10}$$

② sub : $A - B$

using 2's complement for subtraction:

(B)

7) Find the 2's complement of B

* $B: 01100 \rightarrow 10011$

* Add 1 $\therefore 10011 + 1 = 10100$

* 2's complement of B = 10100

Add A and 2's complement of B

$$\begin{array}{r} 01010 \\ + 10100 \\ \hline 11110 \end{array}$$

* take 2's complement and take its ~~negative~~ magnitude.

* Invert 11110: 00001

Add 1: $00001 + 1 = 00100$

~~2's complement of B = 10100~~

magnitude: (210)

* Final Result $(A - B) = \textcircled{-210}$ Ans

III

©

Subtraction B-A

Using 2's complement for subtraction.

1) Invert A: $01010 \rightarrow 10101$

→ Add 1: $10101 + 1 = 10110$

→ 2's complement of A = 10110

Add B and 2's complement of A

$$\begin{array}{r} 01100 \\ 10110 \\ \hline 100010 \end{array}$$

Dropping the overflow bit Result is $00010_2 = 2_{10}$

IV

multiplication A x B

A $\Rightarrow 01010$ B $\Rightarrow 01100$

$$\begin{array}{r} 01010 \\ \times 01100 \\ \hline 00000 \quad (\text{0 from rightmost bit}) \\ + 01010 \quad (\text{Shift left one}) \\ + 10100 \quad (\text{Shift left twice}) \\ \hline 11100 \end{array}$$

Result

$$\left. \begin{array}{l} \text{Result} \\ = (11100)_2 = 6_{10} \end{array} \right\} \text{A}$$

Q2 Ans

* characteristic equation of D Flip Flop:

clk	D	cn	ant1
↑	0	0	0
↑	0	1	0
↑	1	0	1
↑	1	1	1

→ Truth table

D \ Q	0	1
0	0	0
1	1	1

→ K-map

$$\boxed{ant1 = a^+ = D} \rightarrow \text{equation}$$

* characteristic equation of JK Flip Flop.

clk	J	K	cn	ant1
↑	0	0	0	0
↑	0	0	1	1
↑	0	1	0	0
↑	0	1	1	0
↑	1	0	0	1
↑	1	0	1	1
↑	1	1	0	1
↑	1	1	1	0

J \ KQ	00	01	11	10
0	0	1	0	0
1	1	1	0	1

$$\boxed{ant1 = a^+ = J\bar{Q} + \bar{K}Q}$$

Q2 Ans

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↑	1	1	0	1
↑	1	1	1	0

J \ KQ	00	01	11	10
0	0	1	0	0
1	1	1	0	1

$$\boxed{\text{cnt1} = a^+ = J\bar{Q} + \bar{K}Q}$$

① characteristics of T Flip-Flop ^{equation}

clk	T	on	antz
↑	0	0	0
↑	0	1	1
↑	1	0	1
↑	1	1	0

→ truth table

T	Q	TQ	
		0	1
0	0	0	①
1	0	①	0

→ K-map

TQ
 $T\bar{Q}$

$$antz = Q^+ = TQ + \bar{T}Q = T \oplus Q$$

equation.

3 6 mm

11 D flip-flop

Module d-ff (

Output reg q.

Input d.

Input rst-n.

Input clk

);

always @ (posedge clk or negedge rst-n)

begin

if (!rst-n)

begin

q <= 0;

end

else

begin

q <= d;

end

end

end module

① Explanation

→ * ← * → *

① The module is named d-fl.

② it has four ports.

③ the module is named d-fl

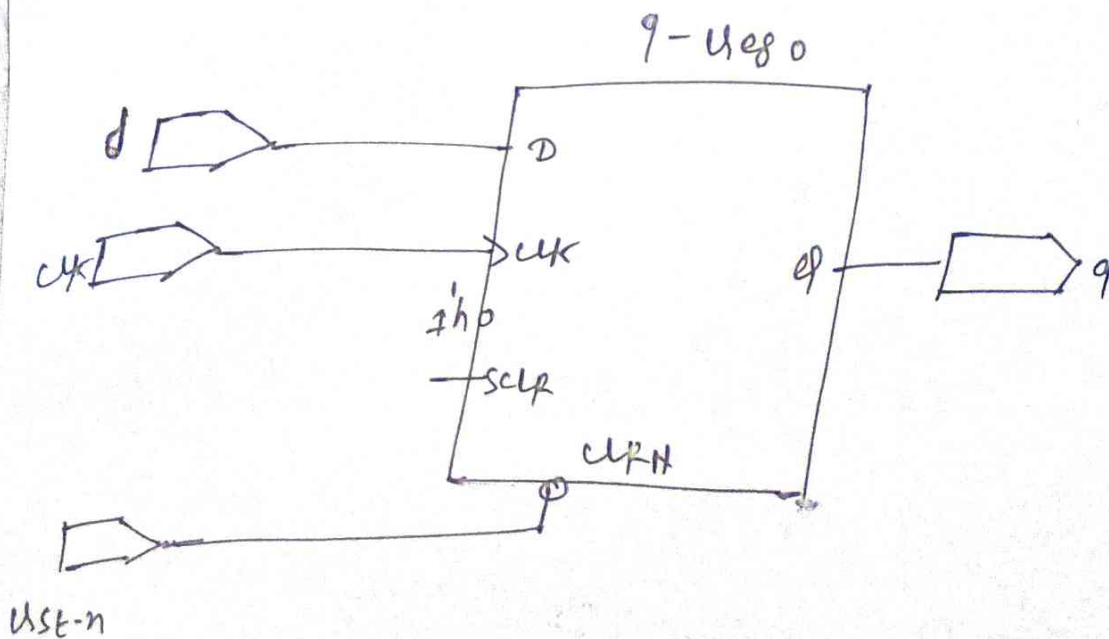
④ it has four ports:

⑤ q (out put): Represent the out of of D flip-flop

⑥ d (Input): Represent the Input data

⑦ rst-n (Input): Represent the active low reset signal

⑧ clk (Input): Represent the clk signal



(93)

module d-ff-tb;

// Inputs

Usg d;

Usg rst_n;

Usg clk;

// out puts

wire q;

// Instantiate the d flip flop module

d-ff uut (

. q (q),

. d (d),

. rst_n'(rst_n),

. clk (clk)

);

// clock generation

always #5 clk = ~clk;

// Test bench Initialize Inputs

d = 0;

rst_n = 0;

clk = 0;

// put de-assuration after some time

50 $\text{Mst} - \eta = 1$:

// Apply Input d changes

10 $d = 1$:

20 $d = 0$:

30 $d = 1$:

End Simulation

100 \$ finish :

end

end module .

4 Ans

① Binary conversion

Dividend	remainder
$100/2 = 50$	0
$50/2 = 25$	0
$25/2 = 12$	1
$12/2 = 6$	0
$6/2 = 3$	0
$3/2 = 1$	1
$1/2 = 0$	1

$$100_{10} = 1100100_2$$

② Octal conversion

8	100	4	↑ 144
8	12	4	
8	1	7	

Read the Reverse

$$(100)_{10} = (144)_8 \text{ Ans}$$

③ Hexa conversion

—*—*—*—*

$$(100)_{10} = (64)_{16}$$

Divide $(100)_{10}$ successively by 16 until the quotient is 0

$$100 / 16 = 6, \text{ Remainder is } 4$$

$$6 / 16 = 0, \text{ Remainder is } 6$$

show Hexa decimal of $(100)_{10} = (64)_{16}$ Ans

④ BCD Conversion

—*—*—*

decimal

① write each digit as a 4 bit Binary

$$1 = 0001,$$

$$0 = 0000,$$

$$0 = 0000,$$

$$\text{BCD} = 0001\ 0000\ 0000$$

Q5 Mr

Full Adder In Data Flow model:

module fulladder (

Input a,

Input b,

Input cin,

output S,

output cout

);

$\&\rightarrow$ and

assign S = $a \wedge b \wedge cin$

assign cout = $(a \wedge b) \vee cin \wedge (a \vee b)$;

end module

II Full Adder In Gate level module

module fa(

Input a ,

Input b ,

Input cin,

out put cout

);

wire x1, x2, x3;

xor (x1, a, b);

and (x3, a, b);

xor (s1, x1, cin);

and (x2, x1, cin);

or (cout, x2, x3);

end module