```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity Traffic_light is
    Port ( clk : in STD_LOGIC;
         clr : in STD_LOGIC;
         light : out STD_LOGIC_VECTOR (5 downto 0));
end Traffic_light;

architecture Behavioral of Traffic_light is
type state is (s0,s1,s2,s3,s4,s5);
signal st : state;
signal count :  integer ;
begin
process(clr,clk,count,st)
begin
if (clr = '1') then
st <= s0;
count <= 0;
elsif (rising_edge(clk)) then
case st is
when s0 =>
if count = 15 then
st <= s1;
count <= 1  ;
light <= "010100";
else
st <= s0;
count <= count + 1;
light <= "001100";
end if;
when s1 =>
if count = 3 then
st <= s2;
count <= 1  ;
light <= "100100";
else
st <= s1;
count <= count + 1;
light <= "010100";
end if;
when s2 =>
if count = 3 then
st <= s3;
```

```vhdl
count <= 1  ;
light <= "100001";
else
st <= s2;
count <= count + 1;
light <= "100100";
end if;
when s3 =>
if count = 15 then
st <= s4;
count <= 1  ;
light <= "100010";
else
st <= s3;
count <= count + 1;
light <= "100001";
end if;
when s4 =>
if count = 3 then
st <= s5;
count <= 1  ;
light <= "100100";
else
st <= s4;
count <= count + 1;
light <= "100010";
end if;
when s5 =>
if count = 3 then
st <= s0;
count <= 1  ;
light <= "001100";
else
st <= s5;
count <= count + 1;
light <= "100100";
end if;
end case;
end if ;
end process;
end Behavioral;
```