

Performance analysis of Graph Coloring algorithms for Register Allocation in compilers

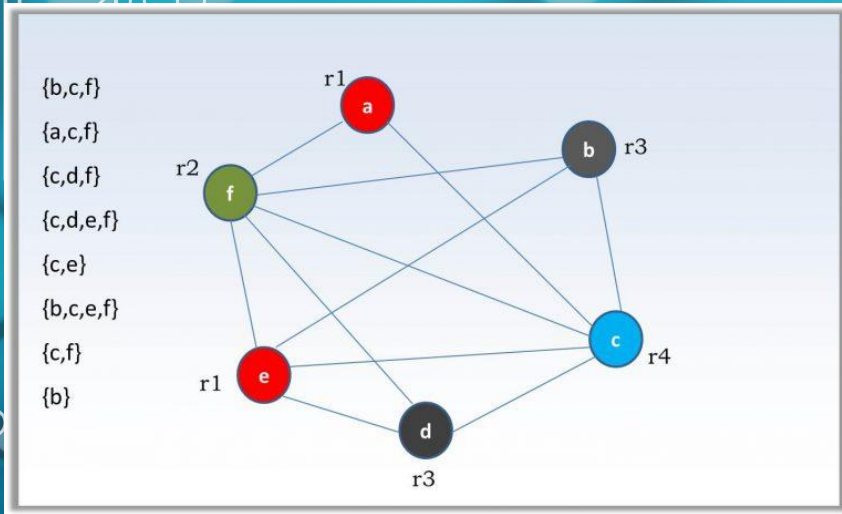
Allocation in compilers

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What is Register Allocation?

Process of assigning variables to registers during final phase of compiler optimisation.





Why Register Allocation?

- Registers - limited resources with faster access than cache and main memory
- Manages data transfer in and out of registers
- Efficient register allocation
 - reduces time of accessing code variables otherwise stored in main memory.
 - Optimizes the performance of compiled code .



Challenges while allocating registers

- Large number of IR variables compared to available physical general -purpose registers.
- Registers reserved for assemblers or operating systems, limiting availability for other operations.

The background of the slide is a teal-colored circuit board. On the left side, there are white lines representing circuit traces, some of which end in small white circles. The right side of the slide has a solid teal background with a subtle gradient.

Problem Statement

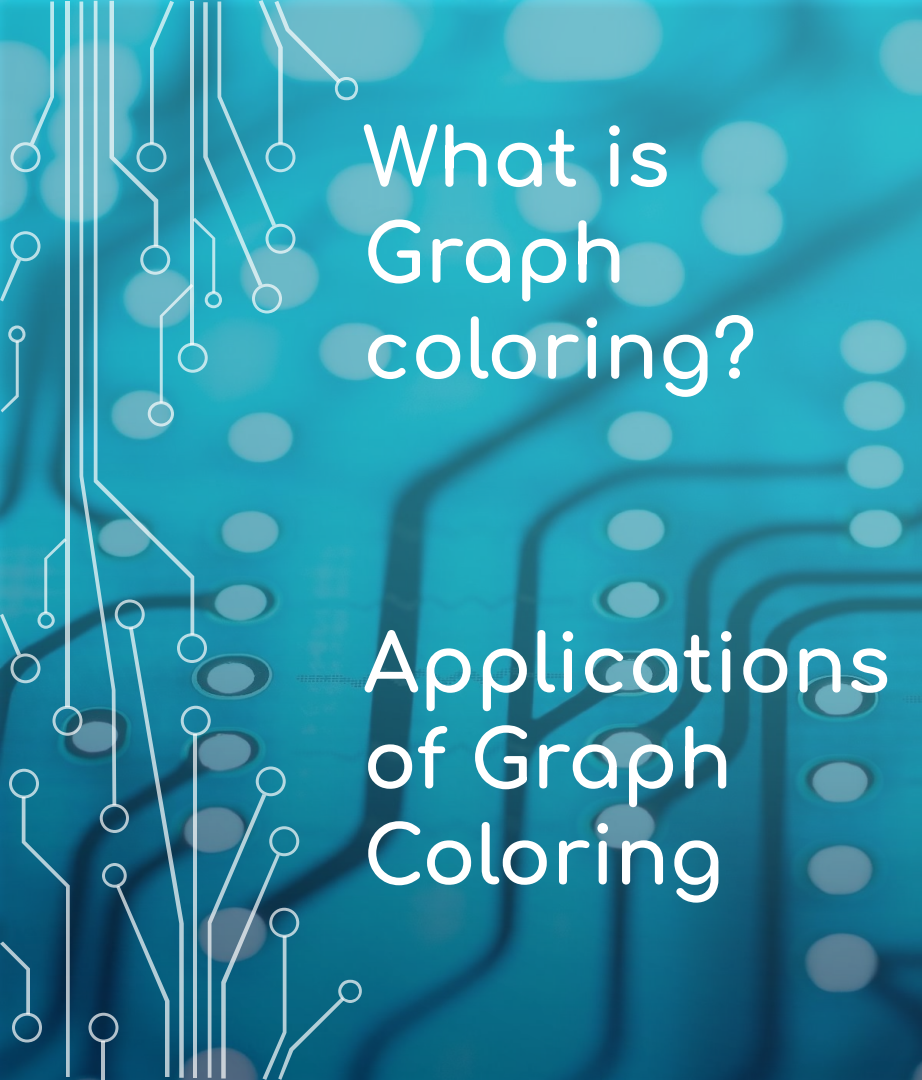
Given limited registers and minimal storage, how can we efficiently allocate the available registers to optimise their usage, increasing the speed of program execution in a compiler?

(Register Allocation Problem)

Approaches

Several approaches to solve the register allocation problem:

- Naive Register Allocation
- Linear Scan Algorithm
- **Graph Coloring Algorithm**



What is Graph coloring?

Technique to assign colors to the vertices (nodes) of a graph in such a way that no two adjacent vertices share the same color.

Applications of Graph Coloring

- Register Allocation
- Map Coloring
- Mobile radio frequency assignment
- Task scheduling
- Sudoku Puzzle



Graph coloring in Register Allocation

Interference Graph:

An interference graph is constructed for IR variables:

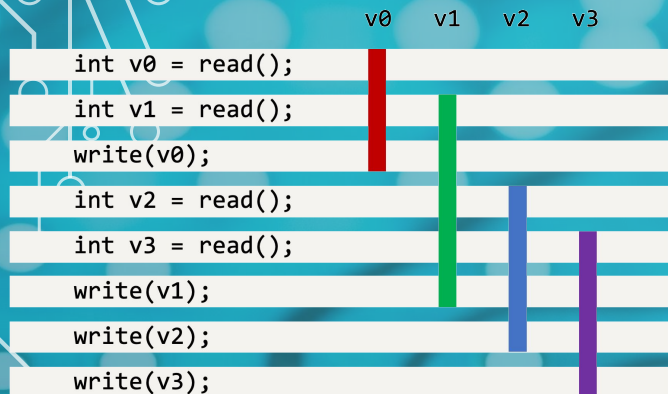
- Nodes – variables,
- Edge - if the corresponding variables interfere with each other (cannot share the same register).

Graph Coloring:

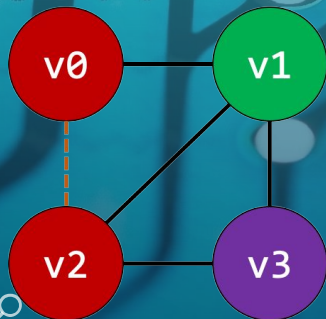
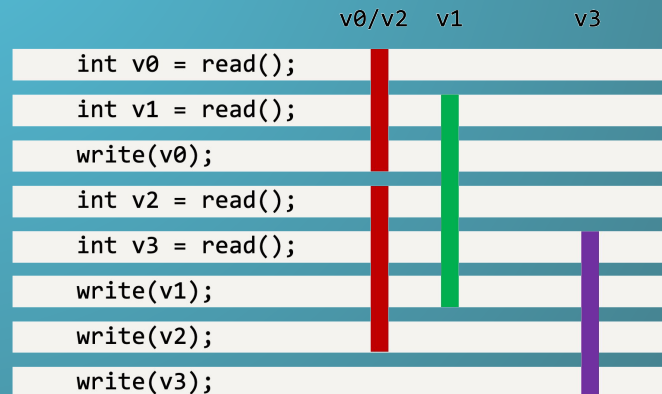
The objective is to assign colors (registers) to nodes in the interference graph.

A coloring is valid if no two adjacent nodes (connected by an edge) have the same color.

Graph coloring for Register Allocation

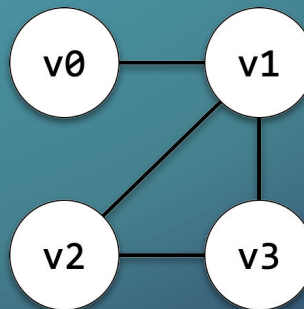


Interaction between variables in an Instruction Set

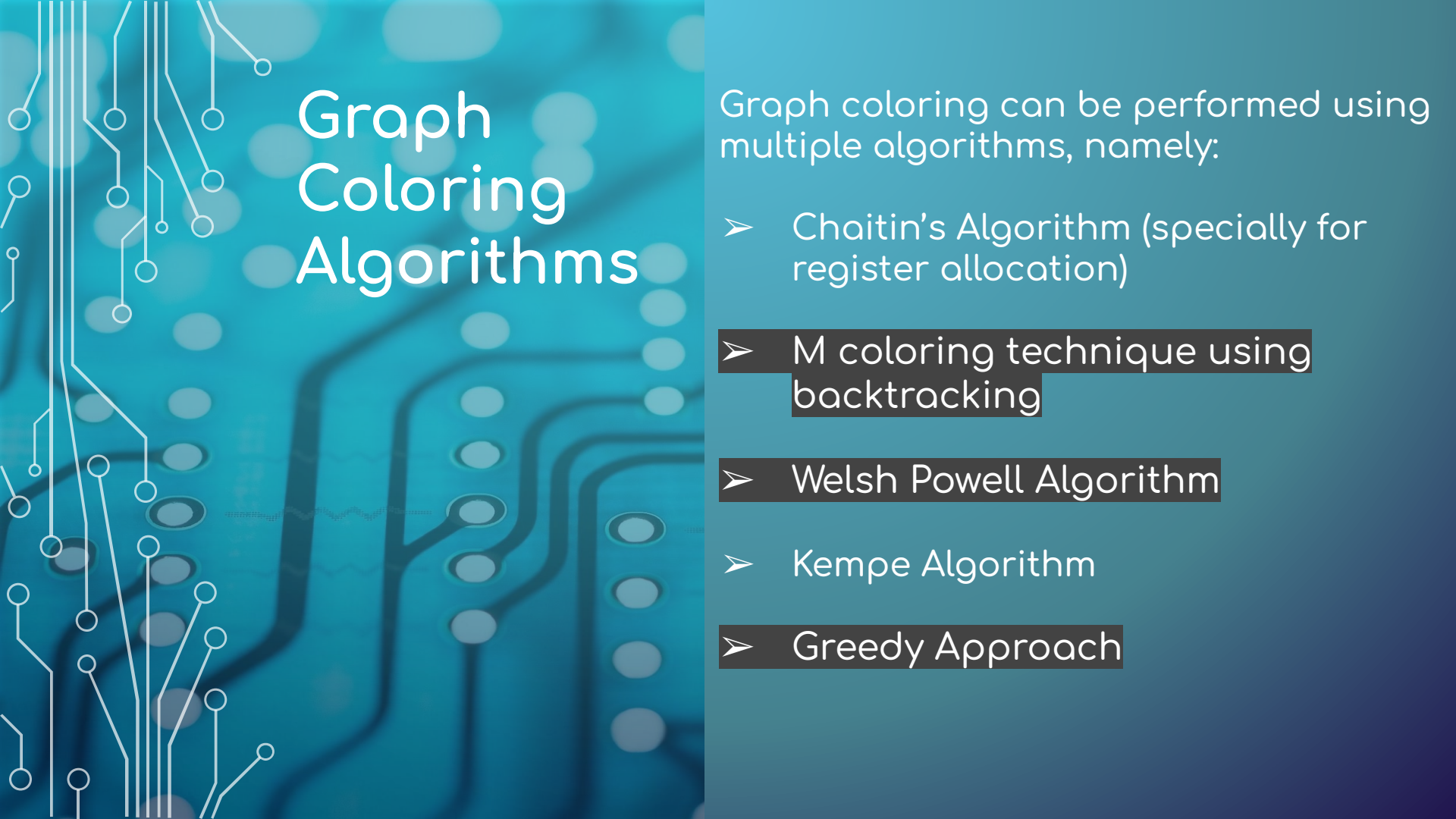


I/P to Graph Coloring Algorithms

O/P - Graph with Colored nodes
(Note - Every color represents a distinct register)



Interference Graph



Graph Coloring Algorithms

Graph coloring can be performed using multiple algorithms, namely:

- Chaitin's Algorithm (specially for register allocation)
- M coloring technique using backtracking
- Welsh Powell Algorithm
- Kempe Algorithm
- Greedy Approach

Datasets

| Graph | Vertices (V) | Edges (E) |
|-------------|--------------|-----------|
| mycie13 | 11 | 20 |
| mycie17 | 191 | 2360 |
| miles1500 | 128 | 5195 |
| queen_14_14 | 196 | 8372 |



Greedy Approach

- Color the first vertex with first color.
- For all the remaining $V-1$ vertices
 - Color it with the lowest numbered color not used by its adjacent vertices
 - If all colors are used, assign a new color.
- Time complexity - $O(V^2)$

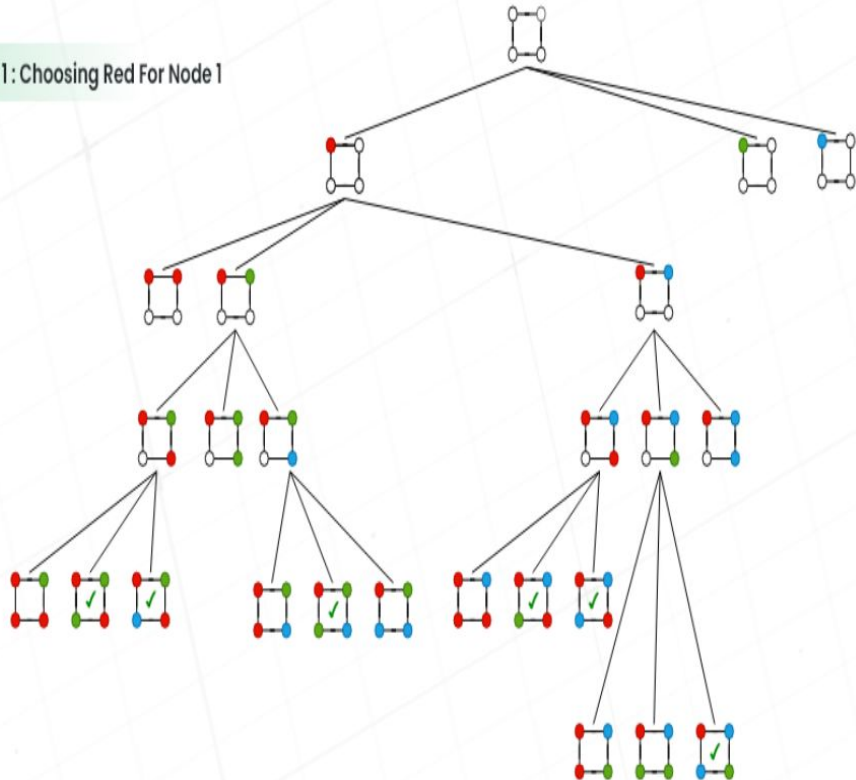
Results for Greedy Approach

| Graph | Vertices (V) | Edges (E) | Chromatic Number | Running Time (s) |
|-------------|--------------|-----------|------------------|------------------|
| mycie13 | 11 | 20 | 4 | 0.002 |
| mycie17 | 191 | 2360 | 8 | 0.008 |
| miles1500 | 128 | 5195 | 76 | 0.016 |
| queen_14_14 | 196 | 8372 | 23 | 0.016 |

Backtracking Approach

- For the selected vertex, try assigning colors one by one from a predefined set of colors while checking if the current assignment is valid (no adjacent vertices have the same color).
- If a valid color is assigned, move to the next vertex and repeat above step recursively.
- If a color cannot be assigned to the current vertex without conflicts, backtrack to the previous vertex and change its color. Repeat the above steps.
- Continue this process until all vertices are colored or until all possibilities have been explored.
- Time Complexity - k^V ,
k is the number of colors

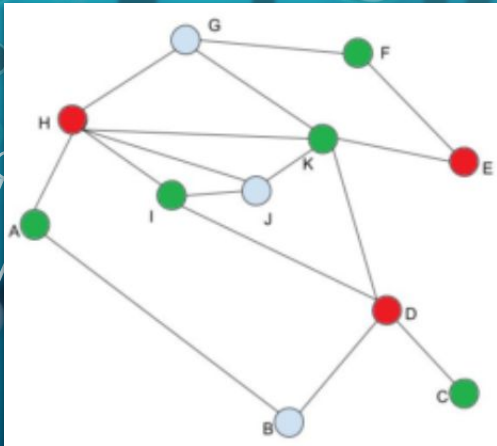
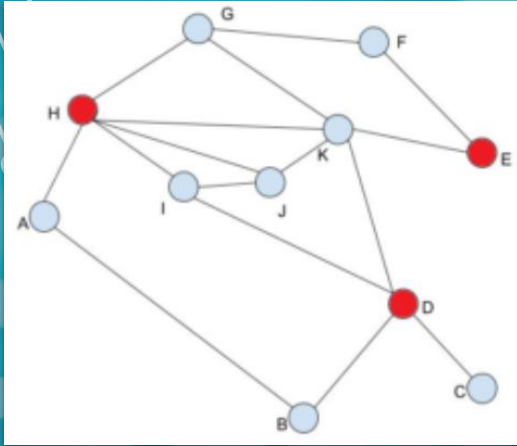
Case 1: Choosing Red For Node 1



Results for Backtracking

| Graph | Vertices (V) | Edges (E) | Chromatic Number | Running Time (s) |
|-------------|--------------|-----------|------------------|------------------|
| mycie13 | 11 | 20 | 4 | 0.008 |
| mycie17 | 191 | 2360 | 8 | 0.008 |
| miles1500 | 128 | 5195 | 76 | 0.030 |
| queen_14_14 | 196 | 8372 | 23 | 0.023 |

Welsh-Powell Algorithm



- Sort the vertices in descending order of their degree.
- Color first vertex with color 1.
- Color all the vertices non adjacent to the vertex with color 1 and assign them the same color (color 1).
- Repeat the above step by picking an uncolored vertex in decreasing order of their degree and assigning it a new color until all the vertices are colored.
- Time complexity - $O(V^2)$

Results for Welsh-Powell algorithm

| Graph | Vertices (V) | Edges (E) | Chromatic Number | Running Time (s) |
|-------------|--------------|-----------|------------------|------------------|
| mycie13 | 11 | 20 | 4 | 0.003 |
| mycie17 | 191 | 2360 | 8 | 0.008 |
| miles1500 | 128 | 5195 | 73 | 0.012 |
| queen_14_14 | 196 | 8372 | 23 | 0.019 |

Comparison of Approaches

| Graph | Greedy Approach | | Backtracking | | Welsh-Powell | |
|-------------|------------------|------------------|------------------|------------------|------------------|------------------|
| | Chromatic Number | Running Time (s) | Chromatic Number | Running Time (s) | Chromatic Number | Running Time (s) |
| mycie13 | 4 | 0.002 | 4 | 0.008 | 4 | 0.003 |
| mycie17 | 8 | 0.008 | 8 | 0.008 | 8 | 0.008 |
| miles1500 | 76 | 0.016 | 76 | 0.030 | 73 | 0.012 |
| queen_14_14 | 23 | 0.016 | 23 | 0.023 | 23 | 0.019 |

The background of the slide is a teal-colored circuit board. On the left side, there are white lines representing circuit traces, some ending in small white circles. The rest of the background is a darker teal with faint, darker circuit patterns and some circular elements.

Future Work

- We would like to work on a dataset consisting of compiler instruction sets.
- Then create an interference graph from it.
- Finally consider spilling used in Chaitin's approach to reduce the number of registers.

References

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4) GeeksforGeeks. (2022, January 24). Register allocations in Code generation. GeeksforGeeks.
<https://www.geeksforgeeks.org/register-allocations-in-code-generation/>

5) Seeing Register Allocation Working in Java. Seeing register allocation working in Java. (n.d.).
<https://chrisseaton.com/truffleruby/register-allocation/>

The background is a vibrant blue gradient. On the left side, there are white, stylized circuit traces and nodes. The right side features a pattern of dark blue, wavy lines and circular bokeh-like shapes, giving it a sense of depth and digital complexity.

Demonstration