# SEC = 0 Case

| SEC | D | WE | $Q_{pub\ N-1}$ | $Q_{pub\ N}$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 |

**Behavior:**
When WE=1, the mux transmits input data that writes to the register as long as D changes over rising clock edge. When WE=0, reg retains previous state

**Summary:**
When secure mode is on, Qpub part retains existing state, and Qsec register is enabled with a write toggle.
When secure mode is off, Qsec is erased, and Qpub functions as normal register

# SEC = 1 Case

| SEC | D | WE | $Q_{pub\ N-1}$ | $Q_{pub\ N}$ |
|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 |

**Behavior:**
When SEC=1, Qpub holds its previous value

| SEC | D | WE | $Q_{sec\ N-1}$ | $Q_{sec\ N}$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 |

**Behavior:**
When SEC=0, NAND => INV will always pass 0 to the positive-edge reg, regardless of D and WE values.

| SEC | D | WE | $Q_{sec\ N-1}$ | $Q_{sec\ N}$ |
|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 |

**Behavior:**
When SEC=1, if WE=0, then existing Q_SEC value is transmitted by MUX and sent back to reg. If WE=1, D value is written to reg, as long as D changes on rising clock edge