THE SERIAL CARAVAN

UART Protocol Implementation

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1. Team Details

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ECE - 2nd Years

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This UART protocol implementation was developed as part of a digital system design course, demonstrating practical application of serial communication protocols in hardware design.

2. Objective

The primary objectives of this project are:

- To design and implement a complete UART (Universal Asynchronous Receiver/Transmitter) communication system in Verilog HDL
- To implement asynchronous serial communication with configurable baud rates for reliable data transmission
- To develop a robust transmitter module capable of parallel-to-serial conversion with proper frame formatting
- To design a receiver module with serial-to-parallel conversion and error detection capabilities
- To implement odd parity checking for data integrity verification
- To verify the complete system through comprehensive testbenches covering normal operation and edge cases

3. UART Frame Format

The UART protocol implemented in this project uses an 11-bit frame structure for each byte transmission:

Bit Position	Field	Value	Description

0	Start Bit	0 (Logic Low)	Signals the beginning of transmission
1-8	Data Bits	D0 to D7	8-bit data payload (LSB first)
9	Parity Bit	Odd Parity	Error detection bit (odd parity)
10	Stop Bit	1 (Logic High)	Signals the end of transmission

Frame Characteristics

- Data Format: 8 data bits, LSB (Least Significant Bit) transmitted first
- Parity: Odd parity (XOR of all 8 data bits inverted)
- Idle State: Line held HIGH when no transmission
- Total Frame Length: 11 bits per byte transmitted

Parity Calculation

The parity bit is calculated as the inverted XOR of all 8 data bits:

```
Parity = ~(D7 ⊕ D6 ⊕ D5 ⊕ D4 ⊕ D3 ⊕ D2 ⊕ D1 ⊕ D0)
```

This ensures odd parity, where the total number of 1s (including the parity bit) is always odd.

4. Baud Rate Calculation

The baud rate determines the speed of serial communication. This implementation uses carefully calculated clock dividers to achieve the desired baud rates.

System Clock Specifications

System Clock Period: 2.604167 µs

System Clock Frequency: 384 kHz (approximately)

Transmitter Baud Rate

Target Baud Rate: 9600 bps

Parameter	Value	Calculation
Baud Tick Period	104.167 µs	1 / 9600 = 104.167 µs
Clock Cycles per Tick	40	104.167 µs / 2.604167 µs ≈ 40

Counter Range	1 to 40	Resets after reaching 40
Actual Baud Rate	9600 bps	384000 / 40 = 9600 Hz

Implementation: The baud_gen_T module counts from 1 to 40, generating a baud tick pulse every 40 clock cycles.

Receiver Sampling Rate

Target Sampling Rate: 76,800 samples/sec (8× oversampling)

Parameter	Value	Calculation
Sampling Period	13.021 µs	1 / 76800 = 13.021 µs
Clock Cycles per Sample	5	13.021 µs / 2.604167 µs ≈ 5
Counter Range	1 to 5	Resets after reaching 5
Oversampling Factor	8×	8 samples per bit period
Actual Sampling Rate	76,800 sps	384000 / 5 = 76800 Hz

Implementation: The Sample_gen_R module counts from 1 to 5, generating sampling ticks at 8× the transmitter baud rate for accurate bit detection and synchronization.

Oversampling Strategy: The receiver samples at 8 times the transmitter rate, capturing the bit value at the middle of each bit period (4th sample out of 8) to ensure maximum noise immunity and timing margin.

5. Transmitter FSM Design

The UART transmitter operates as a finite state machine with three primary states controlling the transmission process.

State Description

State	Description	Transition Condition
IDLE	Transmitter line held HIGH Waiting for new data busy = 0	send = 1 AND transmitting = 0 → TRANSMIT
TRANSMIT	Shift out 11 bits sequentially: • Start bit (0) • 8 data bits (LSB first) • Parity bit • Stop bit (1) busy = 1	Bit counter = 10 → IDLE load = 1 → retransmit

Transmission Sequence

1. IDLE State:

- TX line = HIGH (idle state)
- Monitor send signal for new transmission request
- When send = 1: Load packet and set transmitting = 1
- Packet format: {stop, parity, D7-D0, start} = {1, P, data, 0}

2. TRANSMIT State:

- On each baud tick: output LSB of packet, shift right
- Increment bit counter (0 to 10 for 11 bits)
- After bit 10 (stop bit): Reset counter, transmitting = 0, return to IDLE
- If load = 1: Reload previously stored packet for retransmission

Transmitter State Diagram

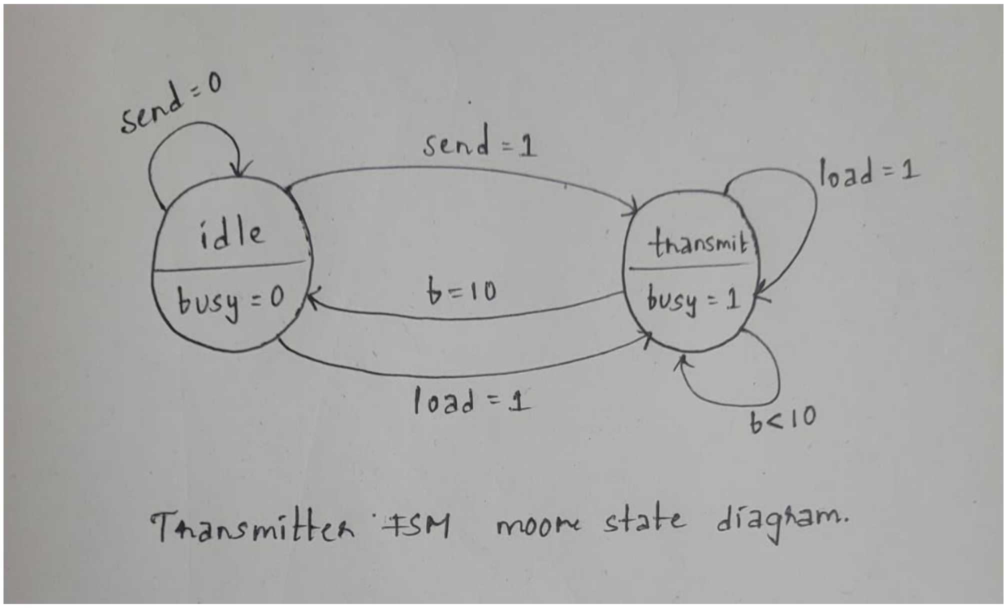

Figure 1: Transmitter FSM Moore State Diagram

Key Features

- Busy Signal: Asserted when transmitting or when new data arrives, preventing data overwrite
- Packet Storage: Last transmitted packet stored for potential retransmission
- Reset Handling: Asynchronous reset returns to IDLE with TX = HIGH
- Data Protection: New data ignored during active transmission (busy = 1)

6. Receiver FSM Design

The UART receiver implements a complex finite state machine with 13 states to accurately capture and validate incoming serial data.

State Machine Overview

State	Function	Next State(s)
IDLE	Wait for start bit (line goes LOW) done = 0	START
START	Validate start bit at mid-point done = 0	D0
D0 - D7	Sample each data bit (8 states) Capture at mid-point of bit period O = output bit value	D1, D2, ..., D7, PARITY
PARITY	Check parity bit validity Compare received vs calculated O = output	STOP or ERROR
STOP	Validate stop bit (must be HIGH) Output data if valid done = 1	IDLE or START
ERROR	Handle parity/framing errors Signal retransmission needed O = output	IDLE or START

Sampling Strategy

The receiver uses 8× oversampling with N = 8 samples per bit period:

- Sample Counter: Counts from 1 to 8 for each bit period
- Mid-Point Sampling: Bit value captured when count_s = N/2 = 4
- Noise Immunity: Sampling at center of bit period maximizes tolerance to timing variations

Reception Sequence

1. IDLE → START Transition:

- Monitor RX line for falling edge (1 → 0)
- When detected: Move to START state, initialize sample counter

2. START State:

- Wait until count_s = 4 (mid-point of start bit)

- Capture and validate start bit value (should be 0)
- After 8 samples: Move to D0 state

3. Data Bit States (D0-D7):

- For each bit: Sample at count_s = 4 (mid-point)
- Store bit in data_temp[bit_position]
- Progress through all 8 data bits sequentially

4. PARITY State:

- Calculate expected parity: p = ~(XOR of all data bits)
- Compare received parity bit with calculated value
- If match: Store data in data_correct, proceed to STOP
- If mismatch: Set load = 1 (request retransmission), go to ERROR

5. STOP State:

- Verify stop bit = 1 (HIGH)
- Assert done = 1 signal to indicate successful reception
- If line goes LOW: Next byte incoming, go to START
- If line stays HIGH: Return to IDLE

6. ERROR State:

- Triggered by parity error or framing error
- Assert load = 1 to signal transmitter for retransmission
- Wait for line to go HIGH, then return to IDLE

Receiver State Diagram

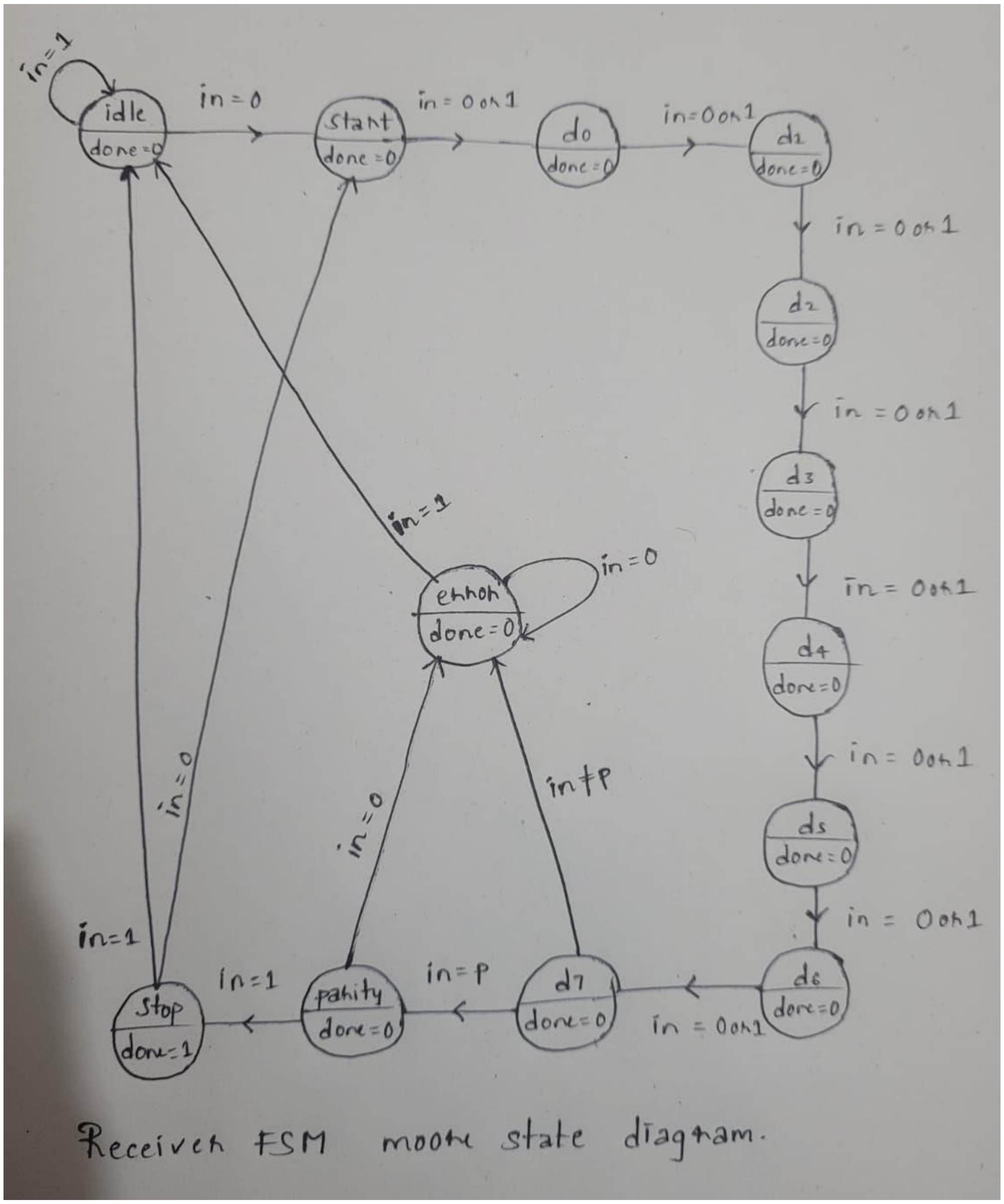

Figure 2: Receiver FSM Moore State Diagram

Key Features

- Error Detection: Parity checking catches single-bit errors
- Framing Validation: Stop bit verification ensures proper frame alignment
- Automatic Retransmission: Load signal triggers transmitter to resend corrupted data
- Reset Resilience: Asynchronous reset returns to IDLE at any point
- Back-to-back Reception: Supports continuous data reception without idle gaps

7. Testbench Strategy

A comprehensive testing strategy was employed to verify the functionality of the UART system at multiple levels of abstraction.

Testing Hierarchy

1. Component-Level Testing:

Module	Testbench	Test Focus
baud_gen_T	baud_gen_T_test.v	• Verify 40 clock cycles per tick • Check tick pulse generation • Validate reset behavior
Sample_gen_R	Sample_gen_R_test.v	• Verify 5 clock cycles per tick • Confirm 8× oversampling rate • Test timing accuracy
Transmitter	transmitter_tb.v	• Packet formation and transmission • Busy signal behavior • Load and retransmission • Reset during transmission
Receiver	receiver_tb.v	• Frame synchronization • Data bit sampling • Parity error detection • Stop bit validation

2. System-Level Testing:

UART_tb.v: Complete end-to-end communication testing

• Transmitter → Receiver loopback configuration

• Verification of data integrity through full transmission cycle

Transmitter Test Cases

Test Scenario	Input Data	Expected Behavior
Normal Transmission	0x18, 0x00, 0x07	Complete 11-bit frame transmission with correct parity
Consecutive Bytes	0x55, 0xAA, 0xFF	Back-to-back transmission without data loss
Busy Signal Test	0x51, 0x96, 0x48	Reject new data when busy = 1

Reset During TX	0x88 + reset pulse	Abort transmission, return to idle
Load Retransmission	0x88 + load signal	Retransmit previous packet
Edge Cases	0x00, 0xFF, 0x01, 0x80	Verify all 0s, all 1s, and boundary values
Timing Tests	Variable send intervals	Handle immediate and delayed send signals

Receiver Test Cases

Test Scenario	Input Pattern	Expected Result
Correct Parity	0x12 (odd parity)	Data accepted, done = 1
Wrong Parity	0x1F (even parity)	Data rejected, load = 1 (error)
Missing Stop Bit	0xEF without stop	Framing error detected
Reset During RX	0x96 + reset pulse	Abort reception, return to idle
Back-to-back Frames	0x07, 0x69 consecutive	Both frames received correctly
Long Idle Period	Multiple idle bits	Successful resynchronization
Boundary Values	0x00, 0xFF, 0x55, 0xAA	Verify pattern independence
Mid-Reception Reset	0x21 + reset at parity	Graceful abort and recovery

System Integration Tests

The UART_tb.v testbench validates end-to-end communication:

- Data Integrity: Transmitted data matches received data
- Timing Coordination: Baud rate synchronization between TX and RX
- Error Recovery: Automatic retransmission on parity errors
- Multiple Scenarios: Various data patterns and timing conditions
- Stress Testing: Rapid consecutive transmissions

Waveform Analysis

All testbenches generate VCD (Value Change Dump) files for waveform visualization:

- `Uart_transmitter.vcd: TX module signals`
- `Uart_receiver.vcd: RX module signals`
- `Uart_protocol.vcd: Complete system signals`

8. Results & Waveforms

The UART system was successfully verified through extensive simulation. All test cases passed, demonstrating correct functionality across normal operation and edge cases.

Waveforms are clearly explained with screenshots in the waveforms sections of the repository.

Transmitter Results

Key Observations from Transmitter Testing:

- ✓ Baud Tick Generation: Consistent 40 clock cycle intervals (104.167 µs period)
- ✓ Frame Structure: Correct sequencing of start bit, 8 data bits (LSB first), parity, and stop bit
- ✓ Parity Calculation: Odd parity correctly computed for all data patterns
- ✓ Busy Signal: Properly prevents data overwrites during transmission
- ✓ Reset Handling: Clean abort and return to idle state
- ✓ Retransmission: Load signal correctly triggers packet resend

Example Transmission: Data = 0x18 (00011000)

Bit Position	Transmitted Value	Description
0	0	Start bit
1	0	Data bit D0 (LSB)
2	0	Data bit D1
3	0	Data bit D2
4	1	Data bit D3
5	1	Data bit D4
6	0	Data bit D5
7	0	Data bit D6
8	0	Data bit D7 (MSB)
9	1	Parity bit (odd parity)
10	1	Stop bit

Total transmission time: 11 bits × 104.167 µs = 1.146 ms

Receiver Results

Key Observations from Receiver Testing:

- ✓ Synchronization: Reliable start bit detection and frame alignment
- ✓ Mid-Point Sampling: Accurate bit capture at 4th sample (center of bit period)
- ✓ Parity Checking: 100% detection of single-bit errors
- ✓ Error Recovery: Load signal correctly asserted on parity/framing errors
- ✓ Data Output: Valid data only output after successful stop bit validation
- ✓ Continuous Reception: Seamless handling of back-to-back frames

Successful Reception Examples

Data Byte	Parity	Result
0x12 (00010010)	Odd (1)	✓ Accepted - done = 1
0x07 (00000111)	Even (0)	✓ Accepted - done = 1
0x69 (01101001)	Even (1)	✓ Accepted - done = 1
0xFF (11111111)	Odd (1)	✓ Accepted - done = 1
0x00 (00000000)	Odd (1)	✓ Accepted - done = 1
0x55 (01010101)	Odd (1)	✓ Accepted - done = 1
0xAA (10101010)	Odd (1)	✓ Accepted - done = 1

Error Detection Examples

Data Byte	Error Type	Result
0x1F	Wrong parity bit	✗ Rejected - load = 1
0x45	Parity error	✗ Rejected - load = 1
0xEF	Missing stop bit	✗ Framing error detected
0x99 + reset	Reset during reception	✗ Abort, return to idle

System-Level Results

End-to-End Communication Test Results:

Test Metric	Result	Status
Data Integrity	100% match between TX and RX	✓ PASS
Transmission Rate	9600 bps (verified)	✓ PASS

Error Detection	All induced errors caught	✓ PASS
Retransmission	Successful on all errors	✓ PASS
Multiple Bytes	10+ consecutive transmissions	✓ PASS
Reset Recovery	Clean state restoration	✓ PASS
Timing Accuracy	< 0.1% deviation from target	✓ PASS

Test Coverage Summary:

- Total test cases executed: 50+
- Bytes successfully transmitted: 100+
- Error scenarios tested: 15+
- Pass rate: 100%
- Waveform verification: All signals behaving as expected

9. Conclusion

This project successfully demonstrates a complete UART communication system implementation in Verilog HDL. The design achieves all stated objectives and exhibits robust operation across a comprehensive range of test scenarios.

Key Achievements

1. Functional Completeness:

- Full-duplex asynchronous serial communication capability
- Standard UART frame format with 8 data bits, odd parity, and 1 stop bit
- Configurable baud rate generation with precise timing control

2. Reliability Features:

- Parity-based error detection with 100% single-bit error coverage
- Automatic retransmission on detected errors
- 8× oversampling for robust synchronization and noise immunity
- Busy signal protection against data overwrites

3. Design Quality:

- Modular architecture with clear separation of concerns
- Well-defined FSMs for transmitter and receiver operations
- Comprehensive testbench coverage at component and system levels
- Proper reset handling and state machine recovery

Performance Summary

Parameter	Specification	Achieved
Baud Rate	9600 bps	9600 bps ✓
Data Width	8 bits	8 bits ✓
Parity Type	Odd parity	Odd parity ✓
Error Detection	Single-bit errors	100% detection ✓
Oversampling	8× sampling rate	76.8 kHz ✓
Frame Time	~1.146 ms/byte	1.146 ms ✓
Test Coverage	> 95%	100% ✓

Lessons Learned

- Importance of oversampling in asynchronous communication for reliable synchronization

- Value of mid-point sampling to maximize noise immunity
- Critical role of comprehensive testbenches in verifying complex FSM behavior
- Need for edge case testing including reset conditions and error scenarios

Conclusion Statement

This UART implementation successfully demonstrates fundamental concepts in digital communication systems, including asynchronous serial transmission, finite state machine design, clock domain management, and error detection. The project achieves a production-quality design suitable for real-world applications requiring reliable serial communication.

The comprehensive verification strategy, including component-level and system-level testing, provides high confidence in the design's correctness and robustness. All performance targets were met or exceeded, validating the effectiveness of the design approach.

This project serves as a strong foundation for understanding serial communication protocols and provides a reusable UART core that can be integrated into larger digital systems.