



TARGETX

16-channel, GPS Transient Waveform Recorder with Self-Triggering and Fast, Selective Window Readout

General Description

The Belle II KLM production readout version of the TARGET ASIC (TARGETX) is a 16-channel transient waveform recorder initially designed to monolithically and inexpensively instrument large deployments of semiconductor photon detectors for large neutrino and muon detectors. The very general nature of the signal recording, the narrow digitization selection window, and fast single conversion make it useful in a number of applications. In order to support large arrays, self-triggering capabilities have been incorporated to permit event-of-interest identification as well as data sparsification.

Intended for detectors needing sampling rates of 0.5-1 Giga-samples per second (GPS), triggered readout rates of up to 100kHz are possible, depending upon occupancy, sample resolution and serial readout speed. Each channel has 512 groups of 32 storage cells ("windows"), or 16,384 storage samples available.

Features

- High density (16 channels)
- Good timing performance
- 9-10 bits of single sample resolution
- Fast conversion ($<5\mu\text{s}/512$ samples)
- Random access to individual samples
- Flexible operating modes
- All biases set with internal DACs

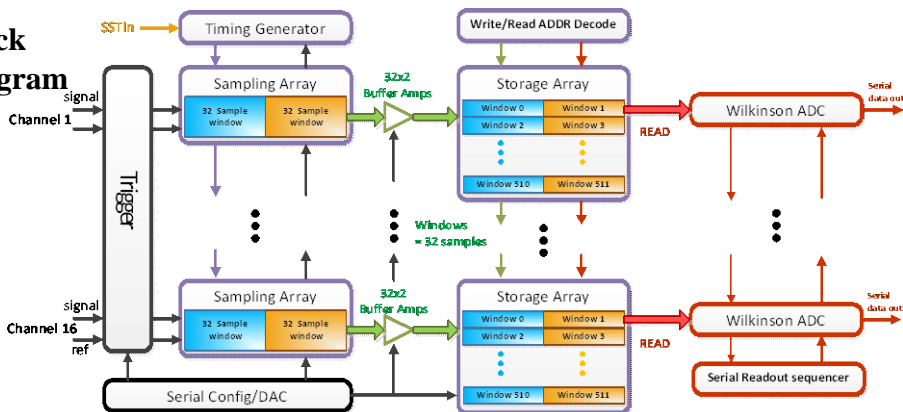
Key Specifications

- Low power ($<10\text{mW}/\text{channel}$)
- Giga-sample per second recording
- Selective (windowed) readout
- 16,384 storage samples/channel

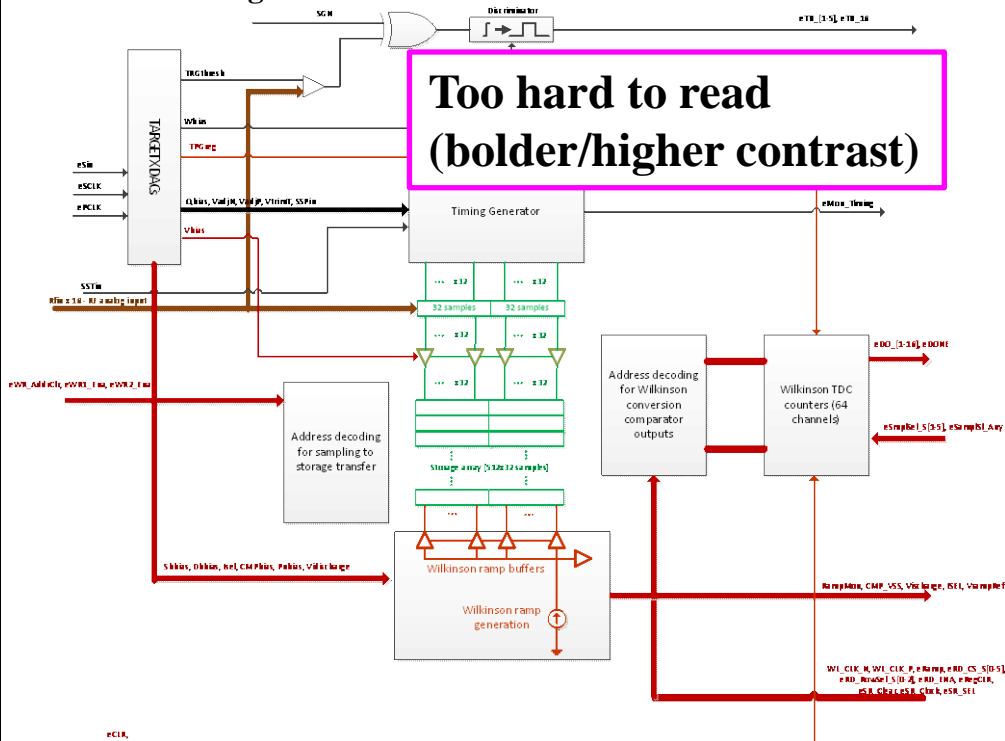
Applications

- Large scintillator-based muon/neutrino detectors
- Low-cost, highly integrated systems
- Collider Detector instrumentation
- Portable/pocket oscilloscope

Block Diagram



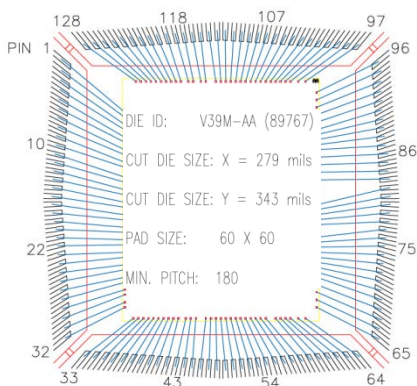
Connection Diagram



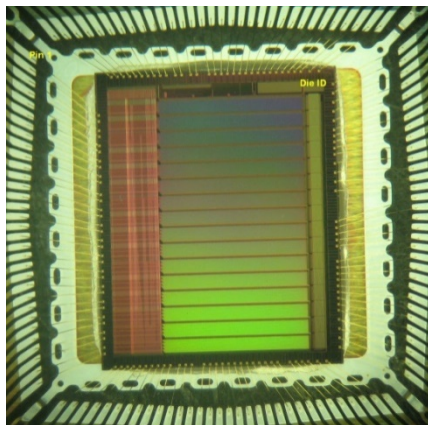
Available Packaging

The currently available TARGETX devices are available in a standard TQFP-128 package.

Bonding Diagram



Die Photograph



Pin-out Functional Listing

A detailed list of pin numbers and functionality. Color coding has been used to clarify signal type and group by functionality. Additional comments are provided to indicate relationships, function, or suggested interconnect values. Light blue signals correspond to analog signals and set via internal DAC, and are primarily for monitoring, except for VadJN, VadJP and VramPRef (which required external bypass capacitors).

 	= VDD
 	= GND
 	= Digital to FPGA
 	= Digital from FPGA
 	= Analog/bias value
 	= Sample speed CTRL
 	= Signal input
 	= Reference terminal
 	= Test point
 	= LVDS inputs

TARGETX ASIC pinout

14-May-14 GSV

Pin #	Pin Name	Connection type	Comments
1 RFin_1	PMT input Ch. 1	termination R	
2 RFin_1	Termination reInput Ch. 1	external, between pins	
3 RFin_2	PMT input Ch. 2	termination R	
4 RFin_2	Termination reInput Ch. 2	external, between pins	
5 RFin_3	PMT input Ch. 3	termination R	
6 RFin_3	Termination reInput Ch. 3	external, between pins	
7 RFin_4	PMT input Ch. 4	termination R	
8 RFin_4	Termination reInput Ch. 4	external, between pins	
9 RFin_5	PMT input Ch. 5	termination R	
10 RFin_5	Termination reInput Ch. 5	external, between pins	
11 RFin_6	PMT input Ch. 6	termination R	
12 RFin_6	Termination reInput Ch. 6	external, between pins	
13 RFin_7	PMT input Ch. 7	termination R	
14 RFin_7	Termination reInput Ch. 7	external, between pins	
15 RFin_8	PMT input Ch. 8	termination R	
16 RFin_8	Termination reInput Ch. 8	external, between pins	
17 RFin_9	PMT input Ch. 9	termination R	
18 RFin_9	Termination reInput Ch. 9	external, between pins	
19 RFin_10	PMT input Ch. 10	termination R	
20 RFin_10	Termination reInput Ch. 10	external, between pins	
21 RFin_11	PMT input Ch. 11	termination R	
22 RFin_11	Termination reInput Ch. 11	external, between pins	
23 RFin_12	PMT input Ch. 12	termination R	
24 RFin_12	Termination reInput Ch. 12	external, between pins	
25 RFin_13	PMT input Ch. 13	termination R	
26 RFin_13	Termination reInput Ch. 13	external, between pins	
27 RFin_14	PMT input Ch. 14	termination R	
28 RFin_14	Termination reInput Ch. 14	external, between pins	
29 RFin_15	PMT input Ch. 15	termination R	
30 RFin_15	Termination reInput Ch. 15	external, between pins	
31 RFin_16	PMT input Ch. 16	termination R	
32 RFin_16	Termination reInput Ch. 16	external, between pins	
33 GND33	0V power (GND = VSS)		
34 VDD34	2.5V power (VDD)		
35 sEn	Serial input data	all bits, last = first	
36 sCLK	Serial clock advance	shift in each bit	
37 sCLK	Parallel clock load	transfer shifted data	
38 sHout	Serial Shift Out	monitor output	
39 GND39	0V power (GND = VSS)		
40 VDD40	2.5V power (VDD)		
41 aTRG_3	Trigger output #3	Ch. 9-12	
42 aTRG_4	Trigger output #4	Ch. 13-16	
43 aTRG_5	Trigger output #5 marker	Multi	
44 aTRG_16	Ch. 16 only	0-15 encoded	
45 GND45	0V power (GND = VSS)		
46 eRD_CS_S0	Read Column Select Addr. 0	Select	
47 eRD_CS_S1	Read Column Select Addr. 1	group of 32	
48 eRD_CS_S2	Read Column Select Addr. 2	group of 32	
49 eRD_CS_S3	Read Column Select Addr. 3	samples	
50 eRD_CS_S4	Read Column Select Addr. 4	for Wilkinson	
51 eRD_CS_S5	Read Column Select Addr. 5	Conversion	
52 VDD52	2.5V power (VDD)		
53 GND53	0V power (GND = VSS)		
54 aWR_AdrClr	Clear Write Address Counter	group of 32 to write	
55 aWR1_Ena	WR 1 Enable	Normally Ena	
56 aWR2_Ena	WR 2 Enable	Normally Ena	
57 WL_CLK_p	Wilkinson Clock LVDS	n	
58 WL_CLK_n	Wilkinson Clock LVDS	p	
59 GND59	0V power (GND = VSS)		
60 VDD60	2.5V power (VDD)		
61 eSmpSel_S5	Converted sample Addr select #5	Most significant bit	
62 eSmpSel_S4	Converted sample Addr select #4		
63 eSmpSel_S3	Converted sample Addr select #3		
64 eSmpSel_S2	Converted sample Addr select #2		

Pin #	Pin Name	Connection type	Comments
65 eSmpSel_S1	Converted sample Addr select #1	Least signif bit	
66 eSmpSel_S0	Enable any samples	off during convll	
67 VDD67	2.5V power (VDD)		
68 GND68	0V power (GND = VSS)		
69 eDO_16	Serial Data Out Ch. 16	MSB to LSB	
70 eDO_15	Serial Data Out Ch. 15		
71 eDO_14	Serial Data Out Ch. 14	MSB to LSB	
72 eDO_13	Serial Data Out Ch. 13		
73 eDO_12	Serial Data Out Ch. 12	MSB to LSB	
74 eDO_11	Serial Data Out Ch. 11		
75 eDO_10	Serial Data Out Ch. 10	MSB to LSB	
76 eDO_9	Serial Data Out Ch. 9		
77 VDD77	2.5V power (VDD)		
78 GND78	0V power (GND = VSS)		
79 eSR_Clear	Clear data Shift Reg	not required	
80 eSR_Clock	Advance Shift Register data	or load, depending	
81 eSR_SEL	Select SR_Clock behaviour	L=SR, H=Load	
82 VDD82	2.5V power (VDD)		
83 GND83	0V power (GND = VSS)		
84 eDO_8	Serial Data Out Ch. 8	MSB to LSB	
85 eDO_7	Serial Data Out Ch. 7		
86 eDO_6	Serial Data Out Ch. 6	MSB to LSB	
87 eDO_5	Serial Data Out Ch. 5		
88 eDO_4	Serial Data Out Ch. 4	MSB to LSB	
89 eDO_3	Serial Data Out Ch. 3		
90 eDO_2	Serial Data Out Ch. 2	MSB to LSB	
91 eDO_1	Serial Data Out Ch. 1		
92 VDD92	2.5V power (VDD)		
93 GND93	0V power (GND = VSS)		
94 eDONE	AND of all DONE	ADC complete	
95 aCLR	Wilkinson Clear	Wilk Start	
96 GND96	0V power (GND = VSS)		
97 VDD97	2.5V power (VDD)		
98 GND98	0V power (GND = VSS)		
99 eRegCLR	Global register clear	clear all registers	
100 eRD_ENA	Enable ReadOut	off = no comp	
101 GND101	0V power (GND = VSS)		
102 VDD102	2.5V power (VDD)		
103 eRD_RS_S2	Select Row Read Addr #2	MSB	
104 eRD_RS_S1	Select Row Read Addr #1		
105 eRD_RS_S0	Select Row Read Addr #0	LSB	
106 GND106	0V power (GND = VSS)		
107 VDD107	2.5V power (VDD)		
108 eRamp	Wilkinson Ramp control	H=Ramp, L=Vdrsc	
109 CMP_VSS	Wilkinson mirror Ref	set to GND	
110 Vdrsc	Wilkinson Ramp Start voltage	set by int. DAC	
111 RampMon	Buffered copy of Wilk Ramp	direct observation	
112 ISEL	Monitor for Wilk Ramp I (V out)	set by int. DAC	
113 VramPRef	Charging node	50-100pF typ	
114 GND114	0V power (GND = VSS)		
115 VDD115	2.5V power (VDD)		
116 eMON_Timing	Monitor timing signals	MUXed	
117 GND117	0V power (GND = VSS)		
118 eTRG_2	Trigger output #2	Ch. 5-8	
119 eTRG_1	Trigger output #1	Ch. 1-4	
120 VDD120	2.5V power (VDD)		
121 GND121	0V power (GND = VSS)		
122 VadJn	Sampling NMOS current Adj	int/ext	
123 GND123	0V power (GND = VSS)		
124 VadP	Sampling PMOS current Adj	int/ext	
125 sStin_p	sStin LVDS	p	
126 sStin_n	sStin LVDS	n	
127 GND127	0V power (GND = VSS)		
128 VDD128	2.5V power (VDD)		

Absolute Maximum Ratings

Supply Voltage (VDD)	-0.4V to +3.6V
Voltage Input Digital lines	-0.3V to +3.3V
Voltage Input Signal pins ¹	+0.4 to +2.8V
Voltage any output pin	TBD
Input Current (non-power)	TBD
Package Input Current	TBD
Max Junction Temperature	TBD
Thermal Resistance	TBD
Package Dissipation	TBD
+ Many other specs	TBD
Storage temperature ²	-65C to +150C

Note 1: Minimal input protection diode structure

Note 2: Soldering process must comply with ASAT Technologies Reflow Temperature Profile Specifications

Operating Ratings

Operating Temperature	-0.4V to +3.6V
Supply Voltage	-0.3V to +3.3V
Output Signal Levels	+0.4 to +2.8V
SSTout strobe jitter	TBD
SSTout Duty Cycle	TBD
Analog Input Pins	TBD
Vpnd	+0.4V to +2.8V

**Some good
measurements to be
done**

Converter Electrical Characteristics

Stored samples in the TARGETX are converted into output digital code using a Wilkinson technique, where a ramp converts the analog value into a binary output time. These time intervals, from the beginning of ramp until the count time is latched using a fast Gray code counter, is proportional to the stored analog value. By changing the ISEL (ramp rate) and VrampRef (external capacitor), the conversion ramp time slope can be manipulated. Performance and number of bits of resolution depend upon this ramp slope and Wilkinson clock provided externally (typically from FPGA).

Symbol	Parameter	Conditions	Typ.	Limits	Units
INL	Integral Non-linearity	Full scale input	TBD	TBD	Bits (min)
DNL	Differential Non-linearity	Full scale input	TBD	TBD	Bits (min)
Tacq	Conv. Cycle time	16 channels * 32x in parallel	1	TBD	us
ENC	Equivalent Noise	No signal	TBD	TBD	Bits (min)

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**Datasheets don't
usually have TOC**

**(PDF are searchable
– so people can
usually find what
they want/need that
way?)**

Input Coupling

To permit the highest possible input frequency response that TARGETX has been designed with a reference signal, tied to an input pedestal voltage (V_{ped}) and used for common mode rejection, to complement the raw input signal. This reference is provided with high ESD protection. The raw high-frequency input is not. Therefore it is highly recommended that a fast, low capacitance RF-rated input protection diode be used on these inputs. The basics of this RF input structure have been evaluated previously and the expected performance is simulated below.

Magnitude [dB]

RF input:

→ S11, S21(?)

- **Smith chart**
- **Amplitude roll-off**



10MHz

100MHz

Frequency

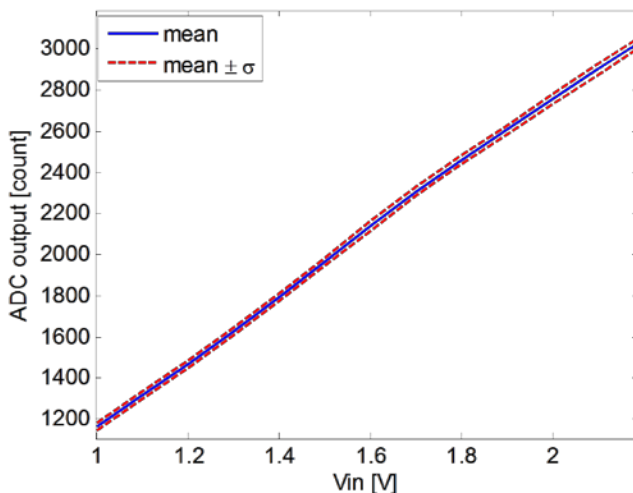
Due to the active elements in the amplification path, the SPICE simulated input frequency is expected to be more like 500MHz for the gain shown on the next page. Unlike TARGET, because the amplifier is on the storage sample output, instead of the input, the gain-bandwidth of the amplifier does not significantly degrade the large amplitude response.

Trigger Functionality

→ Characterize S-curves
**→ Demonstrate pattern
functionality**

ADC Transfer Function

The transfer function of the ADC which shows voltage input to the ASIC versus the output code of the ASIC. The plot is the average of 31 samples.

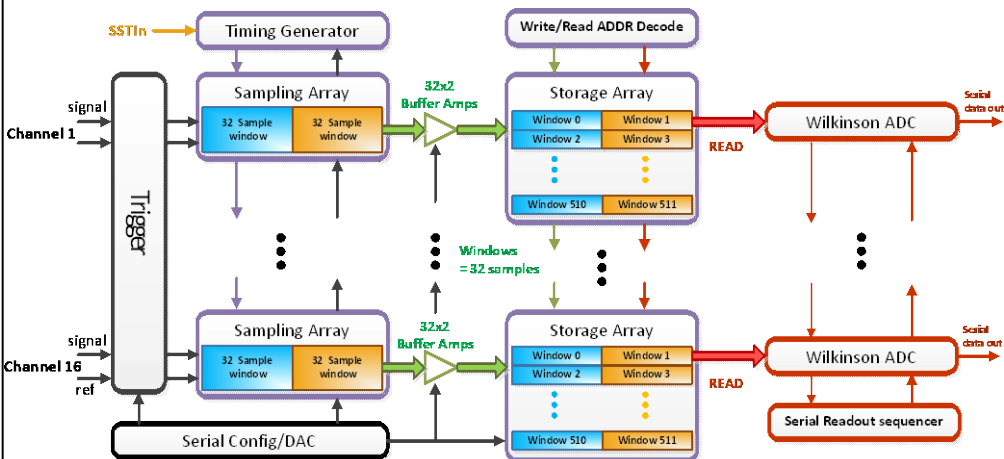


**Need some verbiage
here:**

- **Measure INL
and DNL**
- **Uniformity
channel-channel**

Operational Overview

The figure below outlines the key functional blocks of the TARGETX ASIC. External to this ASIC it is assumed that any gain required is provided externally. While the input is consistent with a low impedance one, external termination is expected to turn any current output device into an input voltage.



TARGETX is a 16-channel device where both a signal and its reference signal are input to the ASIC, to provide a well-defined impedance into the sampling array on die (with stub on die for rest of input line).

Control of the timing samples is provided by a configurable timing generator that is driven by the **SSTin** input LVDS signal, as described in detail in the **Sample Timing Generator** section. In order to provide continuous sampling, sampling and transfer to a much larger storage array is performed on groups of 32. When acquisition occurs in one group of 32, the other group of 32 are being amplified and buffered by **Buffer Amps** and then written into the **Storage Array**. Independent Write and Read controls permit multi-hit functionality and addressing is described in the **Write/Read ADDR Decode** section.

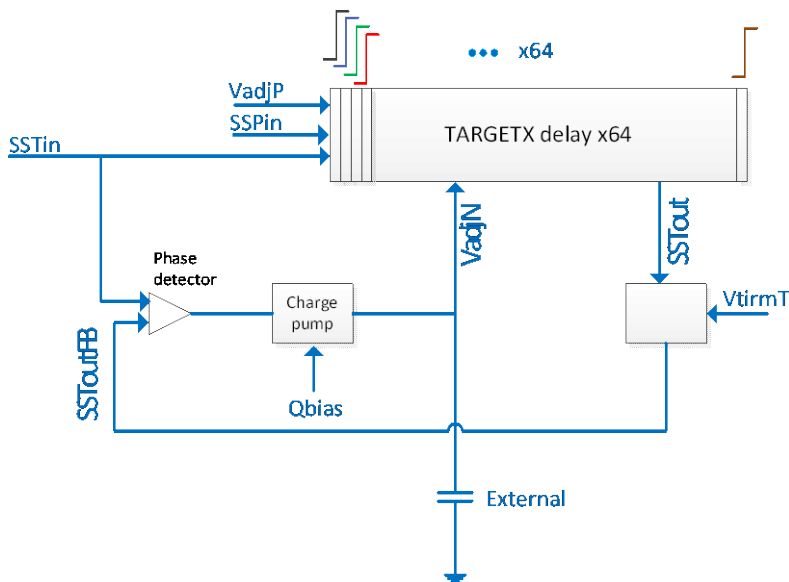
Utilizing all 512 atomic storage groups of 32 samples, a depth of 16,384 samples is available for either multi-event buffering or up to 16 μ s of trigger latency. Groups of 32 are randomly accessible for readout. Once selected, the 32 storage cells in all 16 channels are powered up for Wilkinson ADC conversion. The **Wilkinson Ramp Generator** block (not shown) generates and broadcasts a ramp to all channels. At a separately controlled time a counter is started for each channel. In order to reduce power while allowing for a fast clock speed, separate oscillators are provided for each counter. When the voltage ramp crosses the comparator threshold the counter stops and the count then represents the time (ADC code) corresponding to the voltage held in the storage cell.

Digitized samples are selected (again randomly accessible) and then serial transferred on all 16 channels in parallel. Address decoding and sequencing is performed inside the Serial Readout Sequencer block.

Finally, to simply implementation and external board component requirements, many configuration bits and biases are set via on-chip 12-bit DACs. These are detailed in the **Serial Config/DAC** block.

Sample Timing Generator

The sampling speed of the TARGETX is controlled by adjusting the **VadjP** and **VadjN** voltage lines. Internally, the base delay element is a current starved inverter.



Schematic of the base timing generator cell. Quiescent, both **SSPin** and **SSTin** are low. Sampling begins with **SSPin** being asserted. At a later time, when **SSTin** is asserted high, the switches then open and the instantaneous value at the input to the switch is then stored on the sampling capacitors. As long as **SSPin** is asserted sufficiently far in advance (sampling speed dependent but typically 8ns or more), and stays valid until after **SSTin** has passed, **SSPin** itself is not timing critical. Therefore the rising edge of **SSTin** is the defining timing signal and every effort should be made to maintain its integrity. 64 delayed version of the **SSTin** is generated with desired delay. The delay line loop feedback adjusts **VadjN** for optimum sampling, **SSTin** and **SSToutFB** phase is compared and the output is connected to a charge pump which its strength is determined by **Qbias** value. An external capacitor stores the value of **VadjN**.

Sampling Speed Stabilization

It is known that the sampling speed of these delay timing generators is temperature dependent, typically with a value determined to be something like 0.2%/degree C. In order to compensate for this effect, there are 2 mechanisms available. A continuous ring oscillator copy of the delay time generator (with one additional inverter and that output fed back to the input is available as the **RCO** signal). The **SSPout** for the last stage of the delay chain is also made available for monitoring and feedback. A number of means can be employed to determine and lock the net delay and they will be updated as testing proceeds.

Sampling Speed Adjustment

As seen at the left, by adjusting the VadjN signal we are able to easily cover 0.5-1.5 GSa/s sampling in SPICE simulation. Very conservative values were used for the parasitic capacitances of the timing generator structure and 20% faster operation has been seen in similar ASICs using essentially the same delay generator circuitry, which indicates operation to just over 2 GSa/s may be possible. Multiple methods are available for locking this sampling frequency, as discussed on the preceding page. Sensitivity for a target operating point of 1 GSa/s is presented in the figure below.

Example tuning sensitivity for maintaining stable timebase.

Sampling Speed Measurement

As this is one of the easiest of the adjustments, space reserved for this measurement

Serial Config/DAC

TARGETX, like TARGET2 has a large number of configurable registers. These are loaded via a serial data protocol into a set of shift registers. To permit no-destructive readback and minimize upset to registers not changed, the entire sequence of 363 control bits is shifted into TARGETX via data input pin **SIN** whose data is advanced on the rising edge of the **SCLK** pin. After wending its way through the entire signal chain, the value then appears 446 transfer cycles later on the **SHout** pin. At 50MHz clock rate it takes about 9 μ s to load the entire register array. Once all values have been serially loaded, the actual control registers are updated using the parallel clock (**PCLK**) signal. Long routing delays within TARGETX may limit the speed of these signals internally and will need to be verified via test. A register reset pin (**RegCLR**) is provided though not normally needed.



TARGETX register map

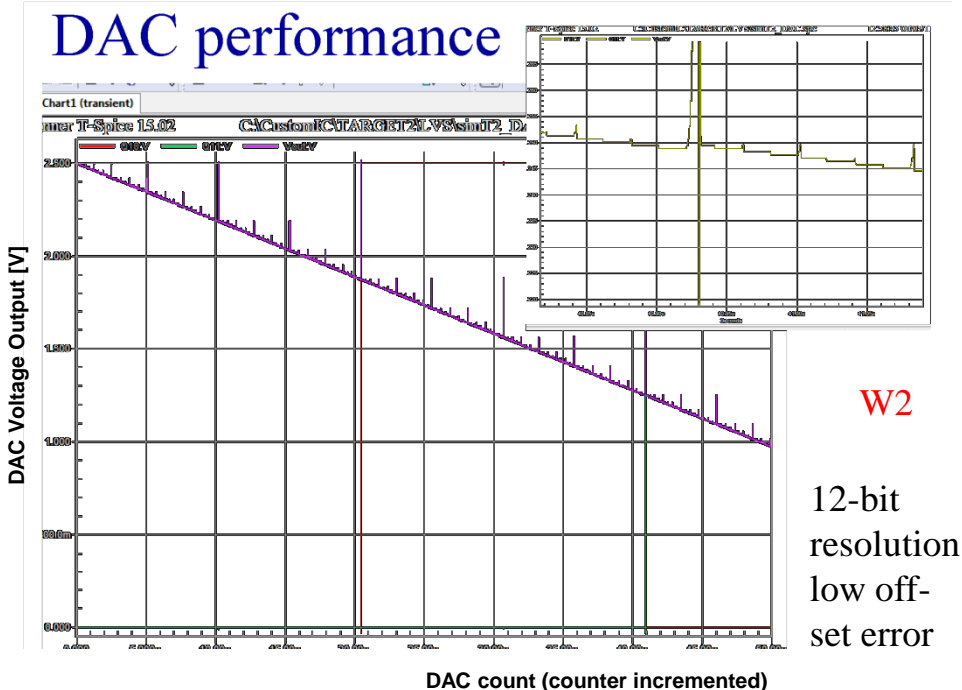
PCLK #	Description	PCLK #	Description	PCLK #	Description	PCLK #	Description	PCLK #	Description
1	Trigger Threshold	17	Trigger Threshold	33	unused (T7)legacy	49	Sbbias	65	SSPin LE
2	Wbias	18	Wbias	34	unused (T7)legacy	50	Vdich	66	SSPin TE
3	Trigger Threshold	19	Trigger Threshold	35	unused (T7)legacy	51	Isel	67	WR_ADDR_Incr1 LE
4	Wbias	20	Wbias	36	unused (T7)legacy	52	Dbbias	68	WR_ADDR_Incr1 TE
5	Trigger Threshold	21	Trigger Threshold	37	unused (T7)legacy	53	Qbias	69	WR_STRB1 LE
6	Wbias	22	Wbias	38	unused (T7)legacy	54	Vqbuff	70	WR_STRB1 TE
7	Trigger Threshold	23	Trigger Threshold	39	unused (T7)legacy	55	VtrimT	71	WR_ADDR_Incr2 LE
8	Wbias	24	Wbias	40	unused (T7)legacy	56	Misc Digital Reg	72	WR_ADDR_Incr2 TE
9	Trigger Threshold	25	Trigger Threshold	41	unused (T7)legacy	57	VadJP	73	WR_STRB2 LE
10	Wbias	26	Wbias	42	unused (T7)legacy	58	VAPbuff	74	WR_STRB2 TE
11	Trigger Threshold	27	Trigger Threshold	43	unused (T7)legacy	59	VadJN	75	MonTiming SEL
12	Wbias	28	Wbias	44	unused (T7)legacy	60	VANbuff	76	SSToutFB
13	Trigger Threshold	29	Trigger Threshold	45	unused (T7)legacy	61	unused (T7)legacy	77	CMPbias2
14	Wbias	30	Wbias	46	unused (T7)legacy	62	Vbias	78	Pubias
15	Trigger Threshold	31	Trigger Threshold	47	unused (T7)legacy	63	TRGGbias	79	CMPbias
16	Wbias	32	Wbias	48	unused (T7)legacy	64	Itbias	80	TPGreg

As noted in the programming chain, there are 3 different types of registered items: a 1-bit register, a 12-bit DAC and a 12-bit buffered output DAC. The 12-bit DACs come in both a unbuffered output, as well as a buffered output version, depending upon whether the DAC needs to drive a significant load. These buffered DACs also have a DAC that controls the strength of the buffer output, which allows for the possibility of disabling the output by powering off the buffer, and overriding the signal external to the ASIC.

The **SGN** bit sets the polarity of the trigger edge for all channels and is held in a 1-bit register. Another 1-bit register selects either the **SSPout** or **SSTout** signals for monitoring of the sampling speed, if that mechanism is chosen. The Gain settings for each channel is a bit more complicated and will be discussed after the 12-bit DAC itself, as well as the meanings and suggested operating values for these biases.

12-bit DACs

A large number of 12-bit DACs are provided for being able to tune a number of adjustable parameters. They are all based upon a class R-2R ladder design, and the typical output response versus DAC code is provided in the figure below. Inset is the transition seem of the most significant bit of the counter. Note that DAC response is inverted with respect to input code: 000000000000b = 2.5V, 111111111111b (4095) = 0.0V.



12-bit DAC Settings

Following sequentially through the programming chain the meaning and suggested operating points/trends of these various settings are discussed in the following pages.

TRGSumbias

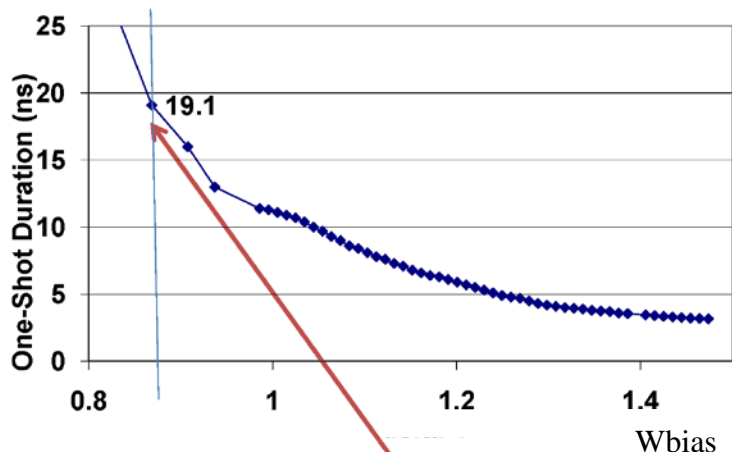
This is the amplifier bias for the Trigger Sum OTA. As it is not driving a heavy load, it need not be driven hard and is governed by the current draw curve for **Vbias**, which is shown on page 7.

TRGbias

This is the amplifier bias for the Trigger Comparator OTA itself. As the circuit is identical to that of TRGSumbias, its response is also shown on page 7.

Wbias

Adjustment of the WBIAS control voltage can be used to tune the 1-shot output width as seen in the figure at left. A comparison with a couple of SPICE reference points indicate that, apart from an observed threshold shift (in part due to level translation offset of an internal buffer amplifier, the same width dependence on WBIAS setting is observed. While narrow output signals can be reliably set, without feedback, temperature dependence is a concern. In future variants the ability to feedback lock using a reference signal will be an important enhancement.



Suggested initial operating point: 20ns = 860mV

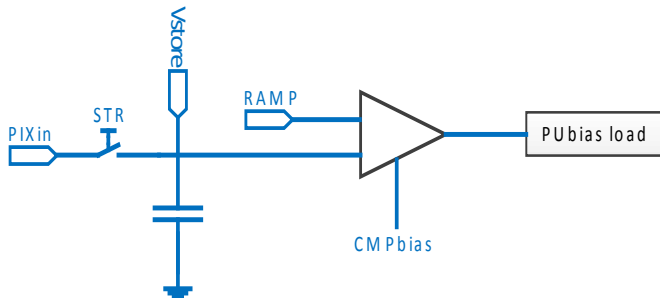
A more comprehensive SPICE simulation of the expected output width as a function of the discharge current, which is independent of the threshold offset observed above.

Temperature Dependence

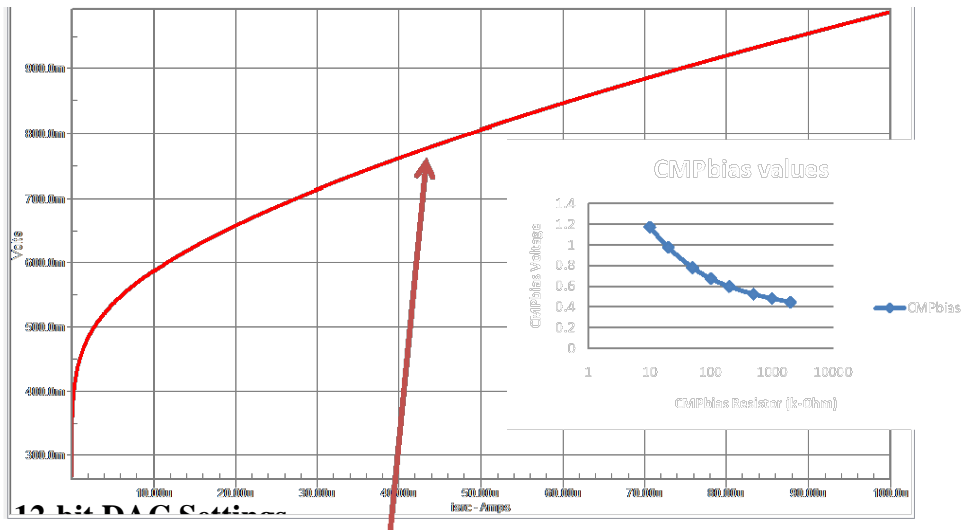
It has been observed that the trigger output width is temperature dependent. Some feedback control is likely to be needed, for which the **TRGin** and **TRGout** (output monitor) signals are provided.

CMPbiasIn (a/k/a CMPbias)

As shown in the circuit at the right is the base storage cell, where two biases work in opposition to each other through the differential pair to compare the V_{store} value with the Ramp voltage. Shout is pulled low to end Wilkinson conversion.



Optimal noise performance is expected to be for about a 4-5x stronger CMPbias than PUBias.



TRGGbias

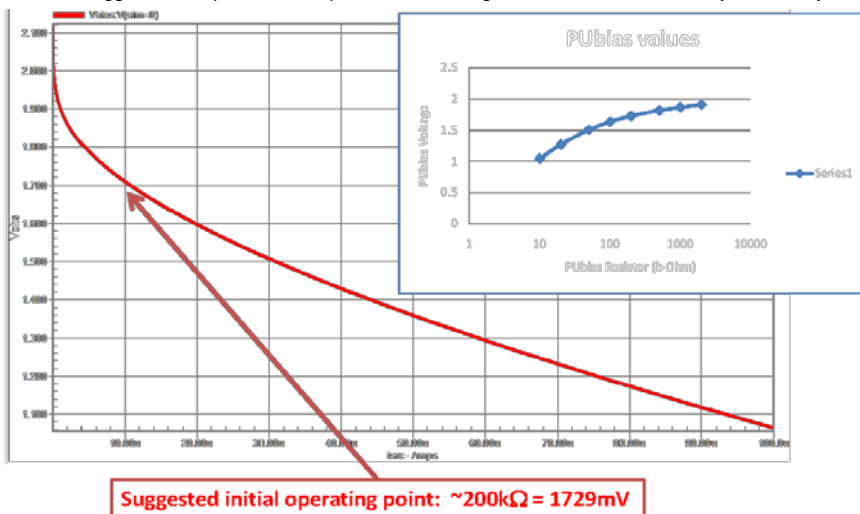
This is the amplifier bias for the Trigger Amplifier OTA, on the input path of every channel. As the circuit is identical to that of TRGSumbias, its response is also shown on page 7.

Sampbias1, Sampbias2 (a/k/a Vbs1, Vbs2)

These are the bias currents for the OTAs that perform the analog gain and transfer as discussed on page 7. For historical reasons they are also known as **Vbs1** and **Vbs2**.

PUBias

As indicated in the diagram on page 14, PUBias works in opposition to CMPbias to enable the differential pair of the compact storage cell to work as a wire-OR ooutput comparator. Something like a 4x-5x stronger CMPbias is suggested for optimum noise performance, though this needs to be studied systematically.



TRGthresh

These thresholds represent the actual thresholds applied to the comparators of the 4 quad trigger outputs, as well the threshold common to all 16 channels.

VdlyN, VdlyP (a/k/a VadjN, VadjP)

These DAC outputs control the sampling timebase adjustment as discussed in detail on page 8.

MonTRGthresh

This DAC sets the monitor trigger channel threshold (typically VDD/2 if using FPGA output as monitor input [TRGin] for continuously monitoring trigger width via TRGout width tracking.

DBbias

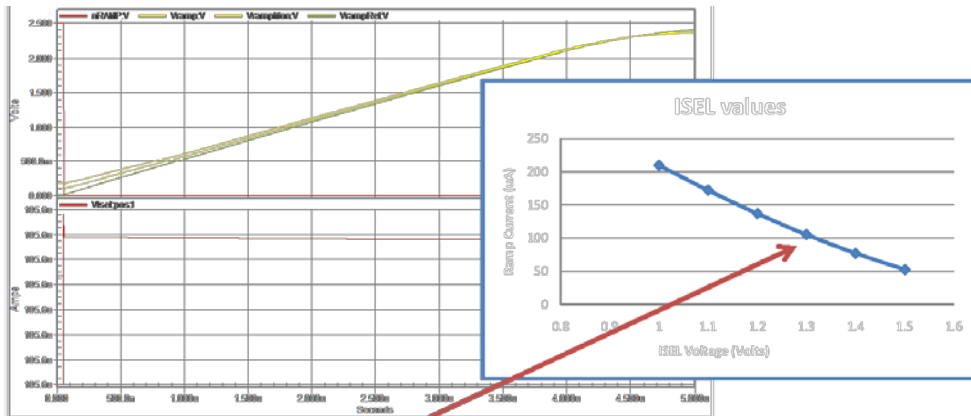
This DAC sets buffered DAC bias strength for the **SBbias**, **IseI** and **Vdischarge** DAC outputs.

SBbias

This DAC sets the SuperBuffer drive strength of the **Vramp** signal fanout.

Isel Voltage Ramp Adjustment and Vdischarge Ramp offset

The Wilkinson ramp slew rate is adjusted by varying the capacitor charging current, denoted **ISEL**, or by changing the ramping capacitor (Cramp). For large values of ISEL, non-linearities in the ramp have been observed. For very fast ramping times, a small capacitor is preferred. A typical value of 200pF is normally used, corresponding to the current values and typical discharge time shown. Note that both the ramp slew rate and Wilkinson clock rate may be adjusted to set the Conversion Gain (mV/count), though with some restrictions. The ramp starting location is set via the **Vdischarge** DAC.

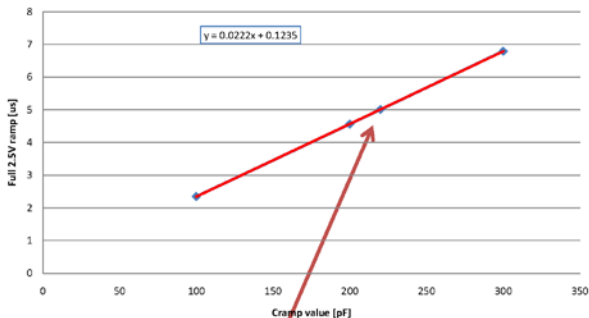


Suggested initial operating point: $\sim 100\mu\text{A} = 1.3\text{V}$

This is the Wilkinson Ramp slope adjustment
Simulation is for 200pF Cramp

Ramping Capacitor [Cramp] dependence

Cramp dependence (ISEL = 1.3V)



Suggested initial operating point: 5us full scale = 220pF

This is the Wilkinson ramp slope adjustment
Quite linear response over this range: 22ns per pF

To complete the discussion of what input ramping capacitance to use, at left is shown the dependence of the full ramping voltage as a function of the Cramp value chosen.

For CTA applications, taking the nominal **ISEL** value set above, about 40pF is the appropriate value for a 1us **Vramp** time.

Storage array addressing

The 64 input samples are partitioned into 2 group of 32 sample writes, which are “ping-ponged” between, allowing continuous sampling. These atomic groups of 32 samples are written into an array that is 512 of such 32 samples deep. Due to wiring restrictions, each input group of 32 samples can only be written to 256 of these 512. This is illustrated in the block diagram on the first page of this datasheet. Another wiring limitation is that the samples are written into the rows in groups, such that bit 0 is not the least significant bit of addressing, though this can be treated as a simple pin redefinition.

Reading is performed completely independently of writing, to allow multi-hit buffering inside the array. Samples in groups of 32 are converted in parallel for each channel. The actual stored analog voltages are left inside the storage cell and interrogated in place, using a very simple and compact comparator inside each storage cell. The rest of the Wilkinson ADC (clock, ramp and counter) are described later, with the 32 registers holding the converted 32 samples is seen at the right of the array.

TARGETX

Single Channel

- Sampling: 64 (2x 32) separate transfer lanes

Recording in one set 32, transferring other (“ping-pong”)

- Storage: 64 x 256 ($256 = 8 * 32$)

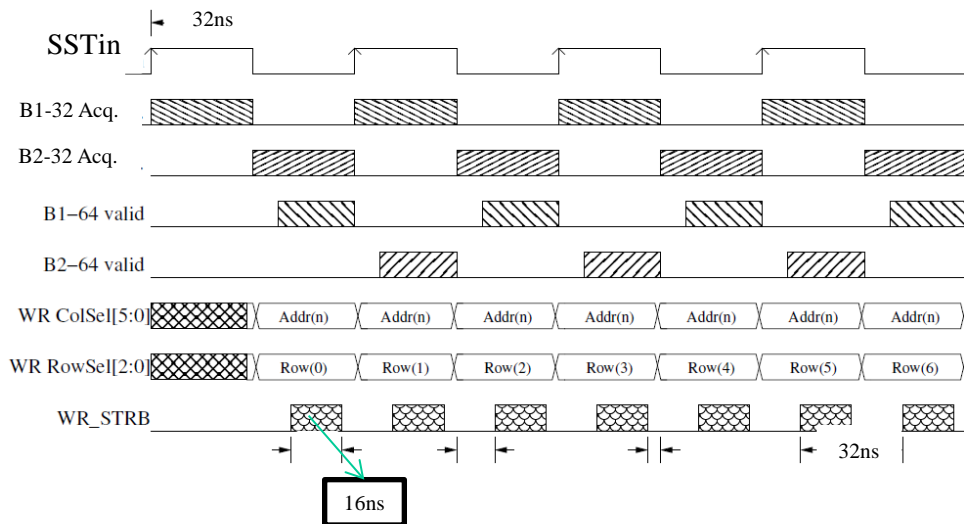
- Wilkinson (32x1):
32 conv/channel

Storage Settling Time

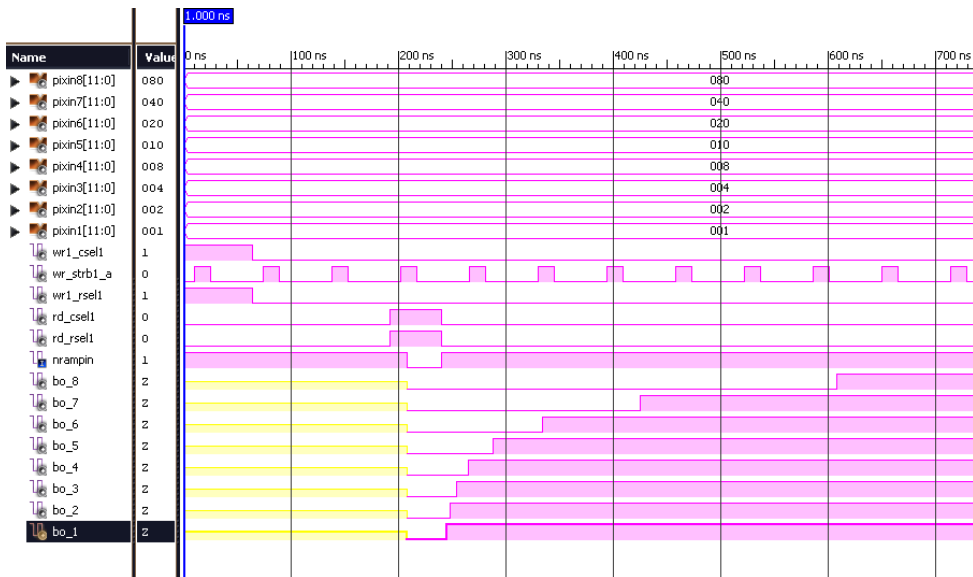
Compared with the analog bandwidth required to couple the analog value into the sampling array, that required for the storage array is greatly reduced. Each buffer amplifier is driving 256 nodes, and simulations indicate settling to 10 bits of resolution in just less than 16ns, which is the value required to run at 4GSa/s continuously, a sampling rate far above the TARGETX capability.

Continuous Sampling

In order to provide seamless sampling, the strobes **SSP_{in}** and **SST_{in}** must be repeated, with a sequential selecting of the Write addresses and transfer of those signals into storage with the Write Strobe (**WR_STRB**) signal. Below is an example timing diagram for acquisition at 1GSa/s.



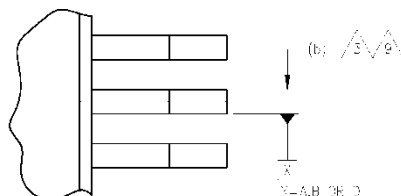
Required state machine



TARGETX Evaluation Board

In order to speed development and to gain experience with using the TARGETX ASIC, an evaluation board is being developed at SLAC....

Package Details (cont'd).



SYM- BO	COMMON DIMENSIONS			NOT E
	MIN.	NOV.	MAX.	
Θ	C"	3.5"	7"	
Θ1	C"	—	—	
Θ2	11"	12"	13"	
Θ3	11"	12"	13"	
C	0.09	—	0.20	11
C'	0.09	—	0.16	11
D2	2.00	—	—	13
F2	2.00	—	—	13
L	0.45	0.60	0.75	
L1	1.00 REF			
R'	0.08	—	—	
R2	0.08	—	0.20	
S	0.20	—	—	

14 X 14	1.00	52	AEA	AEA-FU / AEA-HD
14 X 14	0.80	64	AHB	AHB-FU / AHB-HD
14 X 14	0.55	80	AFC	AFC-FU / AFC-HD
14 X 14	0.50	100	AHD	AHD-FU / AHD-HD
14 X 14	0.40	120	AEE	AEE-FU / AEE-HD

120-pin package relevant variation diagram is AEE.

Needs confirmation!!!

TOLERANCES OF FORM AND POSITION														
SYM- BO	AEC			NOT E	SYM- BO	AED			NOT E	SYM- BO	AEE			NOT E
	MIN.	NOV.	MAX.			MIN.	NOV.	MAX.			MIN.	NOV.	MAX.	
A			1.20	14				1.20	14				1.20	14
A1	0.05		0.15	12		0.05		0.15	12		0.05		0.15	12
A2	0.95	1.00	1.05	14		0.95	1.00	1.05	14		0.95	1.00	1.05	14
b	0.22	0.32	0.38	9,11		0.17	0.22	0.27	9,11		0.13	0.18	0.23	9,11
b1	0.22	0.30	0.35	7		0.17	0.20	0.23	11		0.13	0.16	0.19	7
D	16.00 BSC			4		16.00 BSC			4		16.00 BSC			4
D1	14.00 BSC			5,2		14.00 BSC			5,2		14.00 BSC			5,2
e	0.65 BSC					0.50 BSC					0.40 BSC			
E	16.00 BSC			4		16.00 BSC			4		16.00 BSC			4
F1	14.00 BSC			5,2		14.00 BSC			5,2		14.00 BSC			5,2
N	16.00 BSC					16.00 BSC					16.00 BSC			
TOLERANCES OF FORM AND POSITION														
ccc	0.10					0.08					0.08			
ddd	0.13					0.08					0.07			
NOI	1,8,15					1,8,15					1,8,15			
REF	11-411					11-411					11-411			
ISSUE	A					A					A			

Mechanical drawing details are provided for the leadframe used to package BLAB3A.