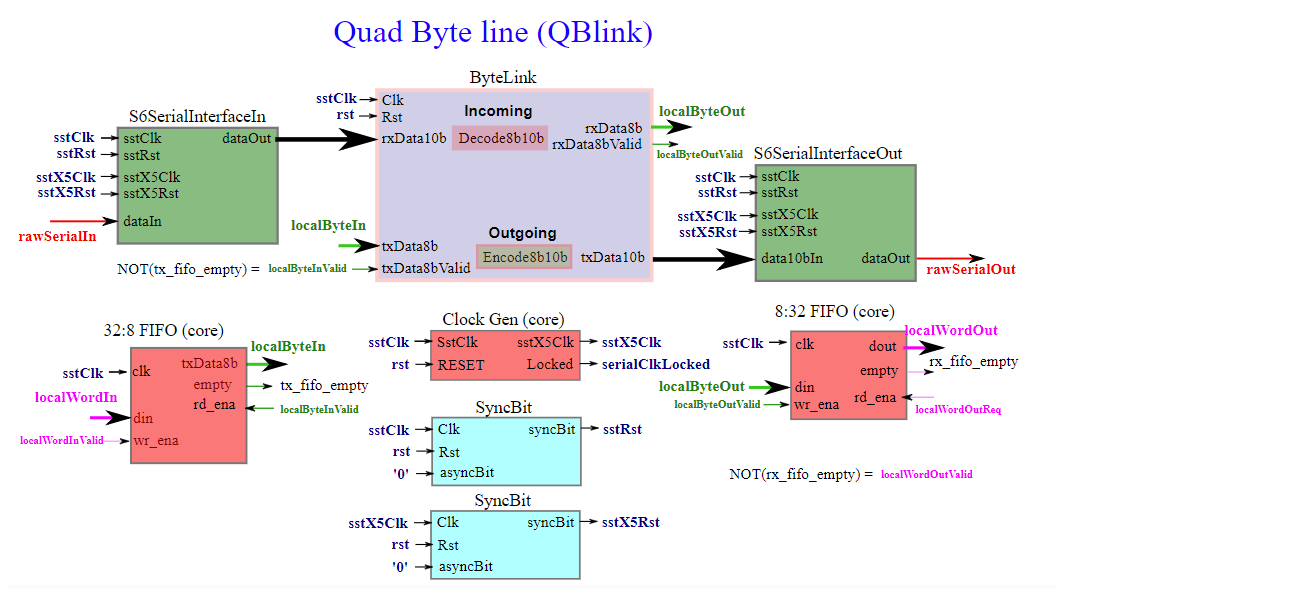
**Hawaii Muon Beamline: Scintillating Tracking Plane Readout**

Nathan Park

**SCROD Firmware**

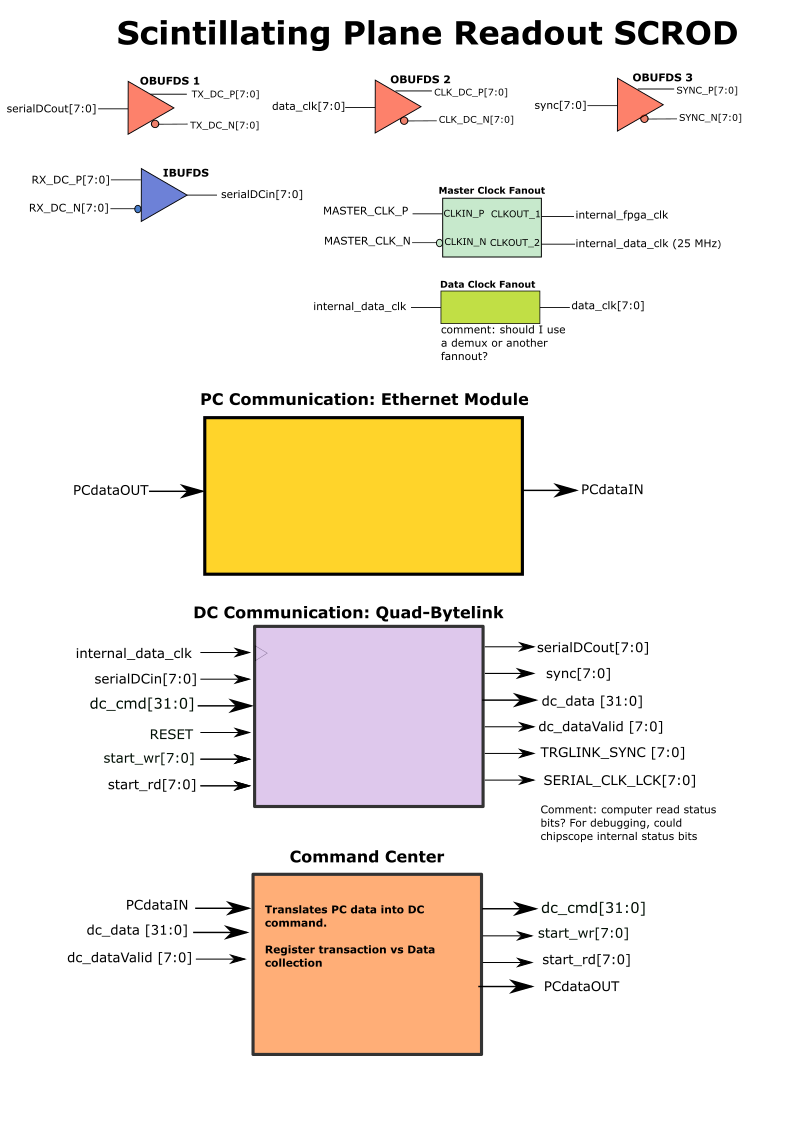
To ensure reliable communication between the SCROD and Daughtercards, a standardized communication protocol called Quad Byte Line (QBLink) was implemented. QBLink was developed by Dr Gary Varner and Dr. Kurtis Nishimura.

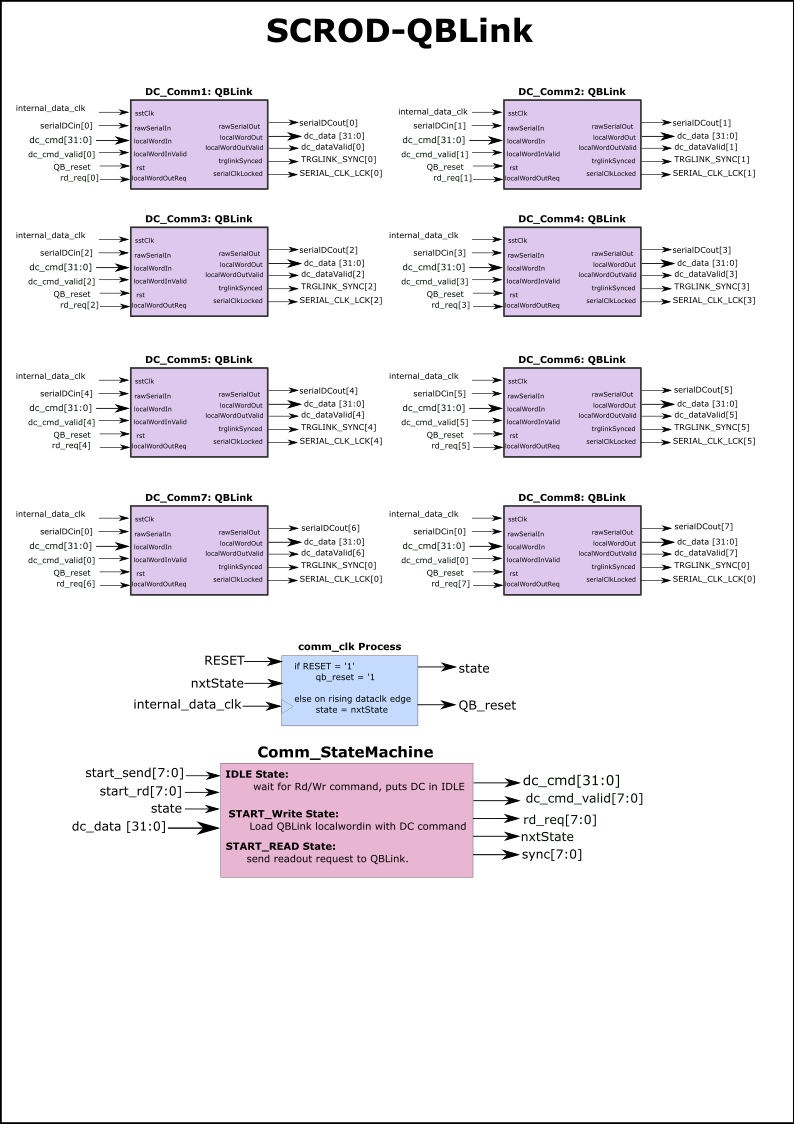


*NOT MINE, NEED TO CITE LATER*

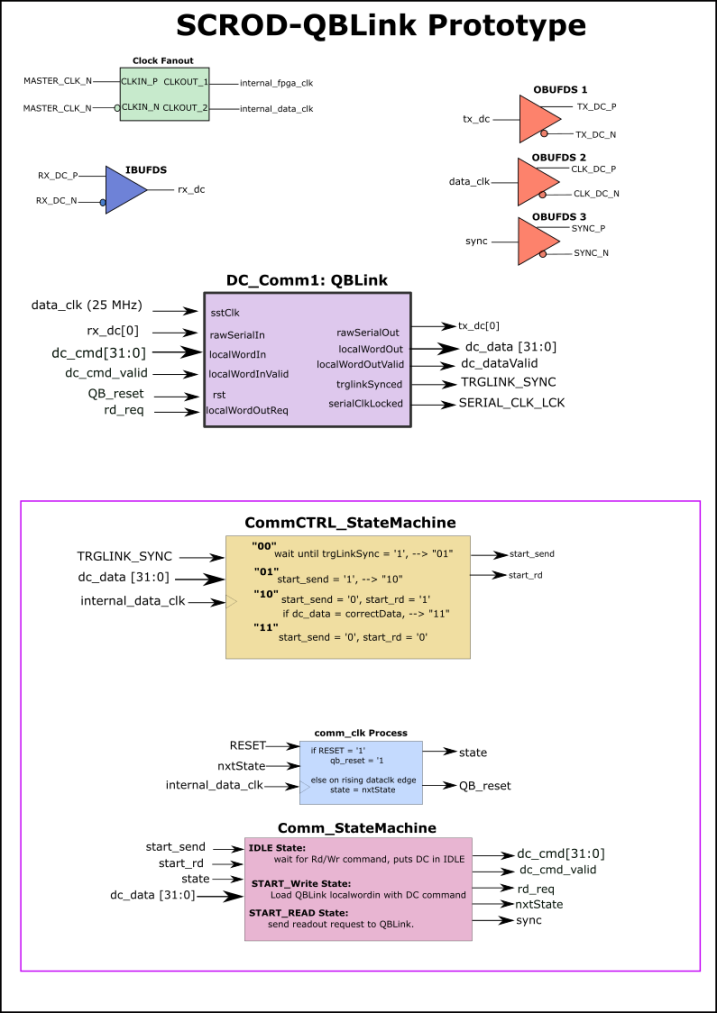
QBLink can transmit and receive 32-bit words simultaneously with another QBLink partner. A transmitted word (localWordIn) is loaded into an input FIFO with localWordInValid. The FIFO sends 8 bits of the word at a time to the ByteLink module, which encodes each byte into a 10-bit word. These 10-bit words are then shifted serially out to the partner (rawSerialOut). QBLink receives data words from its partner, by collecting the serially shifted 10-bit words (raw SerialIn). The collected word is sent to ByteLink to be decoded into an 8-bit word. Four bytes are collected in the output FIFO to recompile the 32-bit word that was sent by the partner. localWordOutReq reads out the FIFO. *A more detailed explanation of the modules and time may be added later.*

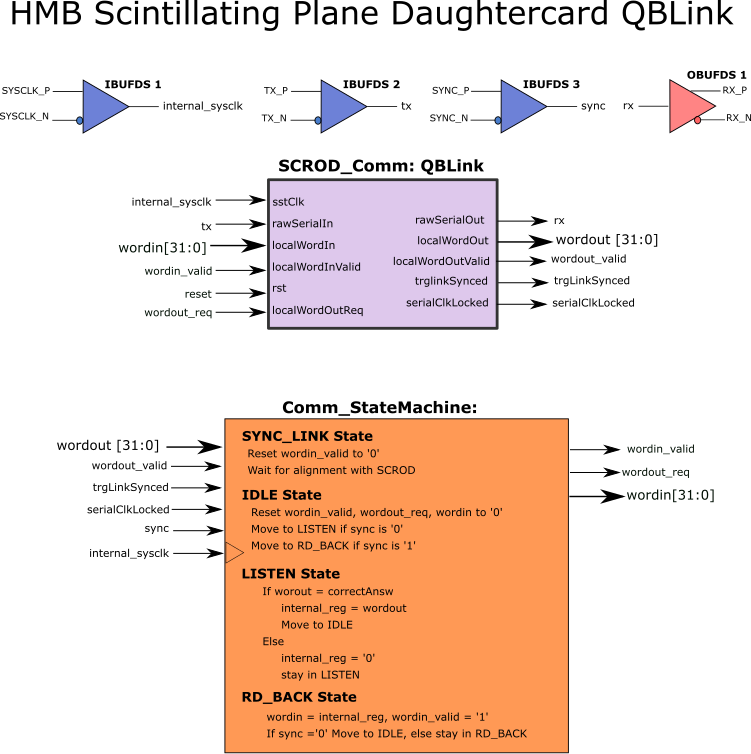
The Scrod has 8 QBLink modules, each serves as a partner for one of the 8 daughercards. The SCROD provides the QBLink clock (data\_clk) to each DC. All serial communication signals are transmitted on differential pairs, so each QBLink output signal goes through a single to differential output buffer. Conversely, each input goes through a differential to single-ended input buffer. The SYNC signal is separate from the QBLink protocol. Its purpose is to synchronize all daughtercards when there is an event.

****

****

**QBLink Implementation Test**

****

****

1. Barebones FW to allow QBLink functionality
2. Simulated register transaction to test QBLink compatibility with SCROD and DC hardware.
3. RJ-45 ports had to be mapped (include diagram of RJ-45 ports, front facing on SCROD and DC, each labeled with proper ref designator.
4. Explain statemachine and register transaction
5. Result: Control statemachine cycled through all states, so write and readback were successful