**Hawaii Muon Beamline Scintillating Tracker Plane Data Acquisition System**

*Technical Report 2018 to 2019*

By: Nathan Park

**1. Introduction**

At the Instrumentation Development Lab (IDLab), the University of Hawaii High Energy Physics group is developing particle detection systems for cutting edge physics research initiatives around the world. As part of this work, the lab must do extensive testing on their new devices. Currently, these tests must be conducted at overseas facilities. Access to these facilities is both costly and very limited. In addition, the need to frequently ship detectors overseas leaves a large carbon footprint from these tests. An in-house testbed would increase the productivity, efficiency, and sustainability of the lab.

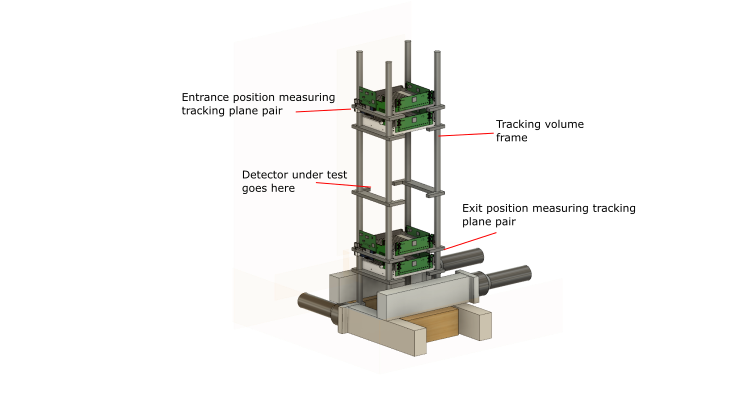
The Hawaii Muon Beamline (HMB) is a particle detector testbed under development at the lab. It would provide a readily accessible means to evaluating and calibrating new detectors, before they are sent to off island research facilities. Unlike most facilities, the HMB does not require an artificial source for particles. It uses naturally occurring cosmic ray muons, which are produced in the Earth’s atmosphere from high energy proton interactions. These robust particles fall towards the ground at near light speed, and are able pass through thick layers of materials without losing energy, making them a reliable source of high energy particles inside the lab. The HMB contains three different detectors that measure various aspects of a muon. The performances of these detectors are used as benchmarks to evaluate the detector-under-test (DUT). This report focuses on one of these detectors, namely the Scintillating Tracker Planes, which measures the trajectories of passing muons [1].

Over the past two years, the HMB mechanical structure has been completed by M.S. Khanh Le, and undergraduate research assistants Zin Jun Lin, Marissa Kurabawa, and Nathan Park. However, the data acquisition system for tracking planes is still under development. This past year, undergraduate research assistants Tommy Lam and Nathan Park revised the system’s electronics hardware and firmware design done by Khanh Le. The aim was to improve the reliability and speed of communication between the master board and the daughtercards interfacing with the detector. This report covers the revised design of the data acquisition system and the status of the HMB project at the end of the 2018 to 2019 academic year.

**2. Hardware**

A light tight chamber houses two pairs of Tracker Planes and the DUT, isolating them from external light that would skew measurements [1]. The two detectors are kept together to ensure they receive the same events under the same experimental conditions. Figure 1. depicts a model of the HMB structure. The top pair of planes measures the entrance position of the muon and the bottom pair measures its exit position. The planes are grouped in pairs to cross validate muon detection. Both planes in a pair must detect a muon in order for there to even be a possibility of an event [1]. For the system to fully recognize a muon event, both planes must detect a muon [1]. Each plane estimates the x-y coordinate position of the muon, as well as its angle of incidence to the planes [1]. When muon passes through a plane it produces light. An array of photosensors locates the area on the plane where the light is the most intense, which corresponds to the position of the muons [1]. The array has two perpendicular branches that sit on the edges of the plane. One branch measures light from the top surface and another branch measures from the bottom surface. Each surface measures along one of the x-y axes.

The photosensor arrays are mounted onto data acquisition circuit boards, called the Daughtercards. Each plane has two Daughtercards, one for each branch of the sensor array. The sensors convert captured light into an electrical signal. The Daughtercards collect, digitize, and store these signals. When the commanded by Standard Controls and Read Out Device (SCROD) master board, the Daughtercards will read their data out to the SCROD. The SCROD then passes the data to a computer (PC). Originally, there would be one SCROD per pair controlling four DCs. Two DCs on the same plane would be daisy chained, with one DC directly connected to the SCROD. Now, one SCROD board will connect to all eight DCs from both the top and bottom planes in parallel. The following sections describe the Daughtercards and SCROD in greater detail.



*Figure 1. CAD model of the HMB Scintillating Tracker Plane mounted on the tracking volume frame.*

**2.1. SCROD Hardware**

The SCROD Rev A5 master board is in charge of receiving commands from the PC, relaying commands to the Daughtercards, and collecting data from the Daughtercards for the PC. Communication between PC and SCROD is maintained through a fiber optic network, while communication between the SCROD and DCs are maintained through RJ45 cables. The main components of the SCROD board include [2]:

1. Gigabit transceiver: interfaces with PC, sends and receive packets of information to and from PC.
2. Xilinx Spartan6 Field Programmable Array (FPGA): parses commands, communicates with Daughtercards, processes data, and sends data to gigabit transceiver.

The SCROD is mounted to an interconnect board, called the SCROD to RJ45 Board. The interconnect board contains a MOLEX power connector for the SCROD and 8 RJ45 ports for connection to 8 tracking plane Daughtercards [3]. The SCROD Rev A5 was designed by Xiaowen Shi and the SCROD to RJ45 Board was designed by Khanh Le.

**2.2. Tracking Plane Daughtercard Hardware**

The Daughtercards (DCs) are responsible for capturing and digitizing muon events seen by the photosensors. The photosensors used are a brand of solid-state silicon photomultipliers, called Hammamatsu Muti-Pixel Photon Counter (MPPC) [1]. Each MPPC is comprised of photodiodes that convert photons into a small amount electric current through the photoelectric effect [1]. The photodiodes contain bound charges that can be excited by photons to become mobile. As these energize charges flow through the diode, they excite other charges, which cause a chain reaction, known as the Avalanche Effect that produces electric current. In order for this to happen, the diodes must be reverse-biased with a sufficiently high voltage source [1]. With a proper bias, the MPPC is capable of detecting single muons, which produce a very small amount of light [1]. The MPPC are most sensitive to light with a wavelength of around 500 nm (green) [1]. Thus, wavelength shifting fibers are placed near the top and bottom surface of the tracking planes to shift the emitted light towards the 500 nm spectrum [1]. These fibersrun parallel to the x/y axis, thus forming the x-y grid used to measure position [1]. Other major components of the DC include [3]:

1. Ultravolt High Voltage: Provides bias for the MPPCs
2. Trim Digital to analog converter (DAC): Sets Ultravolt bias
3. Amplifier stages: Convert MPPC current signals to amplified voltage signals
4. TargetX: Advanced analog to digital converter used to collect, store and digitize MPPC signals
5. Xilinx Spartan6 FPGA: TargetX control, data collection, data readout, and communication with SCROD

The TargetX analog to digital converter (ADC) was designed by Dr. Gary Varner at the IDLab. It converts the electrical signals generated by the MPPCs into digital waveforms that can be plotted and analyzed by the user [1]. It is controlled by the Spartan6 FPGA, which provides all necessary clocks and instructions [1]. The TargetX also helps the DC know when an event has occurred with a digital triggering system. It has 16 trigger bits for each of the 16 MPPC channels. A trigger bit signifies a muon when it is logic ‘1’ (high). Otherwise, there is no muon when the bit is ‘0’ (low). The trigger goes high when the channel voltage surpasses a threshold set by the FPGA. The DC and the SCROD will process these triggers to decide if there’s an event. The Daughtercard board was designed initially by Khanh Le and revised by Tommy Lam.

**3. FPGA Firmware**

The FPGAs are the central processing units on the boards that direct the data acquisition process. This section gives an overview of the firmware implemented on the SCROD and DCs Spartan6 FPGAs. The original firmware, which was written by Khanh Le, was updated by Nathan Park. The update includes several improvements to the firmware structure and functionality. However, the update is still in a prototype phase. The updates need to be integrated with the rest firmware, once the prototype has been fully developed and thoroughly tested. All firmware is written in Very High Speed Integrated Circuits (VHSIC) Hardware Description Language (VHDL).

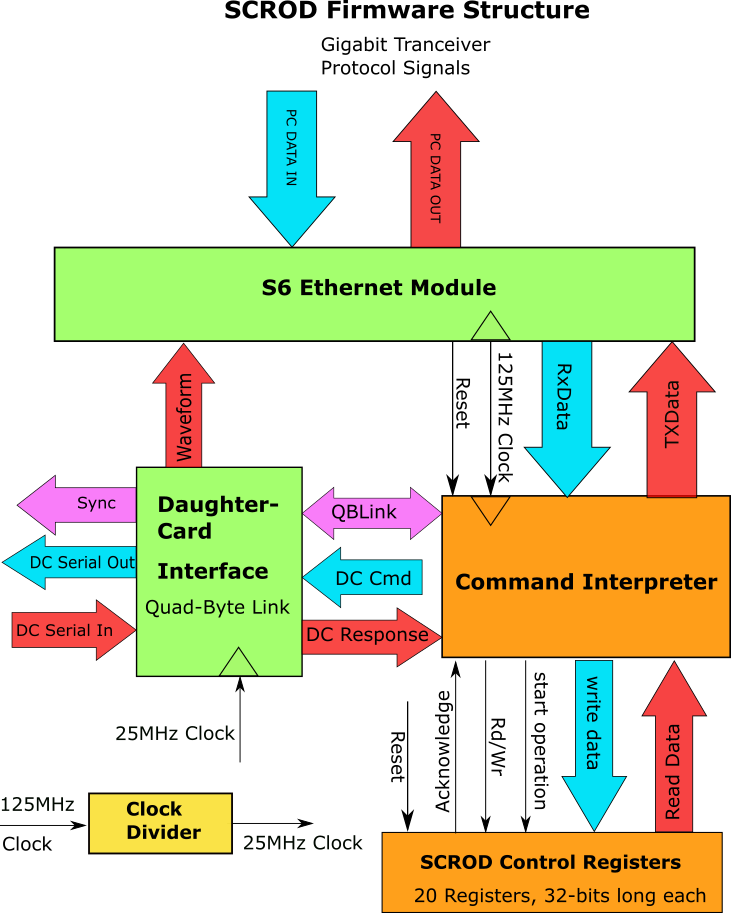
**3.1 SCROD Firmware**

The original SCROD firmware had one large complicated block that was responsible for both command parsing and DC communication. This made it difficult to read and debug. The updated firmware is more modular, isolating major components to make debugging and future updating more tractable. Currently, the firmware is partitioned into three main blocks (see figure 2).

The first block is the S6 Ethernet Module, which interfaces with the gigabit transceiver to collect and transmit packets between the computer and the SCROD. This module was developed by Dr. Kurtis Nishimura, and replaced an older Ethernet Module that was less reliable. The second is the Daughtercard Interface, which is responsible for communicating with the 8 DCs. It is also the port of entry for event data. This unit uses a custom communication protocol, called Quad-Byte Link (QBLink), which was developed by Dr. Gary Varner and Dr. Kurtis Nishimura. The third is the Command Interpreter (CI), which processes command packets received by the Ethernet Module. This module was first developed by Dr. Kurtis Nishimura, and later modified by Dr. Richard Peschke to be compatible with the SCROD Rev A5. The source code for the module was intended for general purpose use. Nathan Park adapted the module to meet needs of the HMB project.

There are four kinds of commands that the CI parses: SCROD Register commands, DC register commands, device pinging, and data readout. Both the SCROD and DC FPGAs have registers that store control settings for the peripheral devices, such as the trim DACs. These registers can be written to and read by the user’s PC through register commands. The user can check if all communication links are established between the PC, SCROD, and DCs with ping commands. Data readout commands are used to extract data from the DCs after the system is triggered by a muon event. The old firmware has existing trigger logic and a data read out command system; however it is not able to full extract waveform data and will need to be revised in light of the changes to the system.

Commands are sent by the PC through Ethernet packets. The packets consist of 32-bit words that must be sent in a certain order so that the CI can parse the command. These words include a header, packet type, device address, command type, and the actual commands themselves. Table 1 and 2 show the formats for register and ping commands. The format is heavily based of that described in the documentation for the S6 Ethernet Module [4].



*Figure 2. SCROD Top Level Block Diagram.*

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | **Table 1. Register Command Packets** | | | |  |
| **Word** | **High Bytes** | | **Low Bytes** | | **Description** |
| 31:25 | 24:16 | 15:8 | 7:0 |
| 0 | 0x00BE11E2 | | | | Header word |
| 1 | packet size | | | | Number of remaining words except packet checksum: 6 |
| 2 | 0x646f6974 | | | | Labels packet as a Register Command |
| 3 | 0x00 | Device label | | Device # | Device labels: (SCROD) 0x00A5, (DC) 0x00DC | Device #: 0x00 (SCROD), 0x01 through 0x08 (DC #) |
| 4 | verbosity (31:24) | Command ID(23:0) | | | Verb(7): suppresses command response. Command ID: unique ID to each command |
| 5 | command type | | | | Ping: 0x70696e67, read: 0x72656164, write: 0x72697465 |
| 6 | Register Value (0x0000 for read operations) | | register address | | Command data |
| 7 | command checksum | | | | sum words 4 through 6 |
| 8 | packet checksum | | | | sum of entire words 0 to 7 |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | **Table 2. Ping Command packets** | | | |  |
| **Word** | **High Bytes** | | **Low Bytes** | | **Description** |
| 31:25 | 24:16 | 15:8 | 7:0 |
| 0 | 0x00BE11E2 | | | | Header word |
| 1 | packet size | | | | Number of remaining words except packet checksum: 6 |
| 2 | 0x646f6974 | | | | packet type: device configuration |
| 3 | 0x00 | Device label | | Device # | Device labels: (SCROD) 0x00A5, (DC) 0x00DC | Device #: 0x00 (SCROD), 0x01 through 0x08 (DC #) |
| 4 | verbosity (31:24) | Command ID(23:0) | | | Verb(7): suppresses command response. Command ID: unique ID to each command |
| 5 | 0x70696e67 | | | | Command Type: Ping |
| 6 | command checksum | | | | sum words 4 through 6 |
| 7 | packet checksum | | | | sum of entire words 0 to 7 |

The packet formatting is set in the CI firmware, which has a state machine that checks each word for errors and decides what action the SCROD will take. Nathan Park designed the device address format (word 3) so that Interpreter will distinguish between SCROD and Daughtercard targets. The original CI was designed to only handle SCROD commands. Nathan expanded the functionality of the CI, enabling it to pass commands to the Daughtercards through the Daughtercard Interface and QBLink.

The control registers on the SCROD are written to by a register programming process located at the top level. The CI sets the ‘Rd/wr’ flag that either puts the process in read mode or write mode, and passes the register value and address specified by the command packet. If in write mode, the process assigns the register value to the addressed register. If in read mode, the process reads the addressed register to the CI. The CI then reads that value back to the PC. A ‘Start Operation’ enable flag is raised by the CI to initiate a register operation. The process raises an ‘Acknowledge’ flag to signify it received the command. A major concern was whether the CI could be compatible with the old firmware’s register architecture. After designing the register programmer, Nathan ran tests to see if he could write and read back registers from a PC, and he did so successfully.

The Daughtercard Interface (DCI) is designed to have 8 QBLink modules, one for each DC. To pass a command to a daughter card, the CI selects the proper QBLink module on the DCI and passes the command word to the module. QBLink then sends the command to its DC. Figure # shows the internal block diagram of the DCI.

**3.2 Daughtercard Firmware**

A fully functioning Daughtercard contains the following firmware functional blocks:

1. Communication with the SCROD
2. Command Interpreter
3. Trim DAC controller
4. TargetX Interface
5. Event trigger logic
6. Registers to store control settings for the TargetX, trigger logic, MPPC biasing, and trim DACs

A QBLink module satisfies the first requirement. A simple message was sent from the SCROD to the Daughtercard and read back to the SCROD to verify that the two boards can communicate. Then, a Command Interpreter was designed so that it would directly handle register programming. Currently, we are testing register operations on the Daughtercard. An issue has come up with the fiber optic media converter that prevents us from establishing a link between the computer and the SCROD. The converter network has to be reconfigured on the PC in order to function again. Khanh’s old firmware has discrete modules for TargetX control, trim DAC control, and trigger logic. It seems promising that these modules can be integrated with the new Command Interpreter with minimal revision.

**4. Project Status and Future Work**

The communication links between the PC, SCROD, and Daughtercards are crucial components to the HMB Scintillating Tracking Plane data acquisition system. Prior to this year, these links were not very reliable. The old PC-SCROD Ethernet module would often time out, requiring the whole system to be reset periodically. This would result in loss of data. Also, the old Ethernet module had poor documentation and was unfamiliar to most of the current lab members. In addition, the parsing of PC commands, communication with the DCs and processing of event data were all entangled in one block inside the SCROD FPGA, making it very difficult to make progress on the firmware. The improvements made to the firmware will ensure we have robust communication links and a more organized firmware structure.

The next milestones for the project are to reconfigure the fiber optic network, complete the DC register programming test, and integrate the missing functional blocks to the DC. Once these tasks are achieved, the event handling system for the SCROD will need to be redesigned.

**5. Conclusion**

The Instrumentation Development lab is involved in groundbreaking physics research. The Hawaii Muon Beamline is a crucial tool to accelerate our progress. The Scintillating Tracker Plane detector is one of the key components of this new testbed, and it is near its completion. Opportunities are abound at HMB for electrical engineering students to test their skills in developing the next generation of particle detection systems.

**References**

[1] K. Le, “Enhanced Scintillating Tracker for Evaluating the 2nd Generation Borehole Muon Detector at the Hawaii Muon Beamline”. Master’s Thesis. UH Manoa Grad. Div., Honolulu, April 2018. Accessed on: April 30, 2019 [PDF].

[2] X. Shi, “SCROD Rev A5.” Schematic. Dept. of Phys., HEPG IDLab, UH Manoa, Honolulu, Jan. 2015. Accessed on: April 30, 2019 [PDF]. Available at: <https://www.phys.hawaii.edu/~idlab/taskAndSchedule/PCBs/SCROD_RevA5/SCROD.revA5.KLM.sch.pdf>

[3] K. Le, “SCROD\_RJ45\_Conn\_Board.”Schematic. Dept. of Phys., HEPG IDLab, UH Manoa, Honolulu, May 2017. Accessed on: April 30, 2019 [PDF]. Available at: <https://www.phys.hawaii.edu/~idlab/taskAndSchedule/PCBs/SCROD_RJ45_CONN_BOARD/SCROD_TO_RJ45_BOARD.PDF>

[4] K. Nishimura. “Raw Data Formats for the Imaging Time-of-Propagation (iTOP) Electronics.” Dept. of Phys., HEPG, UH Manoa, Honolulu. Accessed on: Apri 30, 2019. [Web] Available at: <https://www.phys.hawaii.edu/~kurtisn/doku.php?id=itop:documentation:data_format>