Contents

1 Objective

The main objective of this experiment is design and analysis of a 2-stage opamp.The designed op-amp should have the following specifications:

- A_v = 2000
- GBW=15 Mhz
- C_L = 10 pF
- ICMR=0.8V-1.6V
- Slew Rate=10V/µS

2 Specifications

- Mosfet length of 180nm
- A bias current of 40µA is assumed.
- A voltage supply of 1.8V is used.

3 Two stage Operational Amplifier

A two-stage operational amplifier consists of a differential amplifier at the. input stage, while the second stage is a high gain stage biased by the output of the differential amplifier.The first stage is a differential pair with a current mirror load. The second stage is a common source amplifier. Use a simple current source with a diode-connected PMOS load as the bias circuit.The basic circuit is shown in [Figure 1].

Gain of 1st stage:

$$A_{v1} = -g_{m1,2}(r_{o2}||r_{o4}) \tag{1}$$

Gain of 2nd stage:

$$A_{v2} = -g_{m6}(r_{o6}||r_{o7}) \tag{2}$$

Overall gain of two stage:

$$A_v = A_{v1}A_{v2} = g_{m1,2}g_{m6}(r_{o2}||r_{o4})(r_{o6}||r_{o7}) \tag{3}$$

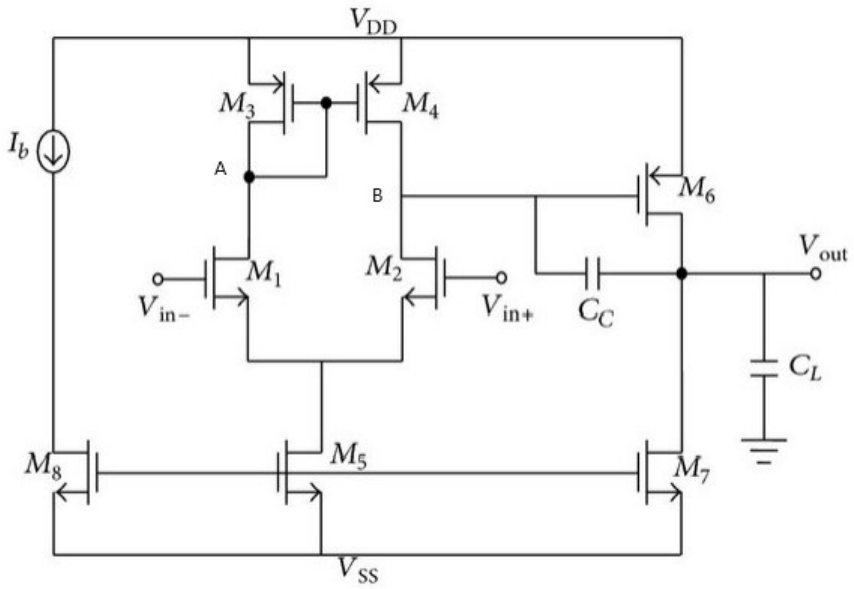

Figure 1: Typical circuit for 2 stage OTA

If we look into node A,we see that:

$$r_{oA} = r_{o3}||r_{o1}||\frac{1}{g_{m3}} \approx \frac{1}{g_{m3}}$$

which is a very low value.Now we consider the nodes B and C.

$$R_1 = r_{o2}||r_{o4}$$

$$R_2 = (r_{o6}||r_{o7})$$

from the above small signal model we get

$$P_1 \approx \frac{-1}{R_1 R_2 g_{m6} C_c}$$

$$P_2 \approx \frac{-g_{m6}}{C_1 + C_2}$$

Thus as we increase C_c , P_1 moves closer to origin and thus pole splitting happens and compared to case without capacitor we will get stable value of phase margin near around 60 degree.

For stability purpose:

$$\omega gc < \omega pc \tag{4}$$

4 Design Specification and Calculations

The various steps involved in designing the circuit are listed below:

1. for a PM of 60 degree, we choose C_c such that

   $$C_c > 0.22 C_L \tag{5}$$

   here C_L is given as 10pF, putting this in above equation we get

   $$C_c > 2.2pF \tag{6}$$

   Assume $C_c = 2.5pF$

2. We know slew rate is given by,

   $$SR = \frac{dV_{out}}{dt} = I_5 C_c \tag{7}$$

   Putting values of SR and C_c we get,

   $$I_5 = 25\mu A \tag{8}$$

3. Design for S3 from the maximum input voltage specification

   $$S_3 = \frac{I_5}{K_p (V_{DD} - V_{in-max} - |V_{T3}| + V_{T1-min})^2} \tag{9}$$

where $K_p = 70\mu A/V^2$, $V_{T3} = -0.43V$

$$\frac{W_3}{L_3} = \frac{W_4}{L_4} = 4.89 \tag{10}$$

$$W_3 = W_4 = 880.2nm \tag{11}$$

4. Verify that the pole of M3 due to C_{gs3} and $C_{gs4} = 0.67W3L3Cox$ will not be dominant by assuming it to be greater than 10 GB

$$\frac{g_{m3}}{2g_{s3}} > 10GB \tag{12}$$

5. Design for S1(S2) to achieve the desired GB.

$$g_{m1} = GB * C_c = 235.62\mu A/V^2 \tag{13}$$

$$\frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{g_{m1}^2}{2K_nI_1} \tag{14}$$

$$S_1 = S_2 = 8.224 \tag{15}$$

$$W_1 = W_2 = 1480.32nm \tag{16}$$

6. Using the min ICMR equation with reference to the given circuit, we get the value of V_{sat5} as :

$$V_{dsat5} = V_{in,min} - V_{gs1} - V_{ss}$$

$$V_{dsat5} = V_{in,min} - \sqrt{\frac{2I_{d1}}{\mu_n C_{ox}\frac{W_1}{L_1}}} - V_{tn1} - V_{ss}$$

Putting the necessary values we get,

$$V_{dsat5} = V_{gs5} - V_{t5} = 0.235V \tag{17}$$

Now we substituing these values in current equation for NMOS transistor M5 we get the value of W-L ratio for M5 as ,

$$\frac{W_5}{L_5} = 3.533 \tag{18}$$

$$W_5 = 603.54nm \tag{19}$$

7. Find S6 by letting the second pole (p2) be equal to 2.2 times GB and assuming that $V_{SG4} = V_{SG6}$.

$$\frac{W_6}{L_6} = \frac{W_4}{L_4}\frac{g_{m6}}{g_{m4}} \tag{20}$$

$$S_6 = 124.66 \tag{21}$$

$$W_6 = 31320nm \tag{22}$$

8. Calculate I_6 from

$$I_6 = \frac{g_{m6}^2}{2k_6 S_6} \tag{23}$$

$$I_6 = 318.1\mu A \tag{24}$$

9. Design S7 to achieve the desired current ratios between I_5 and I_6

$$S_7 = (I_6/I_5)S_5 = 42.663 \tag{25}$$

$$W_7 = 7679.34nm \tag{26}$$

Putting this result in the below relation we get

$$\frac{W_8}{L_8} = \frac{W_5}{L_5}\frac{I_{d8}}{I_{d5}} \tag{27}$$

$$\frac{W_8}{L_8} = 5.36 \tag{28}$$

5 Schematics and output

5.1 Miller compensation technique

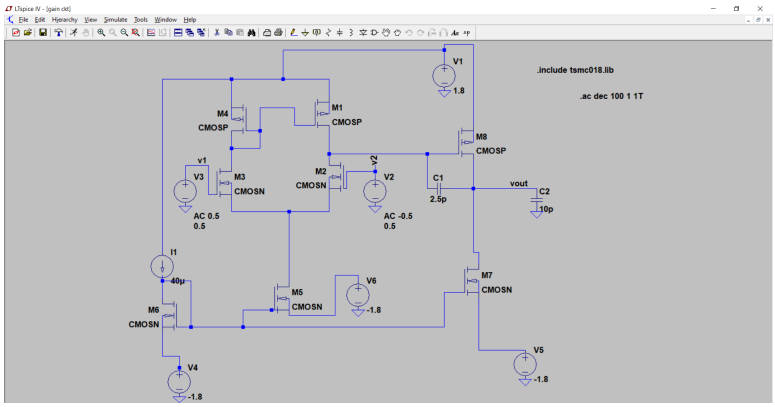

Figure 2: Schematic

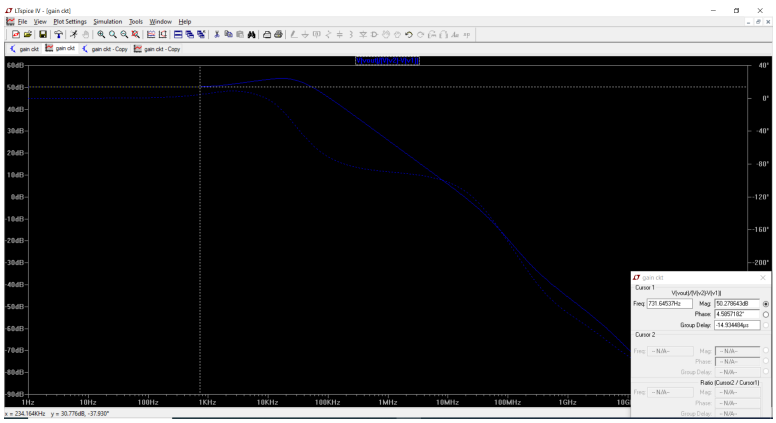

Figure 3: Gain

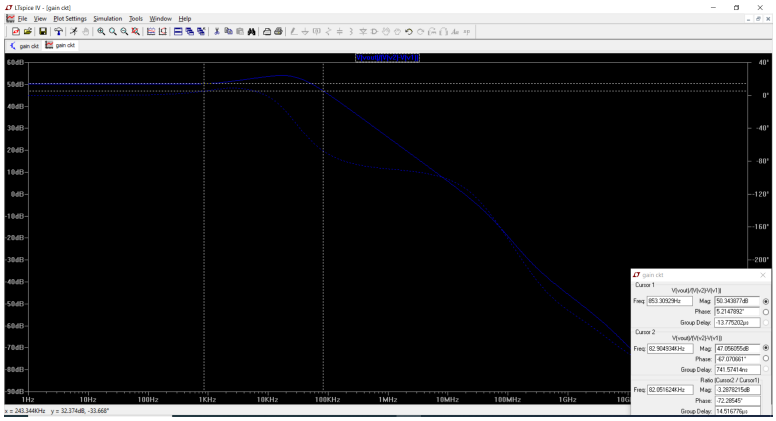

Figure 4: 3 dB frequency

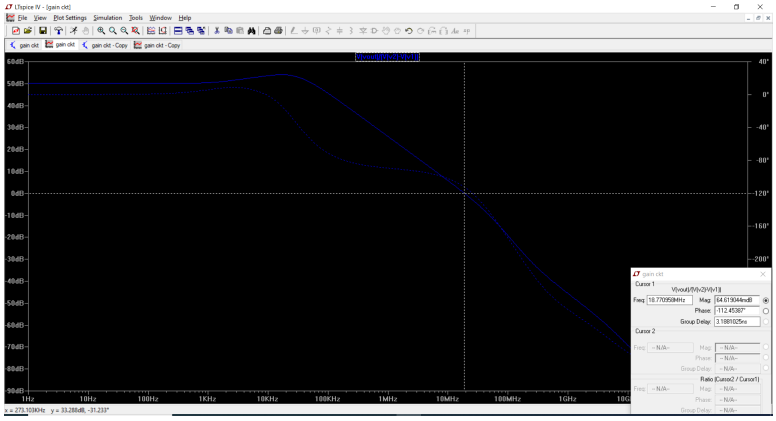

Figure 5: phase at gain crossover frequency

5.2 Nulling resistor compensation

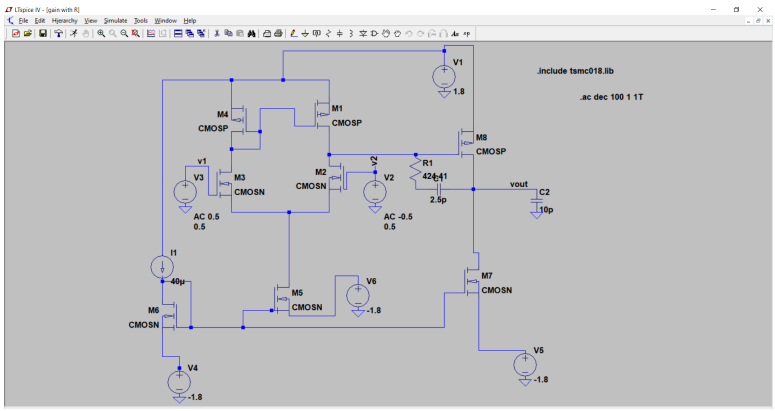

Figure 6: Schematic

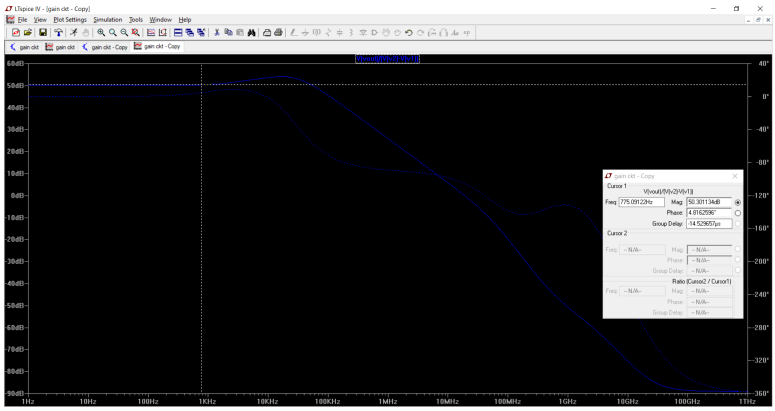

Figure 7: Gain

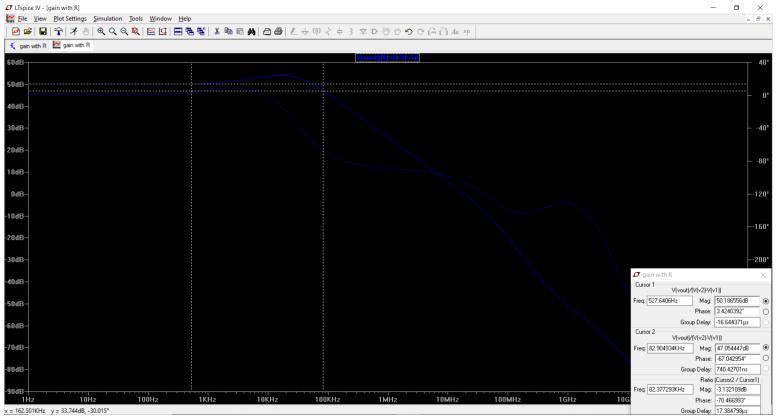

Figure 8: 3 dB frequency

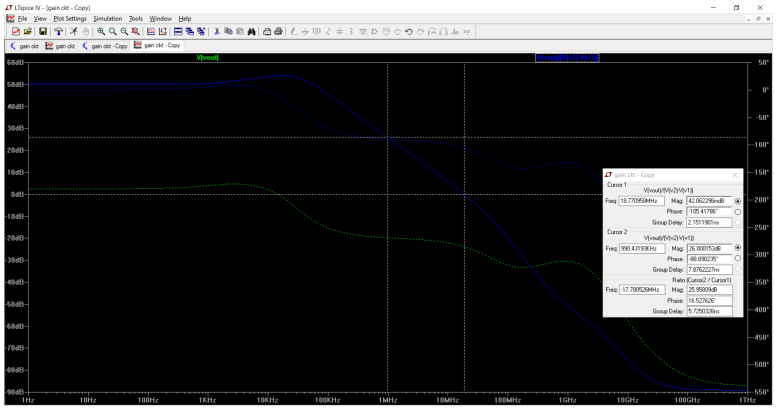

Figure 9: phase at gain crossover frequency

5.3 2 stage without feedback

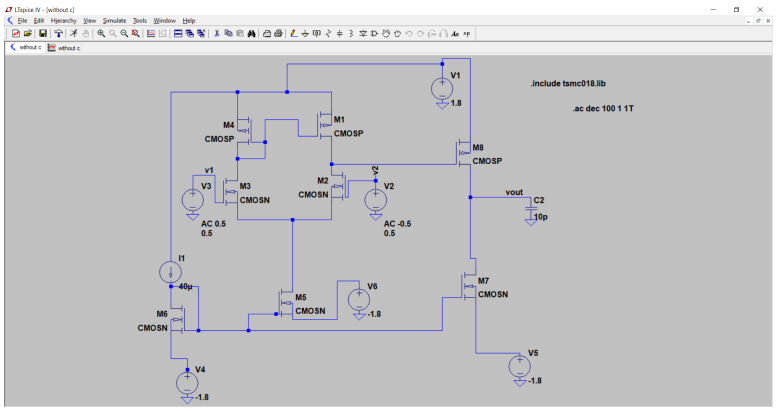

Figure 10: Schematic

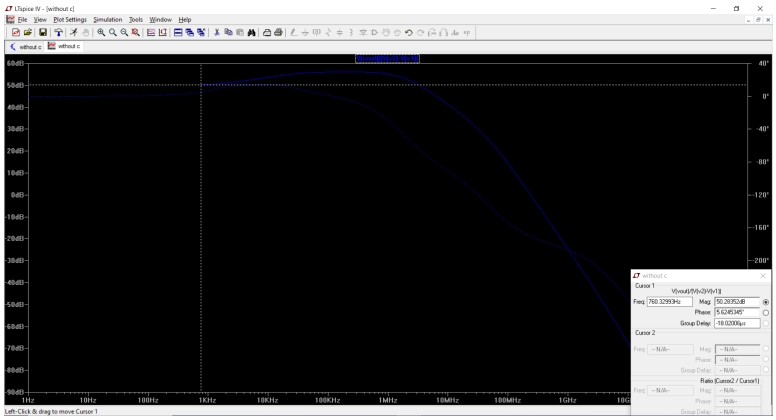

Figure 11: Gain

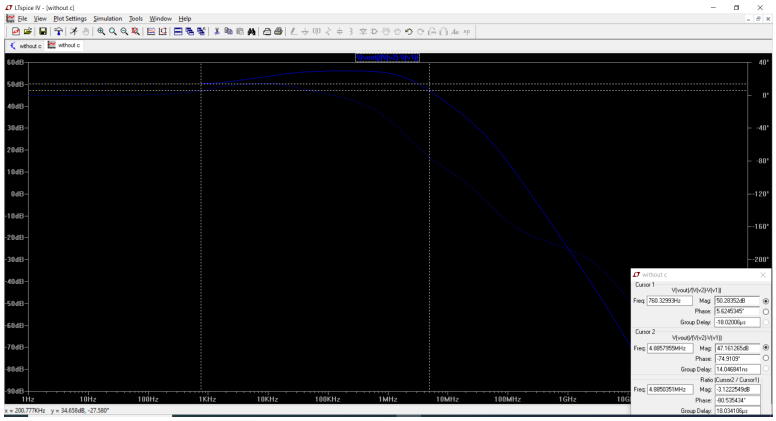

Figure 12: 3 dB frequency

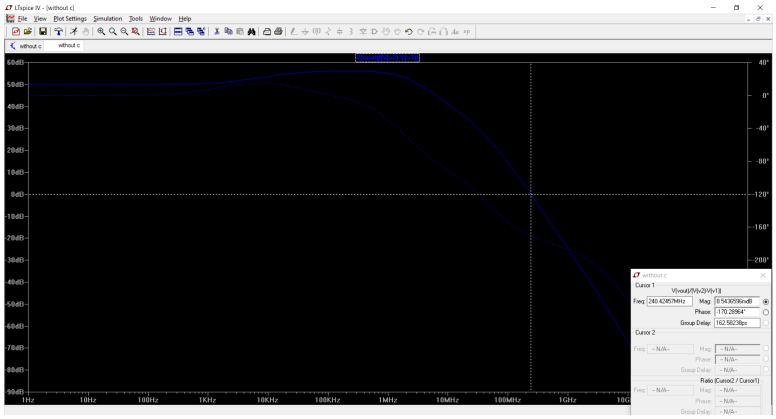

Figure 13: phase at gain crossover frequency

6 Observation

W/L ratios for all transistors							
M_1	M_2	M_3	M_4	M_5	M_6	M_7	M_8
8.224	8.224	4.89	124.66	3.353	124.66	42.663	5.364

Table 1:

- Value of nulling resistance
  $R_2 = \frac{1}{gm2}$
  $R_2 = \frac{1}{2356.2*10^{-6}}$
  $R_2 = 424.41\Omega$

- There is no effect on the gain of the circuit in all 3 methods
  Ideal gain =20 log(2000)=66 dB

Gain in dB		
Miller capacitance	Nulling resistor	2 stage without feedback
50.27 dB	50.30 dB	50.28 dB

Table 2:

BW in dB	
Miller capacitance	Nulling resistor
82.90 KHz	82.9 KHz

Table 3:

- PM with miller approximation
  PM= 180 °+(-112.45°) =67.55°

- PM with nulling resistance compensation
  PM= 180 °+(-105.41°) =74.59°

- Phase margin is higher in nulling resistance compensation technique ,hence stability is higher.

- PM without compensation capacitor
  180°+(-170°)=10 °hence the stability is less.

7 Results

7.1 Miller compensation technique

- Gain =50.27dB
- Bandwidth=82.90 Khz
- Phase at Gain crossover frequency = -112.45°
  PM=67.55 °

7.2 Nulling resistance technique

- Gain=50.30dB
- Bandwidth=82.9 Khz
- Phase at Gain crossover frequency = -105.41°
  PM=74.59 °

7.3 2 stage without feedback

- Gain=50.28 dB
- Bandwidth= 4.88 Mhz
- Phase at Gain crossover frequency = -170°
  PM=10°

8 Conclusion

- The compensation capacitor helps in pole splitting.
- Pole splitting shifts the one pole (less dominant) to the right of unity gain bandwidth frequency and dominant pole to the left.
- Because of pole splitting because of dominant pole the transfer function is like a single pole system.
- The compensation capacitor adds a right half plane zero to the system.

- The RHP zero decreases the phase margin of the system,hence decreasing the stability.
- The power consumption for miller compensation is high.
- So to improve the phase margin and hence improve stability we used a resistor in series with compensation capacitance.
- Adding series resistance reduces the need of selecting high gm ,reducing current,in turn reducing power consumption,
- The 2 stage Op-amp circuit offers high gain.
- The 2 stage Op-amp circuit has higher output voltage swing than OTA.
- The 2 stage Op-amp circuit with miller compensation technique has higher power dissipation than an OTA as gm of mosfet where output is taken has to be approximately 10 times than the gm on mosfet where input is given.
- The Op-amp with desired design specifications was designed.