

DIGITAL SYSTEM DESIGN

ACTIVITY-I

NAME - Devleena Kumari

Roll No. - 2405051

Q1) Implement half adder using data flow modeling in verilog HDL. Hence implement a full adder by calling the half adder module in verilog HDL.

Write the test bench for each of the cases. Show the RTL schematics and output waveforms of half and full adder.

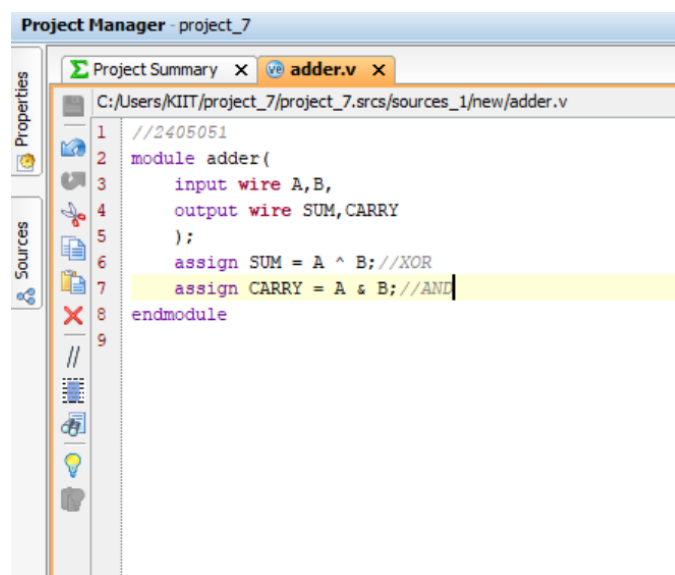
Solution:-

HALF ADDER:-

Truth Table:-

A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

HDL CODE:-



```
Project Manager - project_7
Project Summary x adder.v x
C:/Users/KIIT/project_7/project_7.srscs/sources_1/new/adder.v
1 //2405051
2 module adder(
3     input wire A,B,
4     output wire SUM,CARRY
5 );
6     assign SUM = A ^ B; //XOR
7     assign CARRY = A & B; //AND
8 endmodule
9
```

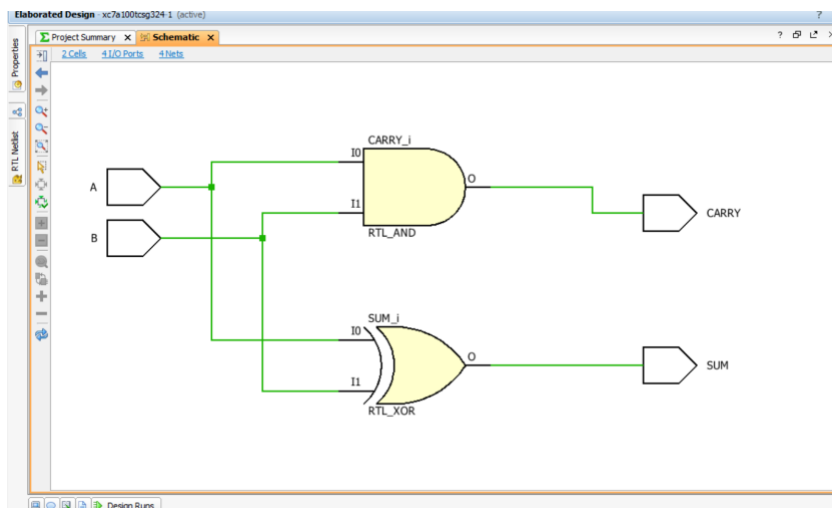
TESTBENCH:-

```
Project Manager - project_7

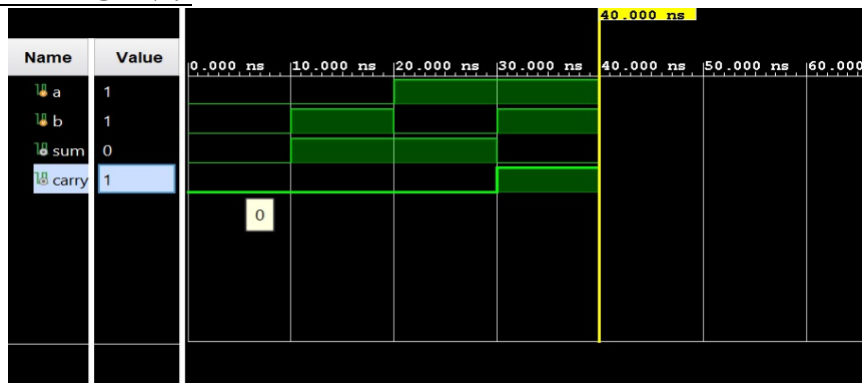
Project Summary x adder.v x adder_test.v x
C:/Users/KIIT/project_7/project_7.srscs/sim_1/new/adder_test.v

1 //2405051
2 module adder_test( );
3     reg A,B;
4     wire SUM,CARRY;
5     adder dut(A,B,SUM,CARRY);
6     initial begin
7         A=0;B=0;#10;
8         A=0;B=1;#10;
9         A=1;B=0;#10;
10        A=1;B=1;#10;
11        $finish;
12    end
13 endmodule
14
```

SCHEMATIC:-



WAVEFORM:-

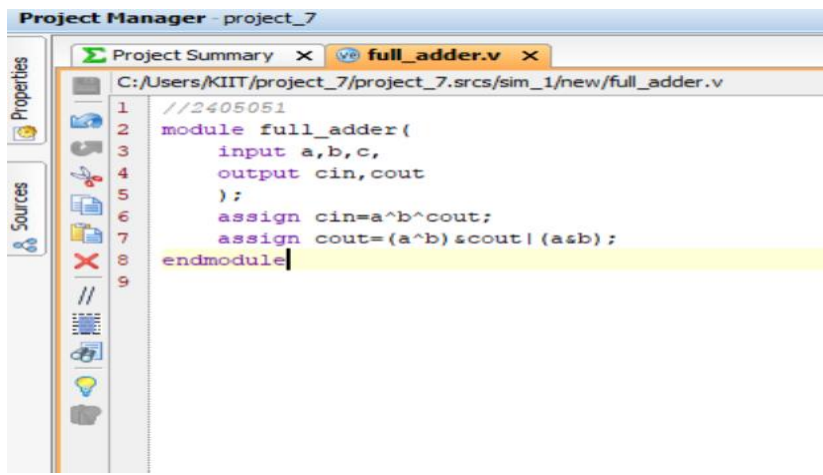


FULL ADDER:-

Truth Table:-

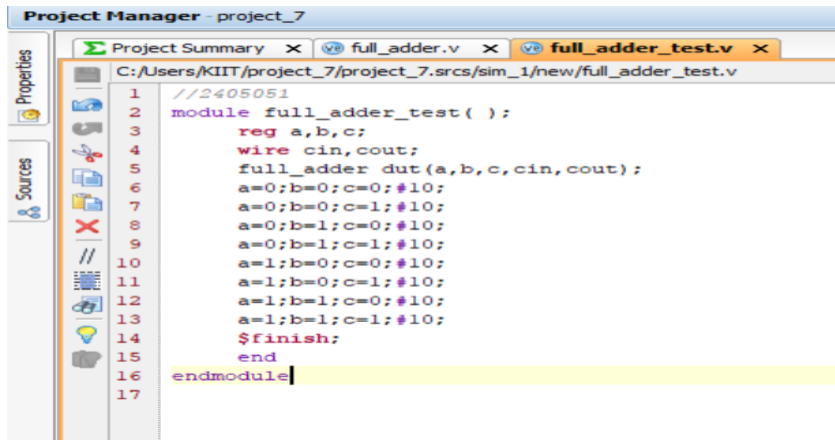
a	b	c	cin	cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

HDL CODE:-



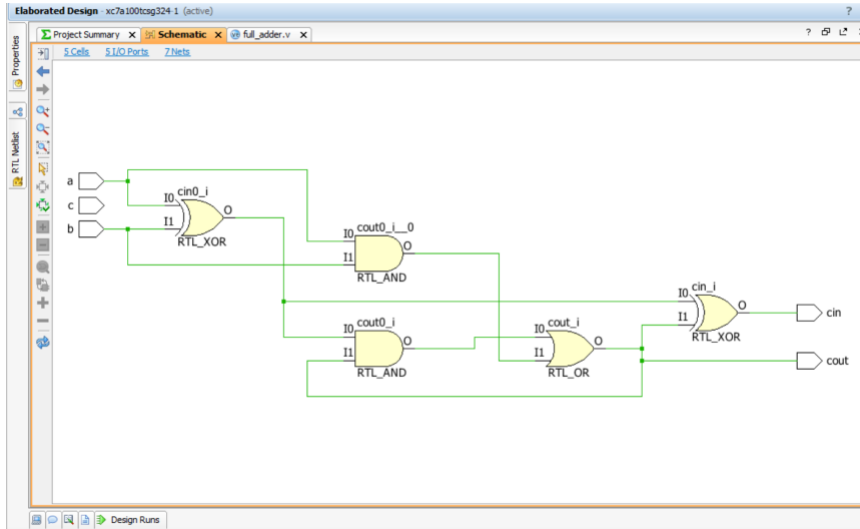
```
1 //2405051
2 module full_adder(
3     input a,b,c,
4     output cin,cout
5 );
6     assign cin=a^b^cout;
7     assign cout=(a^b)&cout|(a&b);
8 endmodule
9
```

TESTBENCH:-

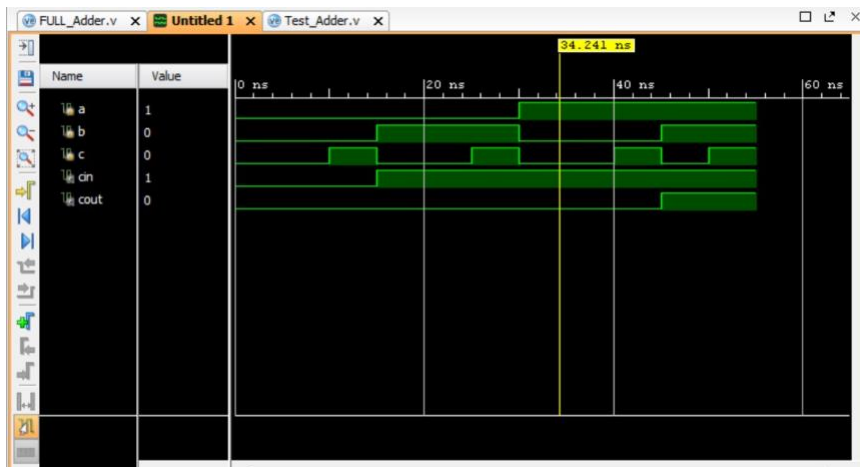


```
1 //2405051
2 module full_adder_test( );
3     reg a,b,c;
4     wire cin,cout;
5     full_adder dut(a,b,c,cin,cout);
6     a=0;b=0;c=0;#10;
7     a=0;b=0;c=1;#10;
8     a=0;b=1;c=0;#10;
9     a=0;b=1;c=1;#10;
10    a=1;b=0;c=0;#10;
11    a=1;b=0;c=1;#10;
12    a=1;b=1;c=0;#10;
13    a=1;b=1;c=1;#10;
14    $finish;
15 end
16 endmodule
17
```

SCHEMATIC:-



WAVEFORM:-



Q2) Implement a 3 to 8 line decoder in verilog HDL. Consider $F(P,Q,R) = \sum(\text{All digits of your roll number upto digit 7})$, and ignore the repetition. Implement the function using 3 to 8 line decoder using verilog HDL.

Solution:-

Digits in Roll no.2405051 ----> {2,4,0,5,0,5,1}

----> unique set {0,1,2,4,5}

Therefore: $F(P,Q,R) = \sum m(0,1,2,4,5)$
(assume order P = MSB , R=LSB)

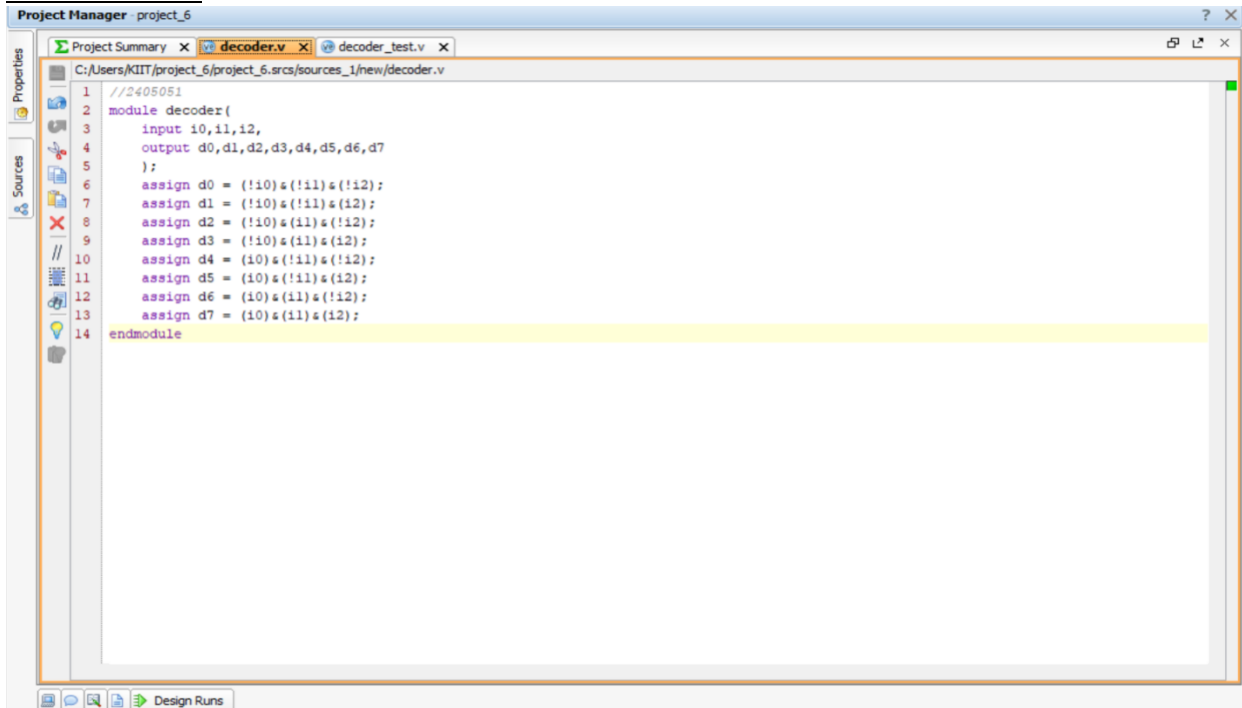
TRUTH TABLE:-

P	Q	R	minterm	F
0	0	0	0	1
0	0	1	1	1
0	1	0	2	1
0	1	1	3	0
1	0	0	4	1
1	0	1	5	1
1	1	0	6	0
1	1	1	7	0

(Checks : F=1 exactly for 0,1,2,4,5.)

$$F = \sim Q + (\sim P \& \sim R)$$

HDL CODE:-



The screenshot shows a Project Manager window titled 'project_6'. It contains a list of files: 'Project Summary', 'decoder.v', and 'decoder_test.v'. The 'decoder.v' file is selected and its content is displayed in the main editor. The code is as follows:

```
1 //2405051
2 module decoder(
3     input i0,i1,i2,
4     output d0,d1,d2,d3,d4,d5,d6,d7
5 );
6 assign d0 = (!i0) & (!i1) & (!i2);
7 assign d1 = (!i0) & (!i1) & (i2);
8 assign d2 = (!i0) & (i1) & (!i2);
9 assign d3 = (!i0) & (i1) & (i2);
10 assign d4 = (i0) & (!i1) & (!i2);
11 assign d5 = (i0) & (!i1) & (i2);
12 assign d6 = (i0) & (i1) & (!i2);
13 assign d7 = (i0) & (i1) & (i2);
14 endmodule
```

TESTBENCH:-

