```
1
2  // Verilog project: Verilog code for traffic light controller
3  `timescale 10 ns/ 1 ps
4  // 2. Preprocessor Directives
5  `define DELAY 1
6  // 3. Include Statements
7  //`include "counter_define.h"
8  module tb_traffic;
9  // 4. Parameter definitions
10 parameter ENDTIME  = 400000;
11 // 5. DUT Input regs
12 //integer count, count1, a;
13 reg clk;
14 reg rst_n;
15 reg sensor;
16 wire [2:0] light_farm;
17 // 6. DUT Output wires
18 wire [2:0] light_highway;
19
20 // 7. DUT Instantiation
21 traffic_light tb(light_highway, light_farm, sensor, clk, rst_n);
22
23 // 8. Initial Conditions
24 initial
25  begin
26  clk = 1'b0;
27  rst_n = 1'b0;
28  sensor = 1'b0;
29  // count = 0;
30 //// count1=0;
31 // a=0;
32  end
33 // 9. Generating Test Vectors
34 initial
35  begin
36  main;
37  end
38 task main;
39  fork
40  clock_gen;
41  reset_gen;
42  operation_flow;
```

```
 operation_flow;
 debug_output;
 endsimulation;
 join
endtask
task clock_gen;
 begin
 forever #`DELAY clk = !clk;
 end
endtask

task reset_gen;
 begin
 rst_n = 0;
 # 20
 rst_n = 1;
 end
endtask


task operation_flow;
 begin
 sensor = 0;
 # 600
 sensor = 1;
 # 1200
 sensor = 0;
 # 1200
 sensor = 1;
 end
endtask
// 10. Debug output
task debug_output;
 begin
 $display("-----------------------------------------------");
       $display("------------------     ----------------------");
 $display("------------ SIMULATION RESULT ----------------");
 $display("--------------             -------------------");
 $display("----------------         --------------------");
 $display("-----------------------------------------------");
 $monitor("TIME = %d, reset = %b, sensor = %b, light of highway = %h, light of farm road = %h",$time,rst_n ,sensor,light_highway,light_farm );
 end
```

```
85
86
87  //12. Determines the simulation limit
88  task endsimulation;
89   begin
90   #ENDTIME
91   $display("-------------- THE SIMUALTION END ------------");
92   $finish;
93   end
94  endtask
95
96  endmodule
```