VISVESVARAYA TECHNOLOGICAL UNIVERSITY

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A Mini-Project Report on

"COMPARATIVE ANALYSIS OF 12-BIT RIPPLE CARRY ADDER AND 12-BIT CARRY SELECT ADDER"

Submitted In partial fulfilment for the award of degree

BACHELOR OF ENGINEERING

In

ELECTRONICS AND COMMUNICATION ENGINEERING

Submitted by

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VISVESVARAYA TECHNOLOGICAL UNIVERSITY

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CERTIFICATE

Certified that the Mini-Project work entitled "Comparative Analysis of 12-bit RCA and 12-bit CSA" is a bonafide work carried out Karthik M (3BR23EC068), Mahantesh Gouda (3BR23EC087) Shivaraj C Patil (3BR23EC152), the bonafide students of Ballari Institute of Technology and Management in partial fulfilment for the award of degree of **Bachelor of Engineering** in **ELECTRONICS AND COMMUNICATION ENGINEERING** of the **Visvesvaraya Technological University, Belagavi** during the academic year 2025-2026. It is certified that all corrections/suggestions indicated for internal assessment have been incorporated in the report deposited in the departmental library. The report has been approved as it satisfies the academic requirements in respect of Mini-Project work prescribed for the said Degree.

Mrs. Nayana M	**Dr.HemanthaKumar R K**	**Dr. Sadyojatha K M**
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External Viva

Name of the Examiner **Signature with date**

1.

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ABSTRACT:

- This project presents a comparative analysis of two commonly used digital adders — the 12-bit Ripple Carry Adder (RCA) and the 12-bit Carry Select Adder (CSA).
- Adders play a crucial role in arithmetic circuits, and their performance directly affects the speed, area, and power consumption of VLSI systems.
- The RCA is simple in design and requires less hardware, but it suffers from high propagation delay due to serial carry propagation.
- The CSA, on the other hand, improves speed by precomputing sum outputs for two possible carry inputs and selecting the correct result using multiplexers.
- In this work, both adders are designed using Verilog HDL and simulated in Cadence tool to verify functionality.
- The designs are synthesized to obtain metrics such as delay, area utilization, and power consumption.
- Based on the results, the CSA shows better speed performance compared to RCA, while RCA provides advantages in terms of lower area and reduced hardware complexity.
- This comparison highlights the trade-offs involved in selecting an appropriate adder architecture for VLSI applications.

INTRODUCTION:

Adders are among the most fundamental arithmetic components in digital and VLSI systems. They are used in ALUs, microprocessors, digital signal processors, and various embedded applications. A Ripple Carry Adder (RCA) is the most basic adder architecture and operates by propagating the carry bit through each full adder stage. Although simple and hardware-efficient, its speed is limited because each stage must wait for the carry from the previous stage . A Carry Select Adder (CSA) improves speed by precomputing sum values for both possible carry inputs (0 and 1).

Once the actual carry is known, the correct result is selected using multiplexers. This reduces the overall delay but increases hardware usage. In this project, both 12-bit RCA and 12-bit CSA are designed using Verilog HDL and evaluated through simulation and synthesis. Their performance is compared based on time delay, gate count, area utilization, and power consumption.

REVIEW OF LITERATURE:

1. M. Morris Mano, in “Digital Design,” explains the ripple carry mechanism and describes RCA as an area-efficient but slow architecture due to linear carry propagation.

2. Jan M. Rabaey, in “Digital Integrated Circuits,” compares various adders and highlights the role of carry-select techniques in reducing delay.

3. Several IEEE research papers propose optimized CSA architectures to further reduce delay by using hybrid carry techniques.

4. Studies conclude that while RCA is efficient in terms of area and power, CSA offers better delay performance, making it suitable for high-speed arithmetic units.

METHODOLOGY AND IMPLEMENTATION:

1. Study the theoretical operation of RCA and CSA.

2. Design 12-bit RCA using structural Verilog modeling.

3. Design 12-bit CSA using multiple 4-bit ripple blocks with multiplexers.

4. Develop testbenches for functional verification.

5. Simulate both adders using Cadence tool.

6. Synthesis and implement both designs to extract:

Area usage

Gate count

Power analysis

Timing (delay).

7. Compare results and prepare analysis.

Implementation:

Tools Used:

CADENCE for simulation, synthesis, and implementation.

Verilog HDL for coding.

Design Flow:

1. Writing Verilog code

2. Behavioral simulation

3. Synthesis & optimization

4. Post-implementation timing and power analysis.

Hardware/Software Requirements:

1. Laptop/PC
2. CADENCE Tool.

12-BIT RIPPLE CARRY ADDER:

A 12-Bit Ripple Carry Adder (RCA) is a simple binary adder built by connecting 12 full adders in series.

Working Principle:

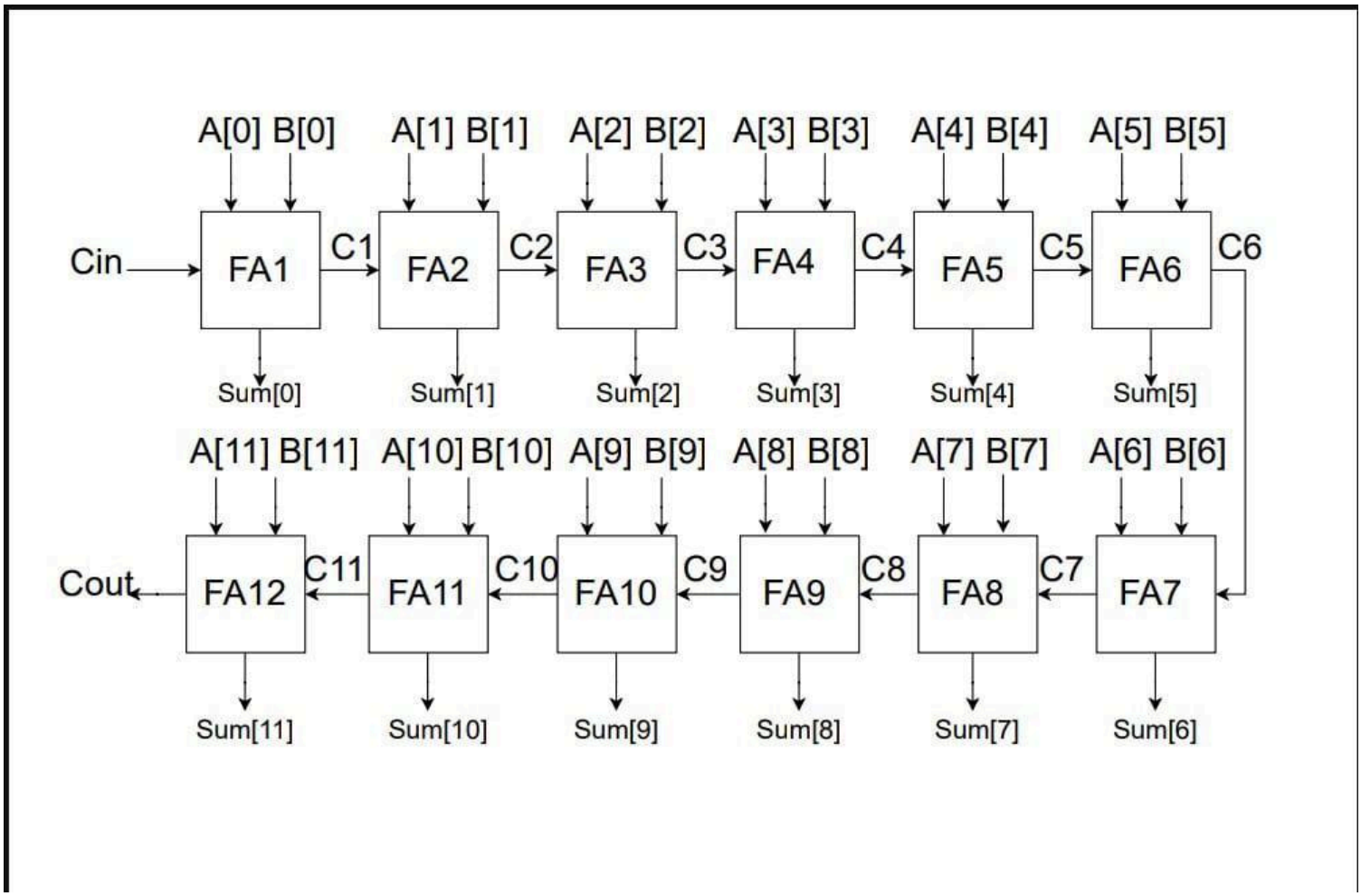
Each full adder generates a sum and carry.

The carry output of the previous stage becomes the carry input of the next stage.

This carry “ripples” through all stages from LSB to MSB.

The final carry-out after the last FA gives the final carry.

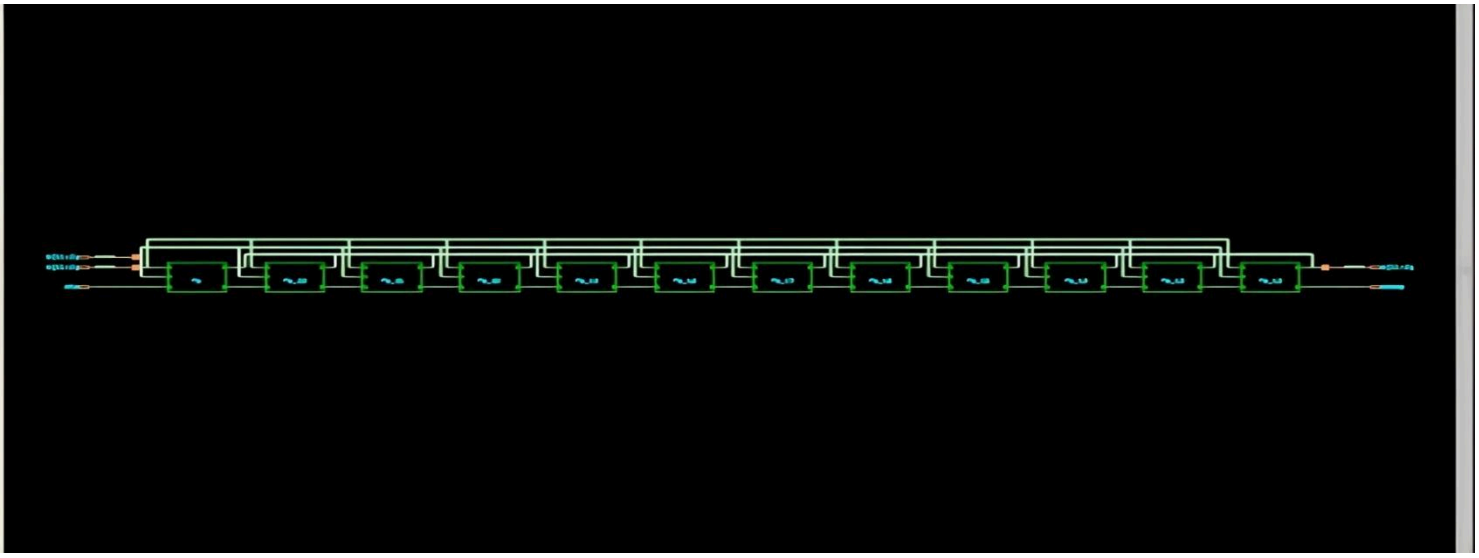
BLOCK DIAGRAM:



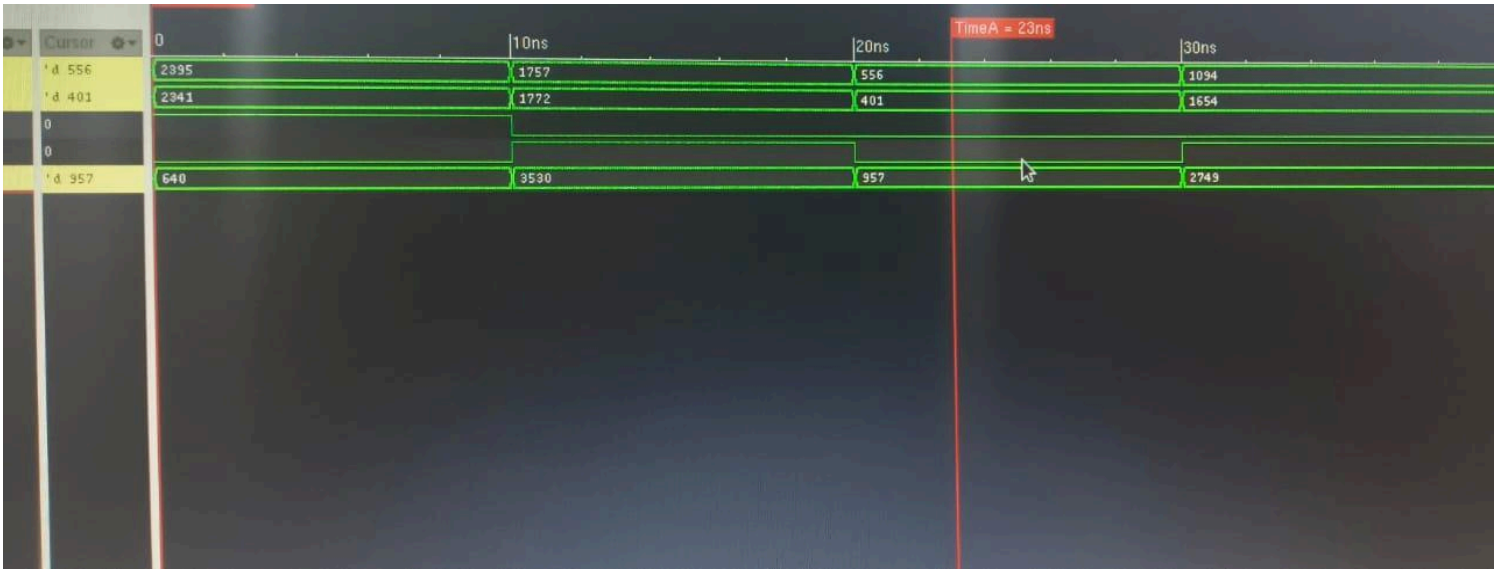
VERILOG CODE FOR 12-BIT RIPPLE CARRY ADDER:

```
module fa (a, b, cin, s, carry);
input a, b;
input cin;
output s, carry;
assign s=a ^ b ^ cin;
assign carry = (a & b) | (b & cin) | (cin & a);
endmodule

module rca (a, b, cin, s, carry);
input [11:0] a, b;
input cin;
output [11:0] s;
output carry;
wire c1, c2, c3, c4, c5, c6, c7, c8, c9, c10, c11;
fa FA1(a [0], b [0], cin, s [0], c1);
fa FA2(a [1], b [1], c1, s [1], c2);
fa FA3(a [2], b [2], c2, s [2], c3);
fa FA4(a [3], b [3], c3, s [3], c4);
fa FA5(a [4], b [4], c4, s [4], c5);
fa FA6(a [5], b [5], c5, s [5], c6);
fa FA7(a [6], b [6], c6, s [6], c7);
fa FA8(a [7], b [7], c7, s [7], c8);
fa FA9(a [8], b [8], c8, s [8], c9);
fa FA10(a [9], b [9], c9, s [9], c10);
fa FA11(a [10], b [10], c10, s [10], c11);
fa FA12(a [11], b [11], c11, s [11], carry);
endmodule

module tb;
reg [11:0] a, b;
reg cin;
wire [11:0] s;
wire carry;
rca UUT (a, b, cin, s, carry);
initial
begin
        a = 12'b100101011011;  b = 12'b100100100101;  cin = 0;
        #10;
        a = 12'b011011011101;  b = 12'b011011101100;  cin = 1;
        #10;
        a = 12'001000101100;  b = 12'b000110010001;  cin = 0;
        #10;
        a = 12'b010001000110;  b = 12'b011001110110;  cin = 1;
        #10;
end
endmodule
```

SYNTHESIS DIAGRAM:



SIMULATION WAVEFORM:



12-BIT CARRY SELECT ADDER:

A Carry Select Adder (CSA) is a faster adder that reduces delay by computing sum and carry in parallel for possible carry inputs (0 and 1).
A multiplexer then selects the correct output when the real carry arrives.

Working Principle:

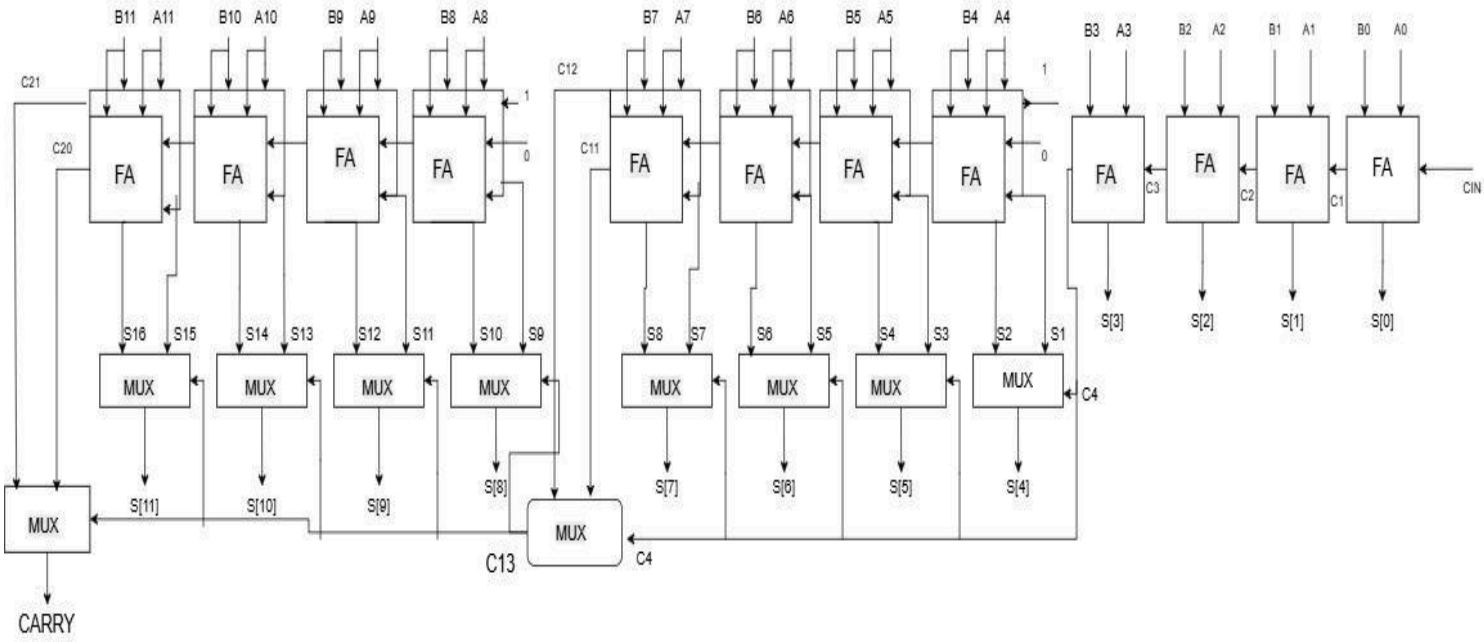
Each block of the CSA contains:

One adder assuming carry-in = 0

Another adder assuming carry-in = 1

A multiplexer to select output.

BLOCK DIAGRAM:



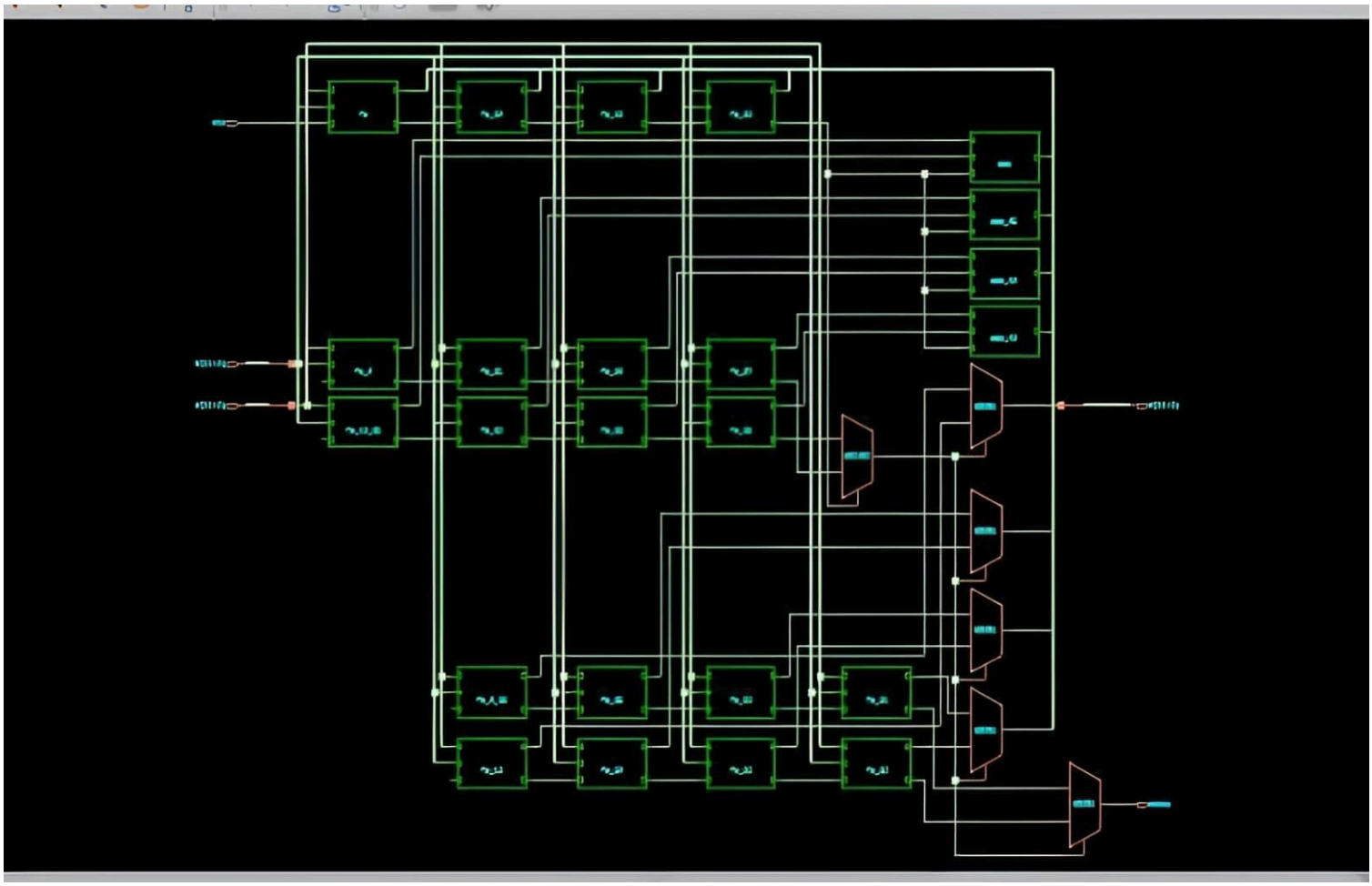
VERILOG CODE FOR 12-BIT CARRY SELECT ADDER:

```
module fa (a, b, cin, s, carry);
input a, b;
input cin;
output s, carry;
assign s=a ^ b ^ cin;
assign carry = (a & b) | (b & cin) | (cin & a);
endmodule

module mux(a, b, s, y);input a, b, s;
output y;
assign y=s?a:b;
endmodule

module csa(a,b,cin,s,carry);
input [11:0] a,b;
input cin;
output [11:0] s;
output carry;
wire c1,c2,c3,c4,c5,c6,c7,c8,c9,c10,c11,c12,c13,c14,c15,c16,c17,c18,c19,c20,c21,s1,s2,s3,s4,s5,s6,s7,s8,s9,
s11,s12,s13,s14,s15,s16;

fa fa1(a[0],b[0],cin,s[0],c1);
fa fa2(a[1],b[1],c1,s[1],c2);
fa fa3(a[2],b[2],c2,s[2],c3);
fa fa4(a[3],b[3],c3,s[3],c4);

fa fa5(a[4],b[4],1'b1,s1,c5);
fa fa6(a[4],b[4],1'b0,s2,c6);
mux m1(s1,s2,c4,s[4]);

fa fa7(a[5],b[5],c5,s3,c7);
fa fa8(a[5],b[5],c6,s4,c8);
mux m2(s3,s4,c4,s[5]);

fa fa9(a[6],b[6],c7,s5,c9);
fa fa10(a[6],b[6],c8,s6,c10);
mux m3(s5,s6,c4,s[6]);

fa fa11(a[7],b[7],c9,s7,c11);
fa fa12(a[7],b[7],c10,s8,c12);
mux m4(s7,s8,c4,s[7]);

mux m5(c11,c12,c4,c13);
```

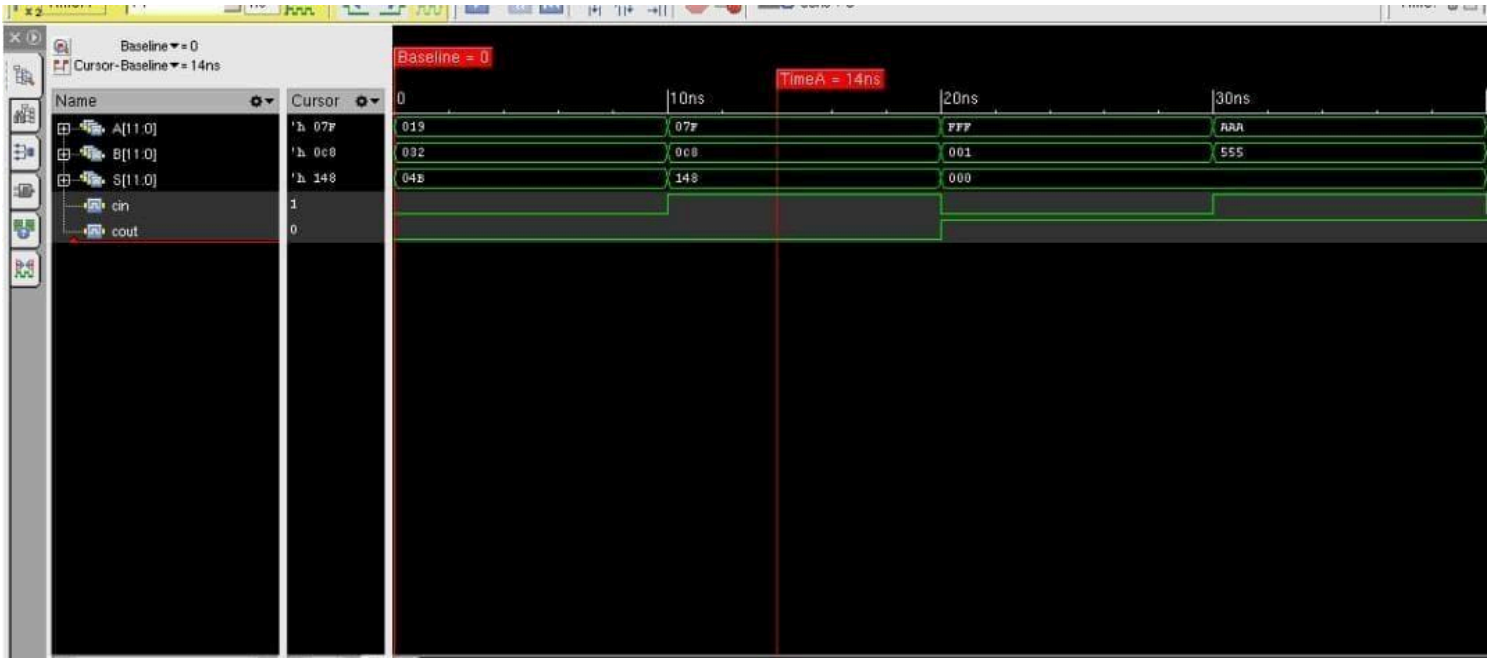
```
fa fa13(a[8],b[8],1'b1,s9,c14);
fa fa14(a[8],b[8],1'b0,s10,c15);
mux m6(s9,s10,c13,s[8]);

fa fa15(a[9],b[9],c14,s11,c16);
fa fa16(a[9],b[9],c15,s12,c17);
mux m7(s11,s12,c13,s[9]);

mux m6(s9,s10,c3,s[8]);

fa fa15(a[9],b[9],c14,s11,c16);
fa fa16(a[9],b[9],c15,s12,c17);
mux m7(s11,s12,c13,s[9]);

fa fa17(a[10],b[10],c16,s13,c18);
fa fa18(a[10],b[10],c17,s14,c19);
mux m8(s13,s14,c3,s[10]);

fa fa19(a[11],b[11],c18,s15,c20);
fa fa20(a[11],b[11],c19,s16,c21);
mux m9(s15,s16,c3,s[11]);

mux m10(c20,c21,c13,carry);
endmodule

module tb;
reg [11:0] a,b;
reg cin;
wire [11:0] s;
wire carry;
csa UUT(a,b,cin,s,carry);
initial
begin
a=12'b111111111111;
b=12'b000000000000;
cin=0;
#10;
a=12'b111111111111;
b=12'b111111111111;
cin=0;
#10;
a=12'b111111111111;
b=12'b000000000000;
cin=0;
#10;
a=12'b111100111111;
b=12'b000010000000;
cin=0;
#10;
```

```
a=12'b111001111111;
b=12'b000000100000;
cin=0;
#10;
a=12'b101011011111;
b=12'b000000000000;
cin=0;
#10;
end
endmodule
```

SIMULATION DIAGRAM:



SIMULATION WAVEFORM:



COMPARISION OF 12-BIT RCA AND 12-BIT CSA REPORTS:

Reports	12-Bit RCA	12-Bit CSA
Area	236.153 mm^2	426.135 mm^2
Power	8.64477×10^{-6} W	15.0380×10^{-6} W
Gate	236.153	426.135
Timing	3.346 ns	1.828 ns

Applications:

- Used in Arithmetic Logic Units (ALU) of microprocessors and microcontrollers.
- Educational and research purposes in VLSI design learning.
- Used in multiplier accumulator and MAC(multiply accumulate) units

CONCLUSION:

- This project successfully implemented and compared 12-bit Ripple Carry Adder and 12-bit Carry Select Adder architectures.
- The results show that RCA is area-efficient but slow due to carry propagation delay.
- CSA, although larger in area and power, provides much better speed performance.
- Therefore, RCA is suitable for low-power and simple applications, while CSA is preferred for high-speed VLSI designs such as ALUs and DSP units.

Reference:

[1] Morris Mano, “Digital Design”, Pearson Education.

[2] Jan M. Rabaey, “Digital Integrated Circuits: A Design Perspective”, Pearson.

[3] IEEE research papers on performance-optimized adder architectures