Multiobjective Optimization for PSIJ Mitigation and Impedance Improvement Based on PCPS/DR-NSDE in Chiplet-Based 2.5-D Systems

Changle Zhi, Gang Dong, Wei Xiong, Deguang Yang, Daihang Liu, Yinghao Feng, Yang Wang, Zhangming Zhu, and Yintang Yang, *Senior Member, IEEE*

***Abstract*—The utilization of modular chiplets in interposer-based 2.5-D heterogeneous systems simplifies fabrication and design, however, it also introduces significant noise challenges. This article presents a collaborative jitter-aware optimization in 2.5-D integrated circuits (ICs), incorporating power supply induced jitter (PSIJ), system impedance, target impedance, and decoupling capacitors, based on the hybrid precomputation and prestorage/duplicate removal-nondominated sorting differential evolution (PCPS/DR-NSDE) algorithm. An automatic channel model algorithm and a uniform decoupling capacitor placement strategy are proposed to improve the design efficiency. Then, the system transfer impedance, simultaneous switch current, sensitivity function, and amplification factor are individually modeled, leading to the assembly and verification of the final PSIJ in the 2.5-D system. A precomputation and prestorage (PCPS) strategy is proposed to handle high-time-consuming modules in the objective function and a duplicate removal (DR) operation is added to improve algorithm performance. The proposed PCPS/DR-NSDE is faster than traditional algorithms and has optimal hypervolume and coverage-metric (C-metric) indicators. The procedures for further obtaining desired solutions in the Pareto front are discussed. The impact of practical constraints and target impedance is also analyzed. This work provides a collaborative optimization and analysis of jitter, noise, and impedance in 2.5-D systems.**

***Index Terms*—2.5-D power distribution network (PDN), chiplet, interposer, multiobjective optimization algorithm, power supply induced jitter (PSIJ), through-silicon via (TSV).**

I. Introduction

IN RECENT years, conventional system-level System-on-Chip (SoC) design has involved fabricating multiple computing units, each tailored for different types of computing tasks, onto a single wafer through photolithography, pursuing "high integration." However, with the failure of Moore's Law and the demand for high-computing throughput and low-power consumption, the adoption of 3-D integrated circuits (ICs) has ensued [1], [2], [3], [4], which have some weaknesses, such as the significant overhead of silicon via [through-silicon via (TSV)], thermal dissipation, and elevated costs. Consequently, chiplet technology has been proposed. It decomposes the original SoC into multiple functional blocks with interconnection interfaces and selects appropriate processes for separate manufacturing. The adoption of interposer-based 2.5-D advanced packaging technology mitigates the need for all advanced processes for integrated manufacturing on the same wafer, significantly reducing dependence on advanced manufacturing processes.

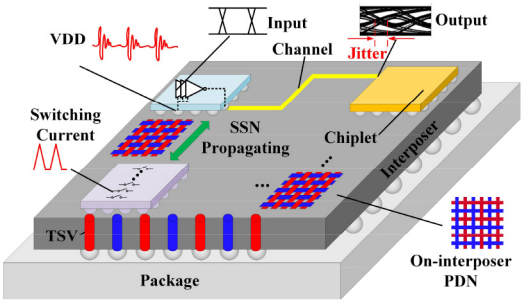

Fig. 1. SSN propagation and jitter generation in the chiplet-based 2.5-D system.

Owing to the arrangement of multiple dies on the interposer, the increased device density and the shared power systems in 2.5-D IC lead to considerable power integrity problems, particularly the jitter issue as shown in Fig. 1. This primarily stems from the imperfect parasitic impedance of the power delivery network (PDN) and the fluctuating current within the circuitry. These factors induce voltage fluctuations, leading to the power supply induced jitter (PSIJ) issue, which has grown critical in parallel interface-based heterogeneous 2.5-D IC to comply with the timing budget of digital data signals [5]. In the current, with input/output (I/O) interface speeds continuously advancing toward multigigabit data rates, the jitter issue has emerged as a significant challenge, being intricately tied to the increasingly stringent timing budget.

Presently, numerous matured techniques exist for the estimation of PSIJ [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21]. The majority focus on PSIJ analytical and numerical modeling for single CMOS

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The authors are with the Key Laboratory of Analog Integrated Circuits and Systems (Ministry of Education), School of Integrated Circuits, Xidian University, Xi'an 710071, China (e-mail: gdong@xidian.edu.cn).

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inverter and inverter chains [7], [8], [9], [10], [11], [12], [13], [14], with a particular emphasis on inverter characteristics rather than complex circuit systems. Xu et al. [15], Moreno-Mojica and Rayas-Sánchez [16], Sun et al. [17], and Sun et al. [18] investigated the factors pertinent to PSIJ in conventional 2-D circuits. Research on PSIJ in heterogeneous 2.5-D systems is limited, with only a few studies, including these topics. In [19], rigorous analysis and characterization techniques of PSIJ in multidie interfaces heterogeneous 2.5-D IC are presented. Shin et al. [20] and Park et al. [21] modeled the system-level PSIJ for high-bandwidth memory (HBM) I/O interface.

As previously mentioned, the generated simultaneous switch noise (SSN) is a significant contributor to jitter. The employment of decoupling capacitors can lower-system impedance and mitigate the issues arising from the noise. Furthermore, a substantial volume of existing research is currently focused on strategies for the placement of decoupling capacitors [22], [23], [24], [25], [26]. In summary, these studies predominantly focus on PSIJ modeling or decoupling methods, with a noticeable absence of comprehensive analysis of other associated components in chiplet-based systems. Importantly, with the rapid development of 2.5-D IC, comprehensive consideration and optimization involving aspects, such as capacitor placement, switching noise, transmission channels, PSIJ, and system impedance among others, represent critical areas of research that warrant further investigation.

In this article, for the first time, we present a multiobjective optimization encompassing PSIJ, impedance, target impedance, and decoupling capacitor in 2.5-D IC, based on the proposed precomputation and prestorage/duplicate removal-nondominated sorting differential evolution (PCPS/DR-NSDE) algorithm. We propose an automatic channel model algorithm and a uniform decoupling capacitor placement algorithm to improve the design efficiency. Then, the system transfer impedance, simultaneous switch current, jitter sensitivity function, and channel amplification factor are combined to enable the final PSIJ modeling in the time domain, which is further verified. Based on the high-time-consuming issue of multiobjective functions in the 2.5-D system, we introduce a precomputation and prestorage (PCPS) strategy for the high-time-consuming modules. This approach significantly reduces computation time compared to traditional calculation methods. The optimization performance of nondominated sorting differential evolution (NSDE) for the proposed objective function is enhanced by incorporating a duplicate reduction operation. Compared to classic multiobjective algorithms, the optimal front obtained by the multiobjective function proposed in this problem exhibits superior indicators. To further identify the required optimal solution in the Pareto front, a normalization-based method is adopted, allowing for manual parameter definition and selection of the most suitable 2.5-D system parameters. In addition, we also investigated the effects of different practical constraints and target impedances on the optimization of 2.5-D ICs. This work provides a collaborative optimization and analysis of jitter, noise, and impedance in 2.5-D systems.

II. Preliminaries

A. Chiplet-Based 2.5-D PDN

In 2.5-D ICs, the interposer draws power from the package through TSV arrays and bump arrays to power multichiplets. Chiplet-based 2.5-D PDNs are not fundamentally different from conventional 3-D PDNs, but the on-chip PDN parameters are diverse due to the use of different process nodes. There are several related research works on 2.5-D ICs [27], [28], [29], [30], which include passive and active interposer design rules and design rules for chiplets under different process nodes, which can be useful as a guide for subsequent research related to 2.5-D systems.

B. Related Works on Electrical Optimization

In recent years, multiobjective optimization has been commonly used in several fields of computer-aided design of circuits. Kim et al. [27] proposed an efficient parallel Bayesian optimization algorithm based on the multiobjective acquisition function to accelerate the optimization process for analog circuit synthesis. Kim et al. [28] proposed a multiobjective optimization method named inverse stack-up optimization for automated stacking design of multilayer printed circuit boards (PCBs), which meets all the design objectives in a short run time and provides an effective and efficient solution for automating interconnect design. Coskun et al. [29] proposed an automated framework to explore the microarchitectural design of the reduced instruction set computer-V (RISC-V) community and correlated multiobjective Bayesian optimization to characterize the design space.

In addition, with the development of machine learning, the research on multiobjective black-box optimization has also made great progress. Park et al. [30] proposed a new design for using the Monte Carlo tree search framework in the black-box optimization problem that places more emphasis on efficient local descent of the samples rather than using the Monte Carlo tree search for explicit space partitioning.

C. Related Algorithms and Key Indicators

The common multiobjective optimization algorithms, such as the multiobjective genetic algorithm (MOGA) [31] and multiobjective particle swarm optimization algorithm (MOPSO) [32]. MOPSO solves the multiobjective problem based on the PSO, where its Pareto dominance is taken into account when comparing particles and nondominated solutions are stored to approximate the Pareto front. Nondominated sorting genetic algorithm II (NSGA-II) is a representative MOGA and the most widely used multiobjective algorithm [33]. Based on the mutation, selection, and crossover operations of traditional genetic algorithms, it adds core nondominated sorting, and crowding distance sorting operations to obtain Pareto front. The NSDE algorithm [34], [35], which inherits the concepts of nondominated sorting and crowding distance sorting from the classical NSGA-II algorithm, is a parallel search multiobjective method that exploits population differences and exhibits excellent performance. We have used the NSDE algorithm in this work

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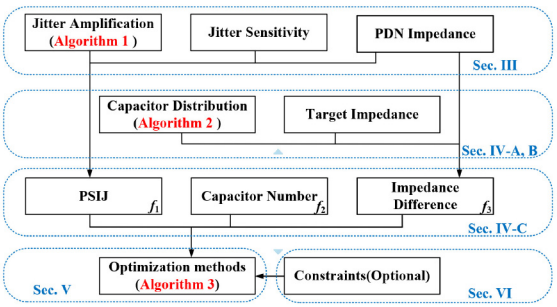

Fig. 2. Framework structure and included algorithms.

In a multiobjective optimization algorithm, a Pareto front is a set of mutually undominated sets of optimal solutions. The Pareto front cannot be assessed by visual inspection, and evaluation indicators need to be introduced. The Ubuntu point, i.e., the optimal point, is unknown for the engineering problem optimized in this article. It is not possible to evaluate the Pareto front through the Ubuntu point.

Since the Ubuntu point is unknown, the hypervolume indicator is the best metric for evaluating the performance among the algorithms, which represents the volume between the solution set and the reference point. The reference point is the worst point of each objective function. Hypervolume is the indicator that is strictly monotonous in the Pareto dominance relationship. The larger the hypervolume value, the better the comprehensive performance of the algorithm and the corresponding Pareto Front. Since the computation of the hypervolume metric is time-consuming, the Monte Carlo estimation-based hypervolume is adopted in this work [36]. The hypervolume indicators in this article are in the form of percentages. Besides, coverage-metric (C-metric) is also a suitable indicator for the no-Ubuntu point problems [37]. The C-metric can be expressed as C(A, B), which represents the percentage of solutions in B dominated by A. When C(A, B) is greater than C(B, A), it means that the solutions in A are better than those in B.

D. Algorithms in This Work

Three algorithms are described subsequently in this article. The framework of this article and the relationship between the algorithms is shown in Fig. 2. A PCPS/DR-NSDE multiobjective algorithm is used to optimize the chiplet-based 2.5-D electrical problem, which is described in detail in Algorithm 3 and is the core algorithm of this article. In addition, other algorithms are also used to assist in the 2.5-D electrical modeling. Algorithm 1 is used to support the PSIJ calculation and Algorithm 2 is used to automatically assign capacitors. As shown in Fig. 2, the electrical characteristics of the 2.5-D IC are modeled and the objective functions are constructed. An optimization algorithm is used to find an optimal solution to the 2.5-D problem while satisfying the given constraints.

III. PSIJ Modeling

In a chiplet-based 2.5-D system, the PSIJ problem is exacerbated due to the compact packaging of multiple chiplets, a significant number of switching circuits, and numerous channels. The simultaneous switching of numerous devices results in the propagation of noise currents and the formation of SSN within the circuit. This SSN adversely affects the direct current (DC) power supply of the buffer, leading to the degradation of the transmission signal. Furthermore, the channel itself also introduces disturbances during the signal transmission process. This section focuses on the modeling of PSIJ in 2.5-D ICs by exploring various factors, including the 2.5-D PDN, interchiplet channels, PSIJ sensitivity (PSIJS) function, and amplification factors.

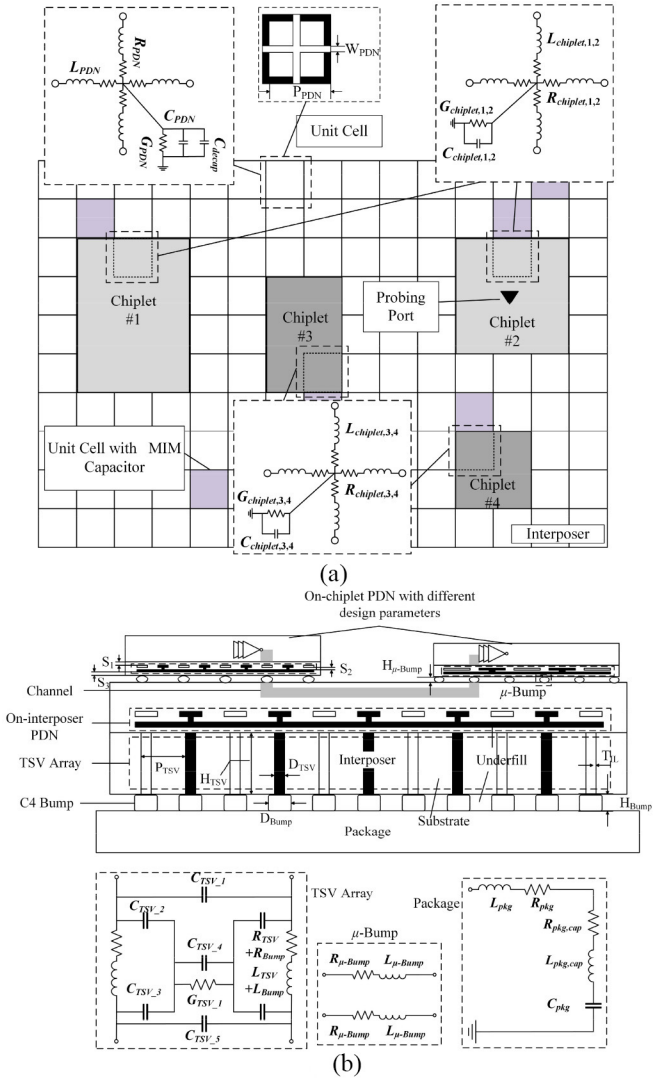

Fig. 3. Chiplet-based 2.5-D test structure. (a) Top view of the overall structure and the equivalent circuit of PDNs in different chiplets and interposers. (b) Cross-section view of the overall structure and the equivalent circuit of TSVs, bumps, and packages.

A. Modeling of 2.5-D PDN

The specific geometry of the heterogeneous 2.5-D IC includes chiplets with different functions and technology, decoupling capacitors, interposers with TSVs powered from package, bumps, etc. In this section, the PDN of each

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TABLE I
RELATED DESIGN PARAMETERS OF THE 2.5-D PDN USED IN THIS ARTICLE

Description	Symbol	Value
Metal width of each PDN grid of chiplet #1, #2	$W_{PDN}^{Chip,a}$	25 μm
Metal width of each PDN grid of chiplet #3, #4	$W_{PDN}^{Chip,b}$	20 μm
Metal width of each PDN grid of interposer	$W_{PDN}^{Interposer}$	30 μm
Pitch between the adjacent two PDN grids of chiplet #1, #2	$P_{PDN}^{Chip,a}$	100 μm
Pitch between the adjacent two PDN grids of chiplet #3, #4	$P_{PDN}^{Chip,b}$	100 μm
Pitch between the adjacent two PDN grids of interposer	$P_{PDN}^{Interposer}$	100 μm
Pitch between adjacent two TSVs	P_{TSV}	200 μm
Space between upper boundary of intermetal dielectric (IMD) and upper metal of PDN	S_1	1.5 μm
Space between two adjacent layers of PDN	S_2	0.8 μm
Space between the lower boundary of the IMD and the lower metal of PDN	S_3	1.01 μm
Thickness of each metal PDN layer	T_{PDN}	0.7 μm
Thickness of SiO_2 insulation layer (IL) outside TSV	T_{IL}	0.5 μm
Diameter of TSV	D_{TSV}	40 μm
Diameter of C4 bump	D_{Bump}	80 μm
Height of TSV	H_{TSV}	50 μm
Height of C4 bump	H_{Bump}	39 μm
Relative permittivity of silicon substrate	ε_{Sub}	11.9
Relative permittivity of IL	ε_{IL}	3.9
Relative permittivity of IMD	ε_{IMD}	3.9
Relative permittivity of underfill	$\varepsilon_{Underfill}$	4.3
Diameter of μ-bump	$D_{\mu\text{-}Bump}$	25 μm
Height of μ-bump	$H_{\mu\text{-}Bump}$	10 μm
Height of IMD	H_{IMD}	1 μm
Thickness of bottom SiO_2 IL	$T_{IL,bot}$	1 μm

component is modeled individually and subsequently assembled. Fig. 3 illustrates the structural parameters of the 2.5-D IC, while Table I provides a detailed explanation. Most of the parameters of the PDN and TSV are referenced in [38] and [39] and are based on actual measurements with high confidence. These parameter settings also meet the current 2.5-D design rules [27], [28], [29], [30]. In the references, the authors have fabricated and tested silicon interposers, grid-type PDNs and TSVs, so the parameter settings are highly informative. Fig. 3(a) shows the PDN models of interposers and chiplets, which are assembled using equipment unit cells. Chiplets are different functional modules packaged with different technologies and manufacturers. Therefore, the structural parameters of PDN within chiplets also exhibit differences. Fig. 3(b) shows the classic TSV/μ-bump modeling, with further details regarding the modeling procedure provided in [40] and [41]. The impedance matrix of each unit structure can be computed. Then the self-impedance Z_{ii} of any point or the transfer impedance Z_{ij} between any two points can be obtained through a cascaded method [41]

$$V_{\text{SSN}}^{i} = \sum_{j}^{j\in\Lambda} Z_{ij} \times I_{\text{switch}}^{j}. \tag{1}$$

Algorithm 1 Channel Model in 2.5-D Systems

1: **Input:** Channel parameters: channel length l_{Ch}, channel width w_{Ch}, channel thinness t_{Ch}, length of unit wire l_{Unit}.
2: **Output:** Channel transmission coefficient S_{Ch}.
3: Initialize the transmission coefficient of unit wire S_{Unit}, and the transmission coefficient of the joint S_{Joint}.
4: **if** $l_{\text{RDL}} \geq_{Unit}$
5: Number of unit wires N=*Round toward zero* (l_{Ch}/l_{Unit}).
6: Length of remaining wire l_{Re}=*Reminder*(l_{Ch}/l_{Unit}).
7: Calculate the transmission coefficient *of* N unit wires S_{Ca} using *S-parameter Cascade*.
8: Calculate the transmission coefficient of the remaining wire S_{Re}.
9: Calculate the S_{RDL} of the total RDL using *S-parameter Cascade* by S_{Ca} and S_{Re}.
10: **else**
11: Calculate the S_{RDL} of the total RDL.
12: **end if**
13: Calculate the final channel transmission coefficient S_{Ch} using *S-parameter Cascade* by S_{RDL} and S_{Joint}.

When multiple switches operate simultaneously, each switch generates a current I_{switch}. By utilizing the transfer impedance and applying the circuit superposition theorem, the V_{SSN} at any point i can be obtained as expressed in (1). λ represents the set of switch current positions j.

Note that the PDN modeling method has high compatibility and is suitable for on-chip and interposer PDNs with different process nodes and parameters. For irregular structures, an equivalent circuit model is not necessary and methods, such as measurements, can be used to extract the impedance matrix.

B. Modeling of Interchiplet Channels

The interposer-based interchiplet channel in 2.5-D IC is illustrated in Fig. 4(a), while the corresponding electrical model of the channel is presented in Fig. 4(b). The modeling of redistribution layers (RDLs) takes into account the crosstalk originating from nearby wires [40]. Additionally, electrostatic discharge (ESD) capacitors are added to both driver and receiver ends [42]. The models also consider the impact of bumps.

If the size of the RDLs is smaller than one-twentieth (1/20 times) of the wavelength of the applied signals, a lumped element model can be employed [43]. Otherwise, when dealing with long transmission lines, distributed effects become prominent, leading to a deviation from quasi-stable conditions, as stated in [44]. In such cases, a distributed parameter model is utilized. To facilitate this, the long transmission lines are divided into multiple shorter wires at first. Then, an algorithm for channel classification and fast calculation is proposed. Algorithm 1 outlines this method, where S represents the insert loss, and l represents the length. The *S-parameter Cascade* operation involves cascading two or more devices and calculating the S-parameter of the whole device. The cascaded S-parameter can be obtained through the cascading

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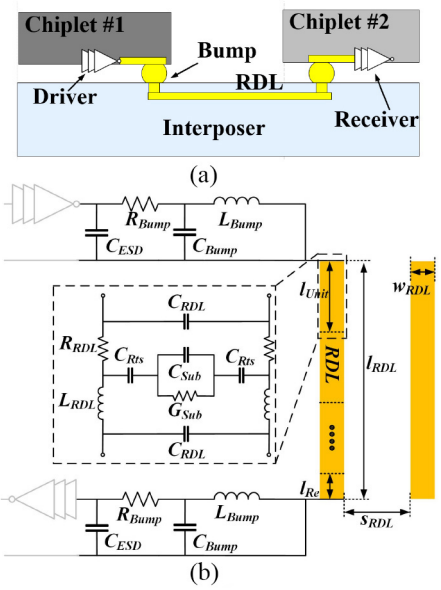

Fig. 4. (a) Physical and (b) electrical model of the channel in 2.5-D IC.

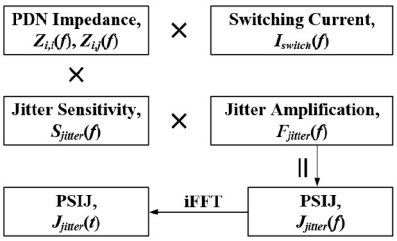

Fig. 5. Overall process of PSIJ calculation.

of impedance parameters and the conversion between S-parameters and impedance matrix.

Finally, the calculation steps for PSIJ in the frequency domain are illustrated in Fig. 5. First, the SSN (V_{SSN}) is obtained by considering the impedance of the 2.5-D PDN and the simultaneous switch current. Next, the PSIJS and jitter amplification factor for the buffer chain are calculated using an empirical model derived by combining the jitter sensitivity function with the channel-related jitter amplification factor. The *iFFT* operation represents the Inverse Fourier transform. We model the PDN in Section III-A and the channel in Section III-B. The remaining sections in Fig. 5 are explained as follows.

Specifically, PSIJS represents the sensitivity of the CMOS buffer chain to power supply noise [8], [20]. As shown in (2), the $T^{\mathrm{DC}}_{p,\max}$ and $T^{\mathrm{DC}}_{p,\min}$ represent the maximum and minimum propagation delays from the input to the output of the chiplet, respectively. $VDD_{\max}$ and $VDD_{\min}$ correspond to the maximum and minimum DC power supplies, respectively.

For accurate results, it is crucial to consider the jitter amplification caused by channel loss [20]. The channel loss, resulting from frequency modulation, varies at each frequency point. Considering the relationship between jitter frequency and Nyquist frequency, the general jitter amplification factor is expressed in (3) [45], [46]. Here, f_0 represents the fundamental

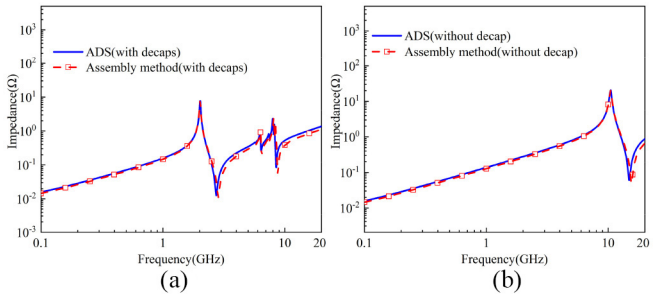

Fig. 6. Verification of the assembly method (a) with ten decoupling capacitors and (b) without decoupling capacitors.

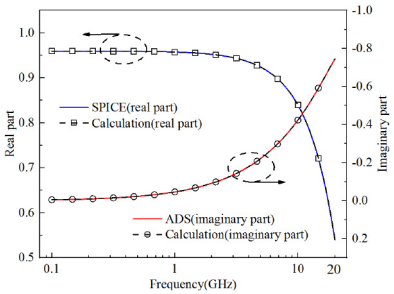

Fig. 7. Verification of the electrical model insert loss and Algorithm 1 in 2.5-D IC of the channel.

frequency of the clock and w denotes the noise frequency associated with the jitter

$$S(f) = \frac{T^{\mathrm{DC}}_{p,\max} - T^{\mathrm{DC}}_{p,\min}}{VDD_{\max} - VDD_{\min}} \operatorname{sinc}\left(f \frac{T^{\mathrm{DC}}_{p,\max} + T^{\mathrm{DC}}_{p,\min}}{2}\right) \quad (2)$$

$$F_{\mathrm{SJ}}(\omega) = \frac{1}{2}\left|\frac{S_{21}\left[f_0 + \alpha(2nf_0 - \omega)\right]}{S_{21}(f_0)} + \frac{S_{21}\left[f_0 - \alpha(2nf_0 - \omega)\right]^*}{S_{21}(f_0)^*}\right| \quad (3)$$

$$\text{where } \begin{cases} \alpha = 1 & (2n-1)f_0 < \omega \le 2nf_0 \\ \alpha = -1 & nf_0 < \omega \le (2n+1)f_0 \end{cases} \quad n = 1, 2, 3, \ldots$$

C. Verification

The numerical results of the 2.5-D PDN model are shown in Fig. 6. The chiplet placement in the test structure is consistent with Fig. 3(a), while other test parameter settings are listed in Fig. 3 and Table I. To validate the accuracy of the proposed impedance modeling method for the 2.5-D PDN with capacitors, ten capacitors of 50 pF are placed uniformly on the interposer. The calculated impedance values closely correspond to the values obtained using Keysight ADS software. The channel modeling and validation of Algorithm 1 in 2.5-D IC are shown in Fig. 7. In this validation case, the parameters are given as follows: $w_{\mathrm{RDL}} = 5\ \mu$m, $s_{\mathrm{RDL}} = 15\ \mu$m, $t_{\mathrm{RDL}} = 0.4\ \mu$m, and $l_{\mathrm{RDL}} = 250\ \mu$m. The calculation results obtained from Algorithm 1 exhibit a good agreement with the ADS simulation. For the transistors in the buffer, the positive metal-oxide-semiconductor (pMOS) transistor has a channel width of 1.8 μm and a channel length of 180 nm. In Fig. 8(a), the jitter value obtained from the eye diagram simulation

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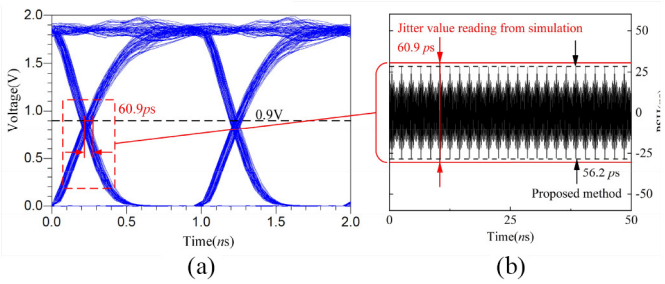

Fig. 8. Verification of the final PSIJ. (a) Eye diagram by ADS. (b) Proposed method.

within the red dashed box aligns well with the value calculated using the proposed method shown in Fig. 8(b).

IV. Problem Formulation

In this section, we collectively establish and analyze several highly relevant problems in chiplet-based 2.5-D IC. These include the PSIJ, the system impedance, the target impedance, and the placement of decoupling capacitors.

A. Decoupling Capacitor

The chiplet, as a predesigned and customized functional chip, is intended for plug-and-play integration. The redesign and replacement of decoupling capacitors on chiplets for impedance optimization deviate from the original purpose of the chiplet system in package (SiP) technology. In contrast, the interposer offers significant design potential for decoupling capacitor allocation. In the interposer-level PDNs, metal-insulator-metal (MIM) capacitors are most suitable due to their ultralow equivalent series inductance and ease of fabrication [47], [48]. The number of capacitors employed has a significant impact on the circuit's impedance. Distributing capacitors effectively on the interposer poses a challenge. Manually allocating capacitors can be a time-consuming task, requiring significant engineering effort. To address this, we propose a more general and compatible algorithm for a uniform capacitor distribution strategy in Algorithm 2. The interposer PDNs are composed of multiple unit cells. By considering the interposer size M×N and the total number of MIM capacitors N_C, the proposed algorithm facilitates a uniform capacitor placement scheme.

An example of the capacitor placement strategy is shown in Fig. 9, where $M_x = 15$, $M_y = 10$, and $N_C = 113$. First, capacitors are placed in each row to obtain scheme S_1, and capacitors are placed in each column to obtain scheme S_2. Scheme S_3 is obtained by intersecting S_1 and S_2. Then place the remaining N_F capacitors around the center point o. Note that when the number of capacitors exceeds half of the unit cells, the placement process for capacitors is converted into a process for unit cells without capacitors. Therefore, in this case, it is necessary to perform a reverse operation, converting the S_4 into a capacitor scheme.

Algorithm 2 Capacitor Distribution Strategy

Input: Number of unit cells at x, y-direction M_x, M_y, number of capacitors N_C.
Output: Final capacitor placement scheme S_4.
if $N_C \geq (M_x \times M_y)/2$ **then**
  $N_U = (M_x \times M_y - N_C)$,
  N_U is the number of unit cells without the capacitor.
Convert the N_C process to the N_U process below, and reverse the final scheme.
end if
while 1
  Find adjacent divisors a and b of N_C(a $\geq b$).
  if $M_x \leq$ a $\cup$ $M_y \leq b$ **then**
    $N'_C = N_C$-1.
  else
    break
  end if
Number of capacitors finally placed $N_F = N_C - N'_C$.
Distance between adjacent capacitors in a row, $d_1 = Round\ toward\ zero((M_x - a)/(a+1))$.
Distance from the last capacitor to the end in a row, $d_2 = M_x - (a \times (d_1 + 1))$.
Distance adjustment factor, $d_3 = Round\ toward\ zero(|d_2 - d_1|/2)$.
Position of the ith capacitor in each row, $p_x(i) = i \times (d_1 + 1) + d_3, i = 1,2 \ldots a$. the capacitor scheme is S_1.
Refer to 14–17, get capacitor scheme S_2 in each column.
The capacitor scheme $S_3 = S_1 \cap S_2$.
Find the center point o of $M_x \times M_y$, and place N_F capacitors around o, get the final capacitor scheme S_4.

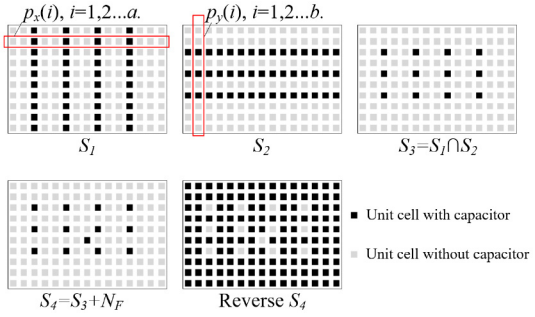

Fig. 9. Example of a capacitor placement strategy.

B. Target Impedance

In traditional circuit design, the target impedance is described by (4). The design parameters are adjusted to ensure that the system impedance remains lower than the target impedance, thereby controlling the noise voltage within an acceptable range. However, the strictness of the target impedance defined in (4) can result in overdesign in high-integration 2.5-D systems. New target impedance strategies have been proposed to reduce the system cost, which decreases the overuse of decoupling capacitors. In this work, we adopt a specific target impedance shown in Fig. 10 [49]. Equation (4) represents the flat region, while the knee point is determined

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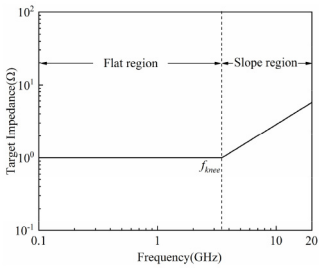

Fig. 10. Target impedance with flat and slope regions.

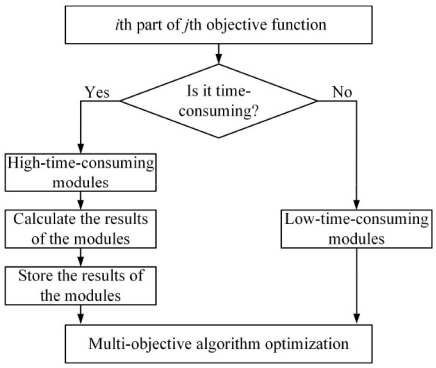

Fig. 11. PCPS operation for multiobjective functions.

by (5). V_{ripple} in (4) represents the maximum allowable ripple voltage in the circuit. Beyond the point f_{knee}, the slope region of the target impedance curve increases at a rate of 20 dB/dec. Equation (6) represents the sum of the actual impedance over the target impedance, where Γ represents the set of frequency points, and (6) is subsequently used as an objective function

$$Z_{\text{target}} = \frac{V_{\text{ripple}}}{I_{\text{switch}}} \tag{4}$$

$$f_{\text{knee}} = \frac{0.35}{T_r} \tag{5}$$

$$\sum_{f(i)\in\Gamma} \left\{ \text{Max}\left(0, Z_{f(i)} - Z_{\text{target}\_f(i)}\right)\right\}. \tag{6}$$

C. Problem Formulation

The modeling and verification of PSIJ and impedance have been discussed earlier. The number of decoupling capacitors, PSIJ, and impedance exhibit conflicting requirements. Therefore, we formulate the contradictions in the 2.5-D system as a multiobjective optimization problem, which can be expressed as follows:

$$\begin{aligned} \min \ \ & F(\boldsymbol{x}) = (f_1(\boldsymbol{x}),\ f_2(\boldsymbol{x}), f_3(\boldsymbol{x})) \\ & f_1 = t_{\text{PSIJ}} \\ & f_2 = N_C \\ & f_3 = \sum_{f(i)\in\Gamma} \left\{ \text{Max}(0, Z_{f(i)} - Z_{\text{target}\_f(i)})\right\}. \end{aligned} \tag{7}$$

$\boldsymbol{x}$ represents the variable matrix. It is worth noting that achieving the minimum value for all objective functions simultaneously is not feasible due to their contradictory nature. Obviously, (7) is a multiobjective optimization problem. The Pareto front represents a set of optimal compromise solutions that cannot be dominated in the multiobjective function space. As the value of one objective function decreases, the values of other objective functions must change accordingly.

Note that the proposed optimization method aims to provide a comprehensive solution for maintaining power integrity. The problem formulation step encompasses a wide range of electrical characteristics. Therefore, depending on the specific problem, additional details can be incorporated into this step to address the issue more accurately.

V. Algorithm

As mentioned earlier, the NSDE algorithm is a parallel search multiobjective method that capitalizes on population differences and exhibits excellent performance, and is used in this article.

In the iteration of a multiobjective algorithm, most of the computation time is spent on computing the multiobjective functions. The objective functions consist of high-time-consuming modules and low-time-consuming modules. For the high-time-consuming modules, PCPS operations, i.e., PCPS operations, are performed before optimization, as shown in Fig. 11. Note that it does not require computing all the results of the objective functions, but rather focuses on computing the independent and time-consuming parts. For example, channel modeling and PDN modeling are time-consuming modules that are independent of each other. If the modules are calculated during the optimization process, it will take a lot of time and the calculation will be repeated many times. In this case, the PCPS strategy is used to save computation time. The strategy is integrated with the NSDE algorithm to form the PCPS-NSDE algorithm. In the process of PCPS-NSDE, after the *Mutation*, *Crossover* and *Selection* operations, duplicates in the intermediate chromosomes and Pareto front of the multiobjective optimization process can be detrimental. Consequently, a duplicate removal (DR) operation has been incorporated to eliminate the duplicated chromosomes

$$\lambda = e^{-\frac{1-\mathbb{K}}{\mathbb{K}+1-k}} \tag{8}$$

$$\hat{\theta} = \hat{\theta}_0 \cdot 2^{\lambda} \tag{9}$$

$$\hat{q}_i^k = \hat{p}_i^k + \hat{\theta}\left(\hat{p}_{i'}^k - \hat{p}_{i''}^k\right) \tag{10}$$

where $i',\ i'' = 1,\ 2, \ldots, \mathbb{R}, i \neq i', i \neq i'', i' \neq i''$.

$$\tilde{q}_{i,d}^k = \begin{cases} \tilde{p}_{i,d}^{k-1}, & r \geq \tilde{\theta} \\ \hat{q}_{i,d}^k, & r < \tilde{\theta}. \end{cases} \tag{11}$$

where $d = 1,\ 2, \ldots, \mathcal{D}, k = 1,\ 2, \ldots, \mathbb{K}$.

The steps of the proposed PCPS/DR-NSDE algorithm tailored for 2.5-D system optimization, are shown in Algorithm 3. The initialization phase involves setting the parameters and creating the chromosomes. Each chromosome consists of $\mathcal{D}$ elements, each representing an optimization parameter. The total count of chromosomes is $\mathcal{R}$. *Mutation*

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Algorithm 3 PCPS/DR-NSDE Algorithm

Input: Z_{Target}, Γ, $\hat{\theta}_0$, $\tilde{\theta}$, $\mathcal{R}$, $\mathcal{K}$, $\mathcal{D}$, all parameters of the entire PDN.
Output: Final Pareto front.
Initialize the r, $\hat{\theta}_1$, $\tilde{p}_i^0$.
Do the *Pre-Computation and Pre-Storage* Operations.
for k = 1 : $\mathbb{K}$ **do**
  Update $\hat{q}_i^k$ by *Mutation* with (10).
  Update $\tilde{q}_i^k$ by *Crossover* with (11).
while $\tilde{q}_i^k$ have duplicates **do**
  Modify $\tilde{q}_i^k$ by *Duplicate Removal*.
end while
  Get $\hat{p}_i^k$ by combining $\tilde{q}_i^k$ and $\tilde{p}_i^{k-1}$.
while $\hat{p}_i^k$ have duplicates **do**
  Modify $\hat{p}_i^k$ by *Duplicate Removal*.
end while
  Arrange $\hat{p}_i^k$ by *Non-Dominated Sorting*.
  Arrange $\hat{p}_i^k$ by *Crowding Distance Sorting*.
  Get $\tilde{p}_i^k$ by *Selection*
end for

operations simulate genetic mutations in organisms that randomly change an element in a chromosome. $\hat{\theta}$ represents the mutation operator, which regulates the scaling of the difference variable and is associated with the number of iterations as expressed in (8) and (9). The initial mutation operator is set as $\hat{\theta}_0$, and k represents the number of algorithm iterations. The process of selecting genes from the original and mutated chromosomes to form a new chromosome group is referred to as crossover, as shown in (10). *Crossover* operations simulate the natural phenomenon of chromosome crossover translocation, as expressed in (11). $\tilde{\theta}$ represents the crossover operator and signifies the probability of the crossover operation and r represents a random number within [0,1]. Both *Mutation* and *Crossover* operations are used to generate new chromosomes.

In the *Nondominated Sorting* operation [33], solutions in the total solution set that cannot be dominated by any other solution are labeled as Set 1. Then, Set 1 is removed from the total solution set and the remaining solutions that cannot be dominated by any other solution are labeled as Set 2. All the solutions in the solution set are sorted by dominance relationship and are divided into many subsets Set i, where i represents the set rank.

In the *Crowding Distance Sorting* operation, to measure the quality of the solutions in Set i, a crowding distance is assigned to each solution. The normalized crowding distance $D_{m,n}$ for the mth individual in the nth objective function is expressed in (12). The objective function is then traversed and the crowding distance $CD_{m,n}$ for the mth individual is obtained in (13). In Set i, a larger crowding distance represents a better solution. The goal of this operation is to make the solutions as dispersed as possible in the objective space to maintain the diversity of the population.

In the *Selection* operation, the chromosome sets from two adjacent iterations are merged and the *Nondominated Sorting* and *Crowding Distance Sorting* operations are performed, with the smaller rank value and the longer crowding distance in the same rank being prioritized. The chromosomes in the top half of the sorting are selected for the next iteration

$$D_{m,n} = \frac{f_n(x_{m+1}) - f_n(x_{m-1})}{f_n(x_{\max}) - f_n(x_{\min})} \tag{12}$$

$$CD_m = \sum_n D_{n,m}. \tag{13}$$

The time complexity of the proposed algorithm is compared with the other three algorithms. We first derived the time complexity of the proposed algorithm as an example. In iteration, the computation of the objective functions to update individual values is the main time-consuming part, while the time for other parts can be ignored. Therefore, the comparison is mainly focused on the number of iterations of the objective functions. The time complexity of executing the objective functions once is set to $O(\boldsymbol{f})$, where $\boldsymbol{f}$ contains all objective function f_i. From above, the total number of chromosomes is $\mathbb{R}$, and the number of iterations is $\mathbb{K}$. Thus, the time complexity of the algorithm is $O(\mathbb{K}\mathbb{R}\boldsymbol{f})$. Besides, due to the adoption of PCPS strategy, the time complexity of executing the objective function once can be recorded as $O(\hat{f})$, and $O(\hat{f})$ is much smaller than $O(\boldsymbol{f})$. Therefore, the time complexity of using PCPS/DR-NSDE algorithm is $O[\mathbb{K}\mathbb{R}(\hat{f})]$. In other algorithms, including NSGA-II, NSPSO, MOPSO, and the individuals in the population, are referred to as particles or chromosomes, but the essence is the same. In calculations using these three algorithms, the number of particles/chromosomes is equally set to $\mathbb{R}$, and the number of iterations is equally set to $\mathbb{K}$. Thus, the time complexity is equally $O[\mathbb{K}\mathbb{R}\boldsymbol{f}]$. The complexity comparison of the four algorithms is shown in Table II.

Overall, the parameters $\mathbb{K}$ and $\mathbb{R}$ are the same for these algorithms, and the difference in time complexity arises from $\boldsymbol{f}$ and $\hat{f}$. Further combined with Table III, it can be seen that a single objective function computation based on the PCPS strategy saves much time, and therefore a complete iteration of the algorithm also saves a significant amount of time, which will be compared in Section VI.

TABLE II
COMPARISON OF THE COMPLEXITY FOR THE FOUR ALGORITHMS

Algorithm	$O(n)$
NSPSO	$O[\mathbb{K}\mathbb{R}(\boldsymbol{f})]$
NSGA-II	$O[\mathbb{K}\mathbb{R}(\boldsymbol{f})]$
MOPSO	$O[\mathbb{K}\mathbb{R}(\boldsymbol{f})]$
PCPS/DR-NSDE	$O[\mathbb{K}\mathbb{R}(\hat{\boldsymbol{f}})]$

TABLE III
COMPARISON OF THE RUNTIME FOR THE THREE OBJECTIVE FUNCTIONS (AVERAGED OVER TEN RUNS)

	Traditional (f_i)	PCPS strategy ($\hat{f}_i$)
Function 1	15.29 s	0.98 s
Function 2	<0.01 s	<0.01 s
Function 3	6.51 s	0.66 s

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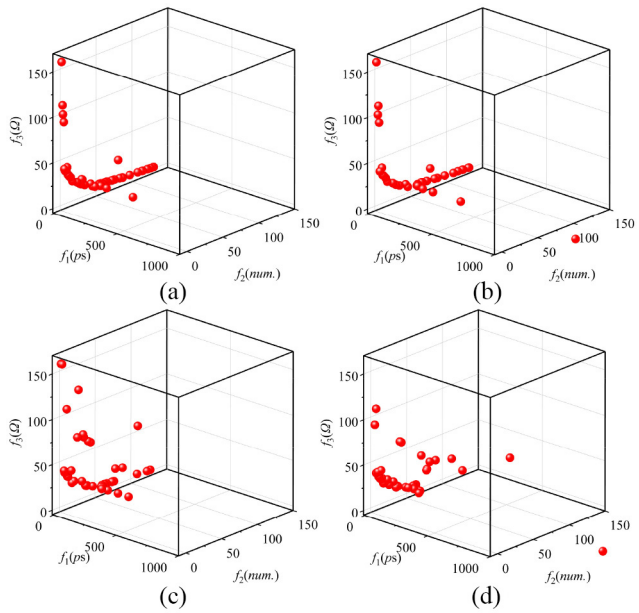

Fig. 12. Pareto fronts of Run 1. (a) PCPS/DR-NSDE. (b) NAGA-II. (c) MOPSO. (d) NSPSO.

VI. Numerical Results

In this section, the proposed PCPS/DR-NSDE algorithm is used to optimize 2.5-D electrical problems and the results obtained are compared with existing algorithms. Then, the methods for selecting desired solutions in the Pareto front and obtaining expected Pareto fronts under practical constraints are discussed. Finally, the effect of the target impedance on the 2.5-D electrical optimization is studied, and the influence of other structures on the 2.5-D system is also discussed.

A. Results and Comparison

To validate the proposed multiobjective optimization algorithm in the 2.5-D system, we use a test structure identical to that depicted in Fig. 3. The design parameters of the test structure are listed in Table I. Most parameters in Table I refer to the actual measurement-based literature [38], [39]. For other parameters, the values are as follows: $C_{pkg} = 26.40\ \mu$F, $L_{C,pkg} = 4.61$ pH, $R_{C,pkg} = 0.54$ mΩ, $L_{pkg} = 6.00$ pH, $R_{pkg} = 0.03$ mΩ, and $C_{\text{ESD}} = 50$ fF.

In this work, the parameters to be optimized are classified into three primary categories: 1) those related to the channel; 2) the buffer; and 3) the decoupling capacitor. These include specific parameters, such as channel dimensions (length, width, height, thickness, etc.), the number of buffer stages, MOS size, and the number of capacitors. The parameters of the hybrid objective functions are given as follows: $\mathcal{K} = 500$, $\mathcal{R} = 50$, $\mathcal{D} = 7$, $\hat{\theta}_0 = 0.4$, and $\tilde{\theta} = 0.1$.

We have chosen to compare our proposed algorithm with three other classical algorithms that demonstrate good performance: 1) NAGA-II; 2) MOPSO; and 3) NSPSO. Each algorithm is run five times and the results from the first run are shown in Fig. 12. Given that the Ubuntu point is unknown in the 2.5-D engineering problem, hypervolume and C-metric serve as the most suitable indicators for evaluating algorithm performance. Owing to the time-intensive computation of the hypervolume metric, the Monte Carlo estimation-based hypervolume is utilized in this work. All indicators used in this article are expressed in percentage form.

TABLE IV
Comparison of Hypervolume Indicator Values of Four Algorithms After Five Runs

Algorithm	PCPS/DR-NSDE	NSGA-II	MOPSO	NSPSO
Mean value	**0.937**	0.933	0.919	0.923
Run 1	**0.937**	0.933	0.929	0.926
Run 2	**0.937**	0.934	0.920	0.929
Run 3	**0.937**	0.932	0.911	0.923
Run 4	**0.937**	0.932	0.928	0.924
Run 5	**0.937**	0.934	0.909	0.911

TABLE V
Comparison of C-Metric Indicator Values of Four Algorithms After Five Runs

	C(PCPS/DR-NSDE,-)			C(-,PCPS/DR-NSDE)		
Algorithm	NSGA-II	MOPSO	NSPSO	NSGA-II	MOPSO	NSPSO
Run 1	**0.98**	**0.96**	**0.98**	0	0.02	0
Run 2	**0.98**	**0.9**	**0.98**	0	0.02	0
Run 3	**0.96**	**0.96**	**0.96**	0	0.02	0
Run 4	**0.96**	**0.96**	**0.94**	0	0	0
Run 5	**0.98**	**0.9**	**0.98**	0	0	0

TABLE VI
Comparison of the Runtime for the Four Algorithms

Algorithm	Average runtime
NSPSO	>1 day
NSGA-II	>1 day
MOPSO	>1 day
PCPS/DR-NSDE	51 min 32 s

The comparison of hypervolume indicators across different algorithms is shown in Table IV. The Pareto front generated by the PSC/DR-NSDE method possesses the maximum hypervolume indicator, demonstrating that the solution set has superior diversity and convergence. At the same time, as shown in Table V, it can be observed that the C(PSC/DR-NSDE, -) values are significantly larger than the C(-, PSC/DR-NSDE) values in all instances when compared with the three competitor algorithms. Meanwhile, it can be found that for the optimization problem in this article, the hypervolume indicator can accurately indicate the optimal algorithm, but there is no obvious difference among the indicator values. The C-metric can show a more distinct difference between the PCPS/DR-NSDE and other algorithms in this study.

The average runtime of five runs of each algorithm is presented in Table VI. It can be seen that the computational time of the objective function with the PCPS strategy is drastically reduced. In sum, the results show that the PCPS strategy-based DR-NSDE algorithm can save considerable time, and has the best performance in the 2.5-D problem.

B. Optimal Solutions Under Different Requirements

$$\begin{aligned} &\min\ \Psi = \gamma_1\varphi_1' + \gamma_2\varphi_2' + \gamma_3\varphi_3' \\ &\varphi_i' = \text{normalization}(\varphi_i) \\ &\text{s.t. } \varphi_1 \le \lambda_1(\text{ps}), \varphi_2 \le \lambda_2(\text{num.}), \varphi_3 \le \lambda_3(\Omega). \end{aligned} \quad (14)$$

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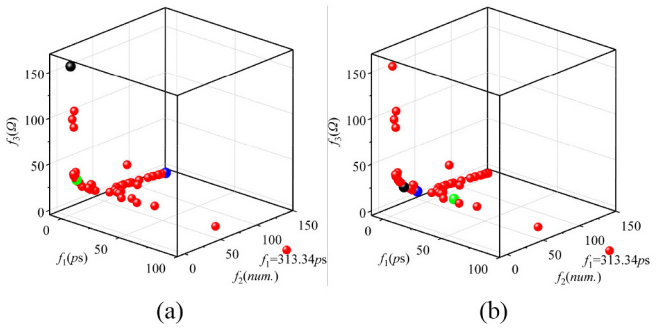

Fig. 13. Pareto fronts with (a) three minimum solutions and (b) three required optimal solutions.

As shown in Fig. 13(a), the minimum PSIJ solution, the minimum capacitor number solution, and the minimum total impedance difference solution are marked in green, black and blue, respectively. Moreover, among the three objective functions, different parameters can be defined in (14) in accordance with specific requirements. The unique solution with the minimum Ψ value can be obtained from all points in Pareto front, which is called the required optimal solution. The required optimal solution differs from the multiobjective optimization process and is calculated based on the defined parameters. φ_i represents the ith objective function value in the Pareto front. γ_i represents the weight coefficient of the ith objective function. λ_i represents the upper limit of the ith objective function in the Pareto front.

For instance, when $\gamma_1 = 1$, $\gamma_2 = 0$, $\gamma_3 = 0$, $\lambda_1 = 50$ ps, $\lambda_2 = 50$, $\lambda_3 = 10$ Ω, the goal of this parameter setting is to obtain a smaller PSIJ when the capacitor number and impedance do not exceed a specific value and the green ball represents the required optimal solution as shown in Fig. 13(b). When $\gamma_1 = 1/3$, $\gamma_2 = 1/3$, $\gamma_3 = 1/3$, the goal of this parameter setting is to make the three objective functions uniformly, and the corresponding required optimal solution is marked in black. When $\gamma_1 = 0.2$, $\gamma_2 = 0.2$, $\gamma_3 = 0.6$, the blue ball represents the required optimal solution, denoting less impedance. The first six cases in Fig. 14(a) and (b) show the corresponding impedance curves and placement schemes of the three minimum function solutions and the three required optimal solutions. For the contradictory multiobjective functions, achieving the minimum value for one function means that other functions cannot reach the optimal values, or might even yield poor values. For example, the minimum capacitor can reach zero, but the impedance curve at this time is bad. This method can identify solutions for various requirements within a single Pareto front.

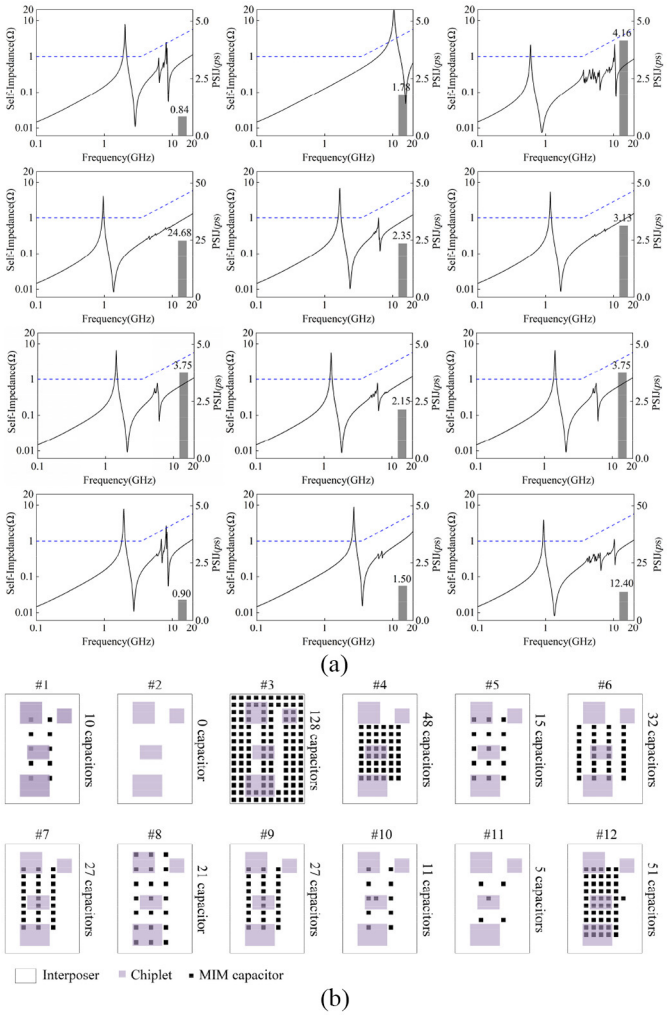

Fig. 14. Three minimum function solutions and the three required optimal solutions in the Pareto front. (a) Real impedance and target impedance curves. (b) Decoupling capacitor placement schemes.

C. Pareto Fronts Under Multiconstraints

Unlike the above approach of searching for the optimal solution in the Pareto front, a more intuitive and effective method is to introduce constraints in the proposed algorithm under more stringent conditions. General multiobjective optimization aims to find the compromise Pareto front where the value of each function is minimized. However, in the real 2.5-D design, there could be additional constraints rooted in the actual circuit, such as the channel jitter not exceeding a certain threshold, or the capacitor number in the interposer not exceeding a certain value, among others. As a result, the multiconstraints of the multiobjective functions are considered in

$$\begin{aligned} \text{s.t. } & f_1 \le \mathbb{N}_1(\text{ps}) \\ & f_2 \le \mathbb{N}_2(\text{num.}) \\ & f_3 \le \mathbb{N}_3(\Omega). \end{aligned} \tag{15}$$

To examine the influence of constraints on system multiobjective optimization, two sets of test cases with constraints $\mathbb{N}_1 = 20$ ps, $\mathbb{N}_2 = 50$ and $\mathbb{N}_3 = 30$ Ω and $\mathbb{N}_1 = 5$ ps, $\mathbb{N}_2 = 30$ and $\mathbb{N}_3 = 20$ Ω, are adopted, respectively. Each set comprises eight test cases with varying constraints, including case I with f_1, f_2, and f_3 constraints, case II with f_2 and f_3 constraints, case III with f_1 and f_3 constraints, case IV with f_1 and f_2 constraints, case V with f_1 constraints, case VI with f_2 constraints, case VII with f_3 constraints, and case VIII with no constraint. Fig. 15 shows the average values of each function of the Pareto front, where 50 represents the total number of solutions in the Pareto fronts, and the numerator represents

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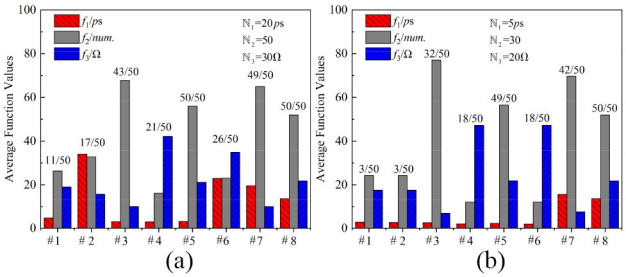

Fig. 15. Average values of each function under different constraints. (a) First set of test cases. (b) Second set of test cases.

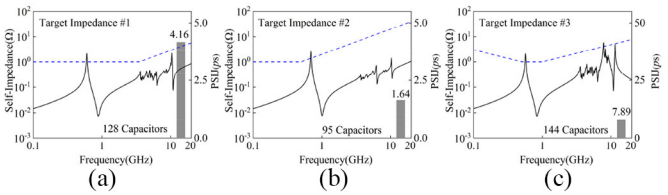

Fig. 16. Minimum sums of impedance difference in Pareo fronts under three different target impedance curves. (a) Target impedance 1. (b) Target impedance 2. (c) Target impedance 3.

the number of solutions that meet the constraints. In most cases, a specific constraint degrades the performance of other aspects of the 2.5-D circuit, reflecting a tradeoff. For example, in case III of each set, when the PSIJ and impedance are constrained, the capacitor number will increase. Furthermore, it can be found that although an increase in impedance elevates the SSN, there is no positive correlation between PSIJ and impedance. In each set, Case IV has a small PSIJ value, but the impedance is considerably high.

In addition, to clearly illustrate the tradeoffs in the multiobjective optimization process for 2.5-D circuits under constraints, six additional specific test cases with varying constraints are selected for analysis. These cases include case I with $\mathbb{N}_2 = 30$, $\mathbb{N}_3 = 20\ \Omega$, $\gamma_1 = 1$, $\gamma_2 = 0$, $\gamma_3 = 0$, case II with $\mathbb{N}_1 = 5$ ps, $\mathbb{N}_3 = 20\ \Omega$, $\gamma_1 = 0$, $\gamma_2 = 1$, $\gamma_3 = 0$, case III with $\mathbb{N}_2 = 30$, $\mathbb{N}_3 = 20\ \Omega$, $\gamma_1 = 0$, $\gamma_2 = 0$, $\gamma_3 = 1$, case IV with $\mathbb{N}_1 = 2\ ps$, $\gamma_1 = 0$, $\gamma_2 = 0.5$, $\gamma_3 = 0.5$, case V with $\mathbb{N}_2 = 5$, $\gamma_1 = 0.5$, $\gamma_2 = 0$, $\gamma_3 = 0.5$, case VI with $\mathbb{N}_3 = 10\ \Omega$, $\gamma_1 = 0.5$, $\gamma_2 = 0.5$, $\gamma_3 = 0$. The results of these cases are shown in the final six cases of Fig. 14(a) and (b). The first three cases show that when two parameters meet the constraints, the minimum value that the remaining parameter can reach is notably worse than the unconstrained cases mentioned above. The last three cases show the situation of a single constraint. When one objective function value satisfies a constraint, the other functions can be appropriately selected by setting proper weight coefficients. In the final three cases, under a single constraint, the remaining two uniform function values are selected from the Pareto fronts. Moreover, when the constraints and weight coefficients are manually defined, the proposed method can effectively guide the 2.5-D design.

D. Pareto Fronts Under Improved Target Impedance

According to the profound understanding of the circuit, various improved target impedances have been proposed. This article explores the effects of different target impedances, labeled as 1, 2, and 3 from [49], [50], and [51], on the multiobjective optimization of 2.5-D circuits. The Pareo fronts derived from multiobjective optimization of 2.5-D circuits vary according to the different target impedances. In Fig. 16, we compare the solutions with the smallest impedance differences in each Pareto front. It is observed that the number of optimal capacitors and the corresponding jitter values vary under different target impedances. Therefore, in the predesign stage of the chiplet-based circuits, the selection of a suitable target impedance becomes a pivotal decision, guided by the specific requirements of the system.

E. Other Methods to Improve System Performance

In this article, the electrical characteristics are improved by adjusting the channel structure, capacitor placement scheme, and chip placement scheme. In addition, the structure of the TSV array also affects the electrical performance of the system, such as a square or honeycomb TSV structure, formed by multiple ground TSVs [52], [53] and electromagnetic shielding of the signaling TSVs in the middle, can improve the system signal quality. In future work, we will consider the impact of the TSV array scheme on 2.5-D electrical properties.

In addition, optimizing the PDN parameters can further improve the electrical performance of 2.5-D IC. For example, a wider PDN grid results in lower resistance, making it easier to meet the target impedance in the low-frequency range. Increasing the TSV pitch can reduce mutual inductance and lower the PDN impedance at mid-to-high-frequency range. In future research, the optimization of PDN parameters will be investigated considering practical constraints.

F. Conclusion

In this article, for the first time, a novel PCPS/DR-NSDE algorithm is proposed to address the PSIJ, impedance, target impedance, and decoupling capacitor-based multiobjective problem in 2.5-D IC. An algorithm based on length judgment, minimum unit division, and *S*-parameter cascade is proposed to model the channel. Meanwhile, a uniform decoupling capacitor placement strategy is discussed to improve the design efficiency. A PCPS strategy is applied for the high-time-consuming modules. Compared to classic multiobjective algorithms, the gained Pareto front has the best-hypervolume C-metric indicators among the four algorithms. Selecting appropriate constraints and target impedance, the proposed method is valuable in the 2.5-D IC predesign.

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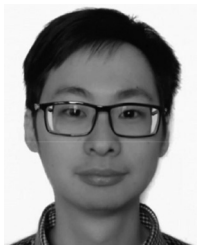
Changle Zhi received the B.S. degree in microelectronics science and engineering from the Harbin University of Science and Technology, Harbin, China, in 2018, and the Ph.D. degree in microelectronics and solid-state electronics from Xidian University, Xi'an, China, in 2023.

He is currently a Postdoctoral Fellow with the School of Integrated Circuits, Xidian University. His research interests include high-density integration technology and chiplet-based microsystem design.

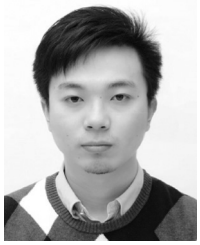
Gang Dong received the B.S., M.S., and Ph.D. degrees in microelectronics and solid-state electronics from Xidian University, Xi'an, China, in 2000, 2003, and 2004, respectively.

He is currently a Professor with the School of Microelectronics, Xidian University. His research interests include high-density integration technology and chiplet-based microsystem design.



Wei Xiong received the B.S., M.S., and Ph.D. degrees in microelectronics and solid-state electronics from Xidian University, Xi'an, China, in 2013, 2016, and 2023, respectively.

His research interests include high-density integration technology and chiplet based microsystem design. His research interests include 3-D integration and microwave passive device design.



Deguang Yang received the B.S. degree in integrated circuit design and integrated system from the Qingdao University of Science and Technology, Qingdao, China, in 2019. He is currently pursuing the Ph.D. degree in microelectronics and solid-state electronics with Xidian University, Xi'an, China.

His research interests include artificial intelligence-based signal and power integrity design and analysis for 3-D ICs.

Daihang Liu received the B.S. degree in integrated circuit design and integrated system from Xidian University, Xi'an, China, in 2019, where he is currently pursuing the Ph.D. degree in microelectronics and solid-state electronics.

His research interests include artificial intelligence-based electrothermal design and analysis for 3-D ICs.

Yinghao Feng received the B.S. degree in integrated circuit design and integrated system from Xidian University, Xi'an, China, in 2020, where he is currently pursuing the M.S. degree in integrated circuit engineering.

His research interests include artificial intelligence-based electrothermal design and analysis for 3-D ICs.

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Yang Wang received the B.S. degree in integrated circuit design and integrated system from Xidian University, Xi'an, China, in 2018, where he is currently pursuing the Ph.D. degree in microelectronics and solid-state electronics.

His research interests include artificial intelligence-based signal and power integrity design and analysis for 3-D ICs.

Zhangming Zhu received the B.S., M.S., and Ph.D. degrees in microelectronics from Xidian University, Xi'an, China, in 2000, 2003, and 2004, respectively.

Since 2009, he has been a Professor with the School of Microelectronics, Xidian University, where he is the Director of the Institute of Integrated Circuit. He has published more than 170 papers in IEEE journal. His current research interests include ADC/DAC and AFE, analog integrated circuits, RF integrated circuits, integration of opto-sensing and computing, and intelligent edge computing for sensors.

Prof. Zhu serves as an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEM PART II—EXPRESS BRIEFS and as an Editor in Chief for the *Microelectronics Journal* (Elsevier).

Yintang Yang (Senior Member, IEEE) received the B.S. and M.S. degrees in semiconductor devices and microelectronics from Xidian University, Xi'an, China, in 1982 and 1984, respectively.

He was a Professor and an Advisor of Ph.D. candidates. He is successively the Director of the Research Institute of Microelectronics, the Deputy Dean of the School of Technical Physics, the Dean of the School of Microelectronics, and the Vice President of Xidian University. His current research interests include high-speed data converters, 3-D integrated circuits, network-on-a-chip, and new semiconductor devices.

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