TCI Tester: Tester for Through Chip Interface

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1 TCI AND FAMILY CHIPS

TCI[1] is an inductive coupling wireless chip-to-chip interface. For forming a link with TCI, the transmitter coils are placed just above receivers' ones, and data are transferred between them through the magnetic field. Each TCI channel needs two inductors, one for a high-speed clock signal (1-8GHz) and the other for the data directly transfer digital data synchronized with the clock signal without any modulation. TCI has the following advantages. First, the inductor consists of common wires in the CMOS process technology without the particular process technology, unlike the TSV. Also, ESD (Electro Static Discharge) protection device is unnecessary, since TCI is electrically contact-less.

In order to embed TCI links on various chips, IPs (Intellectual Properties) have been developed for the Renesas 65nm SOTB process supported by VDEC[3]. TCI IP consists of coils, transmitter, receiver, and SERDES (Serializer/De-serializer). The coils for the data and clock signals are realized by duplex winding for its transceiver and receiver, which allows switching the communication direction of the link within a few clock cycles. The internal VCO's frequency is designed to be 2.5GHz. Hence, 35-bit data can be transferred at 50MHz of the operational frequency. In other words, this IP can be treated as a simple 35-bit uni-directional registered channel. The diameter of each coil is 240μm × 240μm to build a link between the chip with 80μm thickness. The size of the entire IP is 510μm × 410.8μm. We designed family chips[2] including an embedded CPU, accelerators and shared memory with TCI IP as shown in in Table 1 to try various combination.

2 TCI TESTER

2.1 Overview of TCI Tester

TCI Tester is designed to be stacked on TCI family chips for monitoring how TCI IP on the target chip works.

Table 1: Spec. of family chips

TCI Tester	Chip for testing TCI
GeyserTT	MIPS R3000 host processor
CCSOTB2	Coarse grained reconfigurable accelerator
SNACC	Neural Network Accelerator
KVS	Key value store accelerator
SMTT	Shared Memory for Twin Tower
Process	Renesas 65nm DLSOTB_V3 CMOS 7 Metal
Area	3mm × 3mm (TCITester) 6mm × 6mm (SMTT) / 6mm × 3mm (others)
Chip Thickness	80μm
Supply Voltage	0.75V (digital) / 1.2V (TCI)
Target Freq.	100MHz (SMTT) / 50MHz (Others)
TCI IP	35bit/50MHz 2.5GHz transfer clock
CAD	Synopsys Design Compiler 2016.03-SP4 Synopsys IC Compiler 2016.03-SP4

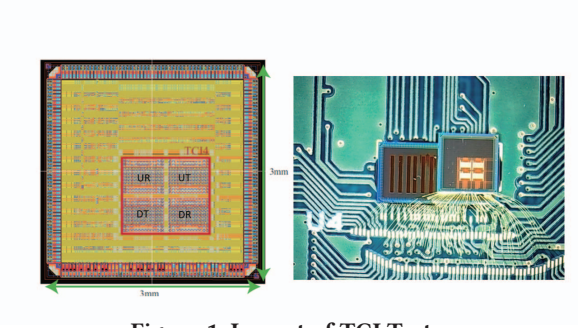

Figure 1: Layout of TCI Tester

TCI Tester consists of the TCI IP (TCI4), serial interface, on-chip router, data memory in the memory controller, and the loop check module. These modules are used in each mode of TCI Tester. Like other target chips, TCI Tester provides four sets of TCI IP (called "TCI4") as shown in the left side of Fig.1. The right side shows an example to stack TCI Tester on CC-SOTB2. The specification of TCI Tester is also the same as other target chips as shown in Table.1.

TCI Tester has three modes: RAW mode, CUBE mode and LOOP mode for testing the target chip. (1) RAW mode controls TCI handshake signals directly from outside the chip. Only a transfer is done by manipulating handshake lines. The overwrite error, frame error and parity error can be detected by checking each signal. (2) CUBE mode behaves just like the family chips, that is it can send and receive the 35bits packets. (3) LOOP mode generates packets, receives them and check the transferring results iteratively. If error is found, it stops, otherwise it works forever.

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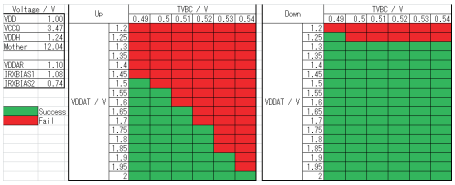

Figure 2: Voltage of transmitter for which communication succeeded

3 TESTING RESULTS WITH TCI TESTER

TCI Tester has been stacked on family chips in Table 1 like the photo shown as Fig. 1. Various measurement data have been acquired, but here, from the page limitation, we show the basic performance of the TCI IP measured with two stacked TCI Testers. They communicate with each other bi-directionally; upward (data transfer from the lower chip to the upper chip) and downward (data transfer from the upper chip to the lower chip).

First, we evaluated the basic characteristics of the TCI IP. The performance of the transmitter is controlled by its supply voltage VDDAT and the bias voltage TVBC. TVBC scales the clock frequency TxCLK generated by the ring oscillator, and with higher TVBC, higher TxCLK is generated. Data are transferred synchronized with TxCLK. The sensitivity of the receiver is controlled with two bias voltages IRXBIAS1 and IRXBIAS2. We found that whether data is successfully transferred or not is highly depending on TVBC and VDDAT.

Fig.2 shows whether the data transfer is successfully done or not depending on VDDAT and TVBC. Cells marked green is the case the data transfer was successful, and the red one means failed. In this figure, two columns "UP" and "DOWN" respectively mean upward and downward communications. Since the higher TVBC makes a higher operational clock, the high VDDAT is required. The results show that there is a big difference between upward ("UP") and downward ("DOWN"). Although the downward communication is successful with more than 1.3V VDDAT, the upward communication requires high VDDAT especially for transferring with a high TxCLK.

We examined the relationship between TVBC and TxCLK (frequency of data transferring), and shows the results with VDDAT=1.5V in Fig.3. Since TxCLK is too high to be directly measured, it was calculated by the width of TXBUSY. SPICE simulation results are also added to the figure. Note that the simulation used the parameter of PDK to DLSOTB_V03 in 2017, the same one used in TCI Tester. When TVBC increased, TxCLK also increased but both results from the real chip are lower than simulation results which achieved 2.5GHz. TxCLK of downward communication reaches 2GHz, while one of upward communication only achieves 1.5GHz. That is, the data transfer performance of the upward direction is worse than the downward direction, and both are lower than the simulation results. The layout analysis results suggested that the resistance of the VDDAT power grid for "UP" coils is much larger than that for the "DOWN" coils, and it is a reason why the performance of "UP" link is worse than "DOWN" link.

In order to investigate the realistic data transfer, we used CUBE mode and checked whether memory writes operations from a chip to another are successful or not. TVBC is controlled so that the maximum data transfer clock was achieved. Note that the TCI IP can transfer 35-bit digital data in a clock cycle. The flow control is disabled for uni-directional communication. As a result, downward communication succeeded when the digital clock was 14MHz or lower. With the same condition, the maximum clock frequency of the upward communication was the only 9MHz. As prospected with the results using RAW mode, it appeared that the transfer performance of upward communication is lower than that of the downward communication.

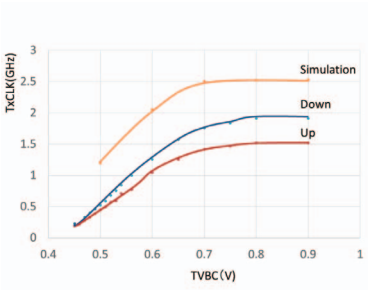

Figure 3: Relationship between TVBC and TxCLK

We tried continuous data transfer tests by using LOOP mode. VDDAT is set to be 1.75V, and TVBC = 0.51V. At that time, it worked at 10MHz digital clock, and continuous data transfer was successful 1×10^9 times on average. When we lowered the operational frequency to 8MHz, no error was detected for more than one day. The results suggest that although the current TCI IP does not work at designed operational clock frequency, once it works at a lower frequency, it has enough reliability.

We also measured the TCI performance of other family chips by stacking TCI Tester on them. For SNACC, CC-SOTB2 and SMTT, the similar problems were found; that is, (1) the data transfer performance of "UP" direction is worse than "DOWN" direction, and (2) the total performance is lower than the simulation results. We think the problem is on the location of the TCI IP, the number of I/O pads for power/ground, and the way to form the power grid. We are now establishing the rule to place the TCI IP related to the location of power I/O pads, and how to make the power grid. These results show that TCI Tester was really useful as a chip for measurement.

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