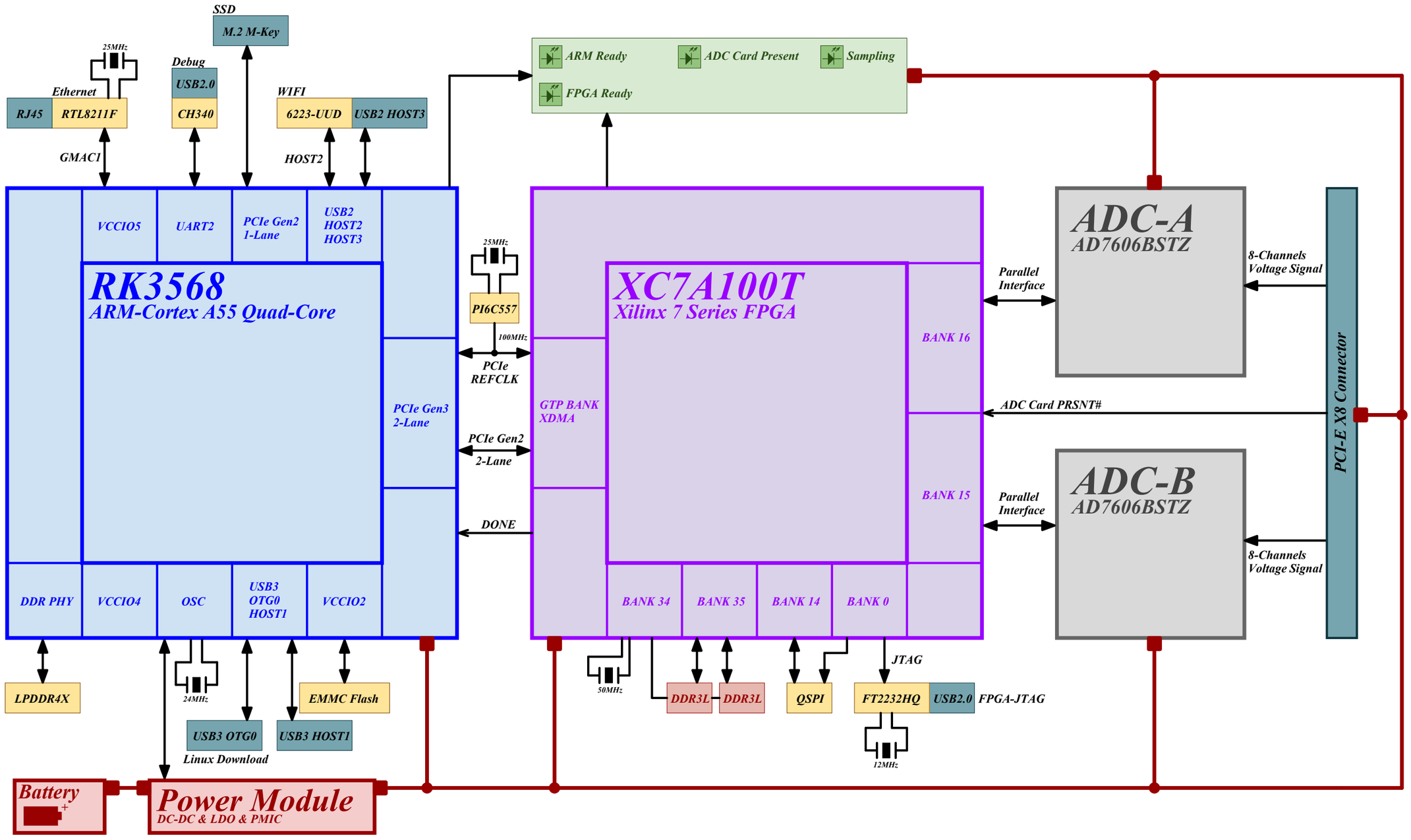
Revision History

Version	Date	Author	Dsecription
V1.0	2025-5-15	Shixuan Liu	First confirmation, some resistors & capacitors have been reserved.
V1.1	2025-7-13	Shixuan Liu	Circuit inspection completed.

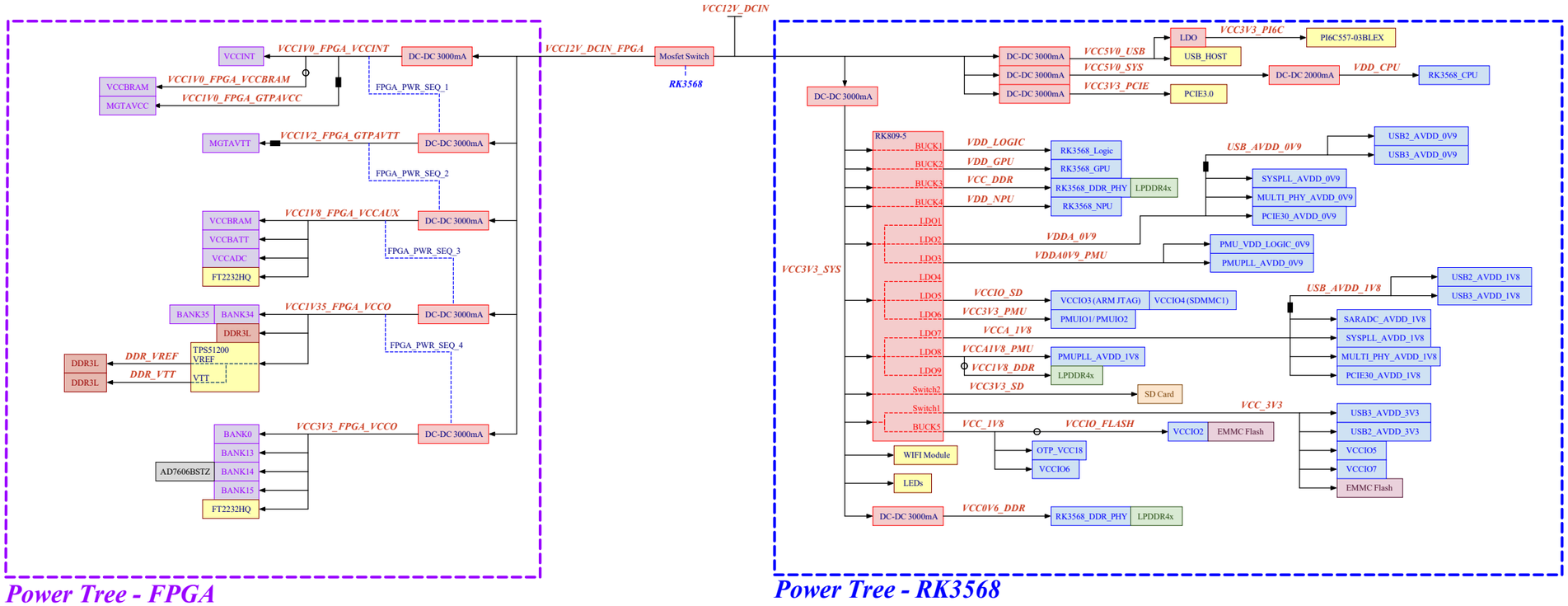
System Block Diagram



Vehicle-Under Fault Positioning and Recognition System

Shixuan Liu 2025.5

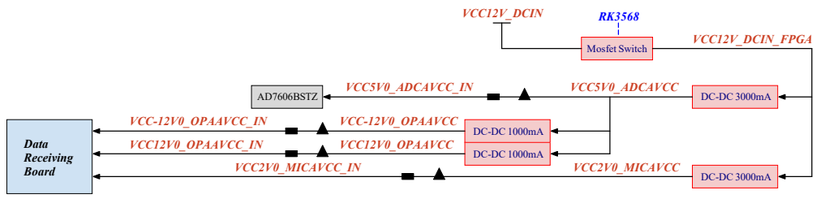
Power Tree - Digital Circuit



Legend

- Pins of ADC
- Pins or Power Domain of RK3568
- Pins or Power Domain of FPGA
- LPDDR4x
- eMMC Flash
- DDR3L
- Other Logic Chips
- DC-DC or LDO
- SD Card Module
- VCC_3V3 — Name of power net
- Short circuit by 0 Ohm resistors
- Ferrite Bead
- Output Control

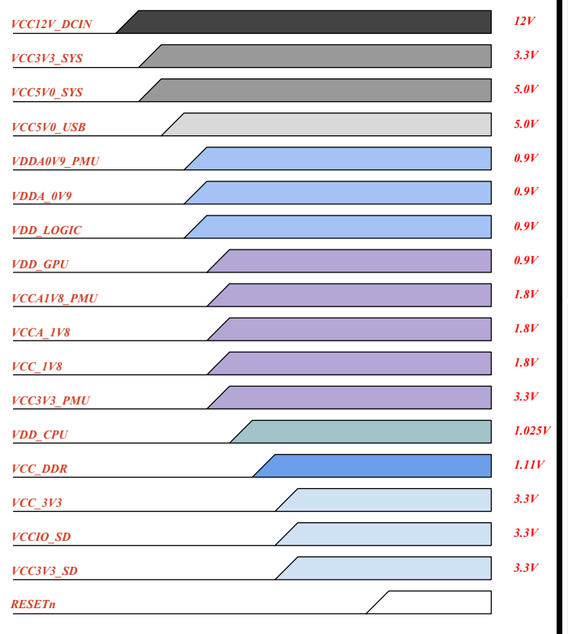
Power Tree - ADC & Analog Circuit



Legend

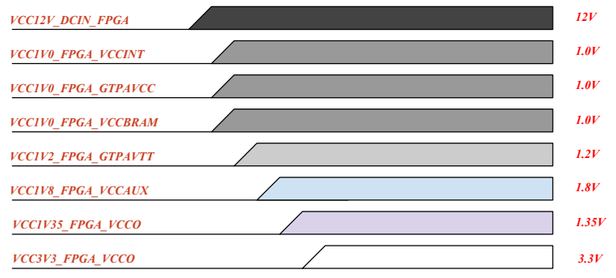
- Pins of ADC
- DC-DC
- Other Logic Chips
- VCC_3V3 — Name of power net
- Short circuit by 0 Ohm resistors
- Ferrite Bead
- RC Snubber Circuit

Power On Sequence - RK3568

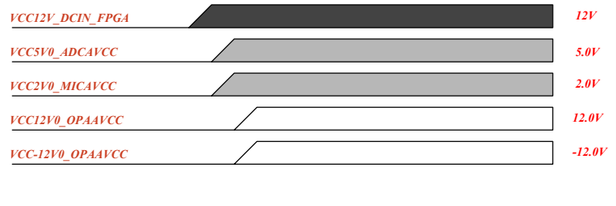


Power On Sequence - FPGA

*NOTE: Ramp time from GND to 90% of VCC*_FPGA_* must in range [0.2 ms - 50 ms]*



Power On Sequence - ADC & Analog Circuit



Contents

Abbreviations

DNP = Do not place this element

PUP = Place under the chip package (only for capacitors)

CTP = Place close to the chip package (only for capacitors)

Differential = Differential Impedance

Single = Single-ended Impedance

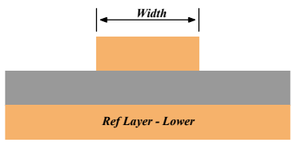
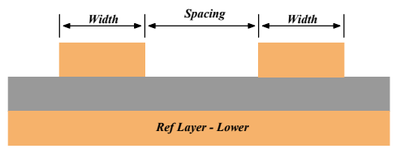
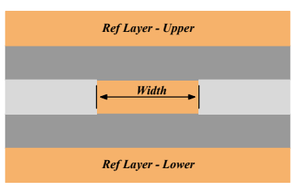
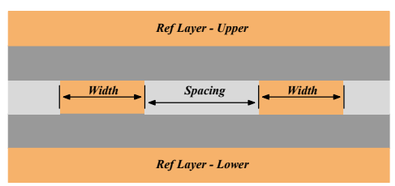
RK3568 Power Domain

Power Domain	Supply Voltage	Notes
PMUIO2	3.3V	
VCCIO1	OFF	
VCCIO3	3.3V	
VCCIO4	3.3V	
VCCIO5	3.3V	
VCCIO6	1.8V	
VCCIO7	3.3V	
PMUIO0	1.8V	Fixed
PMUIO1	3.3V	Fixed
VCCIO2	1.8V	FLASH_VOL_SEL = 1

Impedance Parameters

Impedence Template: JLC081611-1080

Impedance Form	Impedance	Layer	Ref Layer - Upper	Ref Layer - Lower	Width (mil)	Spacing (mil)
Single-ended	50 Ohm	Top		L2	4.12	
	50 Ohm	Top		L3	13.82	
	50 Ohm	L3	L2	L4	4.55	
	50 Ohm	L6	L5	L7	4.55	
	50 Ohm	Bottom	L7		4.12	
Differential	85 Ohm	Top		L2	4.67	6
	85 Ohm	L3	L2	L4	4.62	6
	85 Ohm	L6	L5	L7	4.62	6
	85 Ohm	Bottom	L7		4.67	6
	90 Ohm	Top		L2	4.10	6
	90 Ohm	L3	L2	L4	3.97	6
	90 Ohm	L6	L5	L7	3.97	6
	90 Ohm	Bottom	L7		4.10	6
	100 Ohm	Top		L2	3.6	9
	100 Ohm	L3	L2	L4	3.62	9
	100 Ohm	L6	L5	L7	3.62	9
	100 Ohm	Bottom	L7		3.6	9

Single-ended Traces	Differential Traces
Microstrip Line	Microstrip Line
	
Strip Line	Strip Line
	

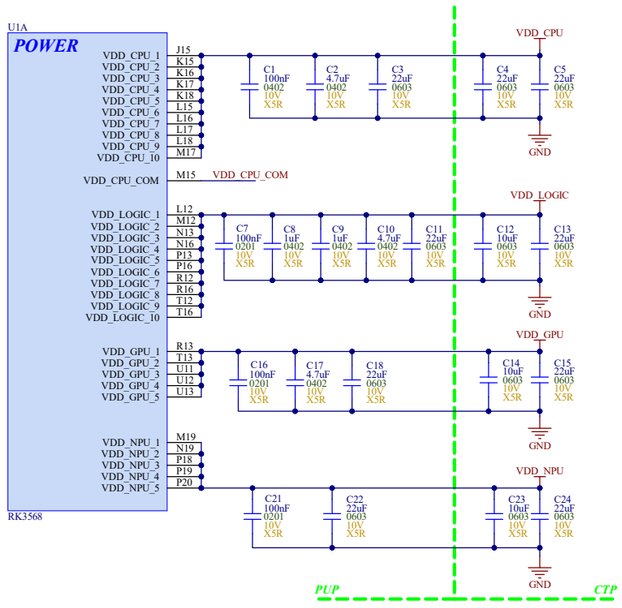
Calculation Basis: https://tools.jlc.com/jlcTools/#/impedanceCalculateNew

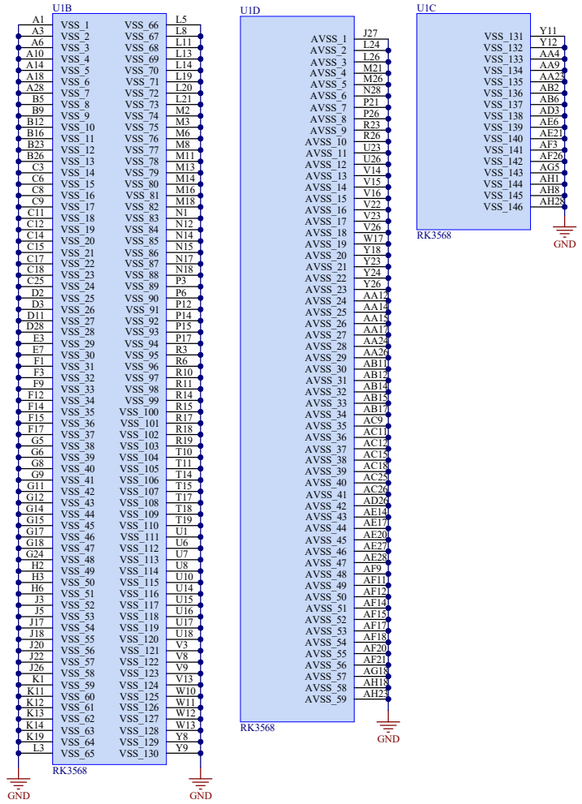
PCB Stacked Structure

Impedence Template: JLC081611-1080

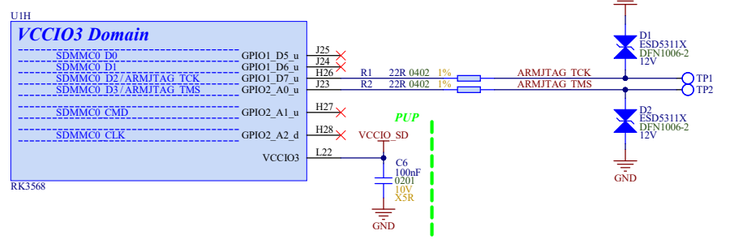
Symmetrical to the above

Power & Gnd

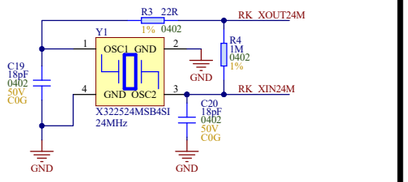




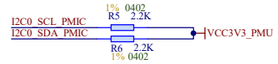
ARM JTAG



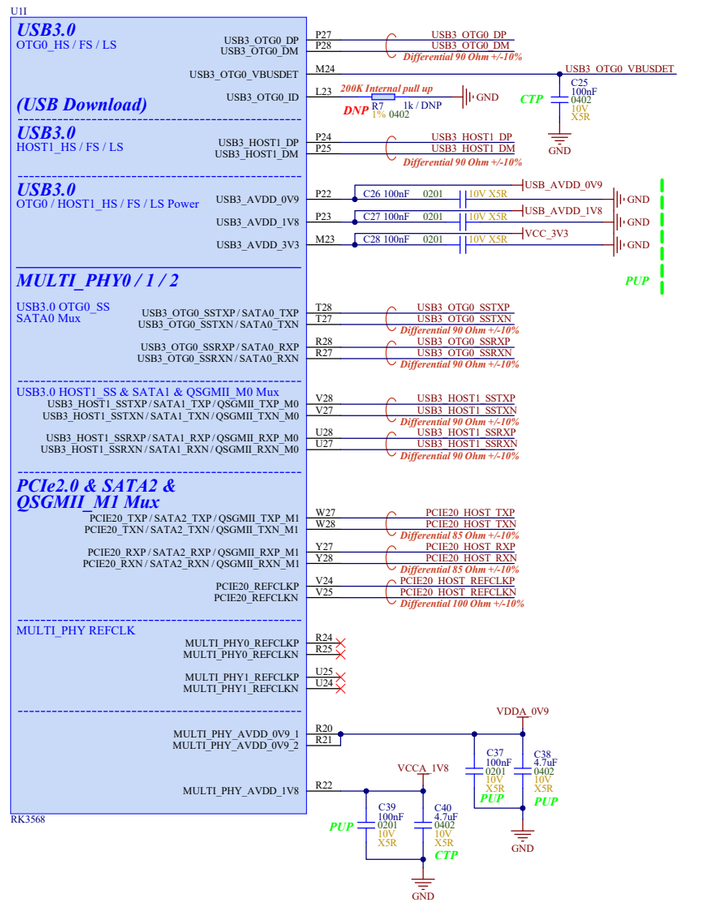
RK3568 System Clock



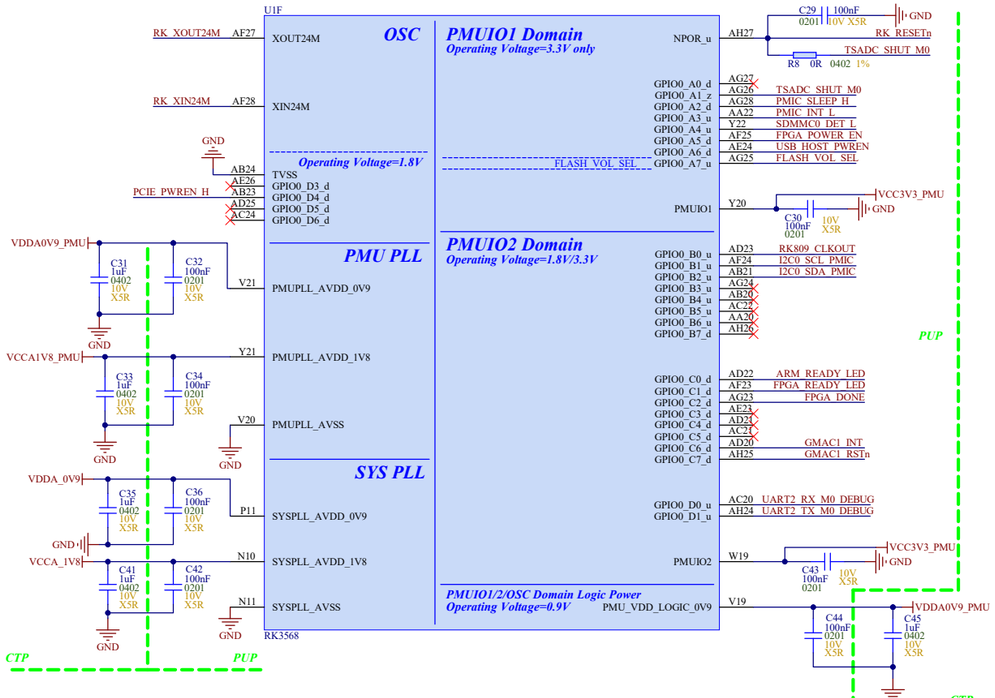
RK3568 PMIC IIC



USB3.0 OTG0 / USB3.0 HOST1



OSC / PLL / PMUIO1 / PMUIO2



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Size	Number		Revision
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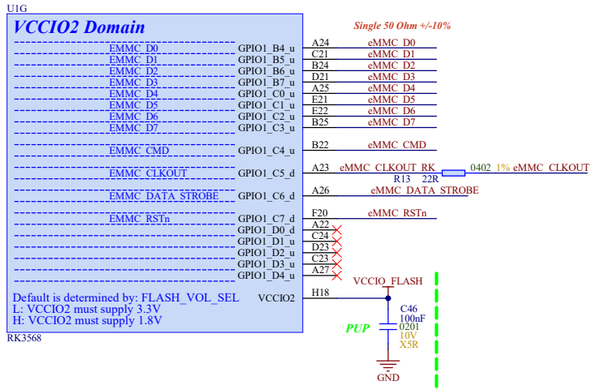
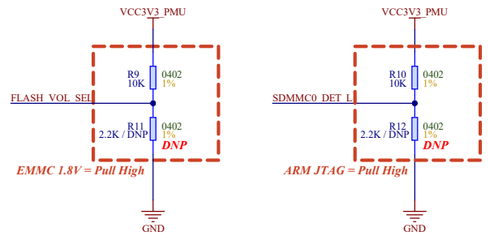
File:	C:\Users\...\RK3568-SCH1.SchDoc	Drawn By:	Shixuan Liu

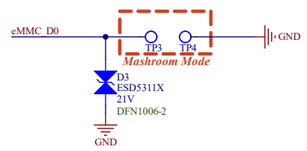
EMMC Flash Controller



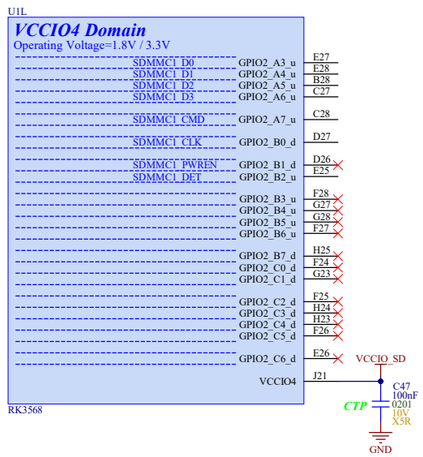
FLASH_VOL_SEL & SDMMC0_DET



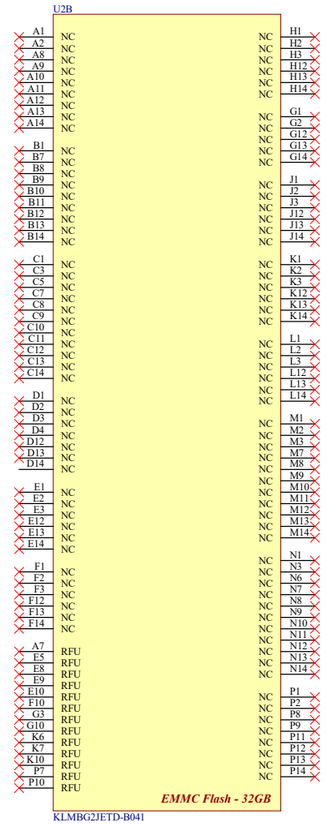
Mashrom Test Point



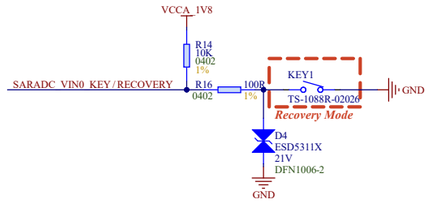
SD Card Control



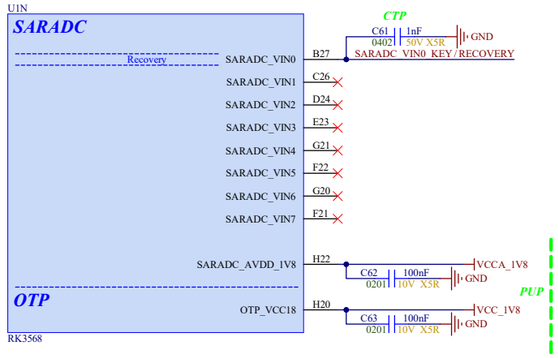
EMMC Flash - NC



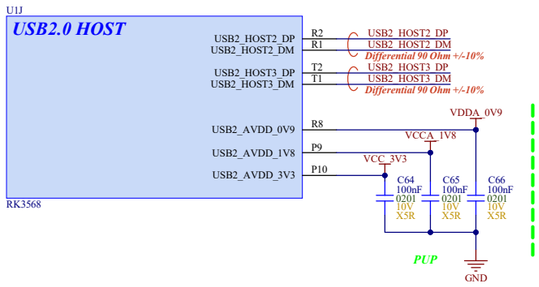
RECOVERY



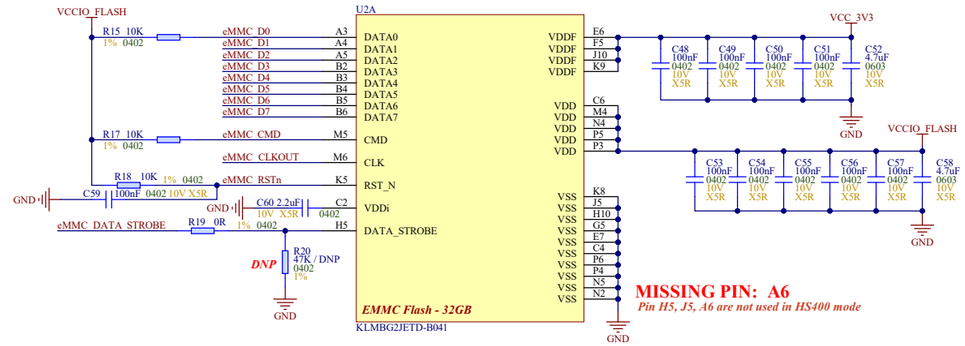
SARADC & OTP



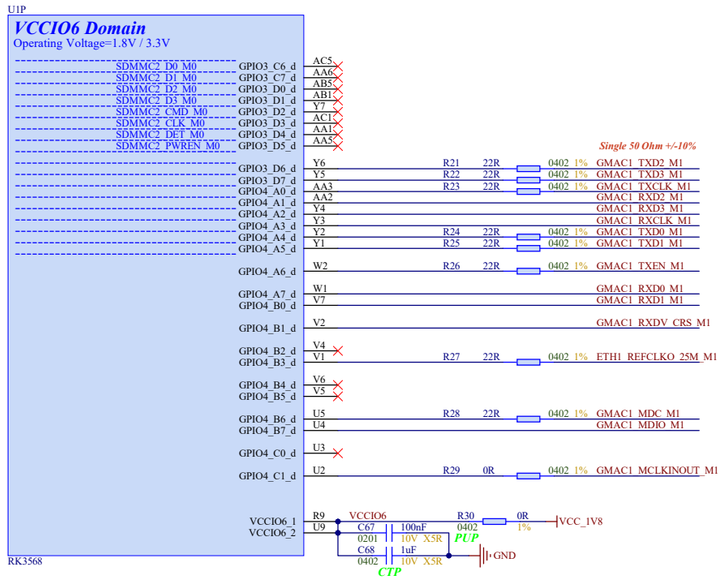
USB2.0 HOST2 / HOST3



EMMC Flash

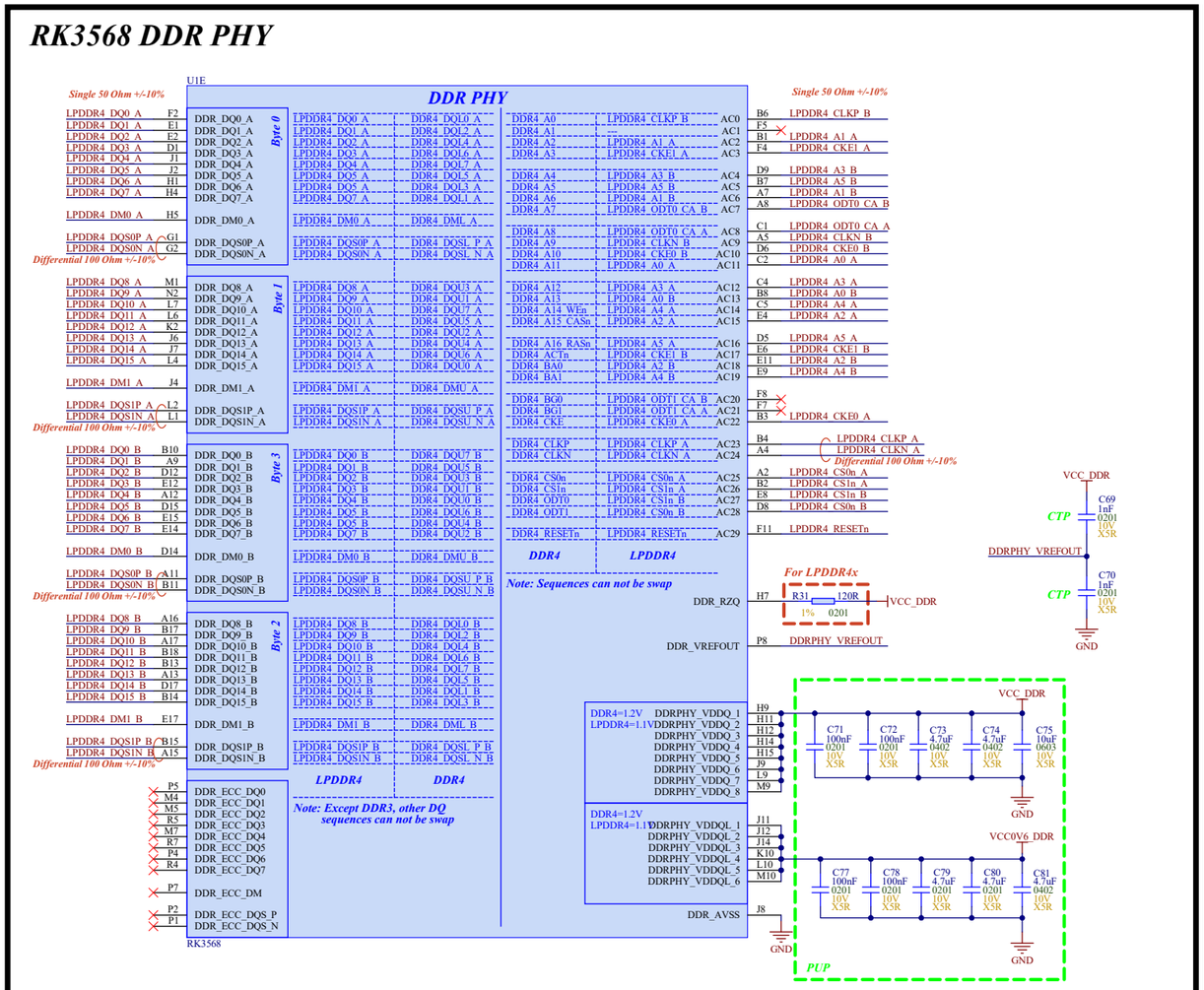


Ethernet

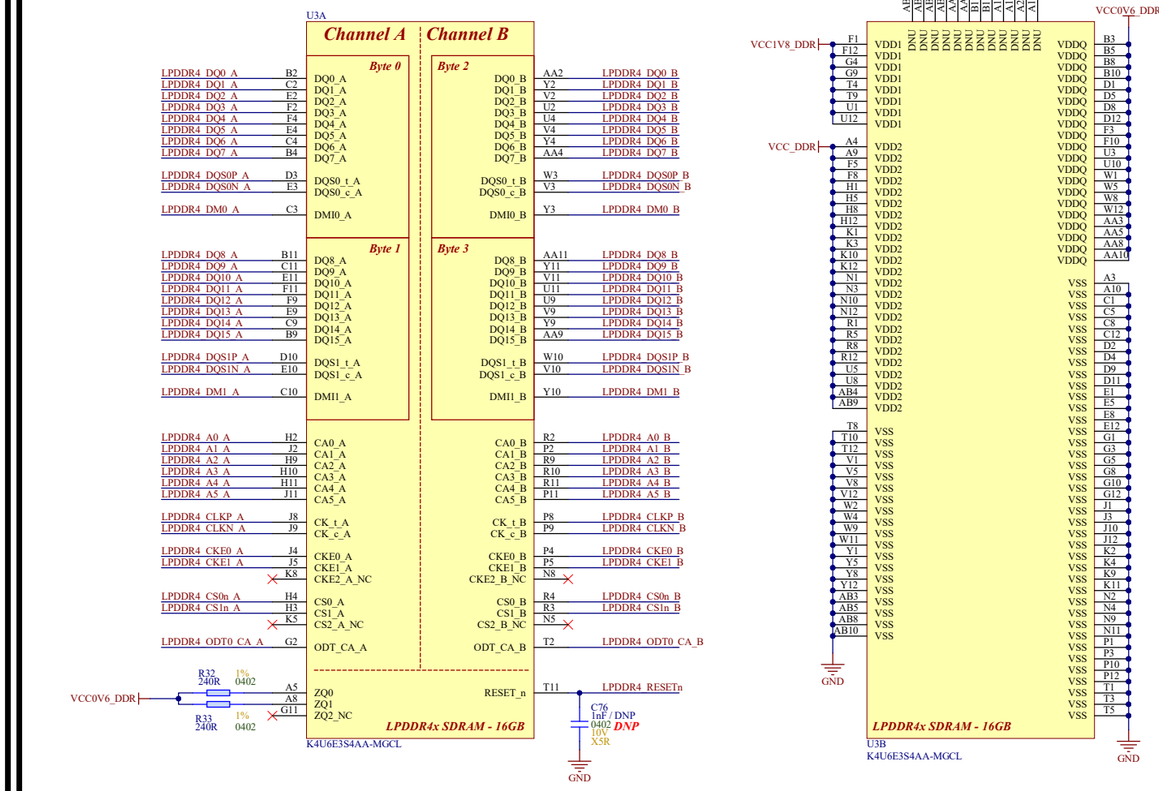


Title: RK3568 Schematic B		
Size: A2	Number:	Revision: V1.0
Date: 7/17/2025		Sheet 2of 15
File: C:\Users\..\RK3568-SCH2.SchDoc		Drawn By: Shixuan Liu

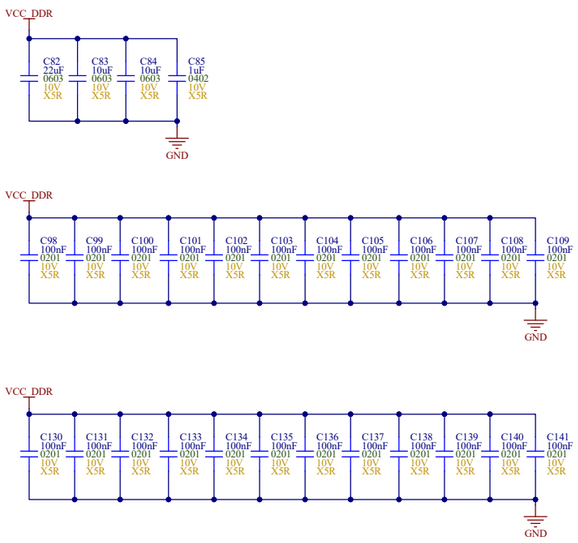
RK3568 DDR PHY



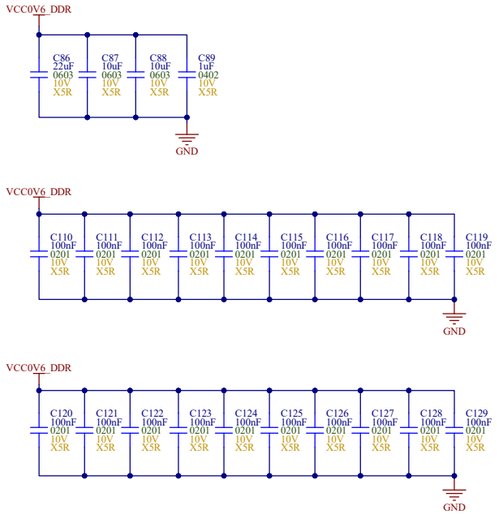
RK3568 LPDDR4x



LPDDR4x Decoupling Capacitors - VCC_DDR



LPDDR4x Decoupling Capacitors - VCC0V6_DDR



LPDDR4x Decoupling Capacitors - VCC1V8_DDR

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Date: 7/17/2025		Sheet 3of 15
File: C:\Users\..\RK3568-SCH3.SchDoc		Drawn By: Shixuan Liu

Unused Modules - RK3568

U1O

MIPI CSI RX

MIPI_CSI_RX_D0P	AG12
MIPI_CSI_RX_D0N	AH12
MIPI_CSI_RX_D1P	AG11
MIPI_CSI_RX_D1N	AH11
MIPI_CSI_RX_D2P	AE11
MIPI_CSI_RX_D2N	AD11
MIPI_CSI_RX_D3P	AD9
MIPI_CSI_RX_D3N	AE9
MIPI_CSI_RX_CLK0P	AG10
MIPI_CSI_RX_CLK0N	AH10
MIPI_CSI_RX_CLK1P	AG9
MIPI_CSI_RX_CLK1N	AH9
MIPI_CSI_RX_AVDD_0V9	W14
MIPI_CSI_RX_AVDD_1V8	Y14

RK3568

GND

U1Q

MIPI DSI TX0 / LVDS TX0

MIPI_DSI_TX0_D0P / LVDS_TX0_D0P	AH17
MIPI_DSI_TX0_D0N / LVDS_TX0_D0N	AG17
MIPI_DSI_TX0_D1P / LVDS_TX0_D1P	AH16
MIPI_DSI_TX0_D1N / LVDS_TX0_D1N	AG16
MIPI_DSI_TX0_D2P / LVDS_TX0_D2P	AH14
MIPI_DSI_TX0_D2N / LVDS_TX0_D2N	AG14
MIPI_DSI_TX0_D3P / LVDS_TX0_D3P	AH13
MIPI_DSI_TX0_D3N / LVDS_TX0_D3N	AG13
MIPI_DSI_TX0_CLKP / LVDS_TX0_CLKP	AH15
MIPI_DSI_TX0_CLKN / LVDS_TX0_CLKN	AG15
MIPI_DSI_TX0 / LVDS_TX0_AVDD_0V9	W16
MIPI_DSI_TX0 / LVDS_TX0_AVDD_1V8	Y17

RK3568

GND

U1R

MIPI DSI TX1

MIPI_DSI_TX1_D0P	AD18
MIPI_DSI_TX1_D0N	AE18
MIPI_DSI_TX1_D1P	AD17
MIPI_DSI_TX1_D1N	AC17
MIPI_DSI_TX1_D2P	AD14
MIPI_DSI_TX1_D2N	AC14
MIPI_DSI_TX1_D3P	AD12
MIPI_DSI_TX1_D3N	AE12
MIPI_DSI_TX1_CLKP	AD15
MIPI_DSI_TX1_CLKN	AE15
MIPI_DSI_TX1_AVDD_0V9	W15
MIPI_DSI_TX1_AVDD_1V8	Y15

RK3568

GND

U1S

eDP_TX

eDP_TX_D0P	J28
eDP_TX_D0N	K27
eDP_TX_D1P	K28
eDP_TX_D1N	L27
eDP_TX_D2P	L28
eDP_TX_D2N	M27
eDP_TX_D3P	M28
eDP_TX_D3N	N27
eDP_TX_AUXP	L25
eDP_TX_AUXN	M25
eDP_TX_AVDD_0V9	M20
eDP_TX_AVDD_1V8	M22

RK3568

GND

U1T

HDMI2.0 TX

HDMI_TX_D2P	AG22
HDMI_TX_D2N	AH22
HDMI_TX_D1P	AG21
HDMI_TX_D1N	AH21
HDMI_TX_D0P	AG20
HDMI_TX_D0N	AH20
HDMI_TX_CLKP	AH19
HDMI_TX_CLKN	AG19
HDMI_TX_HPDIN	AB18
HDMI_TX_REXT	AA18
HDMI_TX_AVDD_0V9_1	V17
HDMI_TX_AVDD_0V9_2	V18
HDMI_TX_AVDD_1V8	W18

RK3568

GND

U1M

VCCIO7 Domain

Operating Voltage=1.8V / 3.3V

GPIO4_C2_d	AF8
GPIO4_C3_d	AA11
GPIO4_C4_d	AH7
GPIO4_C5_d	AD8
GPIO4_C6_d	AE8
GPIO4_C7_u	AG8
GPIO4_D0_u	AG7
GPIO4_D1_u	AH6
GPIO4_D2_d	AB9
VCCIO7	V12

VCC_3V3

C142 100nF 0201 10V X5R

PUP

GND

RK3568

U1V

VCCIO1 Domain

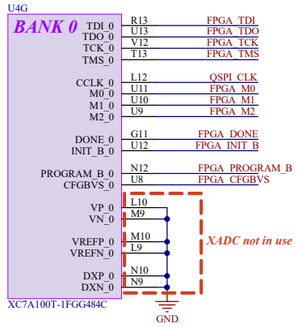
Operating Voltage=1.8V / 3.3V

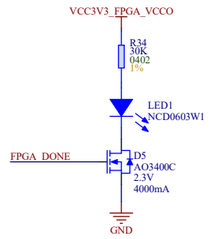
GPIO1_A0_u	D18
GPIO1_A1_u	E18
GPIO1_A2_d	A19
GPIO1_A3_d	B19
GPIO1_A4_d	F18
GPIO1_A5_d	A20
GPIO1_A6_d	C20
GPIO1_A7_d	B20
GPIO1_B0_d	D20
GPIO1_B1_d	E20
GPIO1_B2_d	A21
GPIO1_B3_d	B21
VCCIO1	H17

RK3568

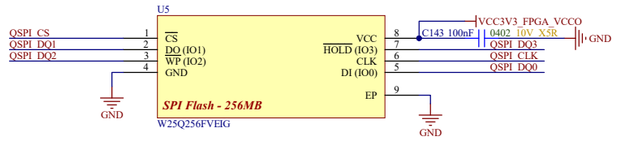
Title	RK3568 Schematic D		
Size	A2	Number	Revision V1.0
Date:	7/17/2025		Sheet 4of 15
File:	C:\Users\..\RK3568-Unused.SchDoc		Drawn By: Shixuan Liu

FPGA Config - BANK 0

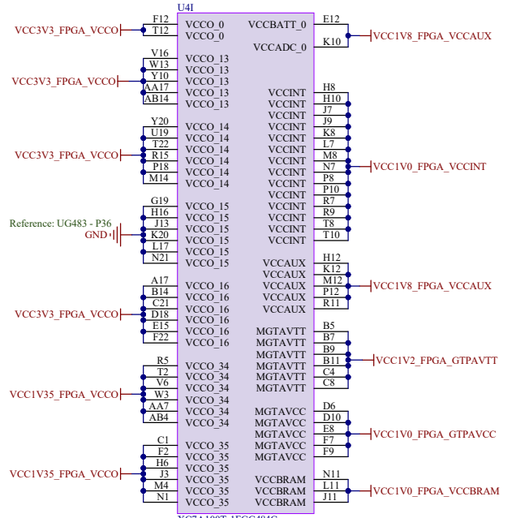


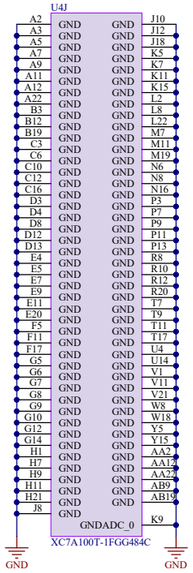


FPGA Config - SPI Flash

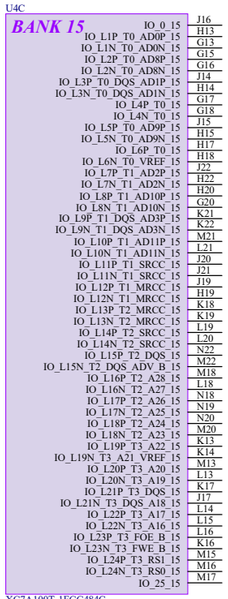


FPGA Power & Gnd

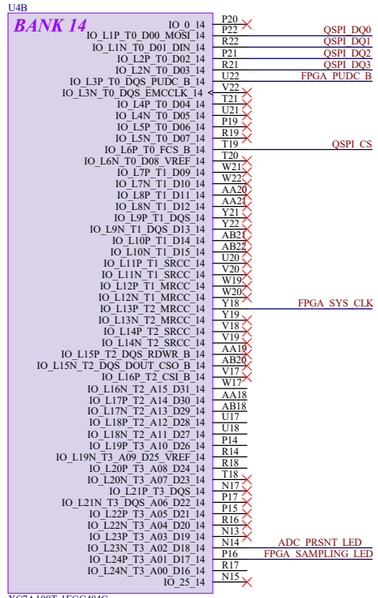




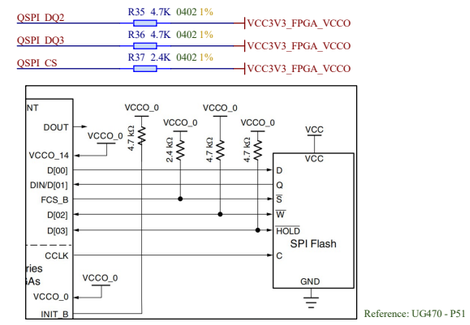
Unused Modules - FPGA



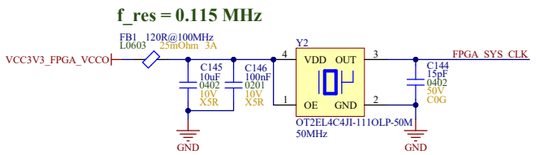
FPGA Config - BANK 14



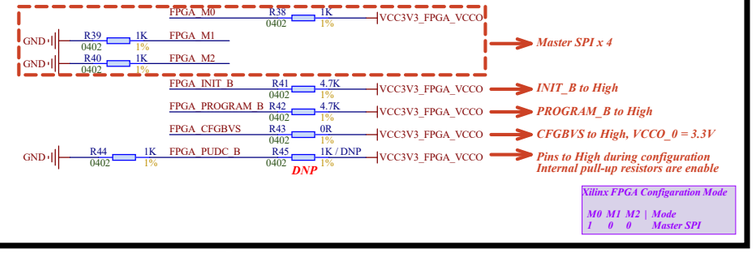
FPGA Config SPI Flash pull up



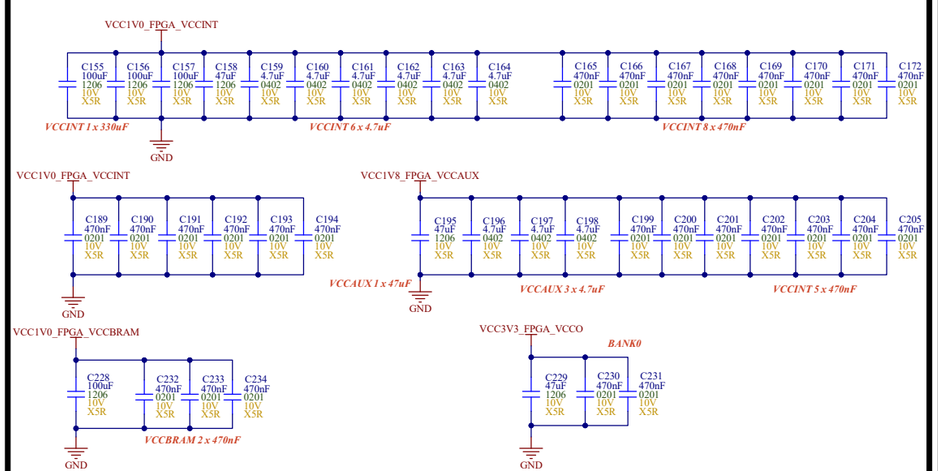
FPGA System Clock



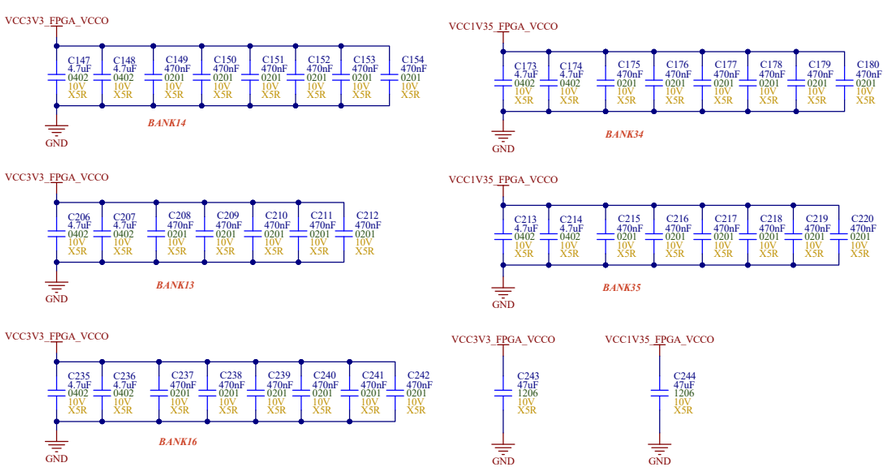
FPGA Config Options



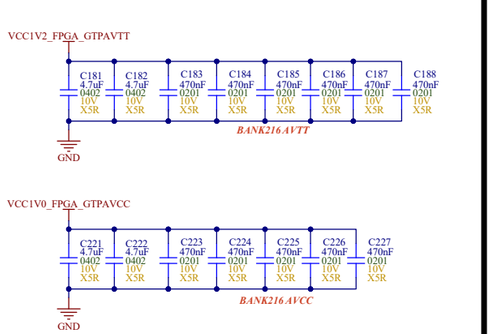
Decoupling Capacitors - FPGA Power



Decoupling Capacitors - HR BANK



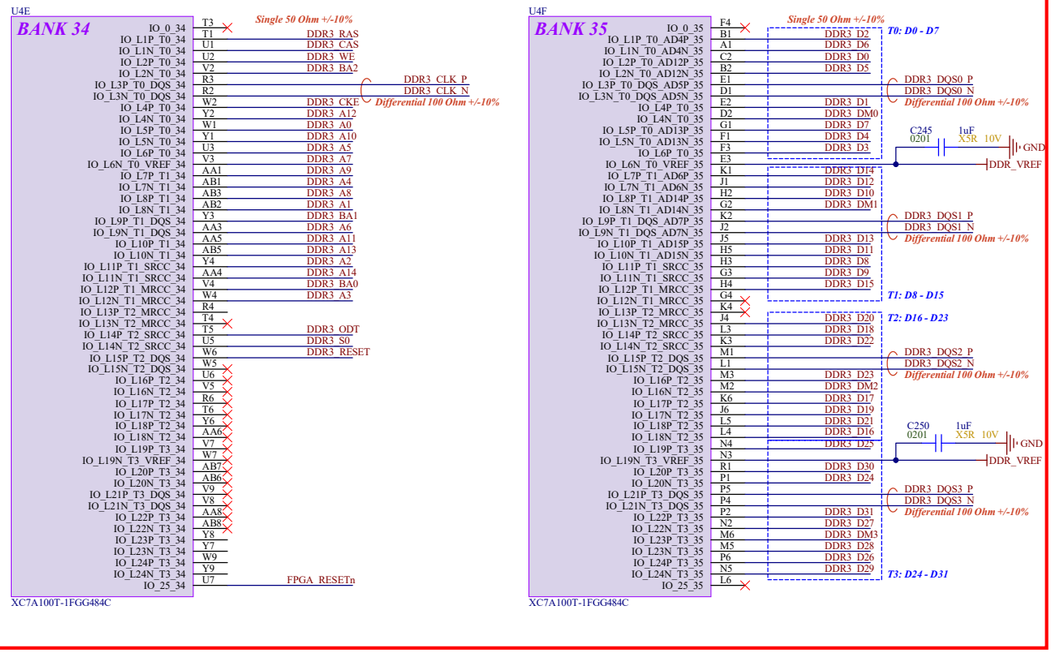
Decoupling Capacitors - GTP BANK



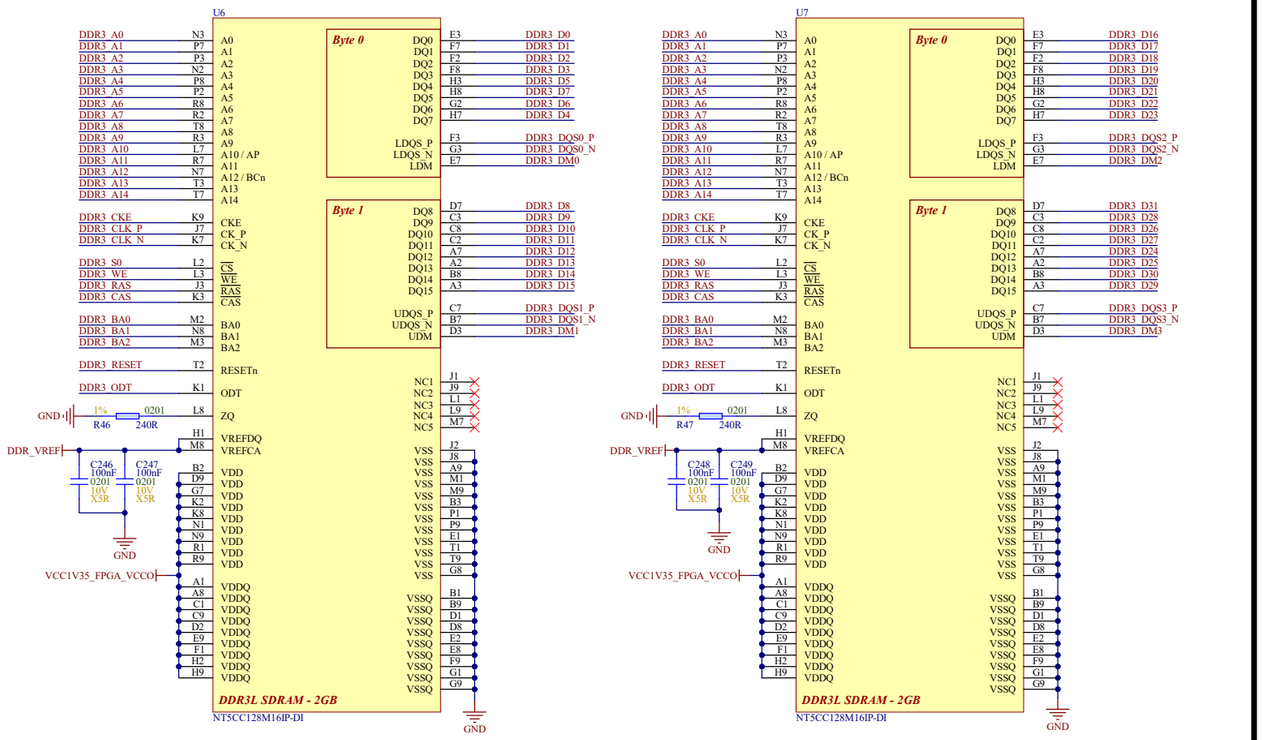
Title	XC7A100T Schematic A		
Size	Number		Revision
A2			V1.0
Date:	7/17/2025	Sheet 5of 15	
File:	C:\Users\..\FPGA-SCH1.SchDoc	Drawn By:	Shixuan Liu

FPGA DDR3L Controller

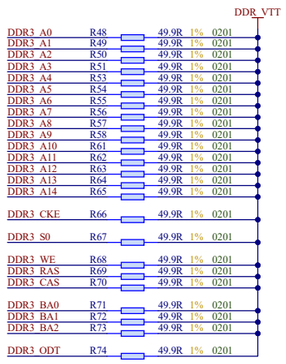
Already verified in Xilinx VIVADO 2018.3



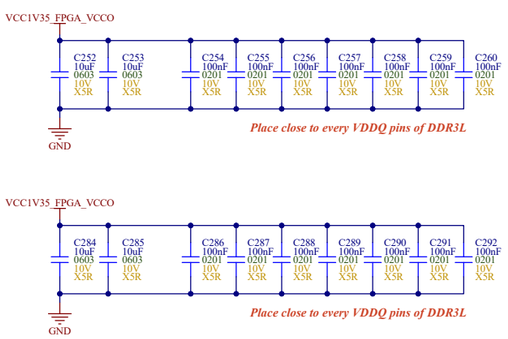
FPGA DDR3L



DDR3L RVTT

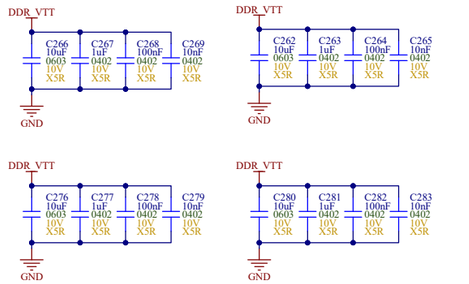


DDR3L VDD & VDDQ Decoupling Capacitors

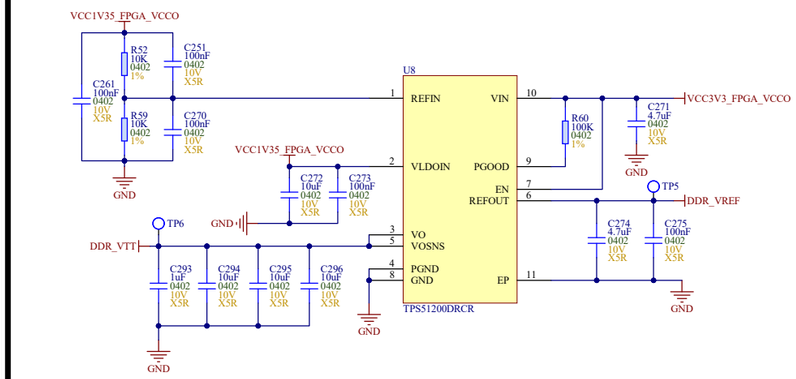


DDR3L VTT Decoupling Capacitors

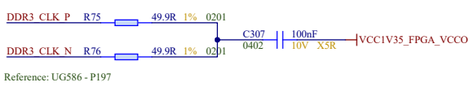
Place close to resistors pull up CA to DDR_VTT



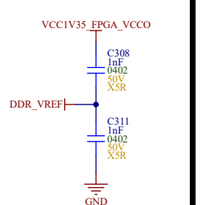
DDR_VREF & DDR_VTT

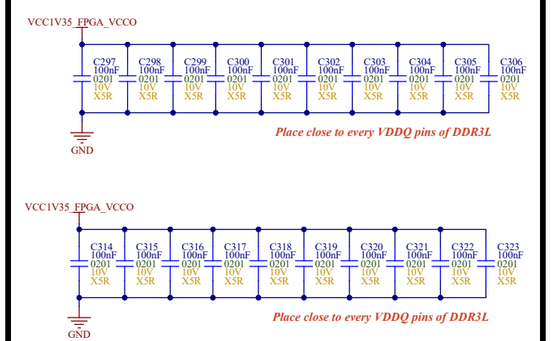


DDR3L Clock Termination

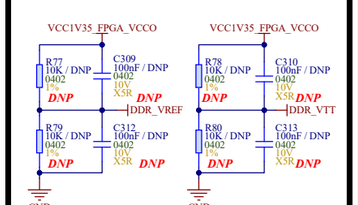


DDR3L VREF



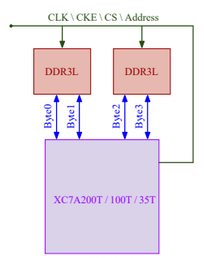


DDR_VREF&DDR_VTT



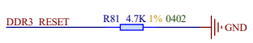
DDR3L Topo Structure

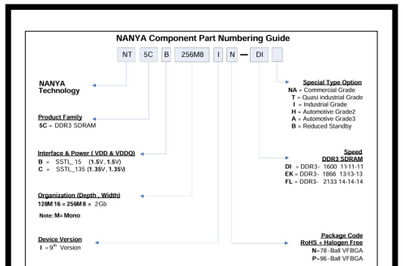
Fly-By Topo



Refer to UG586 P196

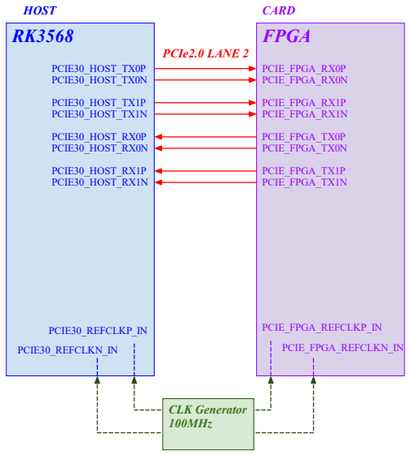
DDR3L RESET & CKE



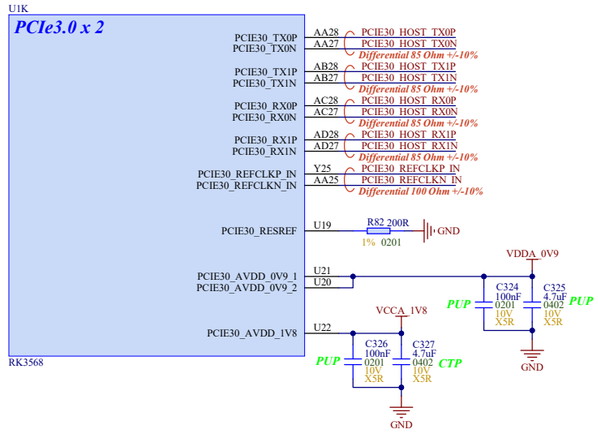


Title	XC7A100T Schematic B	
Size: A2	Number	Revision: V1.0
Date: 7/17/2025		Sheet 6of 15
File: C:\Users\..\FPGA-SCH2.SchDoc		Drawn By: Shixuan Liu

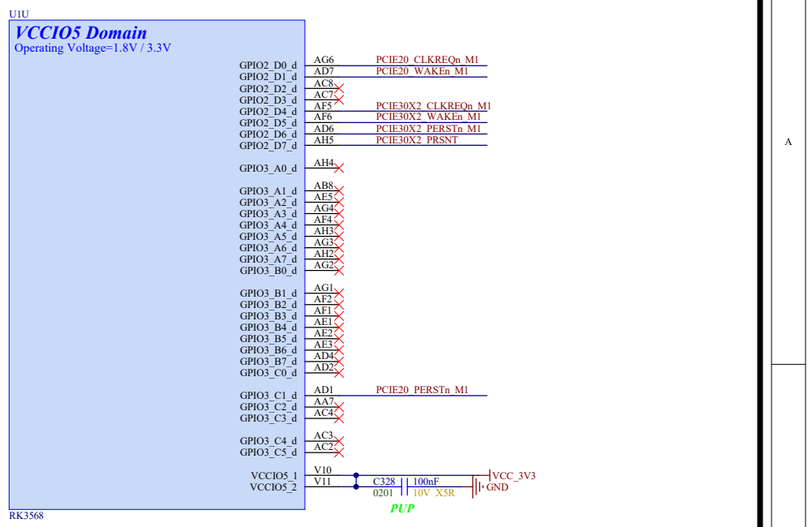
PCIe3.0 Interface



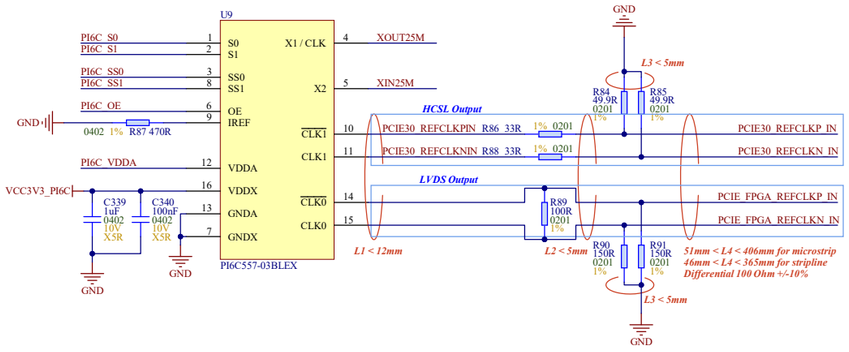
PCIe3.0 HOST



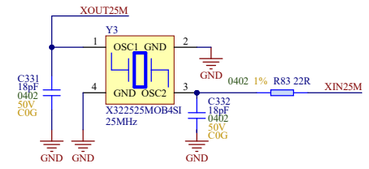
CLKREQ & WAKE & PERST



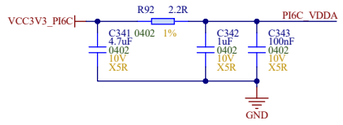
PCIe3.0 REFCLK (Mode: CC)



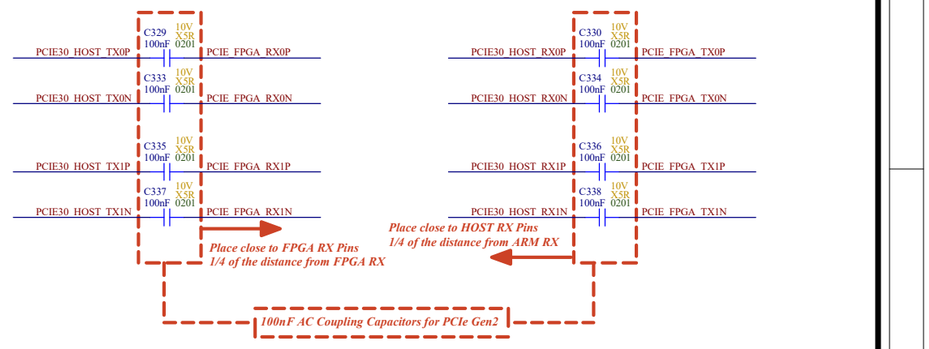
PI6C557 CLK In



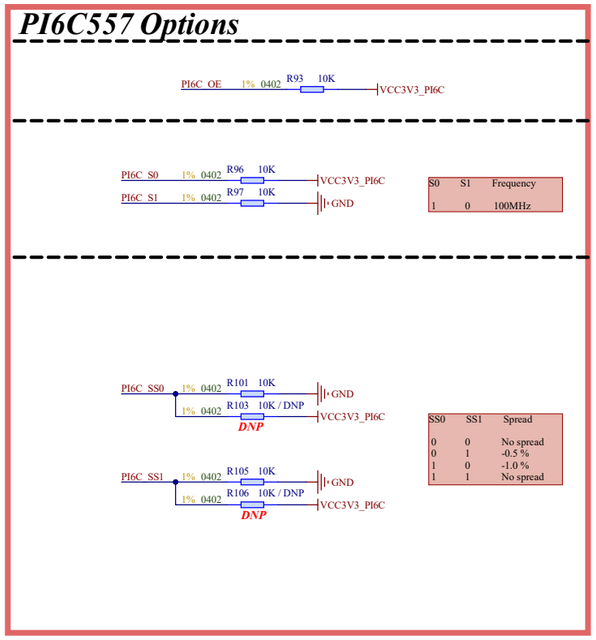
PI6C557 Power



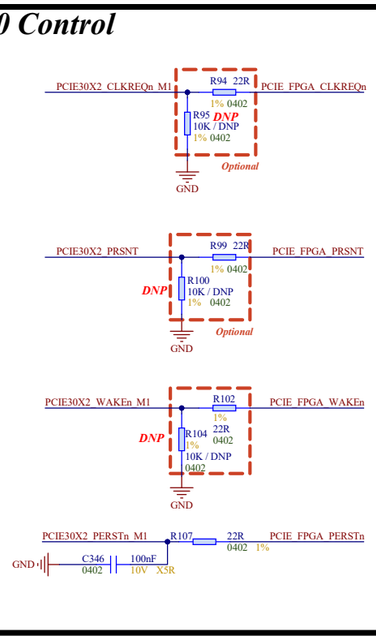
PCIe3.0 Data



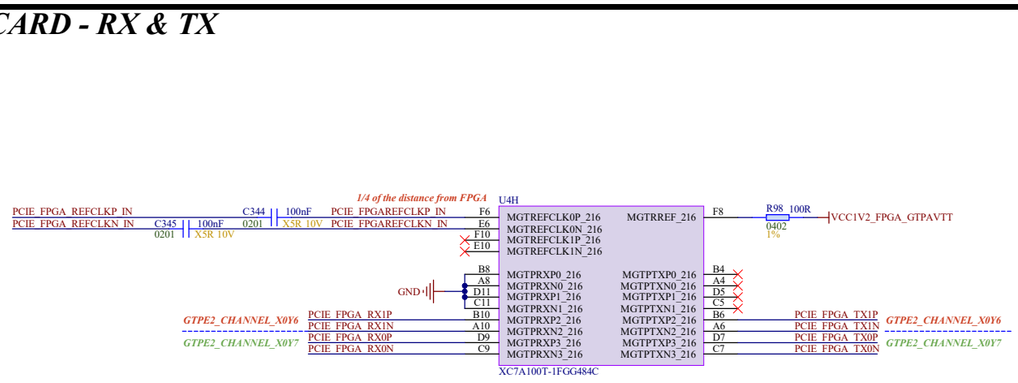
PI6C557 Options



PCIe3.0 Control

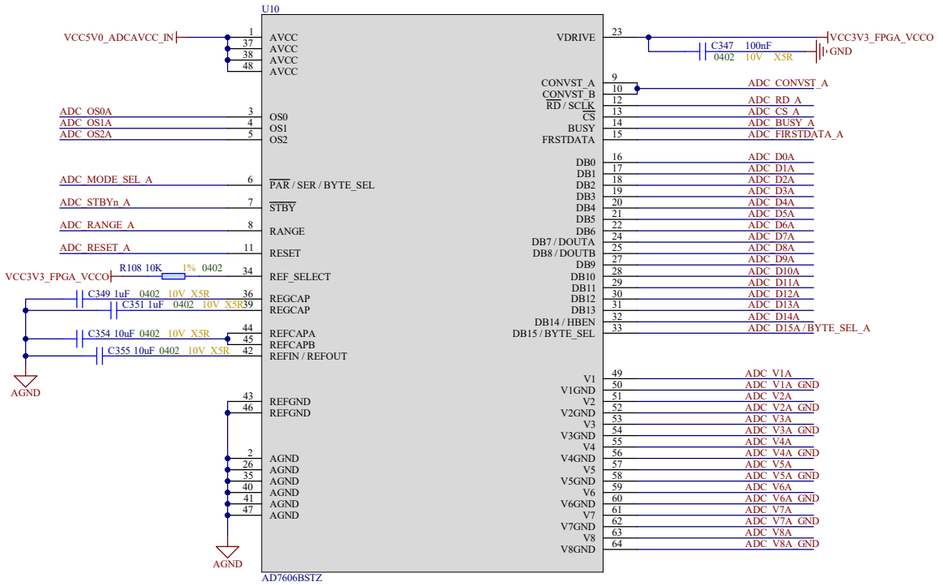


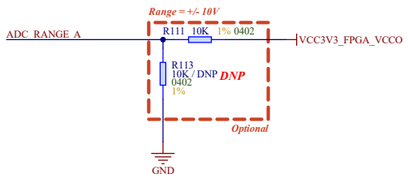
PCIe3.0 CARD - RX & TX



Title	PCIE Interface	
Size A2	Number	Revision V1.0
Date: 7/17/2025		Sheet 7of 15
File: C:\Users\..\PCIE.SchDoc		Drawn By: Shixuan Liu

ADC-A

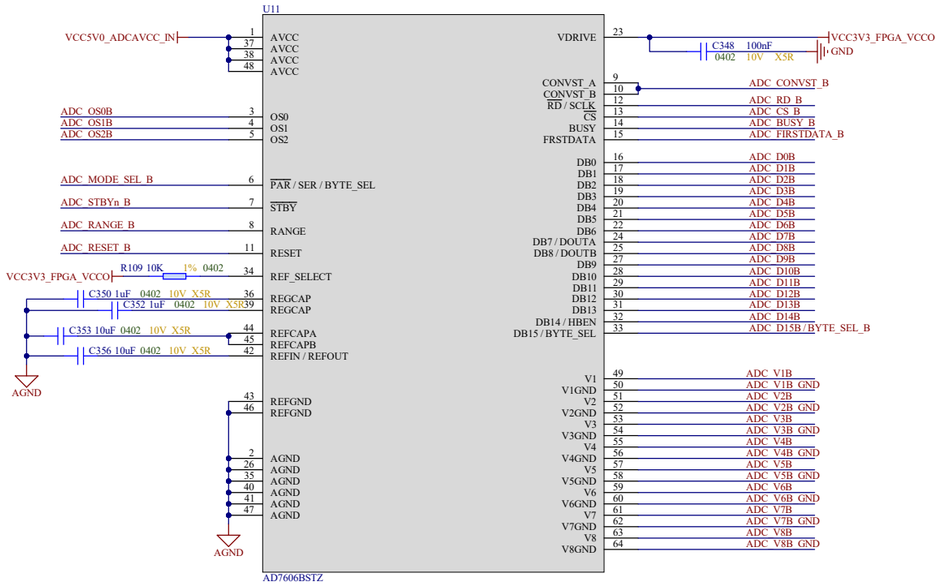


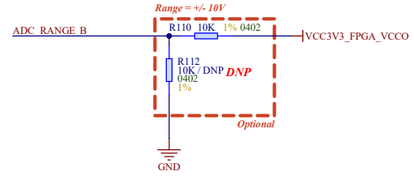


Stay By Option:		
STBY#	RANGE	Mode
0	1	Stay By
0	0	Shut Down

Digital Interface:		
MODE_SEL#	DB15	Interface
0	0	Parallel
1	0	Serial
1	1	Parallel Byte

ADC-B



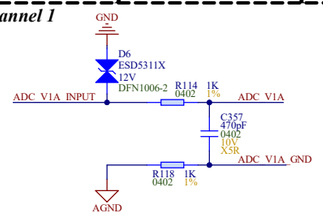


Stay By Option:		
STBY#	RANGE	Mode
0	1	Stay By
0	0	Shut Down

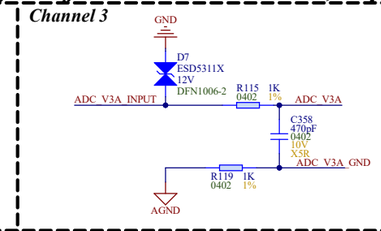
Digital Interface:		
MODE_SEL#	DB15	Interface
0	0	Parallel
1	0	Serial
1	1	Parallel Byte

ADC-A - Operational Amplifier of 1-8 ADC Channels, Input = +/- 10V

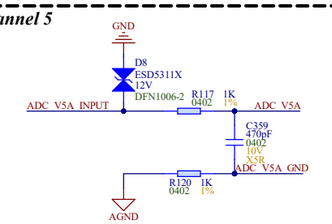
Channel 1



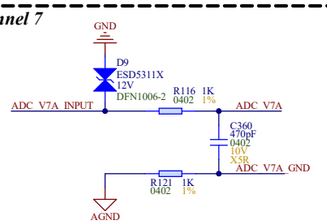
Channel 3



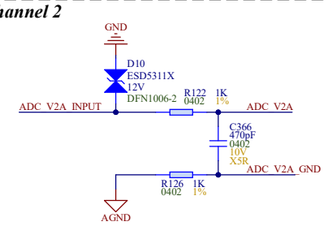
Channel 5



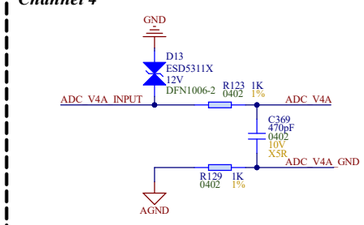
Channel 7



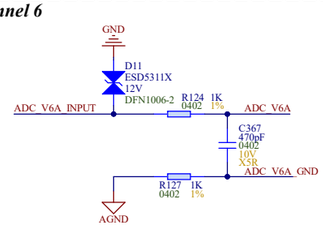
Channel 2



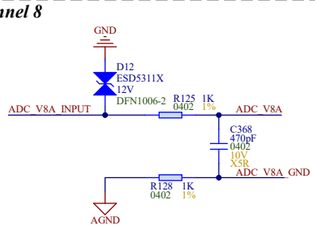
Channel 4



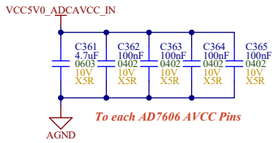
Channel 6



Channel 8

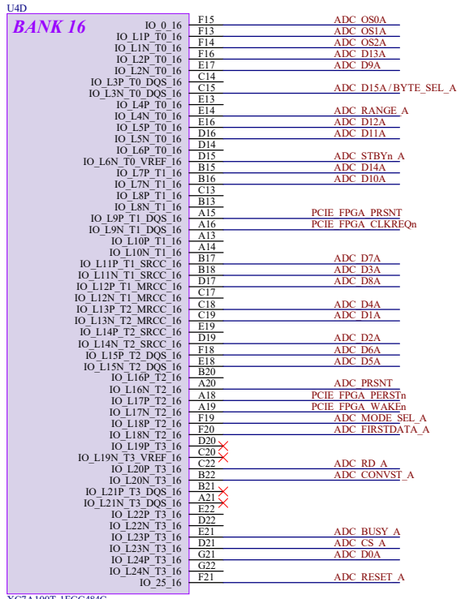


Decoupling Capacitors

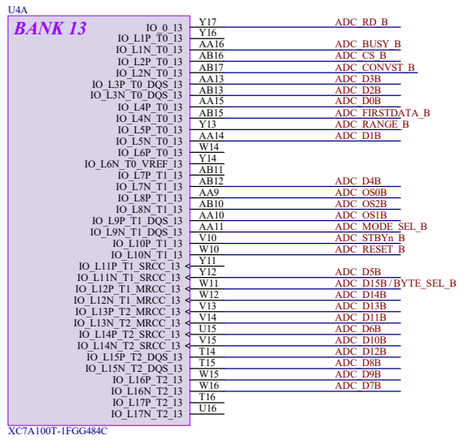


Title	ADC Schematic A		
Size	Number		Revision
A2			V1.0
Date:	7/17/2025		Sheet 8of 15
File:	C:\Users\..\ADC-SCH1.SchDoc		Drawn By: Shixuan Liu

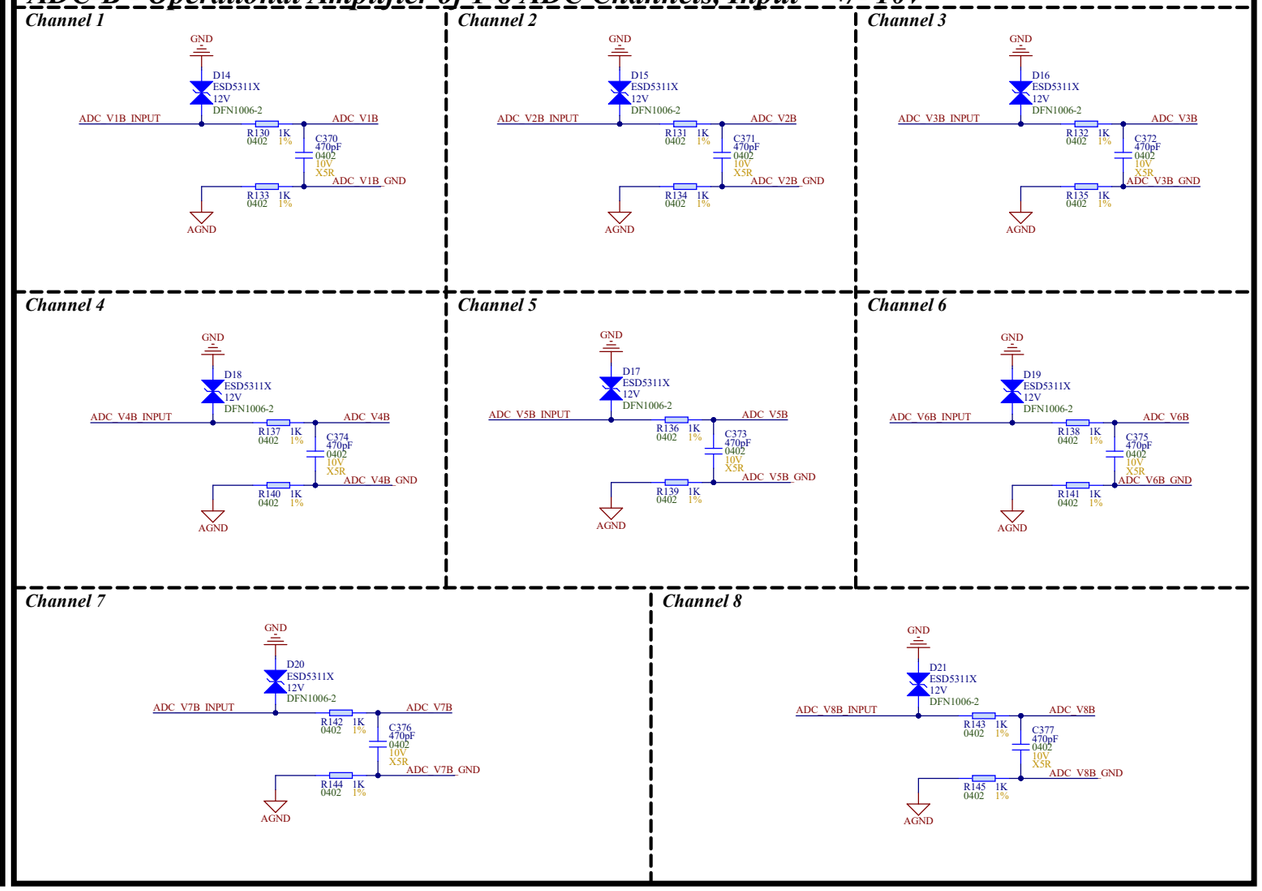
FPAG ADC-A Controller



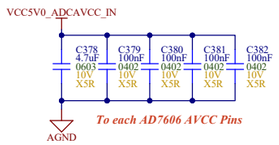
FPAG ADC-B Controller



ADC-B - Operational Amplifier of 1-8 ADC Channels, Input = +/- 10V

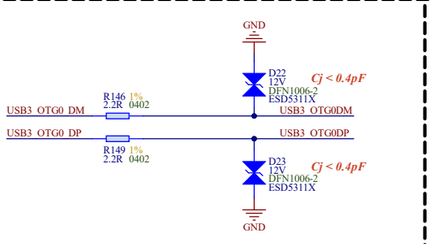


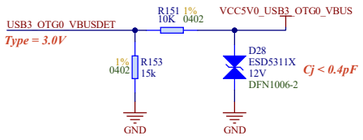
Decoupling Capacitors

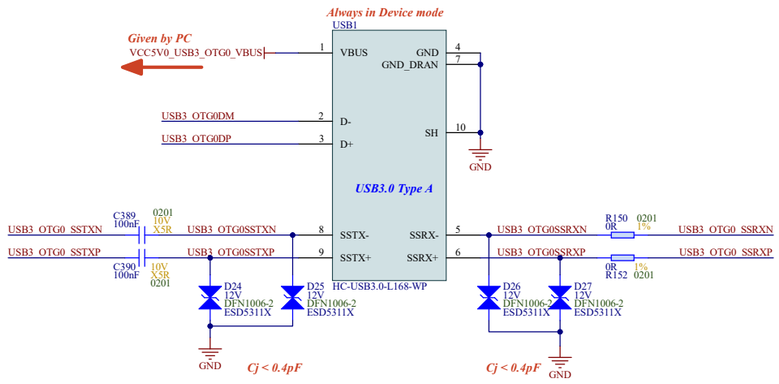


Title: ADC Schematic A		
Size: A2	Number:	Revision: V1.0
Date: 7/17/2025		Sheet 9of 15
File: C:\Users\..\ADC-SCH2.SchDoc		Drawn By: Shixuan Liu

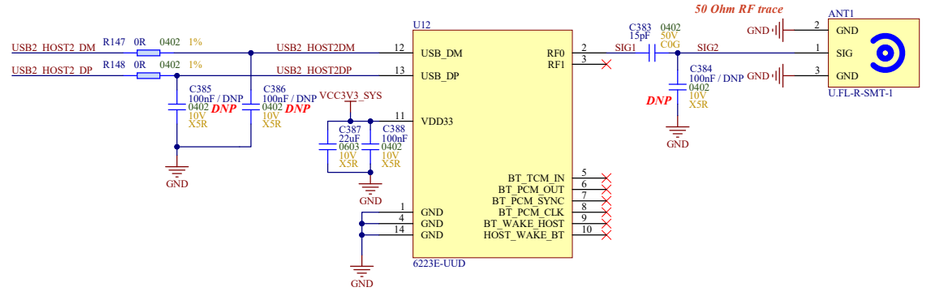
USB3.0 OTG0 (Linux Download - Special Interface)



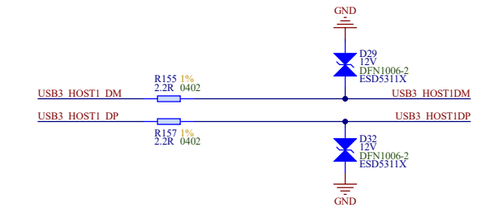


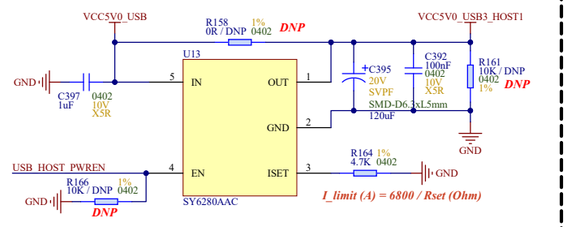


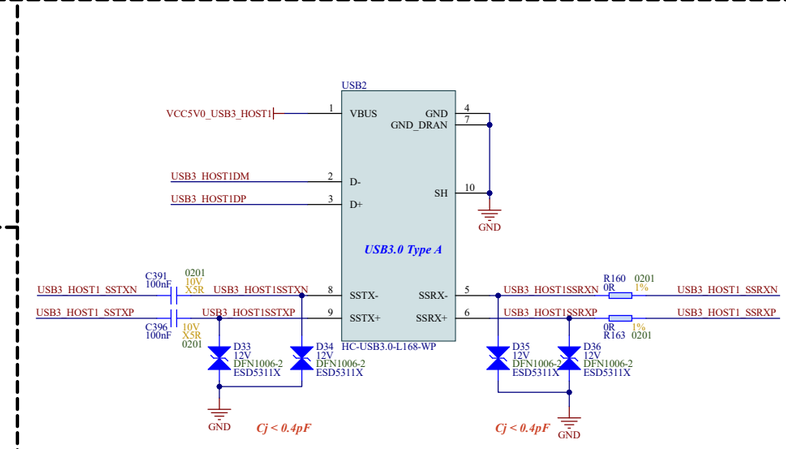
WIFI Module



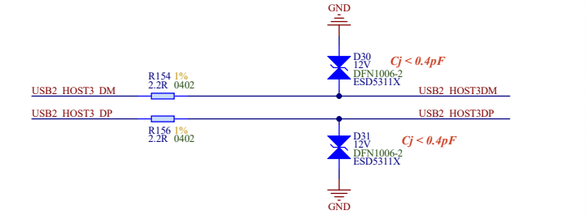
USB3.0 HOST1

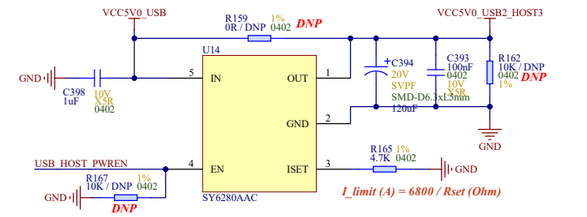


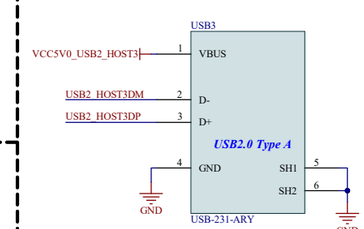




USB2.0 HOST3



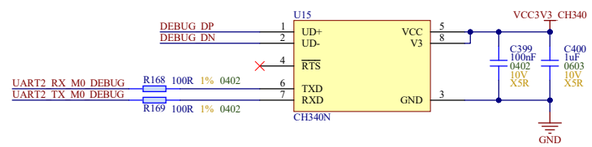


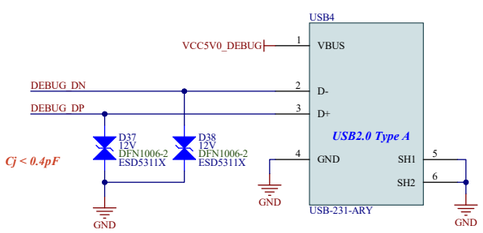


SD Card

REMOVED

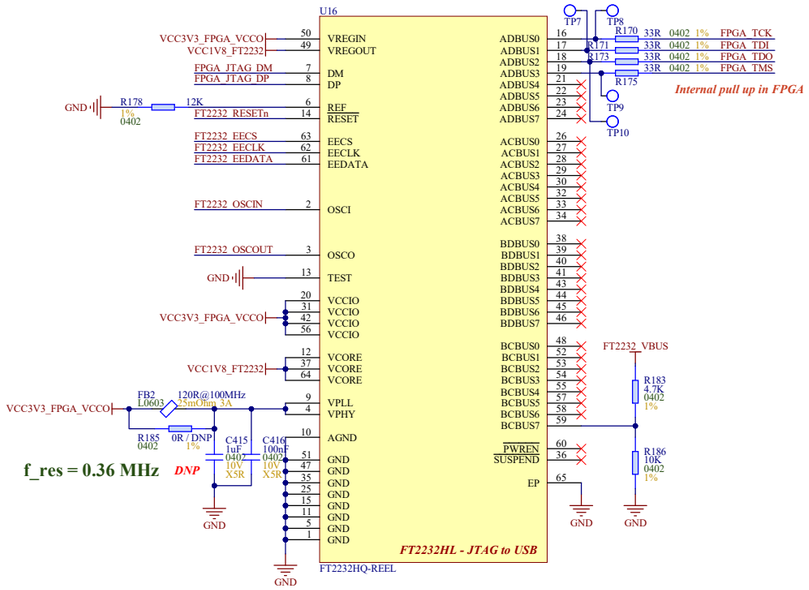
Debug UART to USB2.0 (CH340)





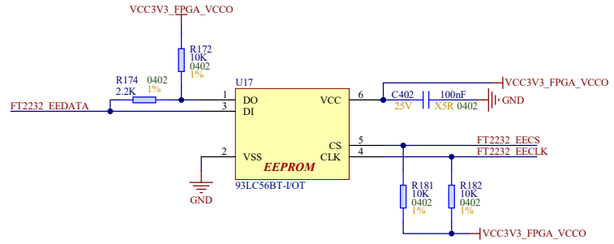
Title	System IO Schematic A		
Size	Number		Revision
A2			V1.0
Date:	7/17/2025	Sheet 10 of 15	
File:	C:\Users\..\SYSTEM-IO1.SchDoc	Drawn By:	Shixuan Liu

FPGA JTAG to USB2.0



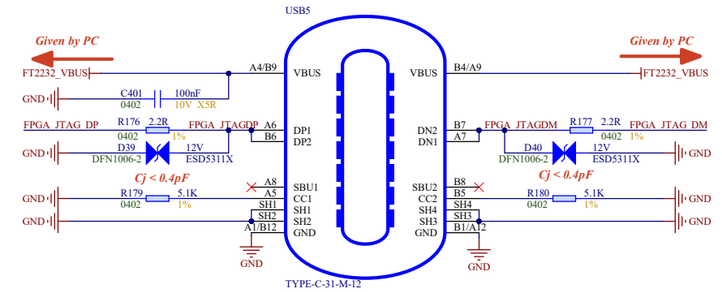
FT2232 Interface

FT2232 EEPROM



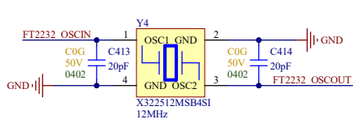
FT2232 Interface

FPGA JTAG USB2.0



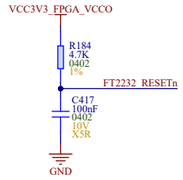
FT2232 Interface

FT2232 Clock



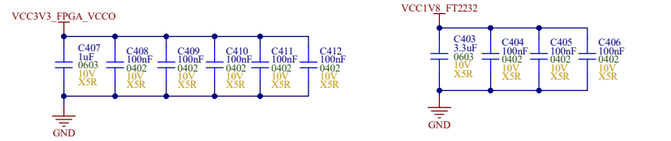
FT2232 Interface

FT2232 Reset



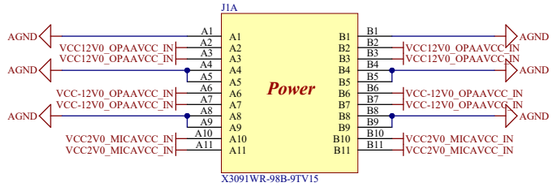
FT2232 Interface

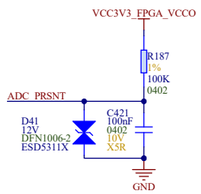
FT2232 Decoupling Capacitors



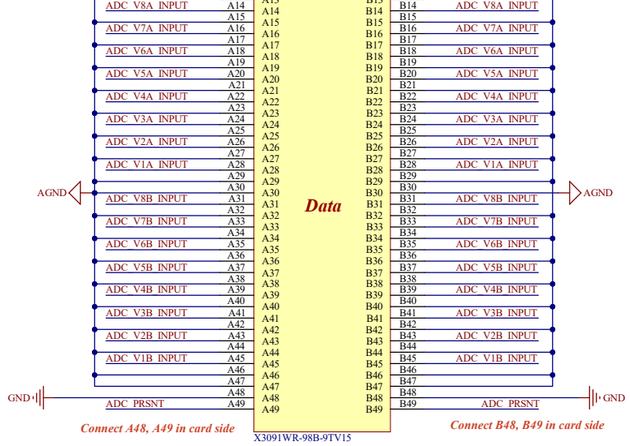
FT2232 Interface

ADC Card Power

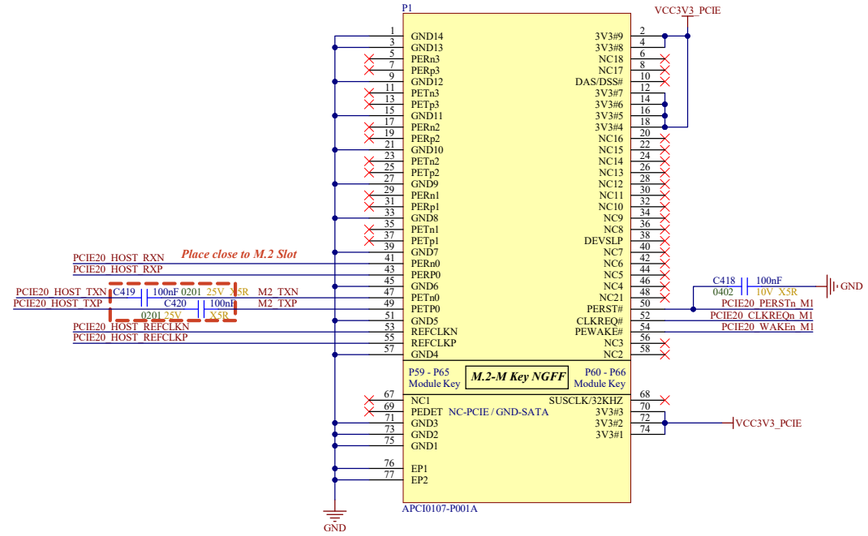




ADC Signal

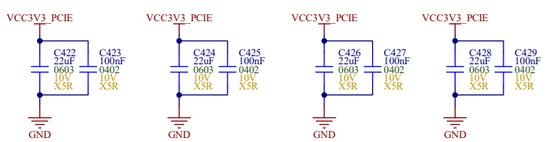


M.2 M-Key SSD



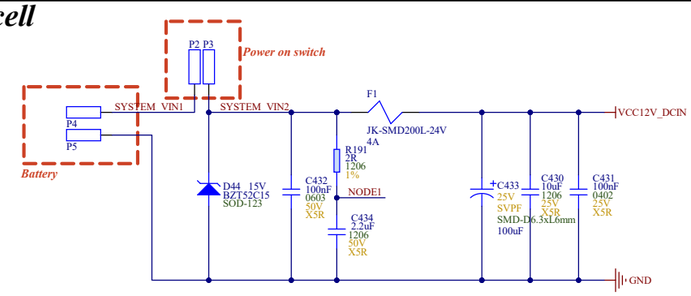
M.2 Key

M.2 M-Key Decoupling Capacitors

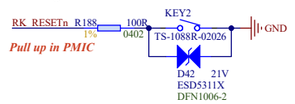


M.2 Key

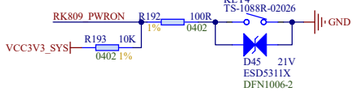
Li-cell



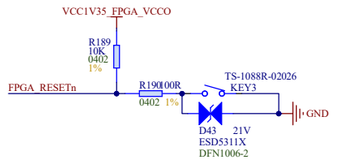
Reset Key - RK3568



RK809 Power On



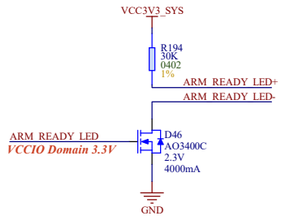
Reset Key - FPGA



Title	System IO Schematic B		
Size	Number		Revision
A2			V1.0
Date:	7/17/2025	Sheet1 lof 15	
File:	C:\Users\..\SYSTEM-IO2.SchDoc	Drawn By:	Shixuan Liu

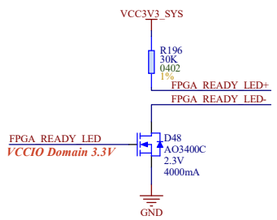
LED - ARM Ready

Controlled by RK3568



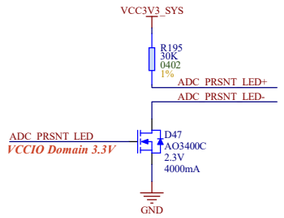
LED - FPGA Ready

Controlled by RK3568



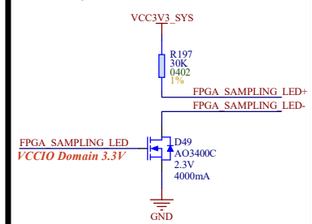
LED - ADC-A Card Present

Controlled by FPGA

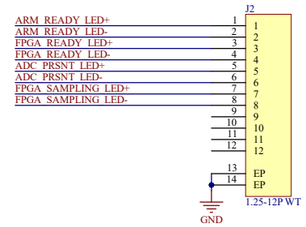


LED - Sampling

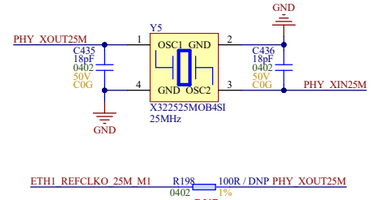
Controlled by FPGA



LED Interface

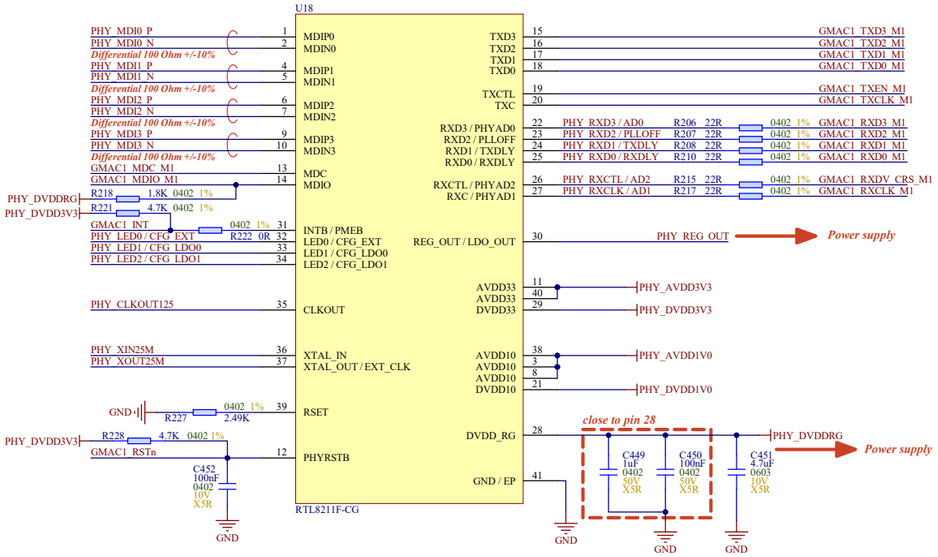


PHY Clock



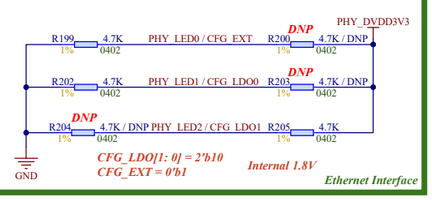
Ethernet Interface

GMAC PHY



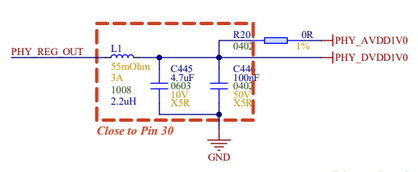
Ethernet Interface

PHY Voltage Config



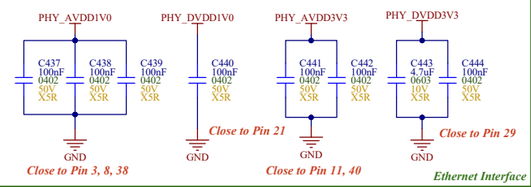
Ethernet Interface

PHY VDD1V0



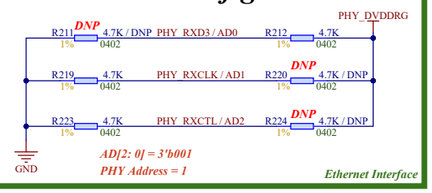
Ethernet Interface

PHY Decoupling Capacitors



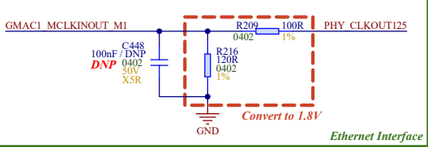
Ethernet Interface

PHY Address Config



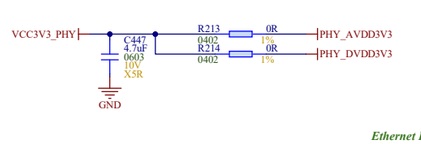
Ethernet Interface

PHY Clock Out



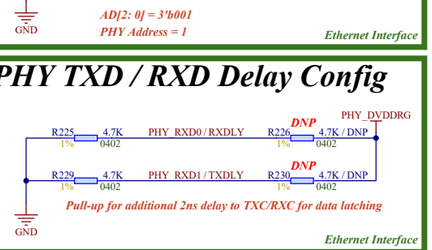
Ethernet Interface

PHY Power 3V3



Ethernet Interface

PHY TXD / RXD Delay Config

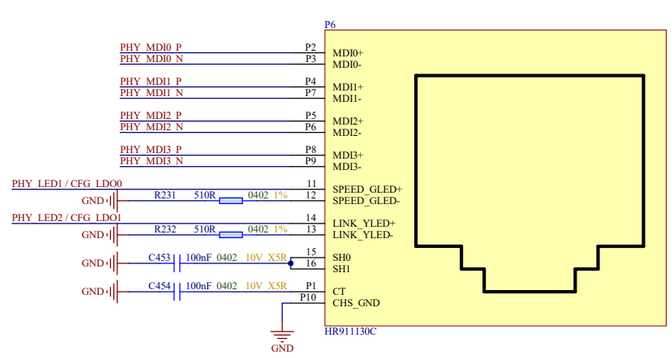


Ethernet Interface

PHY PLL Config @ ALDPS

Ethernet Interface

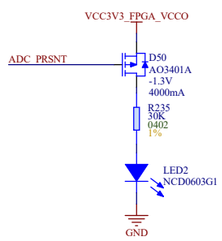
Ethernet Connector



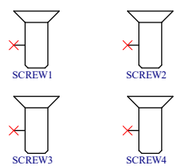
Ethernet Interface

LED - ADC-A Card Present

After insertion

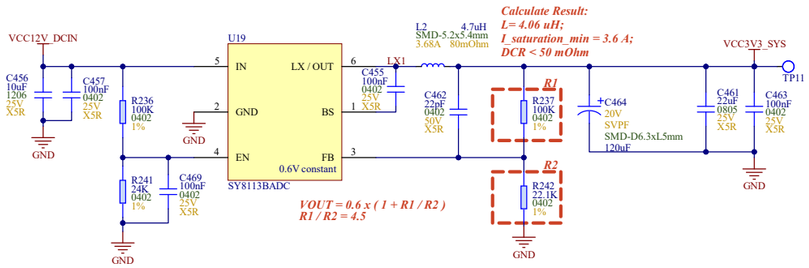


Mechanical



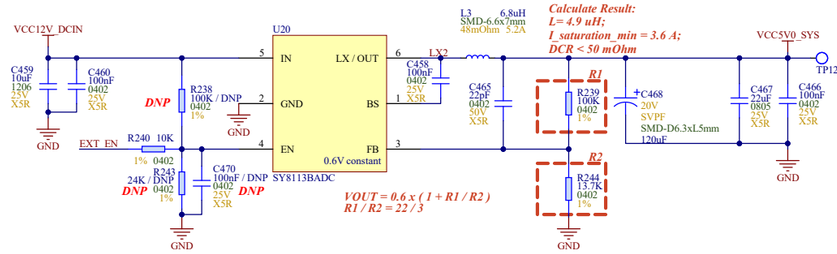
Title: System IO Schematic C		
Size: A2	Number:	Revision: V1.0
Date: 7/17/2025		Sheet 12 of 15
File: C:\Users\..\SYSTEM-IO3.SchDoc		Drawn By: Shixuan Liu

12V_DCIN to VCC3V3_SYS



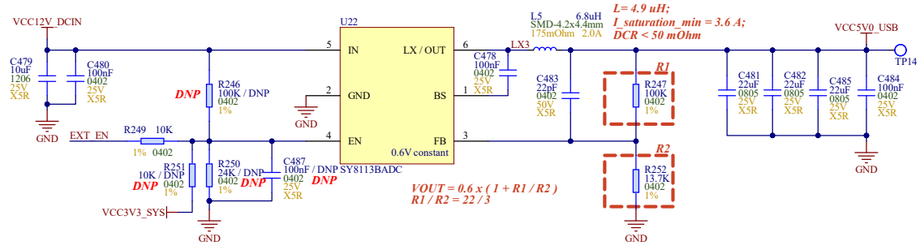
RK3568 Power Tree

12V_DCIN to VCC5V0_SYS



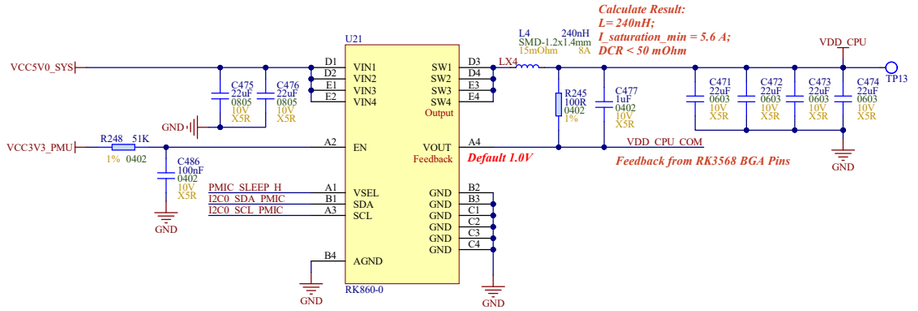
RK3568 Power Tree

12V_DCIN to VCC5V0_USB



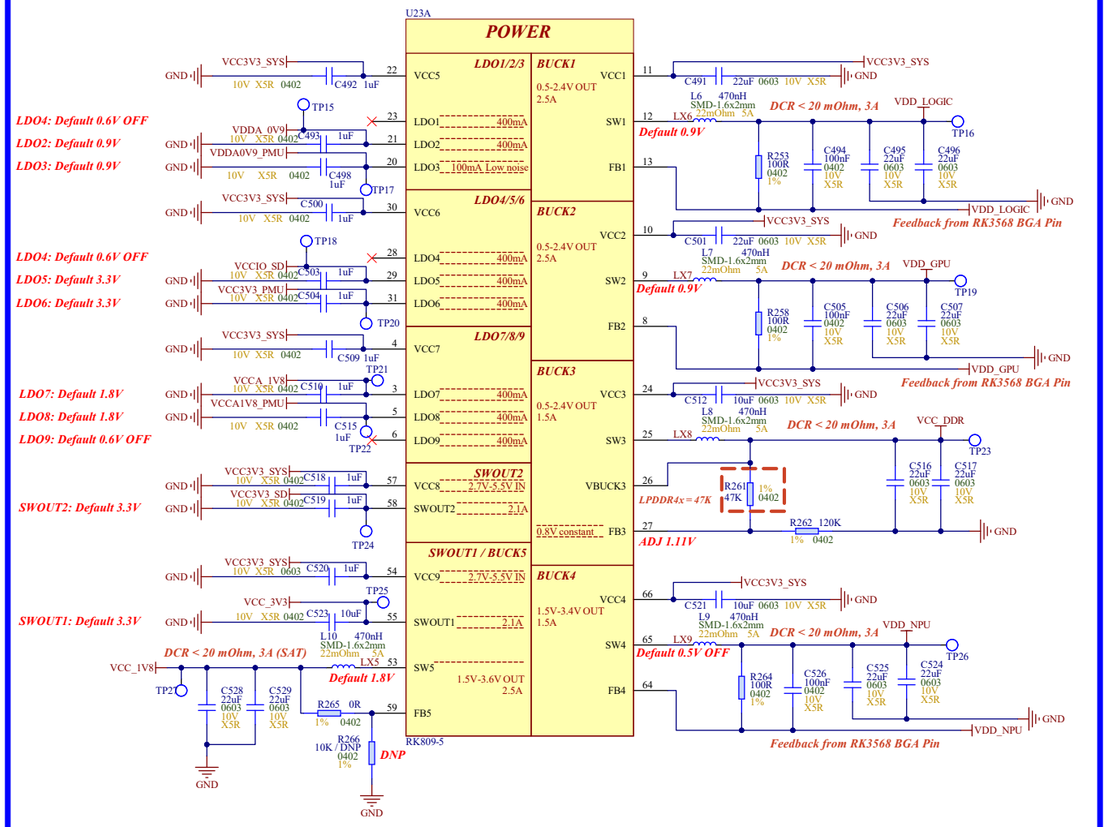
RK3568 Power Tree

VCC5V0_SYS to VDD_CPU

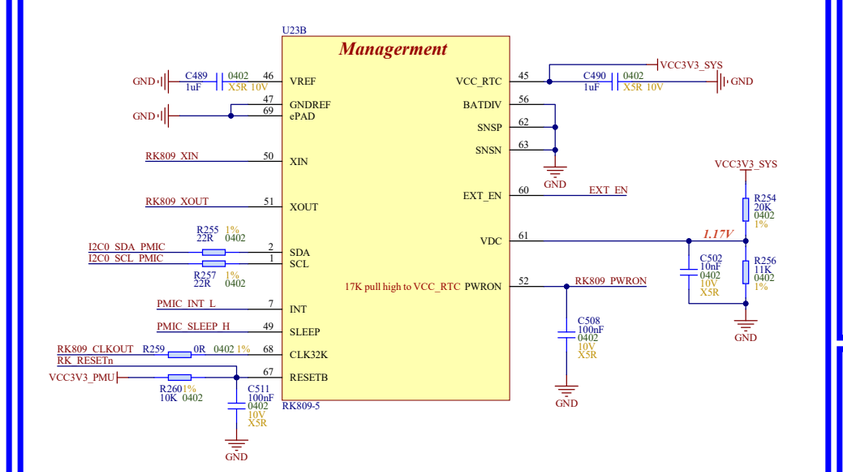


RK3568 Power Tree

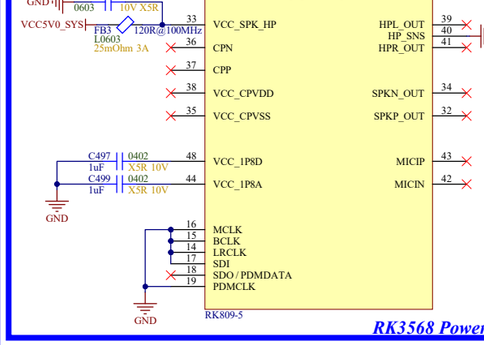
RK809-5 LDO & DC-DC



RK809-5 Management

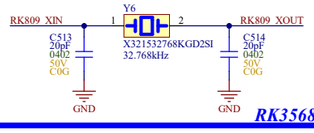


RK809-5 CODEC



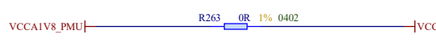
RK3568 Power Tree

RK809-5 Clock



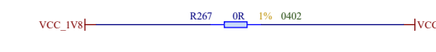
RK3568 Power Tree

VCC1V8_PMU to VCC1V8_DDR



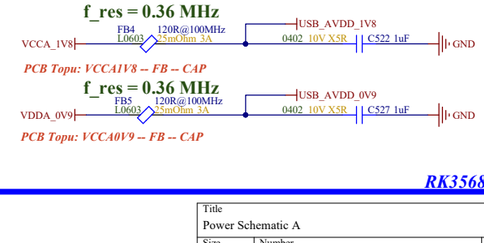
RK3568 Power Tree

VCC_1V8 to VCCIO_FLASH



RK3568 Power Tree

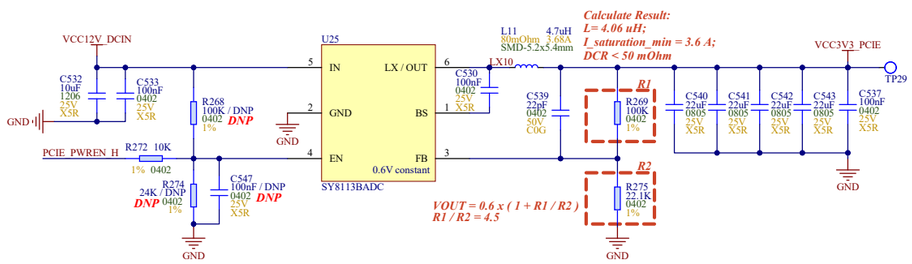
VCCA_1V8/0V9 to USB_AVDD_1V8/0V9



RK3568 Power Tree

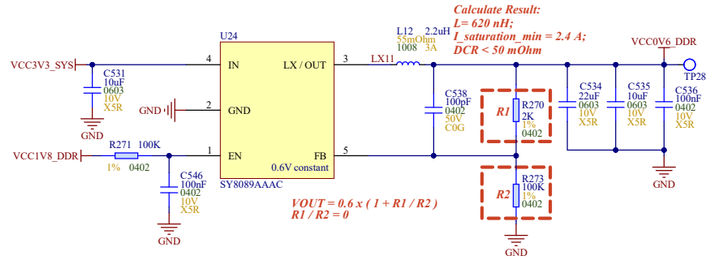
Title: Power Schematic A		
Size: A2	Number:	Revision: V1.0
Date: 7/17/2025		Sheet 1 of 15
File: C:\Users\..\POWER-SCH1.SchDoc		Drawn By: Shixuan Liu

12V_DCIN to VCC3V3_PCIE



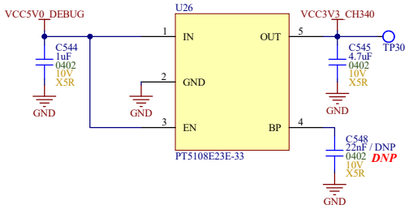
RK3568 Power Tree

VCC3V3_SYS to VCC0V6_DDR

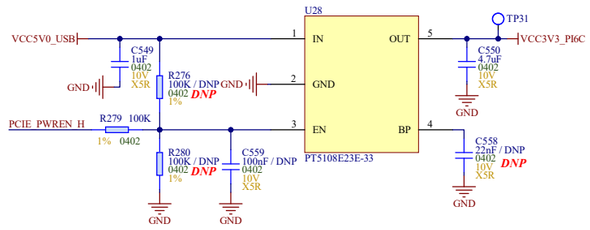


RK3568 Power Tree

VCC5V0_DEBUG to VCC3V3_CH340

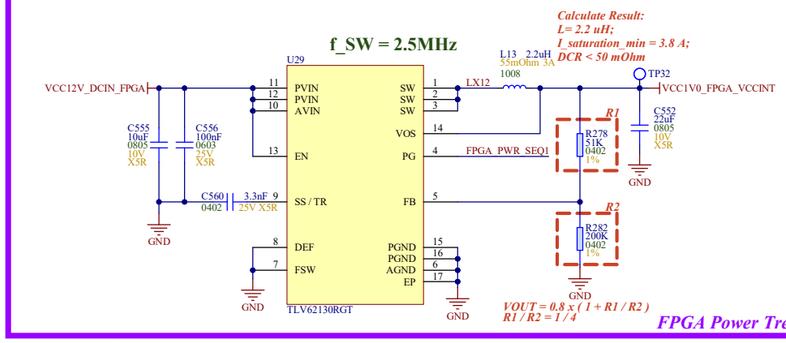


VCC5V0_USB to VCC3V3_PI6C



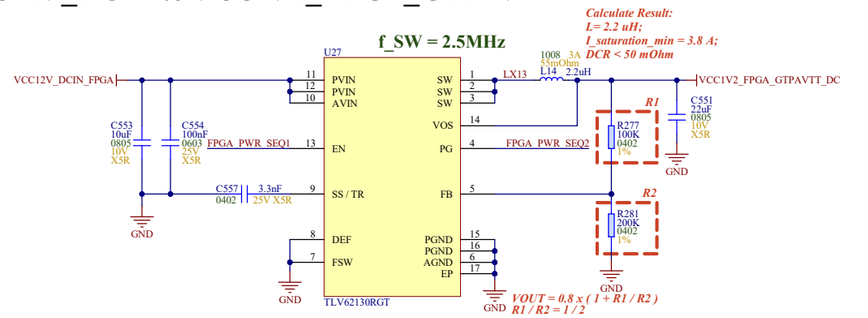
RK3568 Power Tree

VCC12V_DCIN to VCC1V0_FPGA_VCCINT



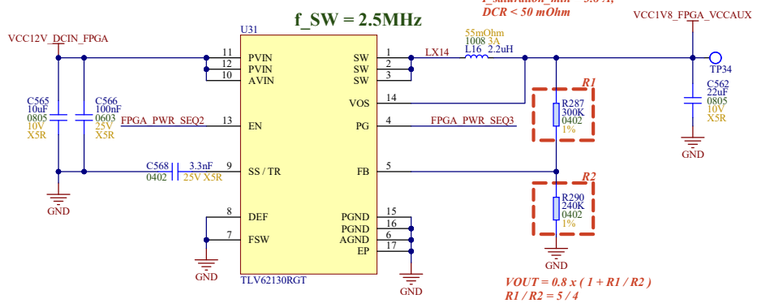
FPGA Power Tree

VCC12V_DCIN to VCC1V2_FPGA_GTPAVTT



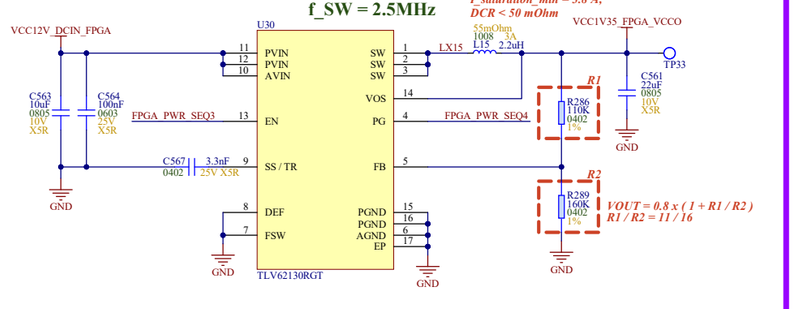
FPGA Power Tree

VCC12V_DCIN to VCC1V8_FPGA_VCCAUX



FPGA Power Tree

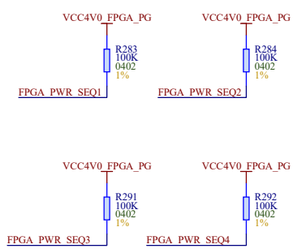
VCC12V_DCIN to VCC1V35_FPGA_VCCO



FPGA Power Tree

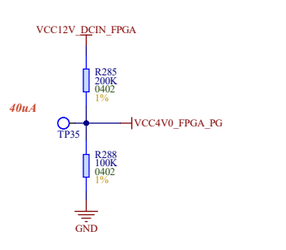
Power on sequence

open drain



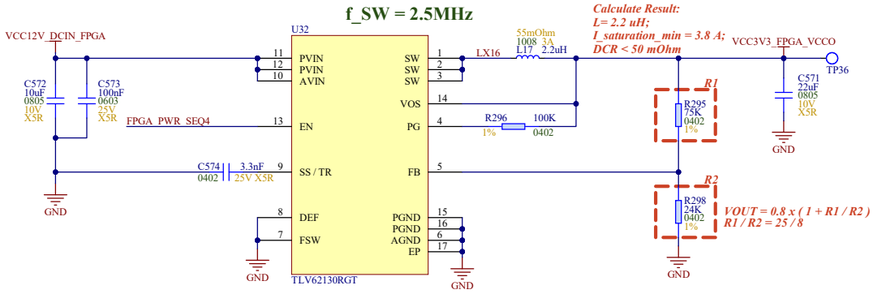
FPGA Power Tree

PG VH



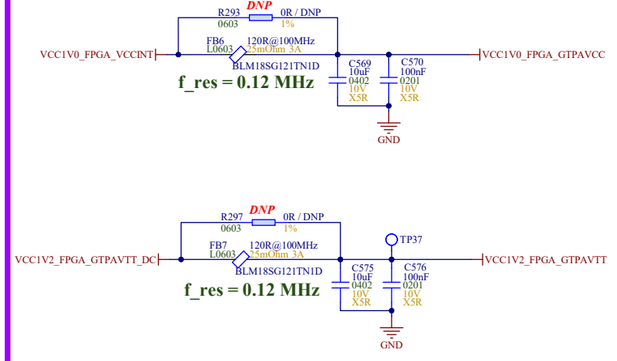
FPGA Power Tree

VCC12V_DCIN to VCC3V3_FPGA_VCCO



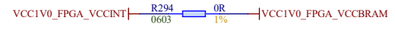
FPGA Power Tree

VCC1V0_FPGA_VCCINT to VCC1V0_FPGA_GTPAVCC



FPGA Power Tree

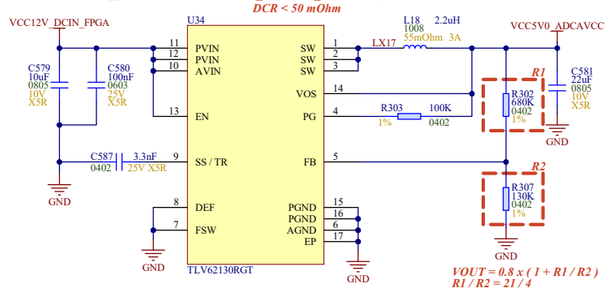
VCC1V0_FPGA_VCCINT to VCC1V0_FPGA_VCCBRAM



FPGA Power Tree

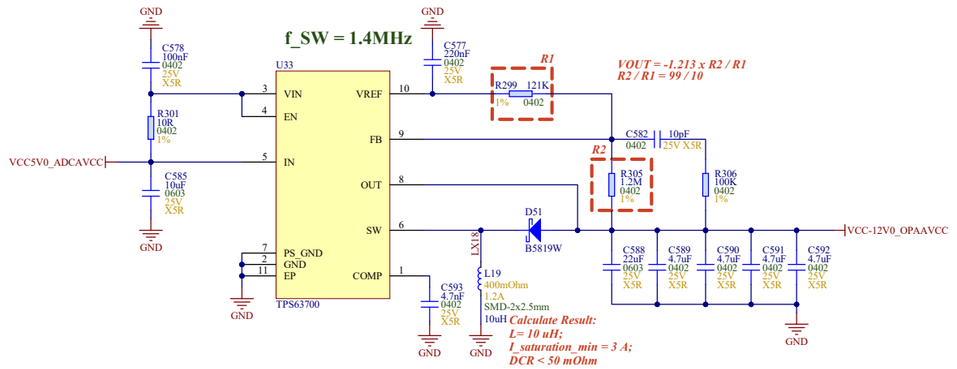
Title		
Power Schematic B		
Size	Number	Revision
A2		V1.0
Date: 7/17/2025		Sheet14of 15
File: C:\Users\..\POWER-SCH2.SchDoc		Drawn By: Shixuan Liu

VCC12V_DCIN to VCC5V0_ADCAVCC



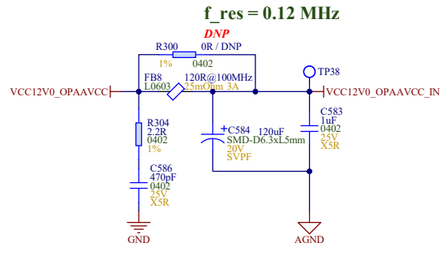
ADC & Analog Power Tree

VCC5V0_ADCAVCC to VCC-12V0_OPAAVCC



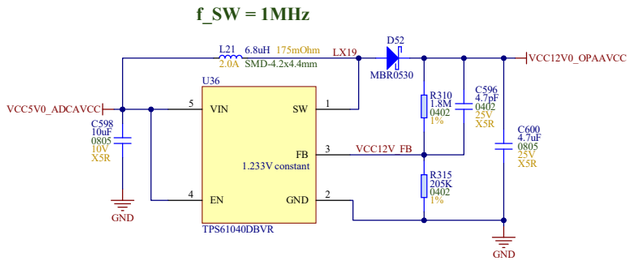
ADC & Analog Power Tree

VCC12V0_OPAAVCC to VCC12V0_OPAAVCC_IN



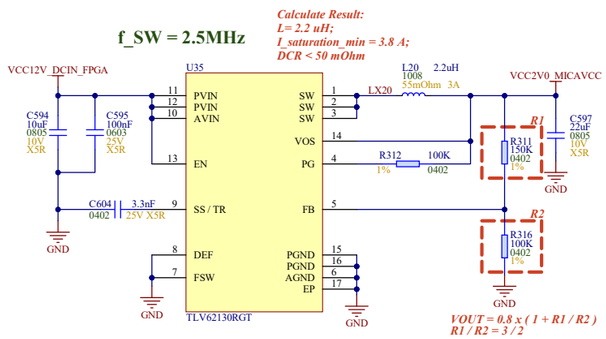
ADC & Analog Power Tree

VCC5V0_ADCAVCC to VCC12V0_OPAAVCC



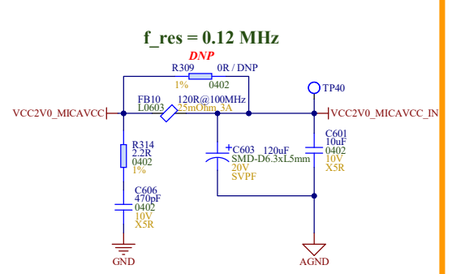
ADC & Analog Power Tree

VCC12V_DCIN to VCC2V0_MICAVCC



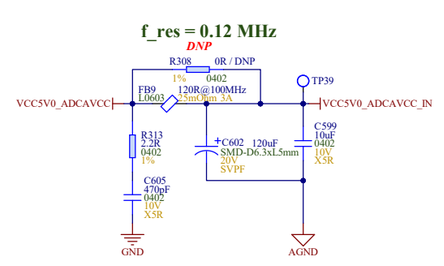
ADC & Analog Power Tree

VCC2V0_MICAVCC to VCC2V0_MICAVCC_IN



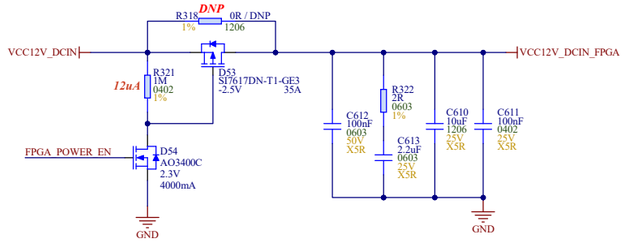
ADC & Analog Power Tree

VCC5V0_ADCAVCC to VCC5V0_ADCAVCC_IN



ADC & Analog Power Tree

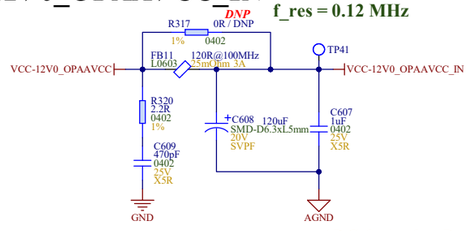
FPGA Power Control



Analog circuit Power Control

REMOVED

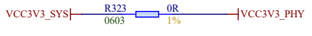
VCC-12V0_OPAAVCC to VCC-12V0_OPAAVCC_IN



ADC & Analog Power Tree

AGND & DGND

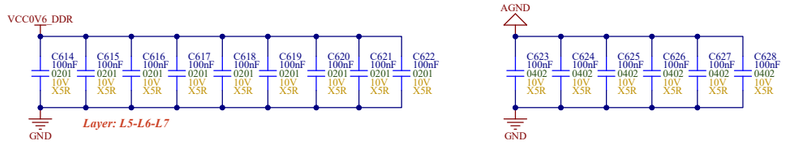
VCC_3V3 to VCC3V3_PHY



RK3568 Power Tree

Reflux Capacitors for high speed signal

Depends on PCB design



Title: Power Schematic C		
Size: A2	Number:	Revision: V1.0
Date: 7/17/2025		Sheet15of 15
File: C:\Users\...\POWER-SCH3.SchDoc		Drawn By: Shixuan Liu