

Devin Pohl

Atlanta, Georgia – United States

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I am a first-year PhD student beginning my research in writing compilers for novel architectures.

I am currently seeking a research internship in the compilers and/or computer architecture space.

Education

- **Georgia Institute of Technology** **Aug 2023 – Present**
Atlanta, GA
 - *Doctorate of Philosophy in Computer Science*
 - Advisor: Vivek Sarkar
 - Research Interests: Compilers, Novel Architectures, High Performance Computing
- **Colorado State University** **May 2022**
Fort Collins, CO
 - *Bachelor of Science in Computer Engineering, Minor in Mathematics, Minor in Computer Science*
 - **Academic Distinctions:**
 - *2022 CEC Silver Medal Candidate:* Recognized as the number one computer engineering undergraduate in all of Colorado
 - *summa cum laude*, 4.0 GPA

Work Experience

- **Compiler Engineer** **Jun 2022 – Aug 2023**
Redmond, WA
 - *Microsoft — DevDiv PLINCO Team*
 - Implemented features and fixing bugs in MSVC's linker, assemblers, and compiler back-end
 - Contributed early implementation work towards ARM64 native toolchain bringup
 - Led implementation effort for automated testing of toolchain determinism
 - Focused on machine-dependent codegen, determinism, and build modernization
- **Platform Engineering Intern** **May 2021 – Aug 2021**
Fort Collins, CO
 - *Hewlett Packard Enterprise — NonStop Low-Level Team*
 - Designed a performance modeling library to mock enterprise-grade RDMA behavior without dedicated hardware
 - Proved feasibility of an implementation method that would drastically reduce startup cost for new customers
 - Worked in C with InfiniBand and NSK to invisibly apply kernel-mode modifications to existing benchmarks and applications
- **Software Development Intern** **May 2020 – Aug 2020**
Fort Collins, CO
 - *Hewlett Packard Enterprise — NonStop Manageability Team*
 - Improved and optimized OSM, the main application for maintaining, updating, and upgrading NonStop servers
 - Migrated critical security procedures from CLI to GUI, cutting down on time overhead and human error for end-users
 - Worked in Java, using Swing, AWT, RMI, and several internal HPE libraries

Notable Projects

- **Syndra Compiler** **Aug 2023 – Present**
CRNCH Lab
 - *Georgia Institute of Technology — Under Tom Conte*
 - Building an optimizing compiler for a dataflow-based superconducting processor
 - Optimizations include SMT-driven optimal scheduling, simultaneous scheduling and register allocation, and profile-guided / speculative optimizations (global instruction scheduling)
 - Written from the ground-up in C++ to compile RISC-V traces and RISC-V assembly to Syndra assembly
- **dmenu-rs** **v5.5.3 Released Nov 2023**
🔗 [arch::aur::dmenu-rs](#)
 - *🐙 Shizcow/dmenu-rs*
 - A program launcher, unit-aware calculator, spellchecker, search engine dispatcher, and general purpose menu for Linux
 - A port of the popular GNU utility dmenu to Rust, garnering thousands of users and 180+ stars on GitHub

Technical Skills

- **Programming Languages:**
 - Low-Level ARM Assembly, RISC-V Assembly, LLVM, MASM, MIPS, x86 and x64 Assembly, UTC IR
 - High-Level C, C++, Matlab, Java, JavaScript/TypeScript, Lisp, Python, Scala, **Rust**
 - Synthetic GLSL, \LaTeX , Spice, Verilog
- **Libraries, and Tools:**
 - Computational Boolector, CaDiCaL, GMP, OpenCL, OpenMP, Rink.rs, SageMath, Z3
 - Graphical X11, XCB, Cairo, Pango, Unicode CLDR, GTK, Qt