Devin Pohl

Atlanta, Georgia – United States

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I am a second-year PhD student continuing my research on exploring new compiler directions for novel architectures.
I have identified research interests in extreme heterogeneity, software-hardware co-design, and constraint programming.

Education

Georgia Institute of Technology — **Aug 2023 – Present**
Doctorate of Philosophy in Computer Science — *Atlanta, GA*
- Advisor: Vivek Sarkar
- Research Experience: Compilers, Non-CMOS Architectures, Superconducting Architectures, Spiking Neural Networks

Colorado State University — **May 2022**
Bachelor of Science in Computer Engineering, Minor in Mathematics, Minor in Computer Science — *Fort Collins, CO*
- Academic Distinctions:
  · *2022 CEC Silver Medal Candidate*: Recognized as the number one computer engineering undergraduate in all of Colorado

Work Experience

Research Intern — **May 2024 – Aug 2024**
Oak Ridge National Laboratory — Abisko Project — *Oak Ridge, TN*
- Researched hardware-software co-design for running spiking neural networks on non-CMOS accelerators
- Implemented a mapping tool with Google OR-Tools targeting heterogeneous memristor crossbar architectures
- Extended processor simulator to correctly support multi-crossbar execution with network logging for profile-guided optimization
- Started a body of work targeting multiple publications on optimal mapping, hotspot minimization, and architecture aware training

Compiler Engineer — **Jun 2022 – Aug 2023**
Microsoft — DevDiv PLINCO Team — *Redmond, WA*
- Implemented features and fixing bugs in MSVC's linker, assemblers, and compiler back-end
- Contributed early implementation work towards ARM64 native toolchain bringup
- Led implementation effort for automated testing of toolchain determinism
- Focused on machine-dependent codegen, determinism, and build modernization

Platform Engineering Intern — **May 2021 – Aug 2021**
Hewlett Packard Enterprise — NonStop Low-Level Team — *Fort Collins, CO*

Software Development Intern — **May 2020 – Aug 2020**
Hewlett Packard Enterprise — NonStop Manageability Team — *Fort Collins, CO*

Notable Projects

Syndra Compiler — **Aug 2023 – Present**
Georgia Institute of Technology — Supervised by Tom Conte and Vivek Sarkar — *CRNCH Lab*
- Building an optimizing compiler for a dataflow-based superconducting processor
- Optimizations include SMT-driven optimal scheduling, simultaneous scheduling and register allocation,
  and profile-guided / speculative optimizations (global instruction scheduling)
- Written from the ground-up in C++ to compile RISC-V traces and RISC-V assembly to Syndra assembly

dmenu-rs — **v5.5.4 Released Aug 2024**
⌨ *Shizcow/dmenu-rs* — *arch::aur::dmenu-rs*
- A program launcher, unit-aware calculator, spellchecker, search engine dispatcher, and general purpose menu for Linux
- A port of the popular GNU utility dmenu to Rust, garnering thousands of users and 200+ stars on GitHub

Technical Skills

- **Programming Languages:**
  - Low-Level   ARM Assembly, RISC-V Assembly, **LLVM**, MASM, MIPS, x86 and x64 Assembly, UTC IR
  - High-Level   **C**, **C++**, Matlab, Java, JavaScript/TypeScript, Lisp, Python, Scala, **Rust**
  - Synthetic   GLSL, LaTeX, Spice, Verilog
- **Libraries, and Tools:**
  - Computational   Boolector, CaDiCaL, **Google OR-Tools**, GMP, OpenCL, OpenMP, Rink.rs, SageMath, Z3
  - Graphical   X11, XCB, Cairo, Pango, Unicode CLDR, GTK, Qt