Devin Pohl

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I am a second-year PhD student seeking industry collaborators for my thesis on compiler directions for novel architectures. I have identified research interests in extreme heterogeneity, software-hardware co-design, and constraint programming.

Education

- **Doctorate of Philosophy in Computer Science** — **Aug 2023 – Present**
  Georgia Institute of Technology — *Atlanta, GA*
  - Advisor: Vivek Sarkar
  - Research Experience: Compilers, Non-CMOS Architectures, Superconducting Architectures, Spiking Neural Networks
- **Bachelor of Science in Computer Engineering**, Minor in Mathematics, Minor in Computer Science — **May 2022**
  Colorado State University — *Fort Collins, CO*
  - *2022 CEC Silver Medal Candidate*: Recognized as the number one computer engineering undergraduate in all of Colorado

Experience

- **Research Intern** — **May 2024 – Aug 2024**
  Oak Ridge National Laboratory — Abisko Project — *Oak Ridge, TN*
  - Published novel co-design methodologies for accelerating spiking neural networks on non-CMOS architectures
  - Developed a constraint-based mapping tool using Google OR-Tools targeting heterogeneous memristor crossbar arrays
  - Extended processor simulator to support multi-crossbar execution with network traffic tracing for profile-guided optimization
- **Compiler Engineer** — **Jun 2022 – Aug 2023**
  Microsoft — DevDiv PLINCO Team — *Redmond, WA*
  - Contributed features and bug fixes to MSVC's linker, assemblers, and compiler back end
  - Improved dynamic linking and post-codegen optimizations during early ARM64 toolchain bring-up
  - Led implementation effort for automated testing of MSVC-wide toolchain determinism

Publications

[1] Devin Pohl, Aaron Young, Kazi Asifuzzaman, Narasinga Rao Miniskar, and Jeffrey S Vetter, **Mapping spiking neural networks to heterogeneous crossbar architectures using integer linear programming**, in *2025 Design, Automation & Test in Europe Conference (DATE)*, IEEE, 2025, pp. 1–7. DOI: 10.23919/DATE64628.2025.10992958.

[2] Jingqun Zhang, Devin Pohl, Prasanth Chatarasi, Jun Shirako, Vivek Sarkar, and Cong Hao, **SHADE: A software and hardware co-design infrastructure for EDDO architectures**, in *LATTE '24 Workshop on Languages, Tools, and Techniques for Accelerator Design*, Available: https://capra.cs.cornell.edu/latte24/paper/17.pdf.

Notable Projects

- **Syndra Compiler** — **Aug 2023 – Present**
  Georgia Institute of Technology — Supervised by Tom Conte and Vivek Sarkar — *CRNCH Lab*
  - Building the first-ever compiler for a general-purpose dataflow-based superconducting processor
  - 48-bit optimizing compiler, assembler, and linker framework written from the ground up in C++
  - Optimizations are highly machine-dependent due to single-port register files and limited core-to-core communication, including SMT-driven optimal scheduling, global instruction scheduling, and novel approaches to dataflow distance requirements
- **dmenu-rs** — **v5.5.4 Released Aug 2024**
  Shizcow/dmenu-rs — *arch::aur::dmenu-rs*
  - A program launcher, unit-aware calculator, spellchecker, search engine dispatcher, and general purpose menu for Linux
  - A port of the popular GNU utility dmenu to Rust, adding extension support and significantly reducing memory footprint

Technical Skills

- **Programming Languages:**
  - Low-Level: ARM Assembly, RISC-V Assembly, **LLVM**, MASM, MIPS, x86 and x64 Assembly, UTC IR
  - High-Level: **C**, **C++**, Matlab, Java, JavaScript/TypeScript, Lisp, Python, Scala, **Rust**
  - Synthetic: GLSL, LaTeX, Spice, Verilog
- **Libraries, and Tools:**
  - Computational: Boolector, CaDiCaL, **Google OR-Tools**, GMP, OpenCL, OpenMP, Rink.rs, SageMath, Z3
  - Graphical: X11, XCB, Cairo, Pango, Unicode CLDR, GTK, Qt