

Experiment No.1

- Aim :- To study and plot forward and reverse characteristics of PN Junction diode.
- Objective :- To find cut-in voltage (V_A)
- Requirements - Diode characteristics trainer kit, Patch cards, multimeter.

Circuit diagram :-

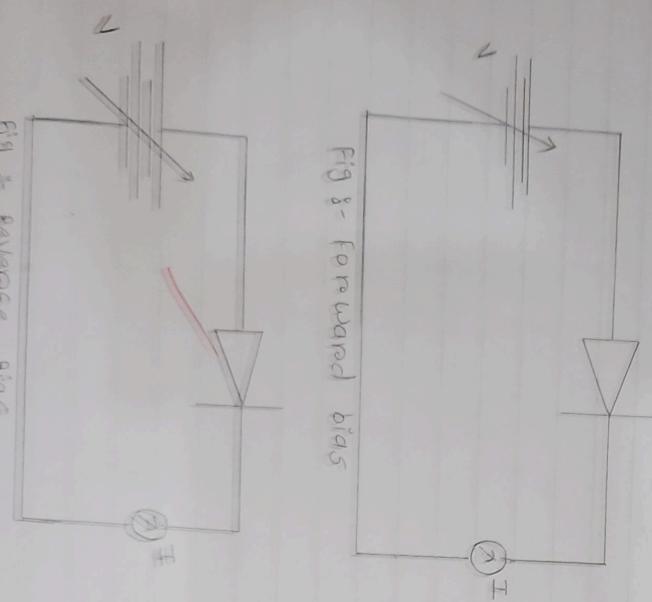


Fig 8 - forward bias

Experiment No. 2

- Aim :- To study and plot forward and reverse characteristics of PN Junction diode.

Theory :-

P-N Junction diode :-

• P-N Junction diode is a p-type zone and n-type zone connected to each other. In p-type holes are majority charge carriers & electrons are minority charge carriers & vice versa. In n-type electrons are majority charge carriers & holes are minority charge carriers & vice versa.

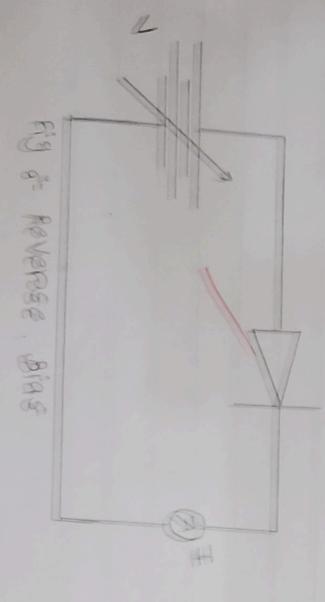


Fig 8 - reverse bias

Experiment No. 1

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- Aim :- To Study and plot forward and reverse characteristics of PN Junction diode.
- Objective :- To find - cut-in - Voltage (V_f)

- Requirements :- Diode characteristics trainer kit, Patch cards, multimeter.

Circuit diagram :-



Fig 1:- Forward bias

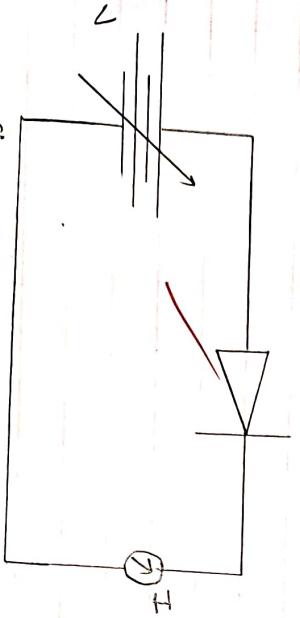


Fig 2:- Reverse bias

- Requirement :- Diode characteristics trainer kit, Patch cards, multimeter.

Theory :-

P-N Junction diode :-

In P-N Junction diode P-type and N-type are connected to each other. In P-type holes are majority charge carriers & electron are minority charge carriers, similarly. In N-type electron are majority charge carriers and holes are minority charge carriers.

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To be known

- Two basic types of materials
- Conductors & Insulators
- Semiconductors

- There are three type of material
- In ideal condition.

- ① Conductor : In conductor current is maximum and resistance is minimum.

- ② Insulator : In insulator resistance is maximum and current is minimum.

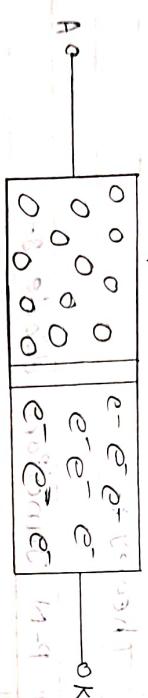


Fig: No bias condition

Fig: No bias condition at room temperature

(ii) Forward Bias Condition.

In forward bias condition P-type is connected to the positive terminal & N-type is connected to the negative terminal. Negative terminal of battery repel the electron and positive terminal of battery repel the holes & the electron forced to move towards the positive terminal so electron flow in anticlockwise and current flow clockwise.

(iii) Reverse Bias Condition.

In reverse bias condition P-type is connected to the negative terminal & N-type is connected to the positive terminal. So holes are attract toward negative terminal & electron is attract toward positive terminal so the electron & holes move away from each other due to which large depletion layer is formed.

Fig :- Reverse Bias Condition.

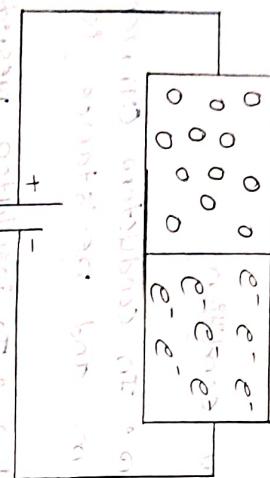
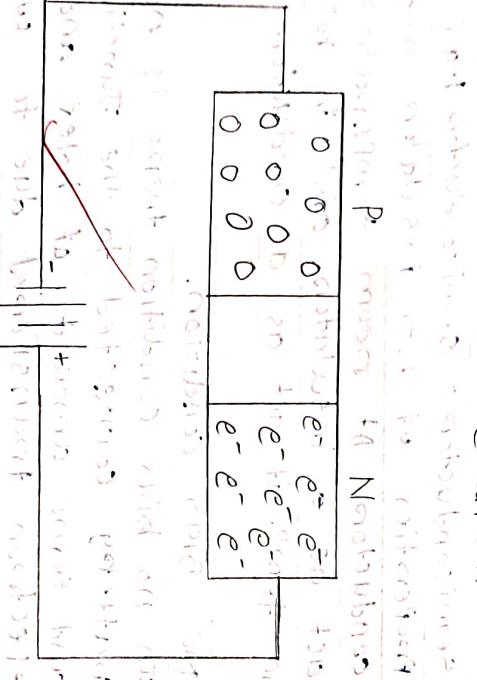


Fig :- Forward Bias Condition.



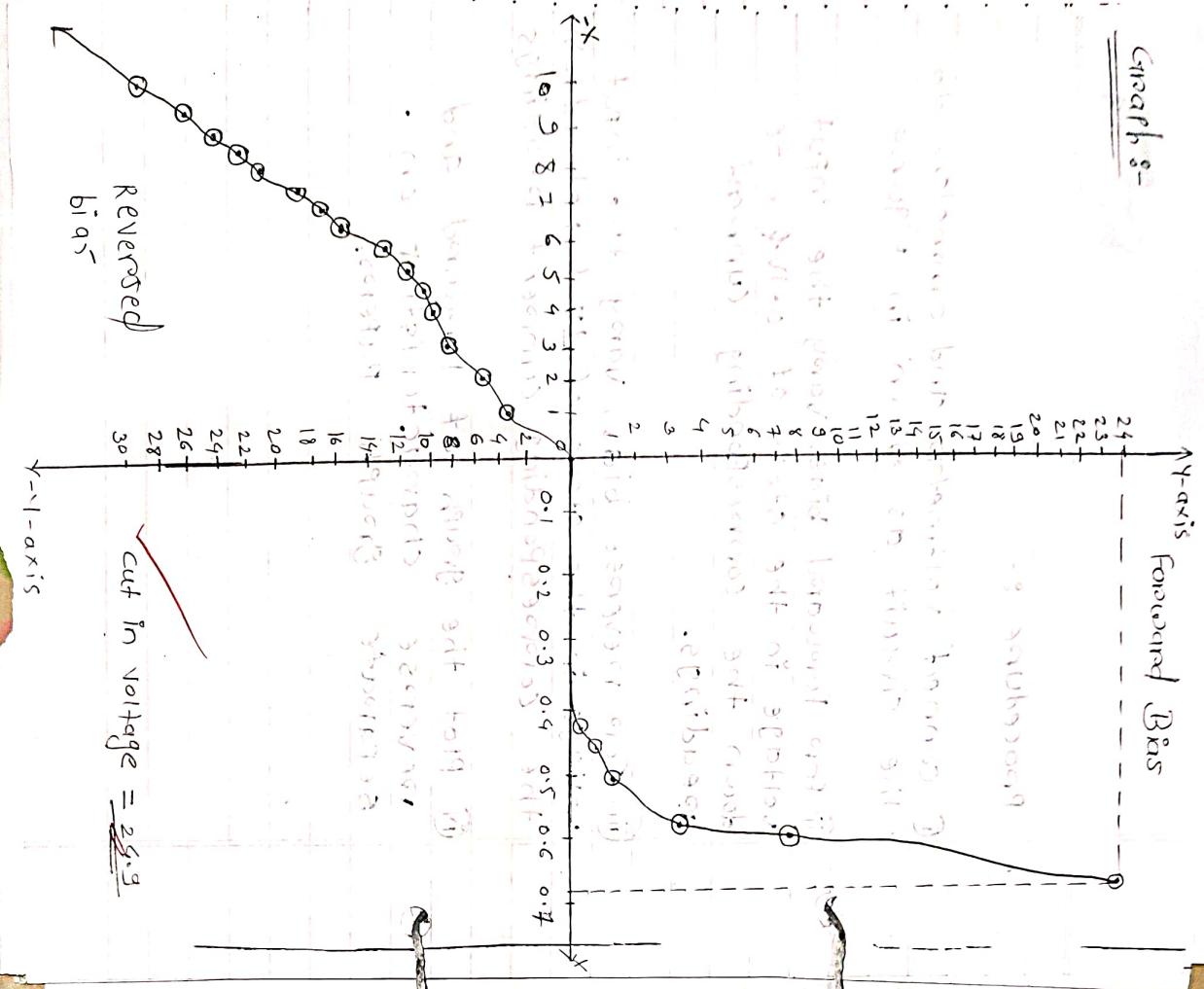
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Procedure :-

- i) Connect voltmeter and ammeter to the circuit as shown in figure.

ii) For forward bias, vary the input voltage in the steps of 0.1V & note down the corresponding current readings.

iii) For reverse bias, vary the input voltage in the steps of 1V & note down the corresponding current readings.



Forward characteristics	Reverse characteristics		
Vf (V)	I (mA)	Vr (V)	I (mA)
0	0	0	0
0.1	0	1	3.3
0.2	0	2	5.1
0.3	0	3	7.2
0.350	0	4	9.4
0.400	0	4.5	10.7
0.440	0.1	5	11.9
0.450	0.2	5.5	13.3
0.500	1.0	6	14.8
0.550	3.4	6.6	16.8
0.600	8.3	7	17.8
0.682	24.9	7.5	19.5
		8	21.2
		8.5	22.9
		9	24.9
		9.5	26.9
		10	29.0

Result

Cut in voltage = 23.9

Cut in voltage = 23.9 0.68

Reversed
bias

cut in voltage = 23.9

Conclusion :-

- In No bias condition, the external voltage isn't applied hence no current flows.
 - In forward biased condition, the depletion layers get thinner & hence we get maximum amount of current due to flow of majority of electrons.
 - In reverse biased condition, the depletion layers get thicker & hence no current flow through junction.
- Cut in cutting voltage :** minimum voltage required to conduct electricity.

~~Forward Cut in~~

Condition	Voltage (V)	Current (A)
No Bias	0	0
Forward Bias	0.2	1.0
Forward Bias	0.5	2.0
Forward Bias	0.8	3.0
Forward Bias	1.0	4.0
Forward Bias	1.2	5.0
Forward Bias	1.5	6.0
Forward Bias	1.8	7.0
Forward Bias	2.0	8.0
Forward Bias	2.2	9.0
Forward Bias	2.5	10.0
Forward Bias	2.8	11.0
Forward Bias	3.0	12.0
Forward Bias	3.2	13.0
Forward Bias	3.5	14.0
Forward Bias	3.8	15.0
Forward Bias	4.0	16.0
Forward Bias	4.2	17.0
Forward Bias	4.5	18.0
Forward Bias	4.8	19.0
Forward Bias	5.0	20.0
Forward Bias	5.2	21.0
Forward Bias	5.5	22.0
Forward Bias	5.8	23.0
Forward Bias	6.0	24.0
Forward Bias	6.2	25.0
Forward Bias	6.5	26.0
Forward Bias	6.8	27.0
Forward Bias	7.0	28.0
Forward Bias	7.2	29.0
Forward Bias	7.5	30.0
Forward Bias	7.8	31.0
Forward Bias	8.0	32.0
Forward Bias	8.2	33.0
Forward Bias	8.5	34.0
Forward Bias	8.8	35.0
Forward Bias	9.0	36.0
Forward Bias	9.2	37.0
Forward Bias	9.5	38.0
Forward Bias	9.8	39.0
Forward Bias	10.0	40.0
Reverse Bias	-0.2	0.05
Reverse Bias	-0.5	0.1
Reverse Bias	-0.8	0.15
Reverse Bias	-1.0	0.2
Reverse Bias	-1.2	0.25
Reverse Bias	-1.5	0.3
Reverse Bias	-1.8	0.35
Reverse Bias	-2.0	0.4
Reverse Bias	-2.2	0.45
Reverse Bias	-2.5	0.5
Reverse Bias	-2.8	0.55
Reverse Bias	-3.0	0.6
Reverse Bias	-3.2	0.65
Reverse Bias	-3.5	0.7
Reverse Bias	-3.8	0.75
Reverse Bias	-4.0	0.8
Reverse Bias	-4.2	0.85
Reverse Bias	-4.5	0.9
Reverse Bias	-4.8	0.95
Reverse Bias	-5.0	1.0
Reverse Bias	-5.2	1.05
Reverse Bias	-5.5	1.1
Reverse Bias	-5.8	1.15
Reverse Bias	-6.0	1.2
Reverse Bias	-6.2	1.25
Reverse Bias	-6.5	1.3
Reverse Bias	-6.8	1.35
Reverse Bias	-7.0	1.4
Reverse Bias	-7.2	1.45
Reverse Bias	-7.5	1.5
Reverse Bias	-7.8	1.55
Reverse Bias	-8.0	1.6
Reverse Bias	-8.2	1.65
Reverse Bias	-8.5	1.7
Reverse Bias	-8.8	1.75
Reverse Bias	-9.0	1.8
Reverse Bias	-9.2	1.85
Reverse Bias	-9.5	1.9
Reverse Bias	-9.8	1.95
Reverse Bias	-10.0	2.0

Experiment No 2

Aim:- To study & verify the truth table of 104748s as four bit comparator.

MATERIAL AND EQUIPMENT:- Digital multimeter patch
oscilloscope, power supply +5V

Circuit Diagram: ~~using~~ ^{using} comparators OR
AND, OR gates & logic symbols

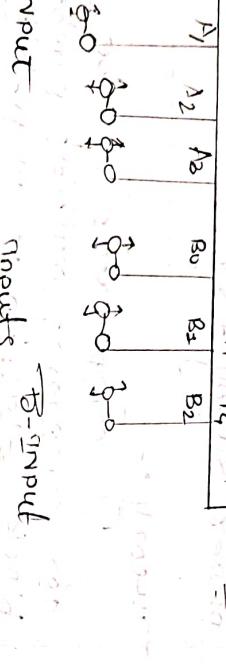
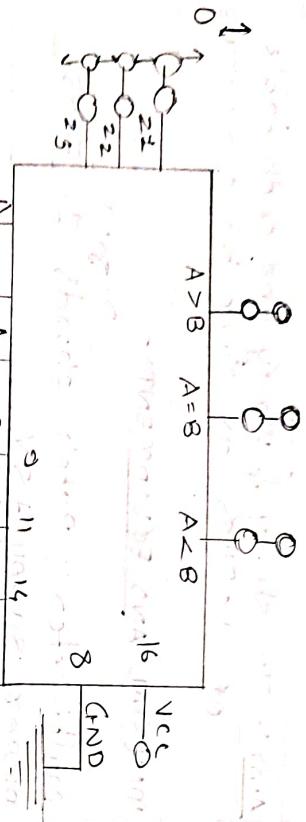
Procedure to obtain 104748s
connection

Theory:- A comparator can be designed for comparing multibit numbers. The block diagram of an n-bit comparator is shown below. It receives two n-bit numbers, A & B as inputs and the outputs one $A > B$, $A = B$, or $A < B$.

Depending upon the relative magnitude of the two numbers, one of the output will be HIGH.

The IC 748s is comparator IC which can be used for 2, 4, 5 bit comparator. The truth table of 2-bit & 4-bit comparator is shown in the following figures.

Circuit Diagram

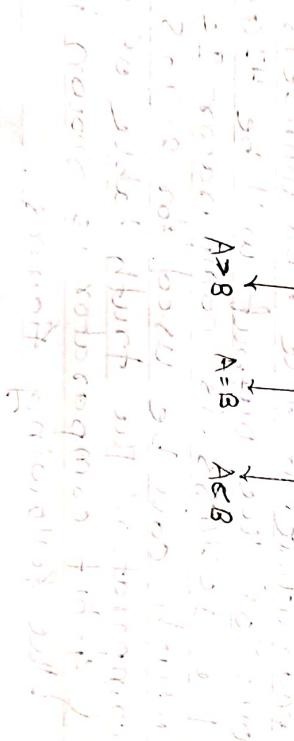
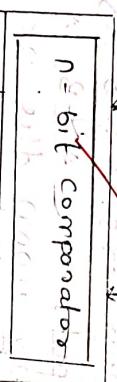


A - Input

B - Input

True ICs can be cascaded to compare words of greater length without external gates. The $A > B$, $A = B$, and $A < B$ cascading inputs of the next stage handling more-significant bits. The stage handling the least-significant bits must have $A = B$ input connected to logic 0 or 1 level. The function of IC 7485 is given by truth tables.

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Procedure:-

- 1) Connect the logic inputs to the logic section.
- 2) Switch 'ON' the power supply.
(A-INPUT) & B3-B0 (B-INPUT) from logic I/P section.
- 3) Also apply the inputs to cascading I/Ps from logic I/P section.
- 4) For 2 bit comparator - apply the inputs to A3-A0 & B3-B0. Change the logic inputs to ascending order corresponding outputs. Repeat the step for the different combinations.
- 5) For 4 bit comparator apply the inputs to A3-A0 & B3-B0. Change the logic inputs as per truth table & observe the corresponding outputs. Repeat the steps for the different combinations.

Function table for 4-bit comparator.

Comparing inputs		Cascading Inputs					Outputs				
A, B	A > B	A = B	A < B	A > B	A = B	A < B	A, B	A > B	A = B	A < B	
A > B	X	X	X	1	0	0					
A > B	1	0	0	1	0	0					
A > B	X	1	X	0	1	0					
A = B	0	0	1	0	0	1					
A = B	0	0	0	0	0	1					
A < B	1	0	1	0	0	0					
A < B	X	X	X	0	0	1					

Result :- True 2-bit & 4-bit comparator using IC 7485 is studied.

Conclusion:- In this experiment we conclude that we learned about 2-bit and 4-bit comparator using IC 7485 & how they work.

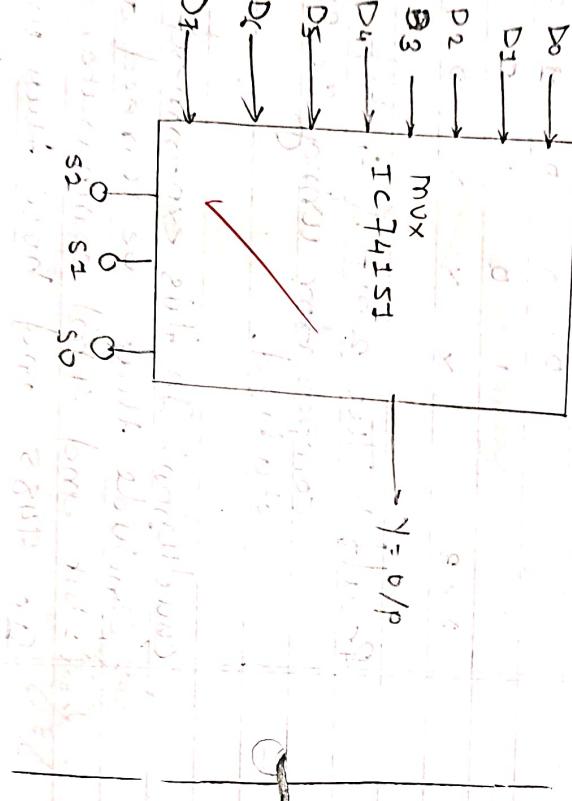
Experiment No. 7

Aim:- To study mux & dmux using IC 74151 & IC 74155.

Material and Equipment:-

Experimental kit of IC 74151 & IC 74155 patch cords.

Diogram:-



Mux

(Multiplexers):-

A multiplexer (mux) or data selector is a logic circuit that accepts several data input and allows only one of them at a time to get through the output. The routing of the desired data input to the output is controlled by select inputs. The shows functional diagram of general multiplexer. In this diagram, the inputs & outputs

The multiplexer acts like digital controlled multi-position switch. The digital code is applied to the select input determines which data inputs will be switch to the output ~~multiplexor~~ selector. The output ~~multiplexor~~ selector input data sources & transmit the selected data to a single output channel. This is called multiplexers.

A 8:1 mux has 8 input signals and 4 output signals. For this circuit control signal be 3. The output of multiplexer depends on the input bit i.e selected. In the circuit the input signals are labeled from D₀ to D₇. Only one output here is transmitted to the output which depends on value of control signals labeled A₀ to A₂.

Procedure:-

- 1) ~~Switch ON~~ the power supply of the kit.
- 2) Connect J1/Ps D₀-D₇ to logic I/P Do to D₇ using patch cords
- 3) ~~Very~~ control inputs. Observe and note O/P proportional to selected J1/Ps as per the truth table.

Observations:-

	INPUTS				O/P
E	A2	A1	A0	Y	
0	0	0	0	0	D0
0	0	0	1	1	D1
0	0	1	0	0	D2
0	0	1	1	1	D3
0	1	0	0	0	D4
0	1	0	1	1	D5
0	1	1	0	0	D6
0	1	1	1	1	D7.

Result:-

Hence the S:1 mux using
S:1 and Y:8 B mux has
studied and verified its truth table.

Done by Bhagwati

Experiment No.

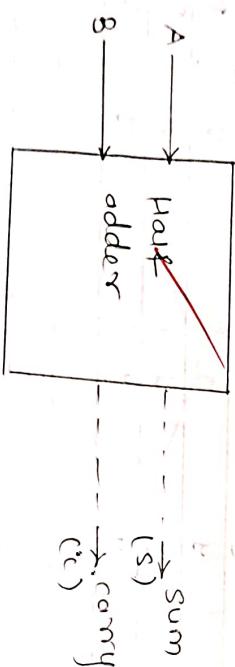
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Aim:- To study & verify truth table of half adder using logic gates.

Equipment :-

Adder trainer kit.

Circuit diagram:-



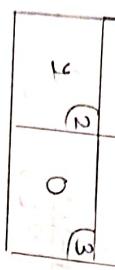
Theory:- Equipment :- Adder trainer kit.

- Adders are digital circuit that carry out addition of number. Adders are key component of arithmetic logic unit. It can be constructed for most of numerical representation like binary coded Decimal (BCD), excess -3, Gray code, etc.
- The most frequent task performed is the binary addition. Apart from this adders are also used in certain digital applications like table index calculation, address decoding etc.

Logic diagram for sum



2 input EX-OR



K-map simplification

A	B	Sum(S)
0	0	0
0	1	1
1	0	1
1	1	0

Truth table for sum output

A	B	Carry(C)
0	0	0
0	1	0
1	0	0
1	1	1

- True truth table and K-map simplification & logic diagram for carry is shown.
- If A & B are binary inputs to half adder then the logic function to calculate C is EX-OR of A & B logic function to calculate carry (C) is AND OR A & B. combining this two logical circuit to implement the combinational circuit of half adder as shown As we know that NAND and NOR are called universal gates or any logic system can be implemented using these two, the half adder circuit can also be implemented using them.
- We know that a half adder circuit has one EX-OR gate of one AND gate.

logic diagram. Por

candy output



2 INPUT AND

A
B
C
D

○	○
○	○
○	○

K-map simplification
for carry output

B A


A hand-drawn diagram of a container. It features a large rectangular base with a smaller rectangular cutout on its left side. A curved line extends from the bottom center of the base upwards and to the right, forming a handle or spout. Below the base, a short vertical line leads down to a horizontal oval at the bottom. To the right of the oval, the word "candy" is written vertically in cursive script, with a red arrow pointing from the word to the oval.

Procedure:-

① Half Adder :- Half adder is a combinational circuit that performs simple addition of two binary nos. If we take some A & B as the two bits whose addition is to be performed the block diagram of a truth table for half adder with A, B. are inputs of sum carry as outputs can be tabulated as follows:-

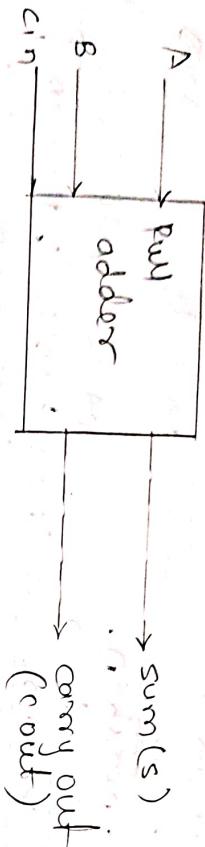
Inputs		Output	
A	B	sum(s)	carry(c)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Teacher's Signature -

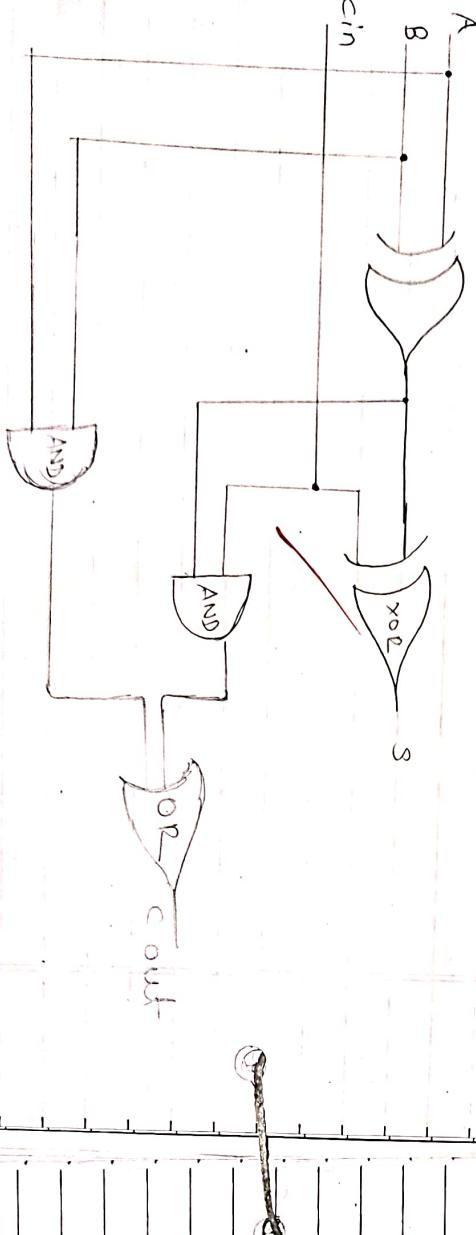
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- The sum output of binary addition carries out above is similar to that of an EX-OR operation while carry output is similar to that of an AND operation.
- The truth table and be verified by K-map. The truth table & K-map simplification & logic diagram for sum output is:

Block diagram of full adder.



full adder logic diagram



Inputs			Output	
A	B	Cin	sum	carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

A	B	00	01	11	10
		0	Y	0	1
		1	0	1	0

K-map for Sum
 $S = A'B'cin + A'B'cin + ABCin$

A	B	C	00	01	11	10
			0	0	1	0
			1	1	1	1

K-map for cout

$c_{out} = AB + A'cin + B'cin$

Conclusion:-

Thus we have studied and verified the truth table of half adder using logic gate.

Harshil Patel
21/11/2021

Practical No.

Aim :- To study and verify Half of full

Equipment :- subtractor trainer kit.

Theory:-

Introduction:-

Subtractor circuits take two binary no. as input & subtract one binary no. from the other binary no. input. Similar to adders it gives out two outputs difference & borrow. There are two type of subtractor.

1. Half subtractor
2. Full subtractor

ii. Half subtractor:

The half subtractor is a combinational circuit which is used to perform subtraction of two bits if has two inputs. A (minuend) and B (subtrahend) and two output difference & borrow. The logic symbol & truth table are shown in Fig. 04.

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Inputs	Output
A 0	Difference Borrow 0
B 0	0 0
A 1	1 1
B 1	1 0
A 0	0 1
B 0	0 0
A 1	0 0
B 1	0 1

Fig 2:- Truth table of HALF subtractor.

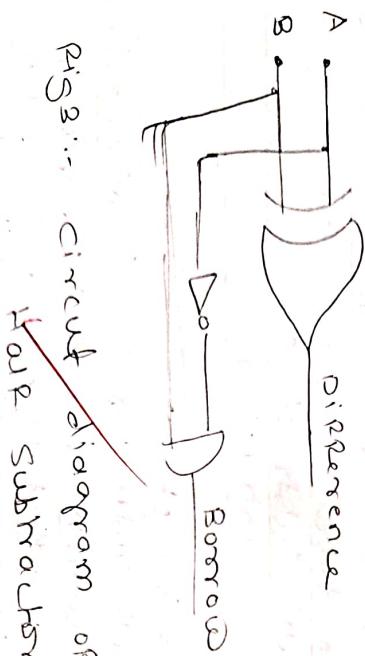
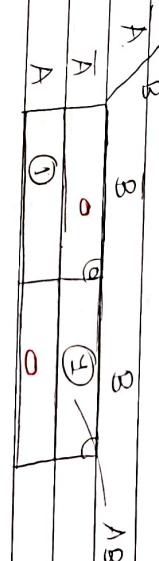


Fig 3:- Circuit diagram of our subtractor

From the equation we can draw the half subtractor circuit in Fig 3.



$$\text{Difference} = \overline{A}B + AB$$

$$= A \oplus B$$

K-map for Borrow :-

A	B	0	0	1	1
0	0	0	0	0	0
1	0	0	1	0	1

$$\text{Borrow} = \overline{A} \cdot \overline{B}$$

The truth table can be verified by K-map.

2) PULL Subtractor:-

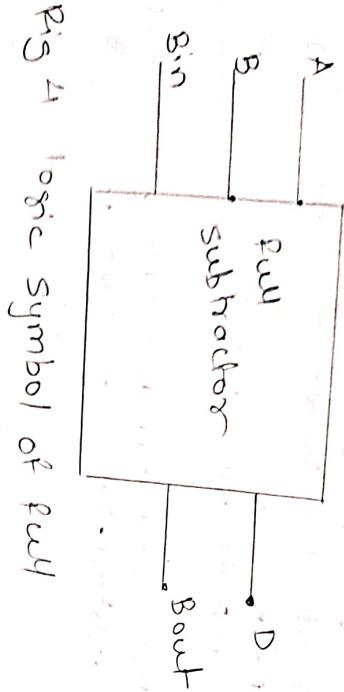


Fig 4 Logic symbol of pull subtractor

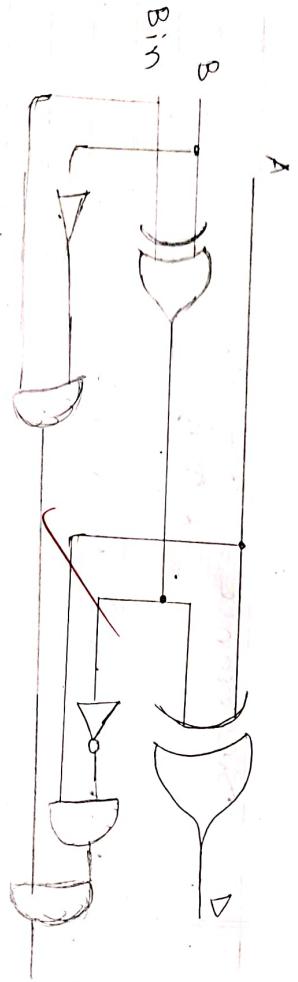


Fig 6. circuit diagram of pull subtractor

Truth table.

A	B	Bin	D	B'out
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	0
1	1	1	1	0

Fig 5:- Truth table of pull subtraction

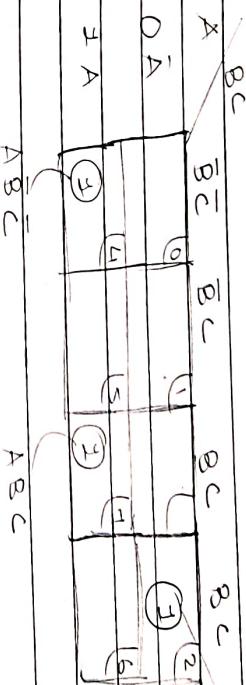
$$D = A \oplus B \oplus \text{Bin}$$

$$\text{B'out} = A \cdot \text{Bin} + A' \cdot B' + B \cdot \text{Bin}$$

From the eqn we can draw the pull-subtractor circuit in Fig 6.

Name of Practical

• K-map for difference.

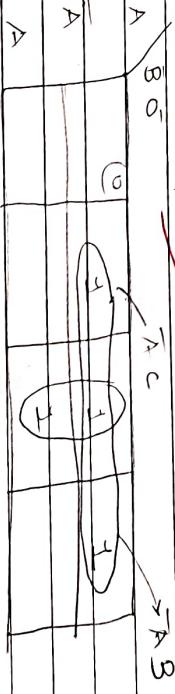


$$D = \bar{A}B\bar{C} + A\bar{B}C + A\bar{B}\bar{C} + AB\bar{C}$$

$$D = \bar{A}B\bar{C} + \bar{A}\bar{B}C + A(B\bar{C} + \bar{B}C)$$

$$D = A \times \bar{B} \times A (B\bar{C} + \bar{B}C)$$

• K-map for Borrow



$$B_0 = \bar{A}C + AB + BC$$

$$B_0 = \bar{A}C + \bar{A}B + BC$$

~~(Conclusion) - Two we've studied topic
gates & OR half & full
subtraction~~

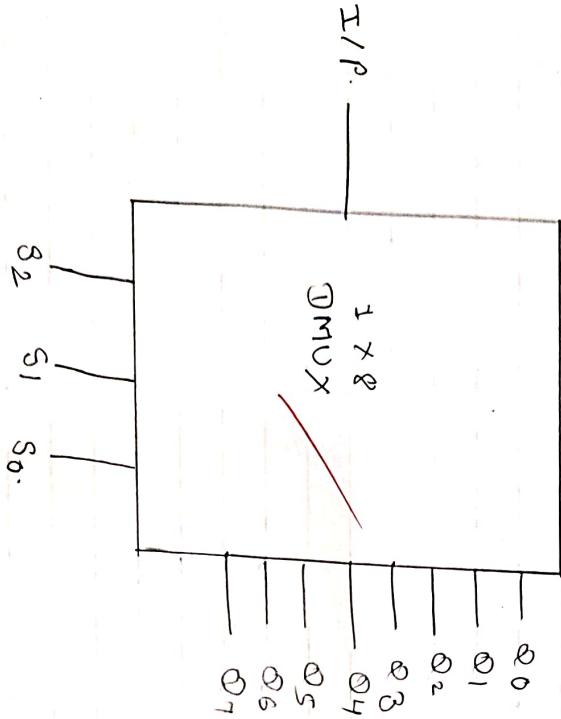
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Practical No. 05

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Aim : To study DMUX using IC 74155
material and equipment :- experimental kit
of IC 74155, patch cords

Circuit Diagram



Theory:-

Demultiplexer

A demultiplexer performs the reverse operation: it takes single input & distributes it over several outputs. So a demultiplexer can be thought of as a distributor since it transmits the same data at different destination thus, where as a no. multiplexer is an N - to - 1 device a demultiplexer is a 1 - to - N (2^n) device. Figure shown the functional diagram of DEMUX.

The larger arrows for inputs & outputs represent one or more lines. The select input code determine the output line to which the input data will be transmitted.

Name of Practical

Procedure:-

1. Switch ON the power supply of the kit
2. Connect 'I/P₁' or '0' to A₁ AD control
3. Select 'I/P' and enable pin
4. Keep Enable I/P at logic 0 vary the A₂ & A₀ I/P's & verify the truth table.

Observation:-

Select input	Outputs
--------------	---------

A ₀	A ₂	A ₁	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇
0	0	0	0	1	1	1	1	1	1	1
0	0	1	1	0	1	1	1	1	1	1
0	1	0	1	1	0	1	1	1	1	1
0	1	1	1	1	1	0	1	1	1	1
1	0	0	1	1	1	1	0	1	1	1
1	0	1	1	1	1	1	1	0	1	1
1	1	0	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	0

Result: Hence the 1.8 DMUX has studied & verified its truth table.

Result: Hence here 1.8 DMUX has studied & verified its truth table.

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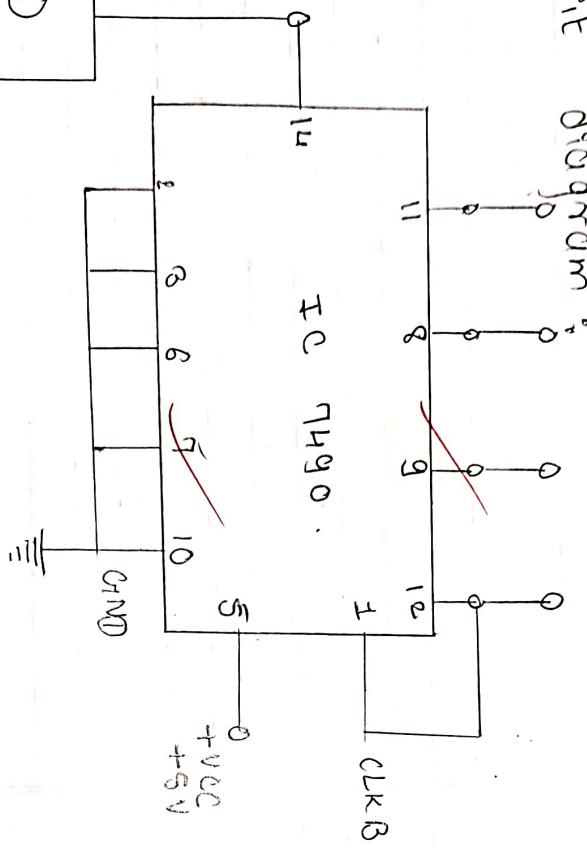
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Name of Practical

Aim : To study decade counter using IC 7490 and verify its truth table.

Material and equipment : Patch cords, IC 7490, IC 7400, LED's

Theory :- The counter has a gated zero reset and also has gated set-to-nine inputs for use in BCD nine's complement applications. To use the maximum count length, the B input is connected to the QA output. The input count pulses are applied to inputs A and the outputs are described in the appropriate truth table. A symmetrical divide-by-ten count can be obtained from the counter by connecting the QA output to A input & applying the input count to the B input which gives a divide-by-ten square wave at outputs QA.



Clock Generator

IC 7490

Teacher's Signature _____

Name of Practical

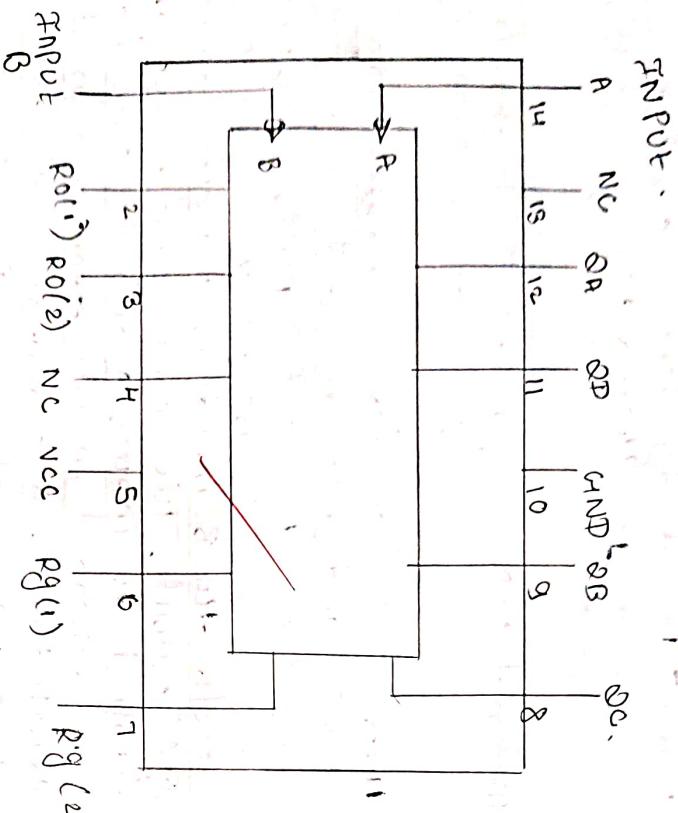
The 7450 integrated circuit counts the no. of pulses occurring at its input the number of pulses counted (up to 5) appears in binary form on four pins of the IC.

When the tenth pulse arrives at the input, the binary output is reset to zero (0000) & a single pulse appears at one output pin.

Procedure:-

- 1) Switch 'No' the power supply of the kit.
- 2) Apply the logic clock pulse as input slowly one.
- 3) Observe the outputs & verify the truth table.
- 4) That is apply the dock pulse to the pin no 24 & observe the O/P after each dock pulse.

Observations :-



Name of Practical

Decimal clock pulse Output

		Q0 Q1 Q2 Q3
0	↑	0 0 0 0
1	↑	0 0 0 1
2	↑	0 0 1 0
3	↑	0 0 1 1
4	↑	0 1 0 0
5	↑	0 1 0 1
6	↑	0 1 1 0
7	↑	0 1 1 1
8	↑	1 0 0 0
9	↑	1 0 0 1

Result:-

It is observed that the decoder counter counts from 0000 to 1001 after 1001 it reset to 0000. Hence it counts 10 clock pulses.

Practical No. 02

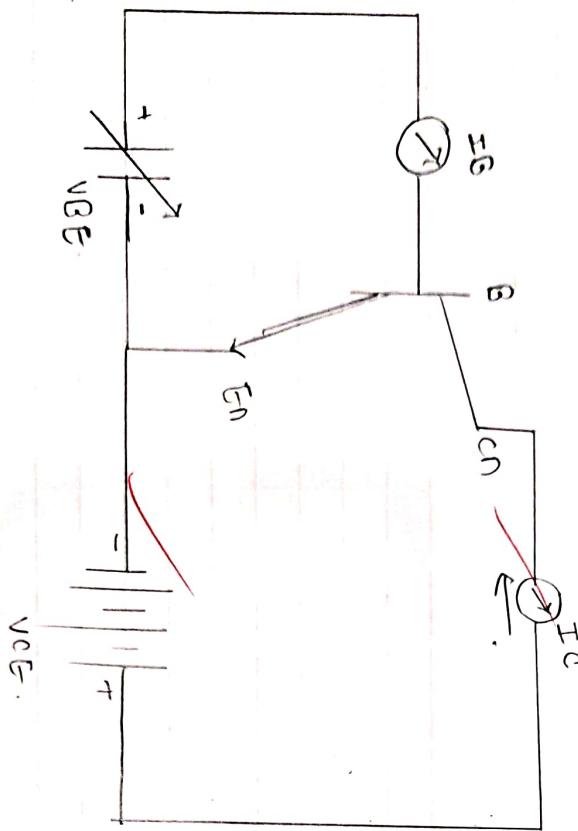
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Practical No. 8

Name of Practical

Aim :- To study & plot input & output characteristic of common emitter (CE) configuration of NPN transistor.

Requirement :- Transistor characteristics trainer kit patch cords.



Theory :-

- CE configuration is the most widely used configuration of transistor.
- Qs characteristic eqn is : $\eta_c = \alpha E + I_{cE0}$
- Emitter terminal is held common to both input & output
- Input characteristic of CE configuration is the graph of I_B vs V_{BE} at constant V_{CE} .
- Output characteristic of CE configuration is the graph of I_C vs V_{CE} at constant I_B .

Name of Practical

Procedure:-

- (i) Make the connections as per circuit diagram.
- (ii) To plot input characteristics, keep V_{CE} constant, vary different values of V_{BE} & note corresponding I_B .
- (iii) To plot output characteristics, keep I_B constant, vary the V_{CE} and note down corresponding I_E .

on X-axis
 $J_{dm} = 0.3 \text{ unit}$
on Y-axis
 $I_{cm} = 30 \text{ unit}$

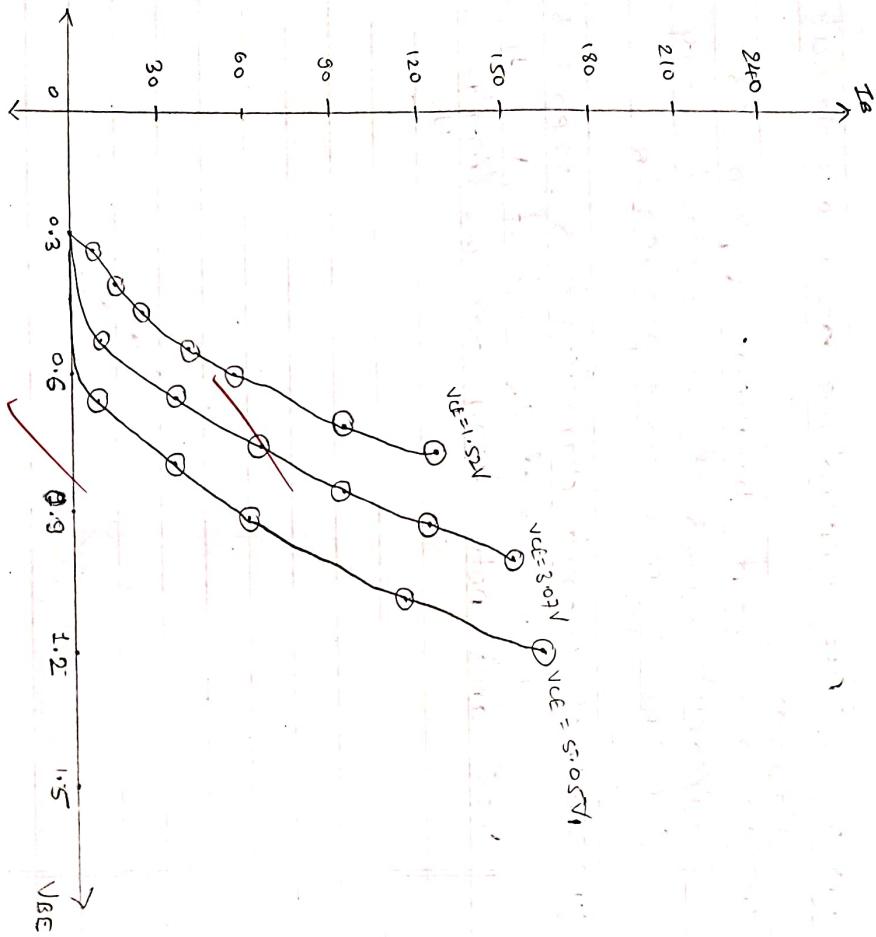
$V_{CE} = 3.07V$
 $V_{CE} = 5.05V$

1) Input characteristics.

$$V_{CE} = 3.07V \quad V_{CE} = 5.05V$$

$$\begin{array}{|c|c|c|c|c|c|} \hline V_{BE} (V) & I_B (\mu A) & V_{BE} (V) & I_B (\mu A) & V_{BE} (V) & I_B (\mu A) \\ \hline 0.1 & 0 & 0.1 & 0 & 0.1 & 0 \\ 0.2 & 0 & 0.2 & 0 & 0.2 & 0 \\ 0.3 & 0 & 0.3 & 0 & 0.3 & 0 \\ 0.41 & 0.4 & 0.4 & 0.01 & 0.4 & 0.1 \\ 0.50 & 0.51 & 0.51 & 0.16 & 0.5 & 5.8 \\ 0.61 & 15.0 & 0.61 & 15.8 & 0.64 & 22.7 \\ 0.70 & 47.4 & 0.75 & 49.1 & 0.75 & 46.7 \\ 0.80 & 68.1 & 0.82 & 69.7 & 0.8 & 70.1 \\ 0.9 & 88.6 & 0.91 & 95.2 & 0.99 & 120.5 \\ 1.05 & 134.8 & 1.07 & 140.5 & 1.14 & 165.0 \\ 1.10 & 152.3 & 1.20 & 178.5 & 1.30 & 1. \\ \hline \end{array}$$

Observation:-



For output

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Scale on x-axis
1cm = 1 unit

on y-axis
2cm = 0.05 cm

Name of Practical
N/A

$I_B = 15.3 \text{ A}$

$I_B = 18.4$

$I_B = 24.3$

Scale on x-axis
1cm = 1 unit

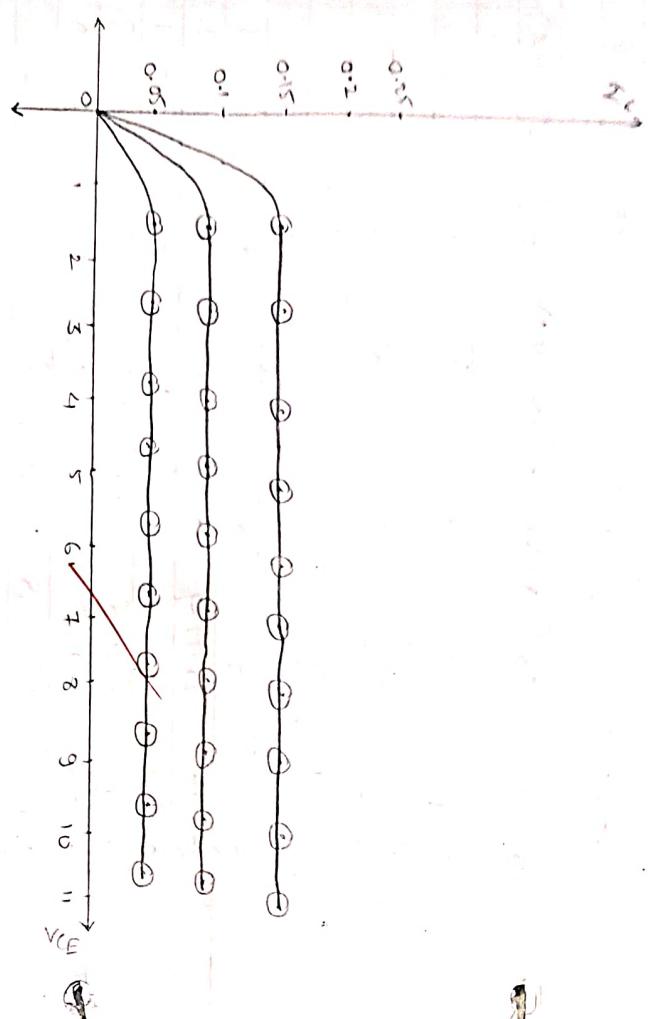
on y-axis
2cm = 0.05 cm

Name of Practical
N/A

$I_B = 15.3 \text{ A}$

$I_B = 18.4$

$I_B = 24.3$



Result: Thus we have studied Input & output characteristic of CE configuration of the NPN transistor.

Result: Thus we have studied Input & output characteristic of CE configuration of the NPN transistor.

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