Computer Architecture - CS2323

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Lab-6 Report

The Code is written in C language and it's aim is to implement a Cache Simulator as per the specifications provided by the user(Direct Mapped Cache, Set Associative Cache, Fully Associative Cache).

IMPLEMENTATION

- Each Block stores Tag decimal value, Valid bit and LastAccessed variable which shows the last accessed number(higher the number means most recently used). Which is given values of 'timer' variable which is global and incremented every time a block is accessed.

- Each line in the cache.access file is taken and Each line must be in the form Mode: 0x00000000 i.e,for example R: 0x00123456 with address always in 8 hex digits with no extra spaces and every line ending with a newline character just after the Hex address.

- The hex Address is taken as a string and converted into a binary String of size 4 times the hex string by a function hexToBinary, And By string cutting according to the number of indexBits(log2(blocks/ASSOCIATIVITY)), offsetBits(log2(size of Block)), andk Total 32 bits of Address we get decimal values of index, tag by stringToDecimal function.

- According to the mode of each line either 'R' or 'W' indicating read and write respectively if there is a Cache hit , the lastAccessed time is changed to current. Or if it is a Cache miss, it is checked whether it is in R or W mode, if it is in R mode, just replace the block's tag By any of the three replacement methods(FIFO-First In First Out, LRU-Least Recently Used, RANDOM- Randomly replacing blocks in the same set or index).

- If there's a Cache miss and the instruction is in W mode, we check whether it is Write through without Allocate(WT) or Write Back with Allocate(WB).
- If it is WT then the address, tag ,set are printed directly without accessing any block and changing.Or if it is WB then the process is the same as when it was a R mode, that is replacing and changing access time and Valid Bit.

CORRECTNESS

I have checked many output files and cross checked with my outputs for those particular Cache configurations and Address modes. I have checked the Direct mapped Cache configuration first with FIFO,RANDOM,LRU policies and cross checked my output tag,set,cache misses and hits.

After that I checked for Fully Associative Cache configuration with all the three replacement policies , and Set associative cache configuration thereafter.