The OpenPicoAmp-100k: an open-source high performance amplifier for single channel recording in planar lipid bilayers.

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Abstract

We propose an upgraded version of our previously designed open-source lipid bilayer amplifier. This improved amplifier is now suitable both for the use in introductory courses in biophysics and neurosciences at the undergraduate level and for scientific research. Similar to its predecessor, the OpenPicoAmp-100k is designed using the common lithographic printed circuit board fabrication process and off-the-shelf electronic components. It consists of the high-speed headstage, followed by voltage-gain amplifier with built-in 6-order Bessel filter. The amplifier has a bandwidth of 100 kHz in the presence of 100 pF input membrane capacitance and is capable of measuring ion channel current with amplitudes from sub-pA and up to ± 4 nA. At the full bandwidth and with a 1 G Ω transimpedance gain, the amplifier shows 12 pA_{rms} noise with an open input and 112 pA_{rms} noise in the presence of 100 pF input capacitance, while at the 5 kHz bandwidth (typical in single-channel experiments) noise amounts to 0.45 pA_{rms} and 2.11 pA_{rms}, respectively. Using an optocoupler circuit producing TTL-controlled current impulses and using 50% threshold analysis we show that at full bandwidth the amplifier has deadtimes of 3.5 µs and 5 µs at signal-to-noise ratios(SNR) of 9 and 1.7, respectively. Near 100% of true current impulses longer than 5 µs and 6.6 µs are detected at these two respective SNRs, while false event detection rate remains acceptably low. The wide bandwidth of the amplifier was confirmed in bilayer experiments with alamethicin, for which open ion channel current events shorter that 10 µs could be resolved.

Outline of the amplifier

The amplifier setup consists of two metallic enclosure cases (Figure 1A). First larger case hosts bilayer membrane chamber and smaller enclosure with input voltage divider and the headstage. Second enclosure case contains voltage-gain amplifier and 6-order Bessel filter.

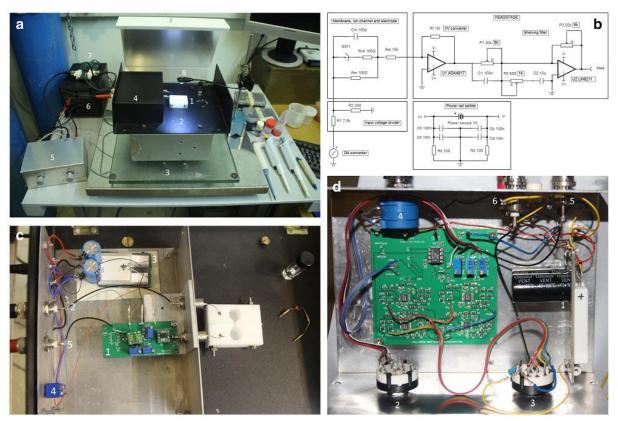


Figure 1. Outline of the amplifier setup. A. General view of the setup. 1-bilayer chamber, 2-bilayer chamber compartment with pivotal lid, 3-anti-vibration table, 4- headstage compartment, 5-voltage gain amplifier, 6- power source, 7-AD/DA converter, 8- light source. B. Electrical schematics of the input voltage divider, schematics of a bilayer membrane composed of membrane capacitance C_m , membrane resistance R_m and ion channel R_i , whose gating is simulated by a time-controlled switch SW1. Pair of electrodes is represented by $R_{\rm el}$. Power supply and headstage schematics are also shown. Bypass capacitors (10 nF and 10 μ F) at the voltage supply pins of the operational amplifiers are omitted for clarity. C. Implantation of the headstage. 1- headstage PCB, 2- input voltage divider, 3- power rail splitter, 4- on/off power switch, 5- output. D. Implantation of the voltage gain amplifier. 1- power rail splitter, 2- voltage gain selector, 3- filter setting selector, 4- offset adjustment potentiometer, 5- input, 6- output.

Power supplies and grounding

Each box is powered via isolated panel socket with a 10 V single voltage that is not referenced to ground. A low-ripple laboratory power source (3 Watts minimum) is an important requirement for a low-noise performance of the amplifier. Good results were obtained using HQ-Power PS603, PS1502A and equivalent laboratory power units. Alternatively, we have designed relatively simple and very low-noise single-voltage power supply based on BD139 transistors.

Details of this power source (schematics, PCB fabrication file and the implementation) can be found in the Supplementary Information below.

Dual voltage rails and virtual ground are generated in close proximity to the circuits. They are created using 100Ω (10W) resistor divider network as shown in schematics in Figure 1B. Since many high-speed and low noise precision operational amplifiers require maximum $\pm 5 V$ voltage supply, this value has been chosen for power alimentation of the complete setup. Hence, two voltage rail splitters are used in the amplifier, one per enclosure case. The 100Ω resistors should be matched to 0.1% to keep the voltage value of the virtual ground as close to zero Volts as possible. No additional grounding arrangement is required as long as the virtual ground and amplifier enclosures are interconnected and have low resistance link to the analog ground of the analog-to-digital converter via BNC cables.

Command signal generation and input voltage divider

All necessary command voltages have to be generated by an external DA converter, preferably with at least 12 bits resolution and ±10V dynamic range. We suggest the MyDAQ (National Instruments) for analog OUT/IN acquisitions up to 200 kS/s or the Analog Discovery II (Digilent) for acquisitions up to 10 MS/s. Both are low-cost devices, for which academic discount is available on the top of their relatively low price. The MyDAQ may be controlled by the open-source WinEDR program (Strathclyde University), while Analog Discovery II is used with the free WaveForms program from Digilent. Alternatively, both interfaces may be controlled by LabView/Matlab with the use of corresponding Application Programming Interface bundles. Even cheaper alternatives exist: PSlab (https://pslab.io/), ISDS205B (Harbin Instrustar Electronic Technology, China) or USB-204 (Measurement Computing Corporation, USA).

The command signals are supplied to the bilayer chamber via the input voltage divider (Figures 1B and 1C). High quality MELF resistors should be used in this circuit to ensure low-noise performance. The command voltage generation by DA-converter should be scaled up accordingly. We found that voltage division at 1/30 to 1/40 is sufficient to eliminate the noise associated with DA conversion at the analog output of the instruments above. This division factor determines the maximal input voltage that can be applied to the experimental chamber; with ± 10 V dynamic range of the DA converters, up to ± 250 -330 mV can be fed to the bilayer chamber in increments of 25-33 μ V. The signal is applied to the chamber compartment via panel mount bulkhead fitting BNC connector, Ag/AgCl electrode and agar bridge. This side of the bilayer membrane makes cis compartment. On the opposite side, the signal is fed to the current-to-voltage converter of the

headstage via agar bridge, Ag/AgCl electrode and BNC connector. Since the inverting input of the operational amplifier of the I-to-V converter creates virtual zero Volts point, this side of the bilayer membrane makes *trans* compartment. No electrode offset nulling circuitry is required if the pair of electrodes is chlorinized in the bleach liquid (Chlorox, eau de Javel etc) with the pins interconnected, which ensures that both have the same potential. Details of electrode fabrication and cleaning can be found in our previous publication [22]. Briefly, measuring and reference electrodes are made from 7 cm long silver wire (Ø0.5 mm), one end of which is bent to helix and another is soldered to a golden pin. Fully chlorinized pair of electrodes should have maximum 5 kOhm of electrical resistance in 1M KCl solution.

The headstage

The schematic circuit of the fast-speed current-to-voltage converter is shown in Figure 1B and the implantation is presented in Figure 1C. Two sides of the corresponding printed circuit boards (PCB) are shown in Supplementary Figure 1. The headstage should be mounted in a separate case in a larger metallic box hosting the bilayer chamber. In order to exclude any mechanical noise, the PCB is to be firmly fixed using a screw and a nut on a metal adapter close to the solder termination of BNC connector coming from the *trans* compartment. We removed all PCB traces around the inverting input of operational amplifier to prevent the interference from PCB leakage currents. The lead from the termination of BNC connector to the amplifier input should be air-wired and should be as short as possible, ideally soldered directly.

The printed circuit boards were designed using EasyEDA Designer software (easyEDA.com) and the JSON source files are provided alongside with GERBER files. PCBs were printed on double-sided FR4 sheets by JLCPCB (Shenzhen JLC Electronics Co., Ltd.). The bottom side of the headstage PCB hosts power supply tracks with bypass capacitors, while the signal tracks are routed on the upper side of PCB. Both 0207 package radial through-hole 1 G Ω resistors and 2010 package SMD 1 G Ω thick film resistors may be used as a feedback element in the headstage with nearly identical performance. We provide additional ground connection point to decrease resistor's stray capacitance (E-shunt). Here, thin wire may be soldered and then wrapped around the R_f resistor near the output side. The trimming resistors are of 3296W package; other resistors are either 1206 package in case of thick film SMD resistors or 0204 package in case of MELF resistors. The ceramic capacitors are of 0805 package. We recommend setting the trimming potentiometers to the values shown in the schematics prior to soldering to facilitate headstage tuning. If other operational amplifiers are to be used, some approximate resistor values may be found in

Supplementary Information below. Surface mount operational amplifiers (SOIC8 and SOP23 packages) were first soldered to SOIC-DIP8 adapters. As outlined in Supplementary Information, we choose ADA4817-1 operational amplifier as an input integrated circuit in I-to-V conversion unit for its low-noise and high-speed performance. Second integrated circuit of the headstage may be any low-noise precision operational amplifier with a bandwidth of at least 20 MHz. This minimal bandwidth is required to extend the frequency response of the headstage to 100 kHz. LM6211, ADA4637, AD8610, LT1028 and LT1128 amplifiers have shown good results. Note that the use of very high-speed amplifier here (ADA4817-1 for example) permits the bandwidth extension to the value above 300-400 kHz. The level of noise, however, becomes comparable to the voltage supply rails, so this high bandwidth is impractical. On the other hand, if only 20 kHz maximal bandwidth is required, then LT1055 or LT1056 precision operational amplifiers can be used in all parts of the amplifier. Assembled PCBs are extensively washed in isopropyl alcohol to remove any solder flux residues. The potentiometer P1 and capacitor C1 set the frequency-response of the amplifier, the potentiometer P3 sets DC gain, while potentiometer P2 together with capacitor C2 are used to prevent amplifier oscillations by adjusting and limiting the high-frequency gain peaking of the headstage. The headstage tuning is performed by applying periodic triangular voltage signal (10-30 V/s, 500 Hz) to a calibrated RC circuit (1 $G\Omega//100$ pF in series with 10 k Ω) and observing the resulting rectangular output signal. The potentiometers P1 and P2 are re-adjusted to obtain maximally rectangular (flat and sharp) pulse. Then the 100 mV DC voltage is applied and the potentiometer P3 is adjusted to bring the output current (i.e. I-to-V converted voltage) to the value predicted by the Ohm's law for the calibrated resistor, hence setting the exact 1 G Ω trans-resistance gain of the headstage. The calibration, i.e. measurement of true value of 1 G Ω resistor may be accomplished by placing this resistor into a voltage divider formed together with precisely measured 10 M Ω resistor. Hence the value of the resistor may be evaluated by sourcing 10 V DC voltage to the divider and measuring the output voltage with microvolt precision. No input offset voltage correction is required in the headstage if suggested precision operational amplifiers are used. Moreover, many precision operational amplifiers including those proposed for the headstage do not even provide offset nulling possibility. Eventual zero adjustment can be left to the second cascade of amplification. The use of the third operational amplifier in the headstage is optional; it may serve as an inverting unity-gain voltage follower, in case if the second cascade of amplification uses inverting topology. It adds, however, some noise; accordingly, low value resistors ($<10 \text{ k}\Omega$) should be used here to limit noise generation.

The voltage-gain amplifier

In order to use the full dynamic range of the AD converter during the observation of very small ionic currents in pA range, further amplification of headstage-generated voltage is required. We propose voltage-gain amplifier in non-inverting topology. The implantation is shown in Figure 1D and two sides of the corresponding PCB are presented in Supplementary Figure 2. With a feedback resistor below 47 k Ω , the bandwidth of the amplifier remains much higher than the bandwidth of the headstage. This ensures that the effective bandwidth of the whole setup is close to the bandwidth of the headstage, at least at low amplification. LT1122, LT1128, LT1028, LT6018 and some other operational amplifiers showed near identical precision and low-noise performance. The offset adjustment may be performed using null pins of the operational amplifier (1, 5 or 8) and panel mounted multi-turn potentiometer according to the datasheet of the op-amp used. If the opamp has no internal nulling possibility, we provide external offset adjustment option using 10 M Ω resistor connected to the inverting input of the amplifier (R_{ref}, Supplementary Figure 2). In this case, the extreme pins of the panel mounted multi-turn potentiometer should be wired to the supply rails, i.e. "offset+" and "offset-" and the middle pin to "wiper". If 47 k Ω feedback resistor is used, than the offset nulling up to ± 25 mV (i.e. ± 25 pA) may be accomplished. This is however at the expense of +0.47% gain error at unity gain. The error can be eventually corrected by re-adjusting DC gain of the headstage (see above). Accordingly, higher offset nulling range is possible with lower value of R_{ref}, provided the readjustment of the DC gain in the headstage. It should be also noted that nulling range in this method is divided by the gain, so the offset adjustment via null pins of the amplifier is the preferred option.

The proposed PCB allows configuration of four different gains, which can be fixed or adjustable. Gain selection is performed by commuting resistors/potentiometers at the points Rg1', Rg2' and Rg3' to the point "Rgain" using single-pole rotating switch. Unity gain is established when no resistor is connected to the "Rgain" point (Supplementary Figure 2).

Given the large bandwidth of the amplifier, the measurement of pA level ion channel currents requires efficient filtering. We propose a 6-order pseudo-Bessel filter based on LTC1563-2 integrated circuit. Two capacitors and six resistors set the cut-off frequency of the filter and four different circuits are used to generate four filter cut-off settings. The outputs of the filter (OUT1, OUT2, OUT3 and OUT4) as well as the by-pass output (OUT_{bypass}) can be commuted to the amplifier BNC output using single-pole rotating switch. A two resistors in series placement is implemented on PCB to allow setting the value of each equivalent resistor to within 1-2% margins of the required theoretical value using commercially available SMD resistors. If different tolerance

SMD resistors are available (1% and 5% for example) then the pre-selection of resistors may allow decreasing this error to below 0.5%. The Table 1 reports the values of resistors and the capacitors for filters with 0.3 kHz, 1 kHz, 3 kHz and 10 kHz cut-off frequencies. The provided PCB may be used to implement any other filters with cut-off frequencies between 256 Hz and 256 kHz according to the procedure described in the datasheet of LTC1563-2 circuit and with the help of free FilterCAD program from Linear Technologies (Analog Devices).

The cost of electronic components used in the described amplifier is estimated to be approximately 125 euros based on retail prices (Table 1) and the overall cost of amplifier implementation is below 250 euros that includes the benchtop low ripple power supply and metallic enclosures cases, one of which serves as a Faraday cage for bilayer chamber. Moreover, these enclosures cases can be self-made and the design of low-noise power supply for electrophysiology amplifier is also available. The overall cost does not include the AD/DA interface that should be purchased separately. The vibration isolation table constructed using marble slab positioned on tennis balls proved to be sufficiently efficient in damping mechanical vibrations. Anti-vibration table consisting of two top cascaded tennis ball–suspended plates provides further improvement in vibration dumping characteristics.

Table 1. Amplifier components

Power supply s	splitter		
Component	Value	Implementation	Price, €
Rd x2	100Ω	10W, wirewound cement filled ceramic	0.68x2
Cb x2	100nF	25V, radial ceramic	0.55x2
Cb' x2	10mF	25V, electrolytic	3.29x2
Connector		Panel mount 2.1mmx5.5mm female socket	6.49
Input voltage o	livider		
Component	Value	Implementation	
R1	7.5kΩ	0204 MELF	0.096
R2	200Ω	0204 MELF	0.236
Connector x2		Coaxial BNC Panel Mount Jack connector	2.27x2
Headstage and	bilayer membra	ne compartment	
Component	Value	Implementation	
PCB board			~1
U1	ADA4817-1	SOIC + DIP8 adaptor	6.06+2.79

IC socket x2		DIP8	0.402x2
Rf	1 GΩ	0207 radial through hole or 2010 smd	0.56
P1	6kΩ	20k 3296W	2.10
C1	100nF	0805 smd	0.123
P2	14 Ω	500 3296W	2.10
C2	10μF	0805 smd	0.123
U2	LM6211	SOP23+DIP8 adaptor	2.50+2.79
P3	6kΩ	20k 3296W	2.10
Cb x4	10nF	0805 smd	0.123x4
Cb' x2	10μF	0805 smd	0.123x2
Connector x2		Coaxial BNC Panel Mount Jack connector	2.27x2
Metallic box		Hammond 1456KK4 enclosure	~35
Metallic box		Hammond 1411L enclosure	~15
Pivot joints x2		S-5005-12-32 pivots 30x19mm	~1
Power switch		Two pole toggle switch	2.38
Voltage gain am	plifier		
Component	Value	Implementation	
PCB board			~1
U5	LT1122	DIP8	7.52
IC socket		DIP8	0.402
Rg1 (gain10)	5.22 kΩ	10k 3296W	2.10
Rg2 (gain30)	1.62 kΩ	2k 3296W	2.10
Rg3 (gain100)	474 Ω	2k 3296W	2.10
Rf	47kΩ	1206 smd	0.087
Cf	10pF	0805 smd	0.123
Cb x2	100nF	0805 smd	0.123x2
C3=C4	10μF	0805 smd	0.123x2
Rref	10ΜΩ	1206 smd	0.087
P1	10kΩ	10k, 7276 series precision potentiometer	11.82
Switch x2		GCK rotary single-pole switch	3.20 x2
Power switch		Two pole toggle switch	2.38
Connector x2		Coaxial BNC Panel Mount Jack connector	2.27x2

Metallic box		Hammond 1411Q enclosure	~20
6 order pseudo-	Bessel filter, 10	kHz	
Component	Value	Implementation	
U1	LTC1563-2	Narrow SOIC14	4.54
Cb x2	100 nF	0805 smd	0.123x2
R1eq=R1+R1'	16.2kΩ	8.2k+8.2k 1206smd	0.087x2
C1	680pF	0805 smd	0.123
R2eq=R2+R2'	150kΩ	150k+0k 1206smd	0.087x2
R3eq=R3+R3'	137kΩ	100k+39k 1206smd	0.087x2
R4eq=R4+R4'	165kΩ	120k+47k 1206smd	0.087x2
R5eq=R5+R5'	11kΩ	10k+1k 1206 smd	0.087x2
C2	1nF	0805 smd	0.123
R6eq=R6+R6'	110kΩ	100k+10k 1206 smd	0.087x2
R7eq=R7+R7'	150kΩ	150k+0k 1206 smd	0.087x2
R8eq=R8+R8'	121kΩ	120k+1k 1206 smd	0.087x2
6 order pseudo-	Bessel filter, 3 k	Hz	
Component	Value	Implementation	
U1	LTC1563-2	Narrow SOIC14	4.54
Cb x2	100 nF	0805 smd	0.123x2
R1eq=R1+R1'	53.6kΩ	47k+6.8k 1206smd	0.087x2
C1	680pF	0805 smd	0.123
R2eq=R2+R2'	511kΩ	330k+180k 1206smd	0.087x2
R3eq=R3+R3'	464kΩ	470k+0k 1206smd	0.087x2
R4eq=R4+R4'	562kΩ	560k+2k 1206smd	0.087x2
R5eq=R5+R5'	45.3kΩ	39k+6.8k 1206 smd	0.087x2
C2	820pF	0805 smd	0.123
R6eq=R6+R6'	365kΩ	100k+10k 1206 smd	0.087x2
R7eq=R7+R7'	511kΩ	330k+180k 1206 smd	0.087x2
R8eq=R8+R8'	412kΩ	390k+22k 1206 smd	0.087x2
6 order pseudo-	Bessel filter, 1 k	Hz	I
Component	Value	Implementation	
U1	LTC1563-2	Narrow SOIC14	4.54

Cb x2	100 nF	0805 smd	0.123x2
R1eq=R1+R1'	162kΩ	150k+12k 1206smd	0.087x2
C1	680pF	0805 smd	0.123
R2eq=R2+R2'	1.54ΜΩ	1M+560k 1206smd	0.087x2
R3eq=R3+R3'	1.4ΜΩ	1M+390k 1206smd	0.087x2
R4eq=R4+R4'	1.69ΜΩ	1M+680k 1206smd	0.087x2
R5eq=R5+R5'	133kΩ	100k+33k 1206 smd	0.087x2
C2	820pF	0805 smd	0.123
R6eq=R6+R6'	1.1ΜΩ	1M+100k 1206 smd	0.087x2
R7eq=R7+R7'	1.54ΜΩ	1M+560k 1206 smd	0.087x2
R8eq=R8+R8'	1.24ΜΩ	560k+680k 1206 smd	0.087x2
6 order pseudo-	Bessel filter, 0.3	kHz	
Component	Value	Implementation	
U1	LTC1563-2	Narrow SOIC14	4.54
Cb x2	100 nF	0805 smd	0.123x2
R1eq=R1+R1'	536kΩ	470k+68k 1206smd	0.087x2
C1	680pF	0805 smd	0.123
R2eq=R2+R2'	5,11ΜΩ	10M//10M+100k 1206smd	0.087x2
R3eq=R3+R3'	4.64ΜΩ	4.7M+0k 1206smd	0.087x2
R4eq=R4+R4'	5.62ΜΩ	4.7M+1M 1206smd	0.087x2
R5eq=R5+R5'	453kΩ	330k+120k 1206 smd	0.087x2
C2	820pF	0805 smd	0.123
R6eq=R6+R6'	3.65ΜΩ	3.3M+330k 1206 smd	0.087x2
R7eq=R7+R7' $5.11M\Omega$		10M//10M+100k 1206smd	0.087x2
R8eq=R8+R8'	4.12ΜΩ	3.3M//4.7M+2.2M 1206 smd	0.087x2

Supplementary Information

1. Supplementary Figures:

Figure 1. Two sides of the headstage PCB.

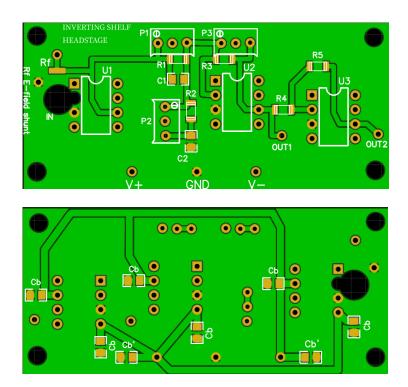


Figure 2. Two sides of the voltage-gain amplifier and 6-order pseudo-Bessel filter PCB.

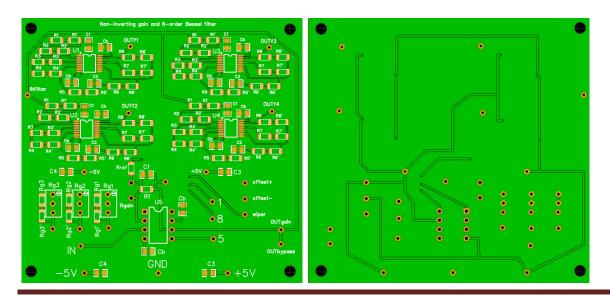
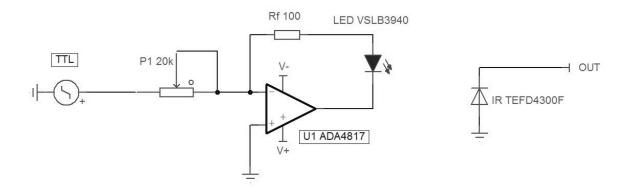


Figure 3. Electrical schematics of a current pulse generating optocoupler circuit. Light-emitting diode VSLB3940 is separated from infra-red receiver TEFD4300F by a metallic shield, in which small aperture was drilled, that is not shown.



2. Low-noise power supply

Figure 4. Electrical schema and actual implementation of the low-noise power source. Resistor R6 sets the output voltage (up to 24V DC) and R4 serves as a short-circuit protector by limiting the output current. Setting R4 to 50% of its value limits the output current to 250 mA that is more than sufficient for the amplifier functioning. Transistors T4 and T5 do not have to be fitted with heat-sinks, since current consumption is estimated to be maximum 150 mA. DCin+ and DCin- may be used to clean the ripple of the available DC power supply, in this case only R8, T5 and C2 are implicated. Note that the output capacitance multiplier circuit formed by R8, C2 and T5 has a time constant of 10 seconds so that it takes almost 1 minute for the output voltage to reach its adjusted value.

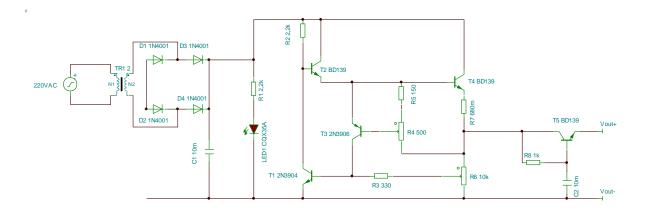




Table 1. Power supply components

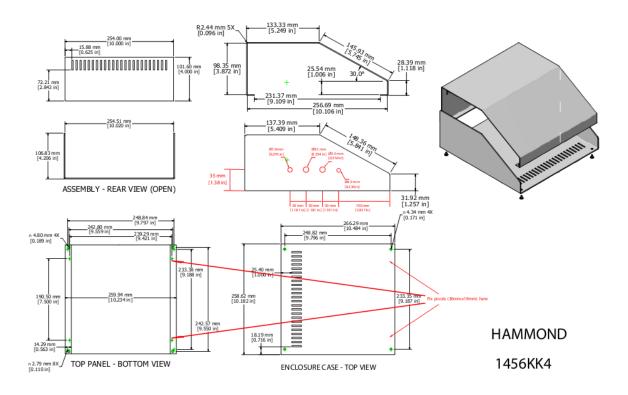
Component	Value	Implementation	Price, €
AC transformer	220in-24out	28TR8 8Watt transformer	~10
Diode bridge		RS201	0.20
C1=C2	10mF	25V, electrolytic	3.29x2
R1=R2	2.2 kΩ	0.25W, axial 0.3	0.10x2
LED1		CQX35A red LED	0.10
T2=T4=T5		BD139 NPN transistor	0.54x3
T1		2N3904 NPN transistor	0.40
T3		2N3906 PNP transistor	0.40
R3	330Ω	0.25W, axial 0.3	0.10
R4	250Ω	500 Ω 3296W potentiometer	2.10
R5	150Ω	0.25W, axial 0.3	0.68
R6	variable	10kΩ 3296W potentiometer	2.10
R7	0.68Ω	10W, wirewound cement filled ceramic	0.68
R8	1kΩ	0.25W, axial 0.3	0.10
Power switch		Two pole toggle switch	2.38
Connector x2		Panel mount « banana » female socket	0.49x2
AC Power cord			
Enclosure		Hammond 1411Q enclosure	~15
Total			~43

3. PCB soldering and cleaning

There are no particularly heat sensitive components in the amplifier, even suggested surface mount operational amplifiers withstand brief heating to 300 °C. We used SMD291AX soldering paste for SMD components and multicore welding wire (Sn63/Pb37) for other soldering. Soldering paste was applied by dot dispensing and we used fine soldering iron set to 250 °C maximum. Usually, only few seconds of heating are required to fix the components. After assembly, PCBs were soaked in isopropyl alcohol for 10 min, then extensively brushed using painting brush, rinsed again in clean isopropyl alcohol, wiped and dried.

4. Engineering details drawings of the enclosure cases.

The required modifications are shown in red.



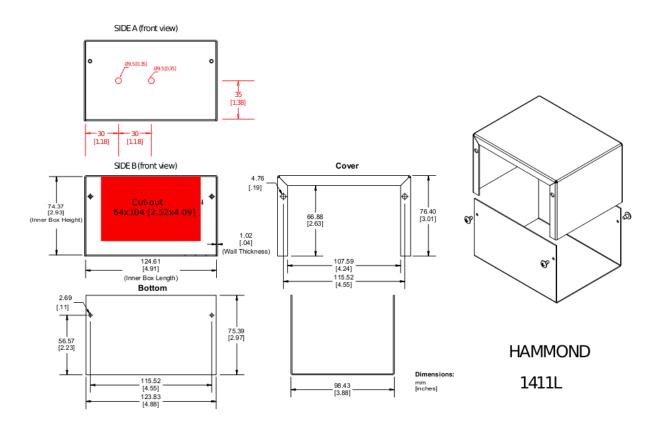


Table 1. Amplifiers bandwidths and noise

Resistive headstage AX OPAT CH 200B: pARMs noise with open input								Resistive head stage AX OPAT CH 200B : p A_{RMS} noise with 100 pF/10 $k\Omega$								
10	100 kHz 40 kHz 20 kHz 10 kHz 1 i		l kHz	0,1 kHz	100 kHz	40 kHz	20 kHz	10 kHz	l kHz	0,1 kHz						
	51.7	9.8	4.8	2.51	0.52	0.071	101	39.5	18.5	7.65	0.67	0.095				

T-NETWORK

R=1G;C=3pF;R=10k(variable);C=470nF

and any of the last announced the same																	
Amplif	ier components	T 10-90,	\mathbf{BW}		p	A _{RMS} n	oise wit	h open i	input			pA	_{RMS} noise	with 10	0 pF/10 l	Ω	
Opal	R _e	με	kHz	BP	100	40	20	10	1	0,1	BP	100	40	20	10	1	0,1
					kHz	kHz	kHz	kHz	kHz	kHz		kНz	kНz	kHz	kНz	kHz	kHz
LM6211	6k	62±1	5.6					3.28	0.77	0.095					3.71	1.05	0.135
		I		1										I			I

NON-INVERTING SHELVING FILTER WITH SNUBBER

R=1G:C=270fF:R=20k(variable):C=109 nF:R=1k

	fier comp		T ₁₀₋₉₀ ,	BW		pA _{PMS} 1	oise wit	hopen	input		pA _{DMS} noise with 100 pF/10 kΩ							
Opal	Opa2	R _e /R _{lim}	μз	kHz	BP 10	40	20	10 kHz	l kHz	0,1 kHz	BP	100 kHz	40 kHz	20 kHz	10 kHz	l kHz	0,1 kHz	
ADA4817	LT1028	13870/39	4.87±0.47	71.9	9.	3.0	1.61	0.90	0.16	0.051		150	58	19.9	7.46	0.39	0.063	
AD8067	LT1028	3815/46	4.76±0.66	73.5	9	16.5	7.75	3.35	0.27	0.065		246	80	26.9	11.12	0.46	0.072	
AD8033	LT1028	2860/39	4.40±0.50	79.5	84	5 10.5	4.24	1.75	0.17	0.055		270	100	29.6	10.91	0.45	0.069	
ADA4637	LT1028	3648/39	3.96±0.56	88.4	50	8.4	3.87	1.81	0.21	0.058		249	83	21.5	7.89	0.35	0.061	

NON-INVERTING SHELVING FILTER WITH EMBE DDE D GAIN
R=1G; Cr-270f; R=10k(variable); C=116nF; Rtm=500(variable); R=1k; field shunt applied

KFIG;C	N=1G;Cr-2/0f;R _c =10k(variable);C _c =110hr; R _{im} =300(variable); R _g =1k; Held shift applied																		
Ampl	lifier comp o	nents	T 10-90,	\mathbf{BW}		p.	A _{RMS} no	oise wi	th open:	inp ut		pA _{RMS} noise with 100 pF/10 kΩ							
Opal	Opa2	$R_{c}/R_{\rm lim}$	μз	kHz	BP	100	40	20	10	1	0,1	BP	100	40	20	10	1	0,1	
						kHz	kHz	kHz	kHz	kHz	kHz		kHz	kHz	kHz	kHz	kHz	kHz	
AD8067	OPA2227	3280/28	3.24±0.67	108	69	31	14.7	6.8	2.92	0.24	0.060	302	157	63.7	18.7	6.95	0.35	0.071	
AD8067	TL072CN	4058/38	4.50±0.67	78	63	28	12.6	6.1	2.42	0.21	0.059	160	110	55.7	18.1	6.95	0.35	0.071	

INVERTING SHELVING FILTER WITH SNUBBER

R_=1G;C_-270f; R_==R_=20k(variable); C_=116nF; C_{tim}=10 mu F, R_{tim}=500(variable); field shunt applied

Amp	lifier compo	nents	T ₁₀₋₉₀ ,	BW	1	A _{RMS} n	oise wi	th open	input			pA	_{RMS} nois	ewith 1	.00 pF/1	Ω 4 0	
Opal	Opa2	R _g =R _e /R _{lim}	με	kHz	BP	40 kHz	20 kHz	10 kHz	l kHz	0,1 kHz	BP		40 kHz	20 kHz	10 kHz	l kHz	0,1 kHz
AD8067	TLC070	3920/43	2.29±0.84	152	143	38.5	7.81	2.79	0.21	0.051	615		68	22.6	7.57	0.80	0.195
ADA4817	AD8067	9890/3.1	2.36±0.59	148	26.7	4.72	2.79	1.61	0.17	0.055	375		49.1	18.1	6.87	0.99	0.350
AD8067	ADA4622	3847/39	2.54±0.54	137							395		83	24.4	7.95	0.55	0.195
AD8067	LT1007	3802/41	3.35±0.33	104	92	30	7.41	2.58	0.20	0.051	365		61	20.0	7.11	0.65	0.147
AD8067	OPA227	3781/40	3.44±1.00	101	79	28	8.05	2.79	0.21	0.053	382		62	22.5	8.10	0.77	0.195
ADA4817	ADA4637	9240/7.9	3.58±0.55	98	12.1	2.95	1.59	0.95	0.14	0.049	187		44.3	16.5	6.05	0.31	0.059
ADA4817	LT1115	14481/17	4.04±0.92	86	12.7	4.50	1.74	0.89	0.16	0.051	350		57.5	21.5	7.55	0.75	0.151
ADA4817	ADA4625	14476/25	6.65±0.47	53	5.65	2.83	1.52	0.82	0.14	0.052	94		40.5	18.9	7.12	0.36	0.059
ADA4817	LT1007	12360/79	11.51±0.49	30	2.79	1.86	1.28	0.78	0.14	0.052	41.5		25.5	15.1	6.35	0.35	0.060