Gowin AHB to AXI Bridge IP

User Guide

IPUG1011-1.0E, 09/15/2022

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Revision History

Date	Version	Description
09/15/2022	1.0E	Initial version published.

Contents

List of Figures

List of Tables

1 About This Guide

1.1 Purpose

The purpose of Gowin AHB to AXI Bridge IP User Guide is to help you learn the features and usage of Gowin AHB to AXI Bridge IP by providing descriptions of the functions, ports, configuration and call.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find related documents at www.gowinsemi.com:

- DS100, GW1N series of FPGA Products Data Sheet
- DS117, GW1NR series of FPGA Products Data Sheet
- DS821, GW1NS series of FPGA Products Data Sheet
- DS861, GW1NSR series of FPGA Products Data Sheet
- DS871, GW1NSE series of SecureFPGA Products Data Sheet
- DS881, GW1NSER series of SecureFPGA Products Data Sheet
- DS891, GW1NRF series of Bluetooth FPGA Products Data Sheet
- DS841, GW1NZ series of FPGA Products Data Sheet
- DS102, GW2A series of FPGA Products Data Sheet
- DS226, GW2AR series of FPGA Products Data Sheet
- DS961, GW2ANR series of FPGA Products Data Sheet
- DS976, GW2AN-55 Data Sheet
- DS971, GW2AN-9X & 18X Data Sheet
- SUG100, Gowin Software User Guide

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
IP	Intellectual Property
AMBA	Advanced Microcontroller Bus Architecture
AHB	Advanced High Performance Bus
AHB-Lite	Advanced High Performance Bus-Lite
AXI4	Advanced eXtensible Interface 4
AXI4-Lite	Advanced eXtensible Interface 4-Lite

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

2.1 Introduction to Gowin AHB to AXI Bridge IP

Gowin AHB to AXI Bridge IP can bridge AHB-Lite bus with AXI4/AXI4-Lite bus.

Table 2-1 Gowin AHB to AXI Bridge IP Overview

Gowin AHB to AXI Bridge IP	
IP Core Application	
Devices Supported	● GW1N series ● GW1NR series ● GW1NS series ● GW1NSR series ● GW1NSE series ● GW1NSER series ● GW1NRF series ● GW1NZ series ● GW2A series ● GW2AR series ● GW2ANR series ● GW2AN series
Delivered Doc.	
Design Files	Verilog (encrypted)
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.8.07 and above)

2.2 Features

- AHB-Lite bus supports standard 32 bits data width and it can only be used as a slave.
- AXI4/AXI4-Lite bus supports standard 32 bits data width and can only be used as a master.
- Support single-transmission and burst-transmission operations in the AHB-Lite to AXI4 bridge conversion.
- Only support single-transmission operation in the AHB-Lite to AXI4-Lite bridge conversion.

3 Functional Description

Gowin AHB to AXI Bridge IP can bridge AHB-Lite bus with AXI4/AXI4-Lite bus, which enables communication between a master device with AHB-Lite bus and a slave device with AXI4/AXI4-Lite bus. In this IP, AHB-Lite port conforms to the AMBA 3 specification, and AXI4/AXI4-Lite port conforms to the AMBA 4 specification.

For example, when using Gowin EMPU M1 soft-core system as a master device with an AHB-Lite bus, Gowin AHB to AXI Bridge IP can enable it to communicate with a slave peripheral module with a standard AXI4-Lite bus interface.

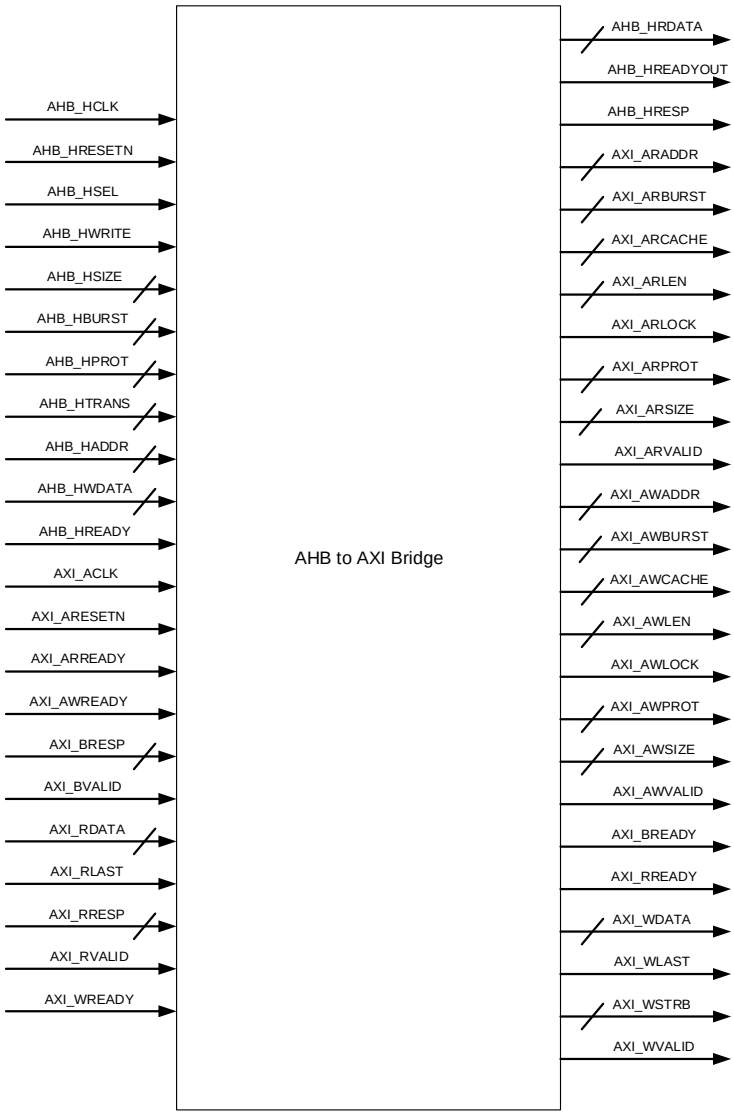
Note!

The data width of this IP interface is fixed at 32 bits.

4 Port Description

The ports of Gowin AHB to AXI Bridge IP are as shown in Figure 4-1.

Figure 4-1 Gowin AHB to AXI Bridge IP Port Diagram



The details of Gowin AHB to AXI Bridge IP I/O ports are shown in Table 4-1.

Table 4-1 Gowin AHB to AXI Bridge IP Port List

Name	I/O	Data Width	Description
AHB-Lite Slave Interface			
AHB_HCLK	Input	1	System Clock
AHB_HRESETN	Input	1	Reset signal, active-low.
AHB_HSEL	Input	1	Slave strobe signal, active-high.
AHB_HWRITE	Input	1	Read and write signal; high: write; low: read.
AHB_HSIZE	Input	3	The size of the transmission data, typically in bytes (8 bits), halfwords (16 bits), and words (32 bits).
AHB_HBURST	Input	3	Burst transmission type, such as 1/4/8/16 bursts.
AHB_HPROT	Input	4	Protect control signal, providing additional information for bus access.
AHB_HTRANS	Input	2	Indicates transmission type, such as continuous, discontinuous, idle or busy.
AHB_HADDR	Input	32	32-bit address bus
AHB_HWDATA	Input	32	32-bit write data bus
AHB_HREADY	Input	1	When the signal is high, it indicates that the transmission on the bus is completed.
AHB_HRDATA	Output	32	32-bit read data bus
AHB_HREADYOUT	Output	1	When the signal is high, it indicates that the transmission on the bus is completed
AHB_HRESP	Output	1	Transmission response signal; high: error; low: okay.
AXI4/AXI4 Lite Master Interface			
AXI_ACLK	Input	1	System Clock
AXI_ARESETN	Input	1	Reset signal, active-low.
AXI_ARREADY	Input	1	Read address ready from slave to master, indicating that the slave can receive address and corresponding control signal.
AXI_AWREADY	Input	1	Write address ready from slave to master, indicating that the slave can receive address and corresponding control signal.
AXI_BRESP	Input	2	Write response from slave to master, indicating write transmission status.
AXI_BVALID	Input	1	Write response valid from slave to master
AXI_RDATA	Input	32	32-bit read data bus from slave to master

Name	I/O	Data Width	Description
AXI_RLAST	Input	1	Indicates that this transmission is the last of the burst read operation from slave to master.
AXI_RRESP	Input	2	Read response from slave to master, indicating read transmission status.
AXI_RVALID	Input	1	Read valid from slave to master
AXI_WREADY	Input	1	Write ready from slave to master, indicating that the slave can receive write data.
AXI_ARADDR	Output	32	32-bit read address bus from master to slave, providing the read start address of one read burst transmission.
AXI_ARBURST	Output	2	Read operation burst type from master to slave
AXI_ARCACHE	Output	4	Read operation storage type
AXI_ARLEN	Output	8	Read operation burst length from master to slave
AXI_ARLOCK	Output	1	Read operation bus access type; 0: normal; 1: exclusive access.
AXI_ARPROT	Output	3	Read operation protect type
AXI_ARSIZE	Output	3	Read burst size from master to slave, providing the number of bytes per burst transmission.
AXI_ARVALID	Output	1	Read address valid signal from master to slave, indicating that the read address and control signal in this channel are valid.
AXI_AWADDR	Output	32	32-bit write address bus from master to slave, providing the write start address of one write burst transmission.
AXI_AWBURST	Output	2	Write operation burst type from master to slave
AXI_AWCACHE	Output	4	Write operation storage type
AXI_AWLEN	Output	8	Write operation burst length from master to slave
AXI_AWLOCK	Output	1	Write operation bus access type; 0: normal; 1: exclusive access.
AXI_AWPROT	Output	3	Write operation protect type
AXI_AWSIZE	Output	3	Write burst size from master to slave, providing the number of bytes per burst transmission.
AXI_AWVALID	Output	1	Write address valid signal from master to slave, indicating that the Write address and control signal in this channel are valid.
AXI_BREADY	Output	1	Response ready from slave to master, indicating that master can receive write response.
AXI_RREADY	Output	1	Read ready from slave to master, indicating that the master can receive data sent by slave.

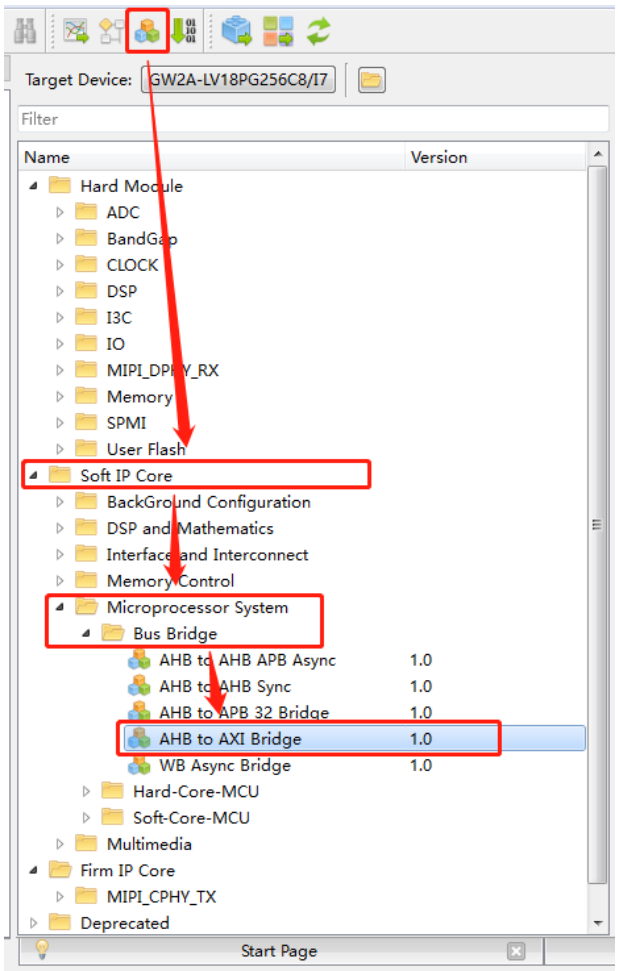
Name	I/O	Data Width	Description
AXI_WLAST	Output	1	Indicates that this transmission is the last of the burst write operation from master to slave.
AXI_WSTRB	Output	4	Write selection number, from host to slave, WSTRB can be any value when WVALID is low, and WSTRB indicates the valid data segment currently transmitted in 8 bits when WVALID is high.
AXI_WVALID	Output	1	Write valid from master to slave, indicating that the write data and strobe signal are valid.

5 Call and Configure

5.1 Call Gowin AHB to AXI Bridge IP

Select "Tools > IP Core Generator > Soft IP Core > Microprocessor System > Bus Bridge > AHB to AXI Bridge" on the interface of Gowin Software to call Gowin AHB to AXI Bridge IP, as shown in Figure 5-1.

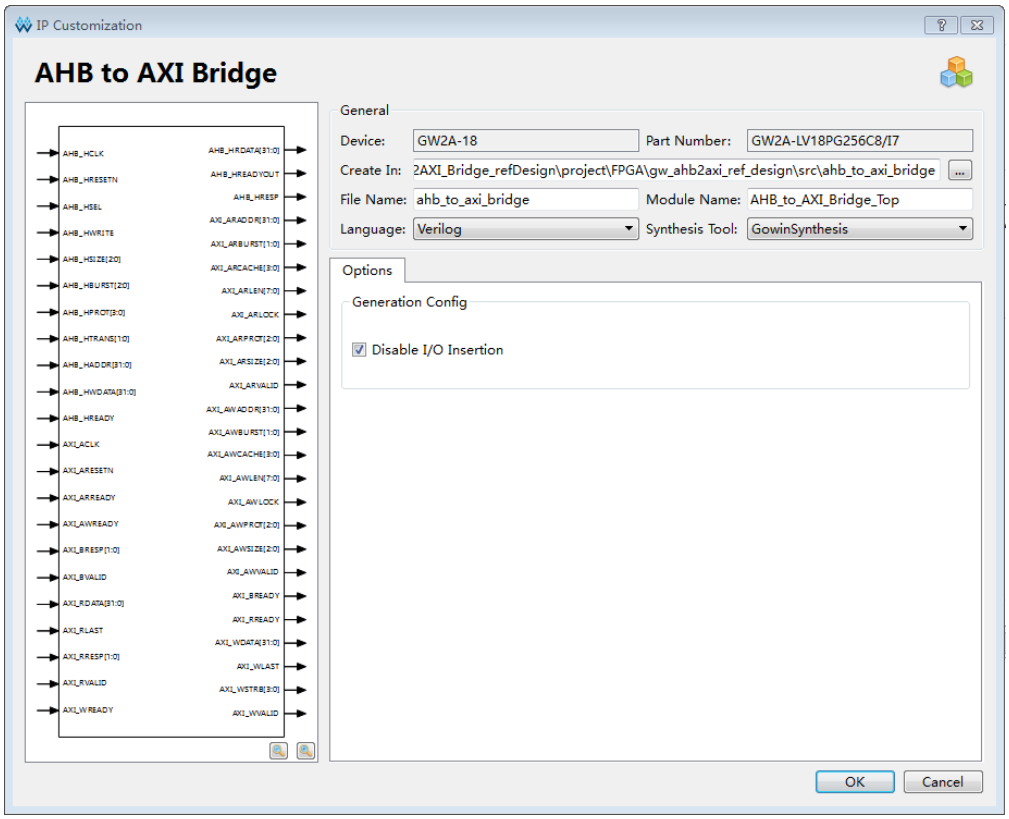
Figure 5-1 Call Gowin AHB to AXI Bridge IP



5.2 Configure Gowin AHB to AXI Bridge IP

The configuration interface of Gowin AHB to AXI Bridge IP is as shown in Figure 5-2.

Figure 5-2 Gowin AHB to AXI Bridge IP Configuration Interface



- Click "Create In" to specify the path of the generated file.
- Click "File Name" to configure the generated file name.
- Click "Module Name" to configure the generated top module name.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