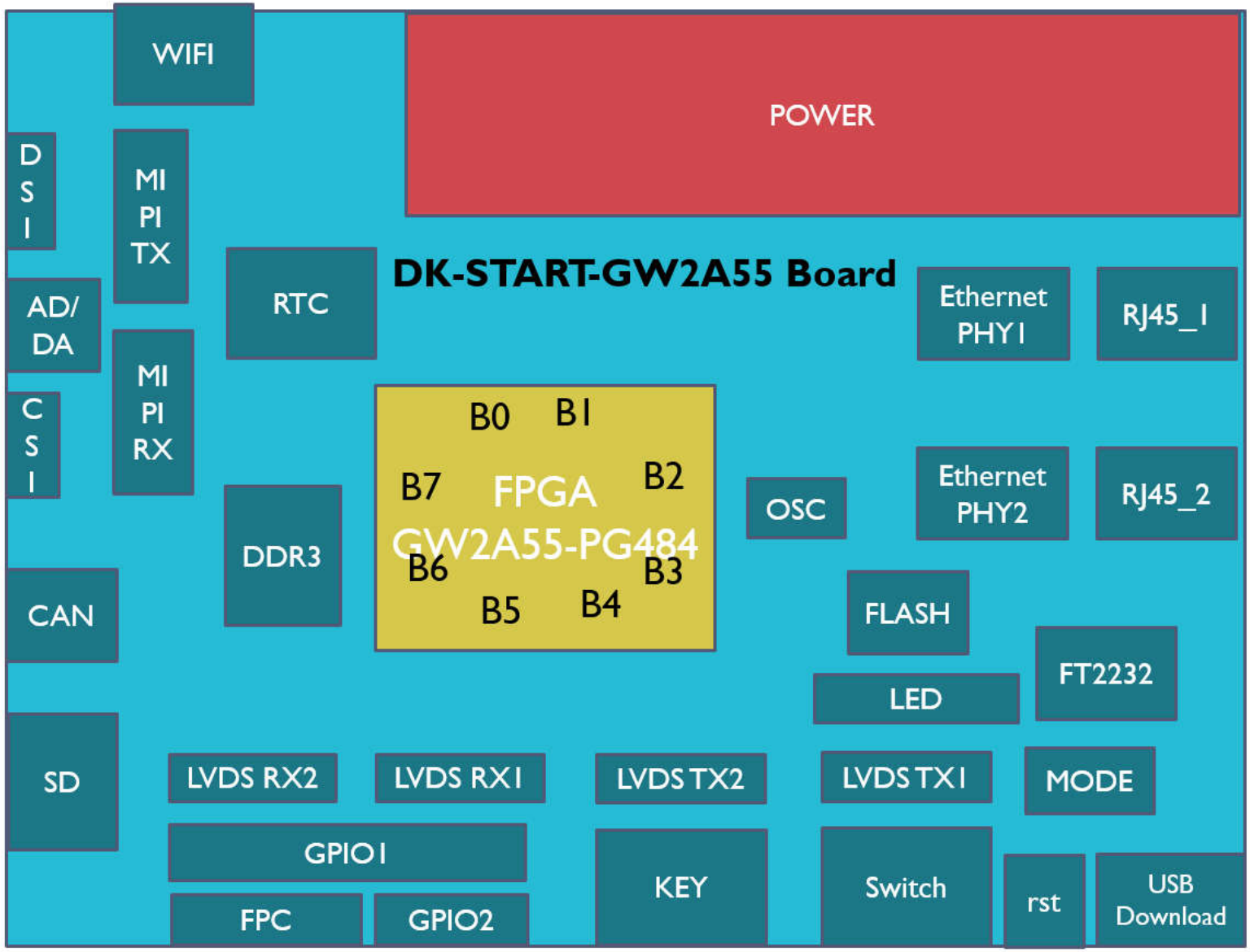

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Size A3	Document Number Block Diagram	Rev V1.3
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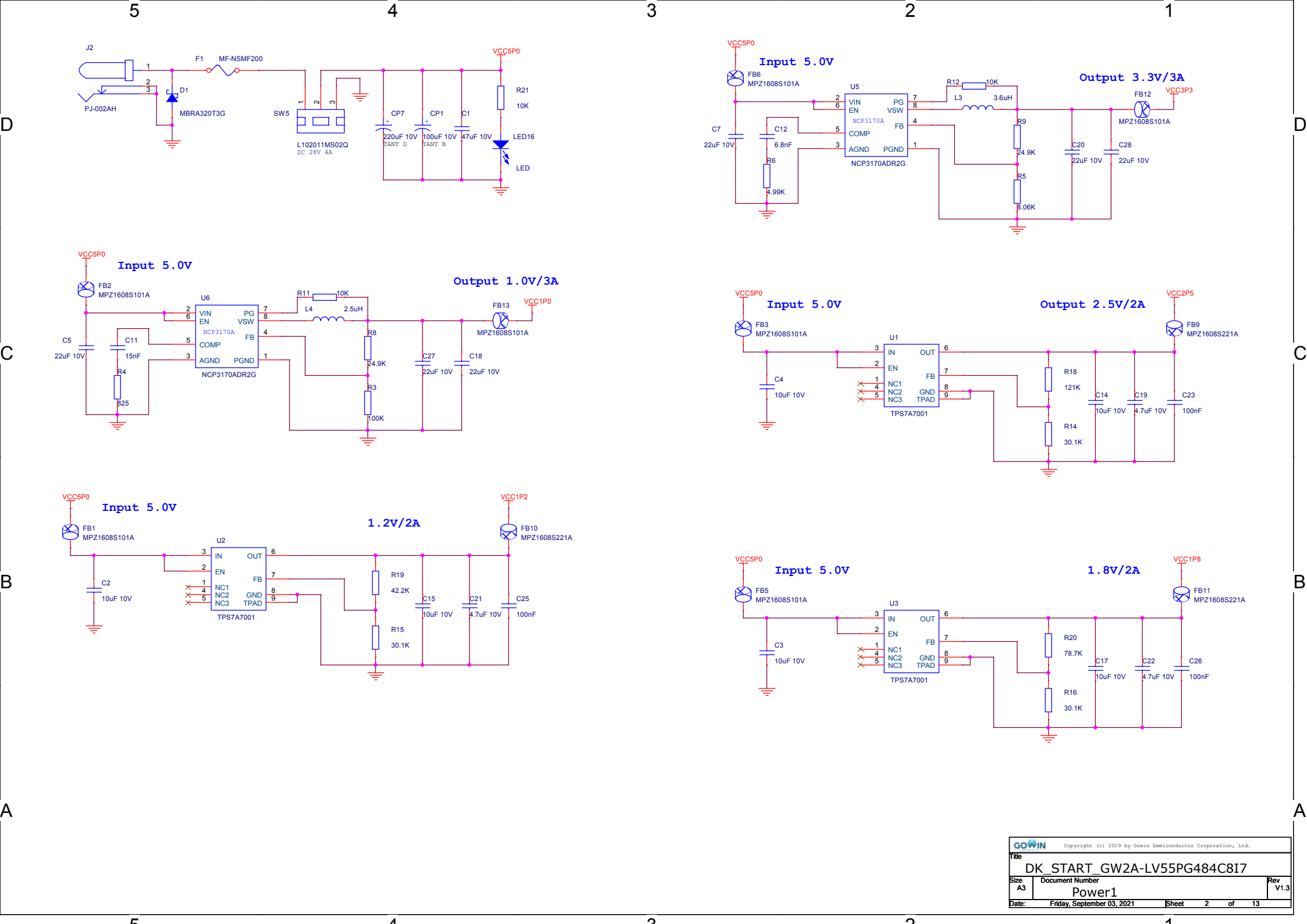

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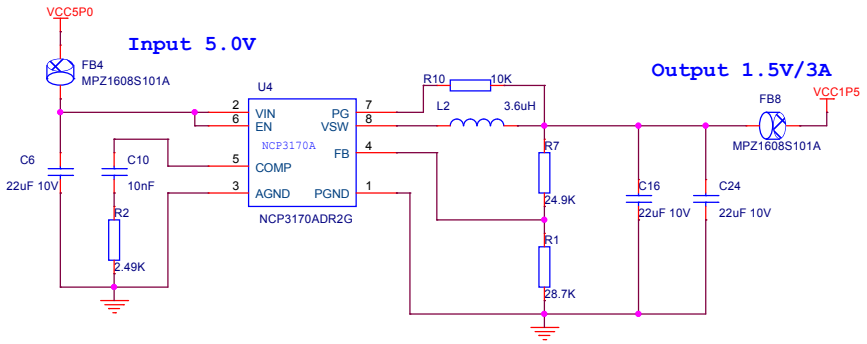
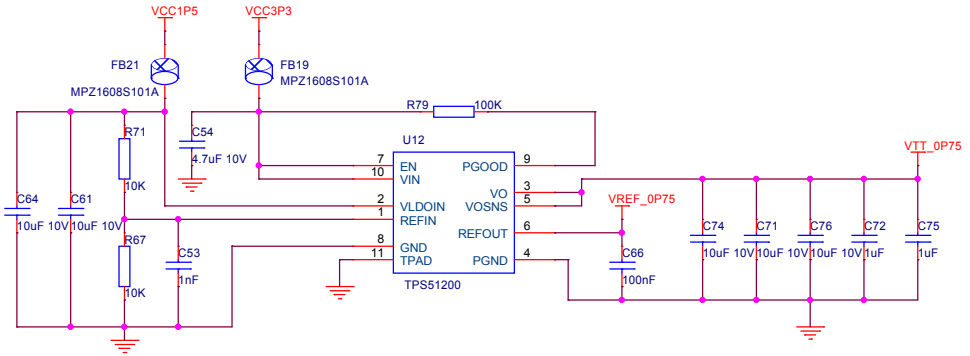
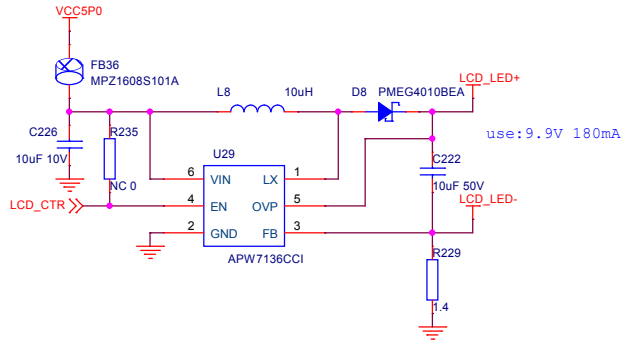
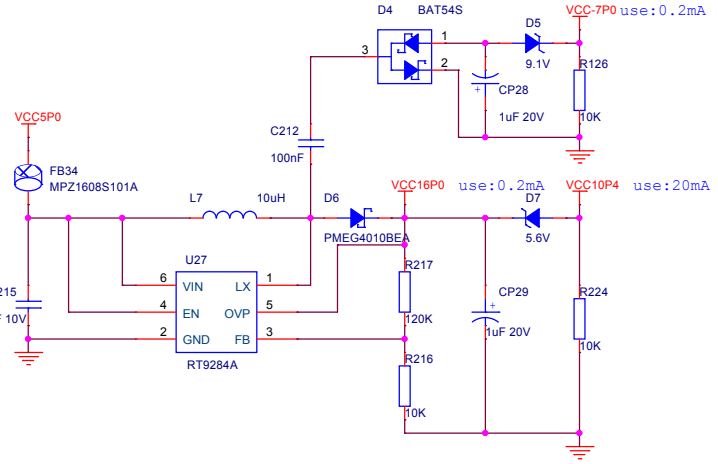
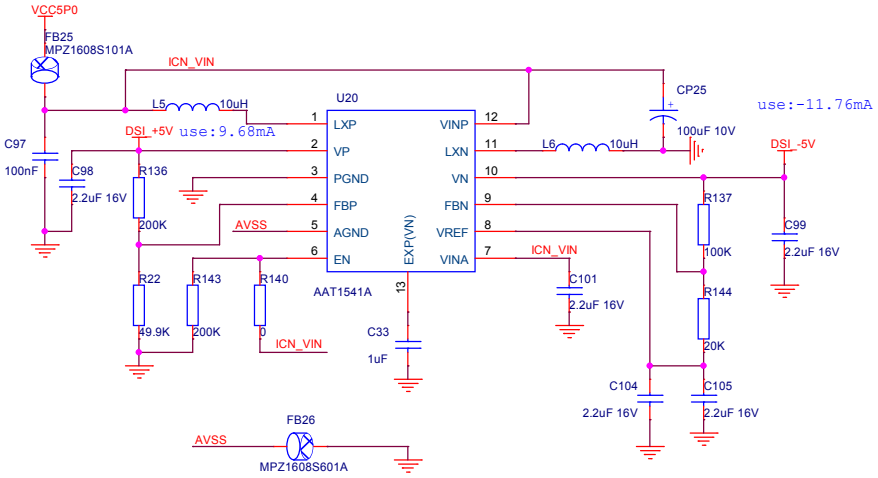
Size A3	Document Number Power1	Rev V1.3
Date: Friday, September 03, 2021	Sheet 2 of 13	

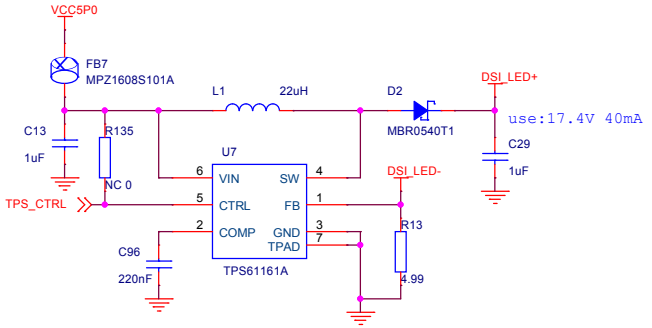












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Title: DK_START_GW2A-LV55PG484C8I7

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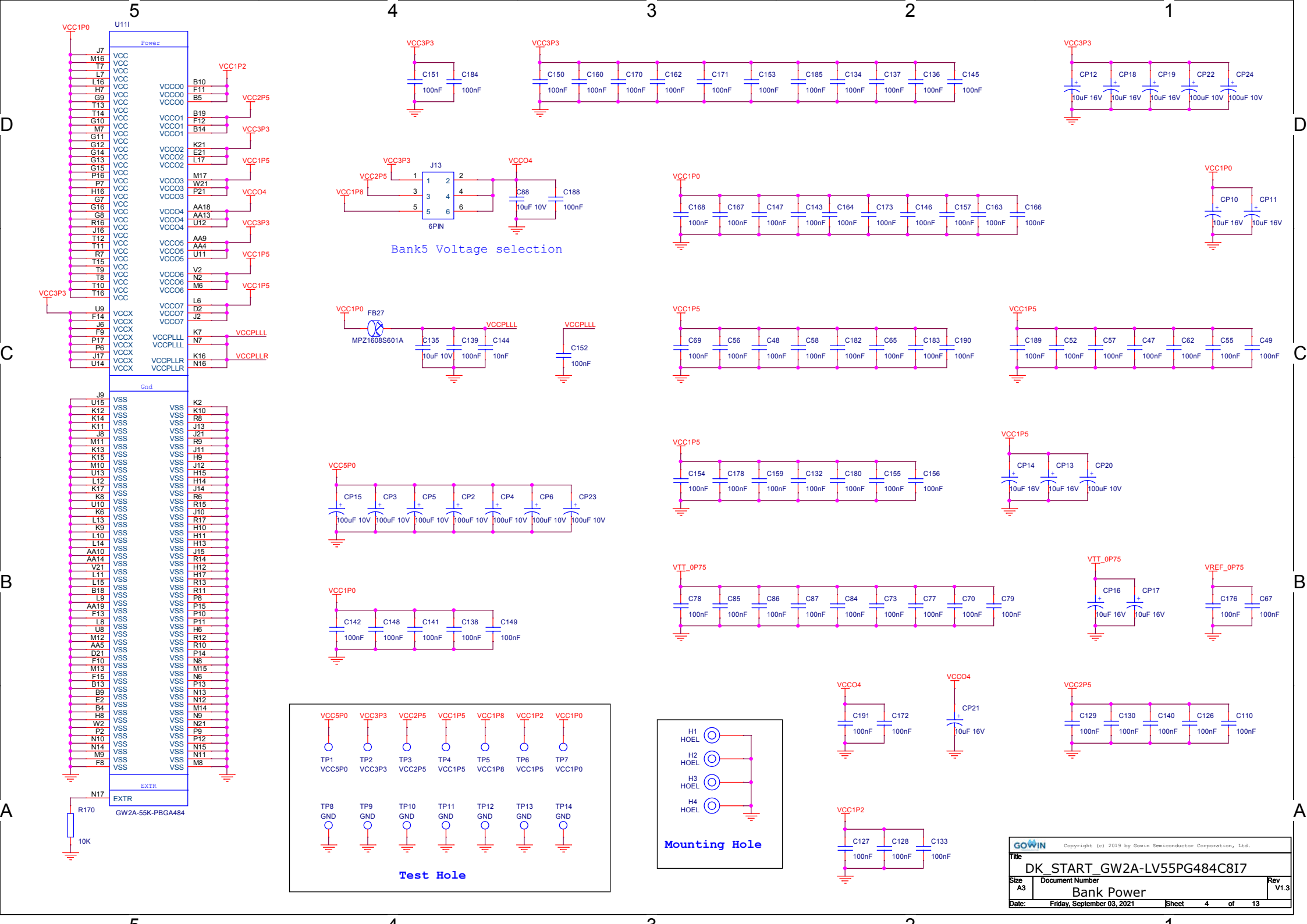
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Gnd
EXTR
GW2A-55K-PBGA484
R170
10K
Bank5 Voltage selection
J13
6PIN
FB27
MPZ1608S601A
Test Hole
TP1 VCC5P0
TP2 VCC3P3
TP3 VCC2P5
TP4 VCC1P5
TP5 VCC1P8
TP6 VCC1P5
TP7 VCC1P0
TP8 GND
TP9 GND
TP10 GND
TP11 GND
TP12 GND
TP13 GND
TP14 GND
Mounting Hole
H1 HOEL
H2 HOEL
H3 HOEL
H4 HOEL
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Title
DK_START_GW2A-LV55PG484C8I7
Size A3
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Bank Power
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Date: Friday, September 03, 2021
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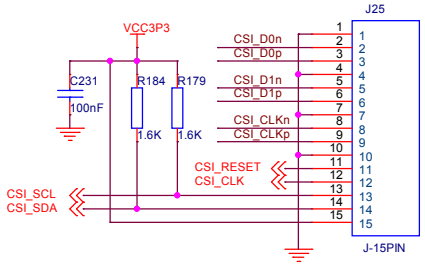
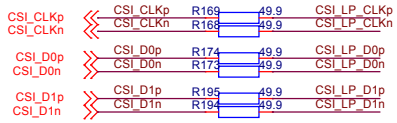
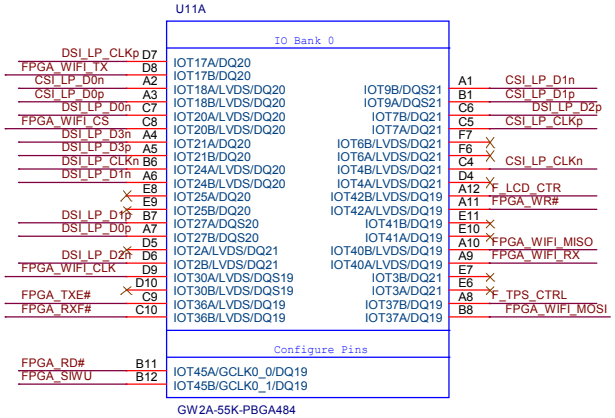
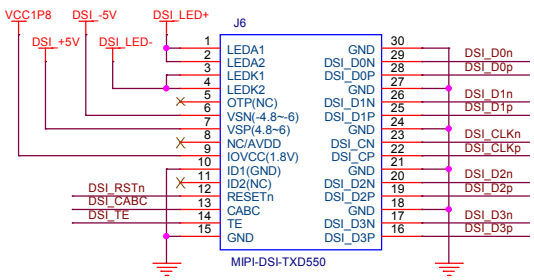


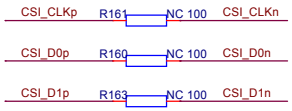
The end resistance is close to the FPGA

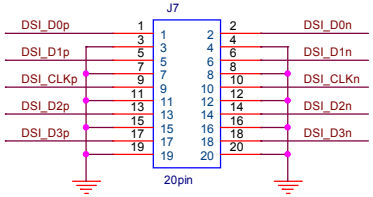


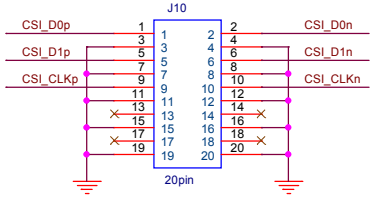


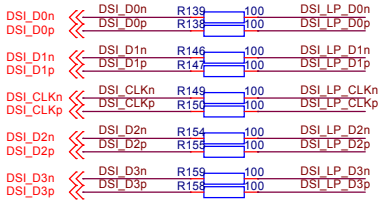


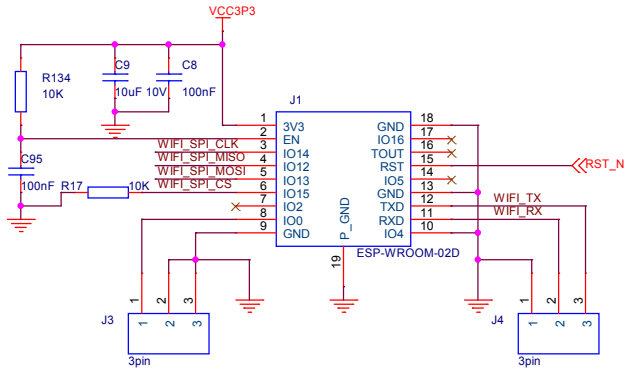
The end resistance is close to the FPGA

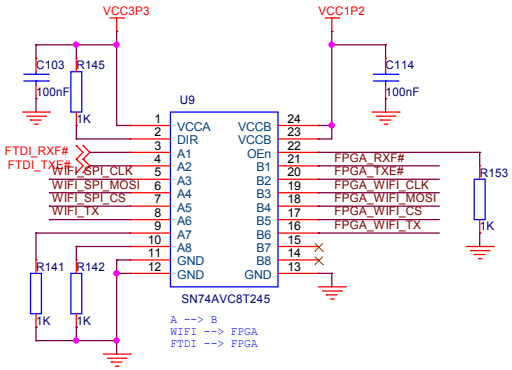


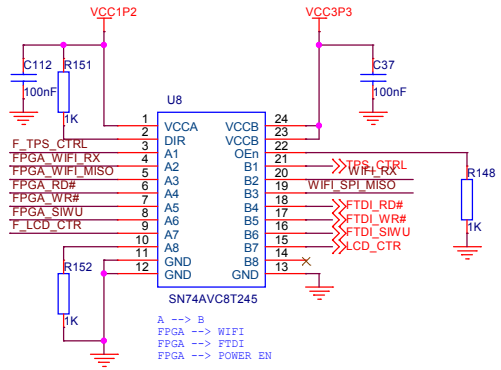












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Size: A3 | Document Number: B0_MIPI-LP_WIFI | Rev: V1.3

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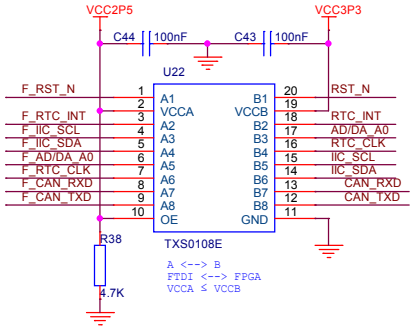

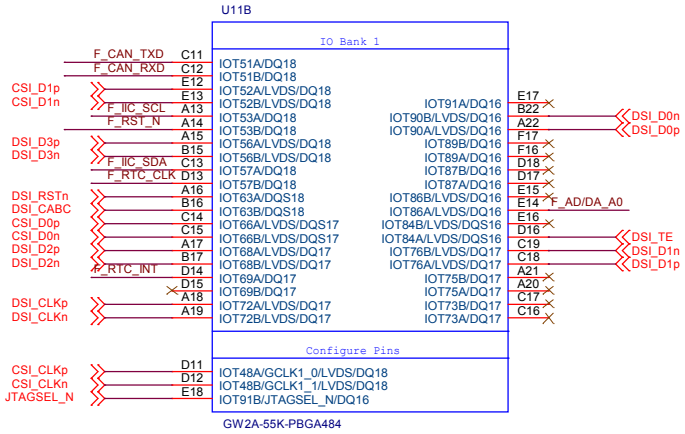

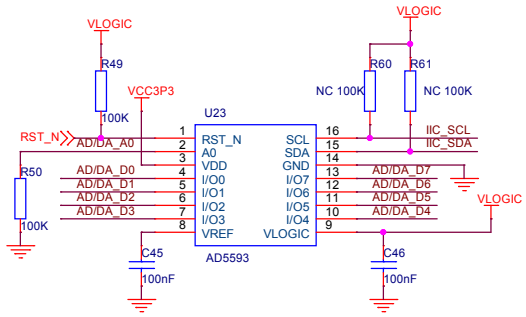

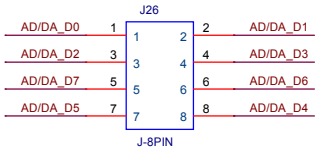

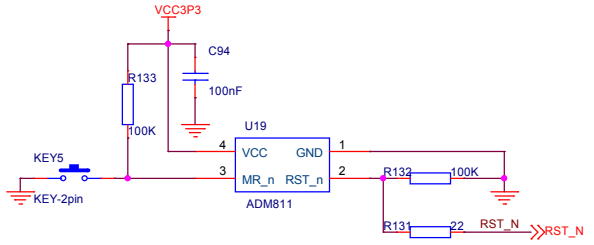

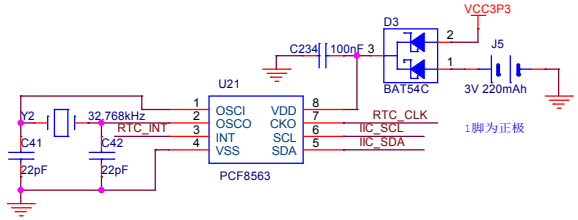

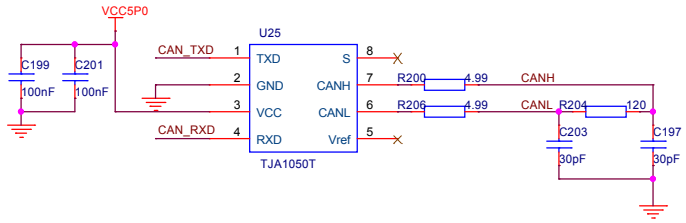

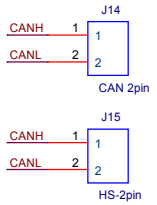

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DK_START_GW2A-LV55PG484C8I7

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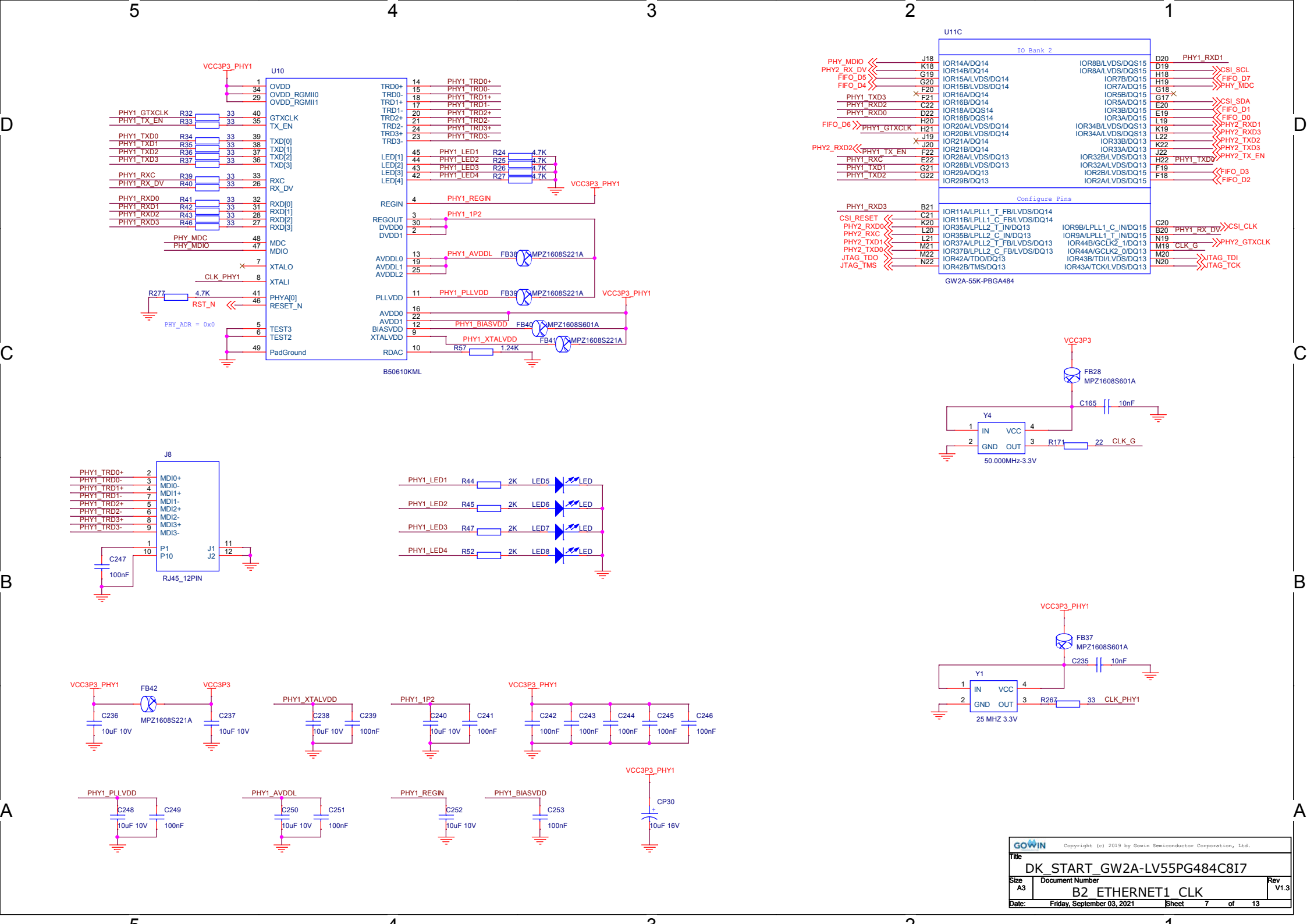
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Y4
50.000MHz-3.3V
Y1
25 MHZ 3.3V
PHY_ADR = 0x0
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Title
DK_START_GW2A-LV55PG484C8I7
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B2_ETHERNET1_CLK
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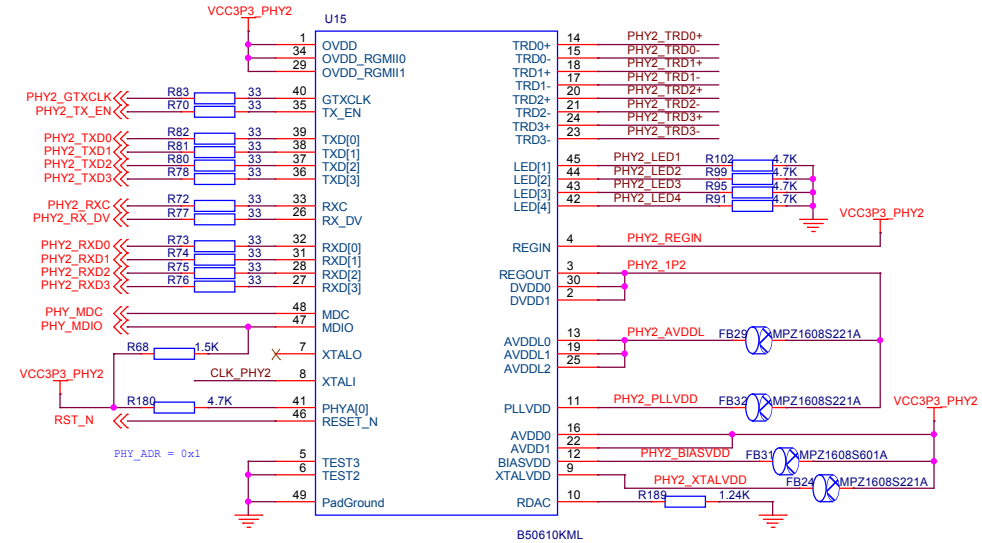

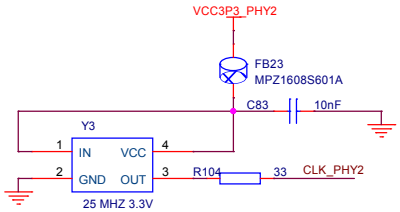

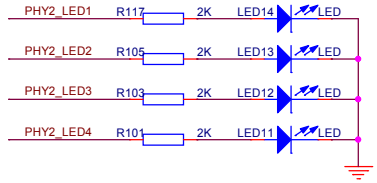

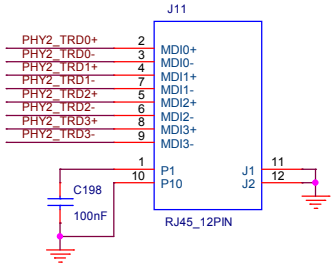

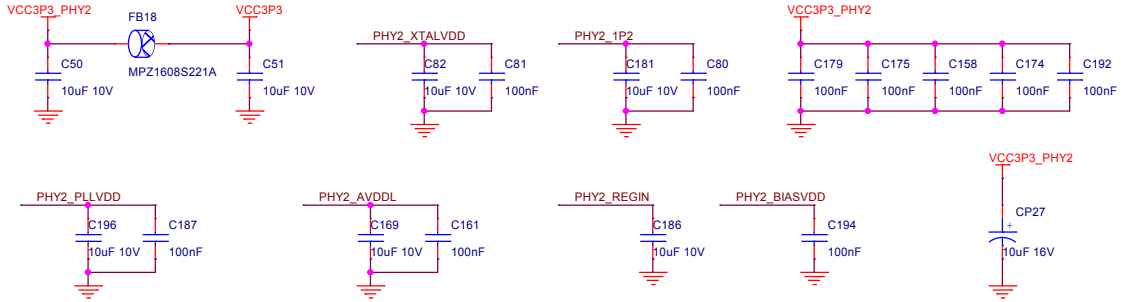

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Size A3	Document Number ETHERNET2	Rev V1.3
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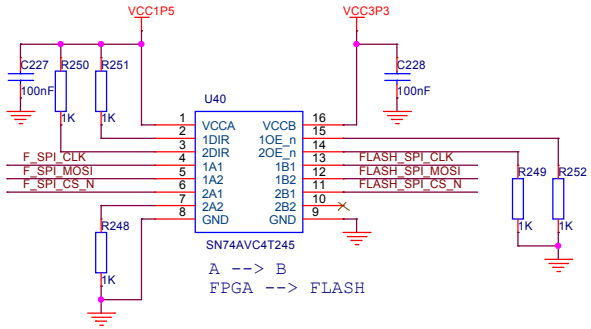
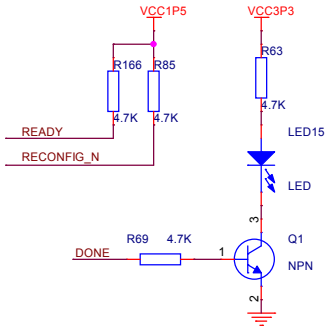
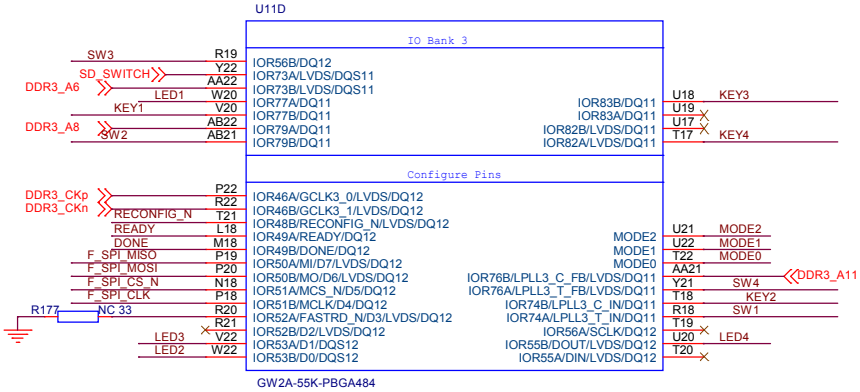
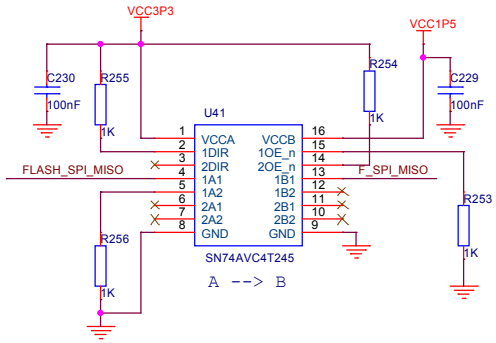
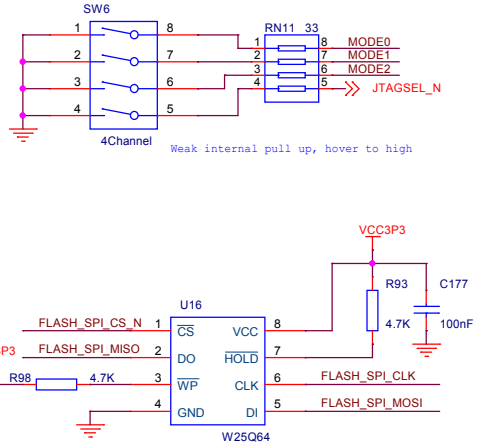


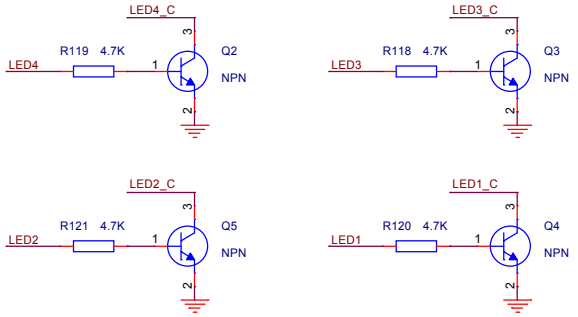
When DIR is raised, connect to VCCA

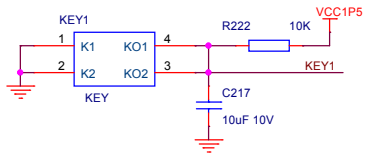


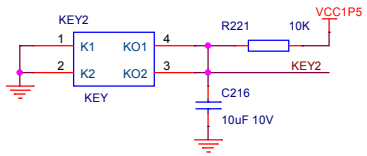


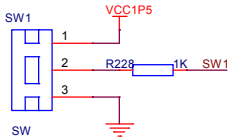


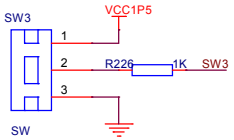


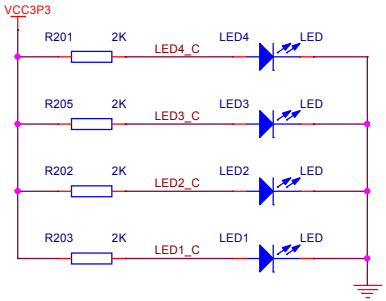


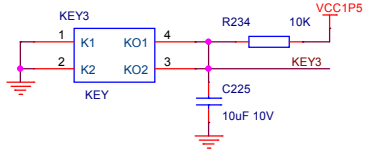


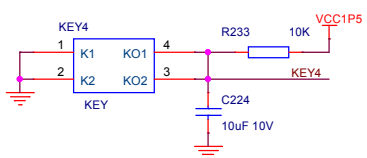


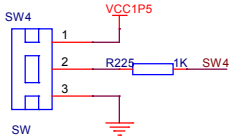


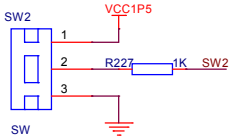












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Title	DK_START_GW2A-LV55PG484C8I7	
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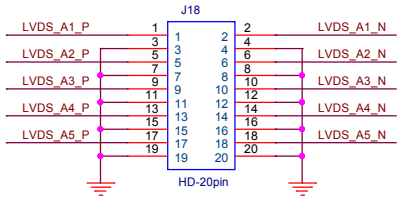

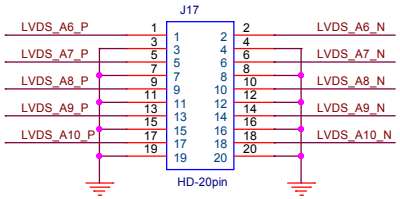

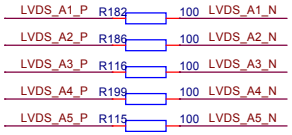

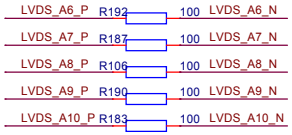

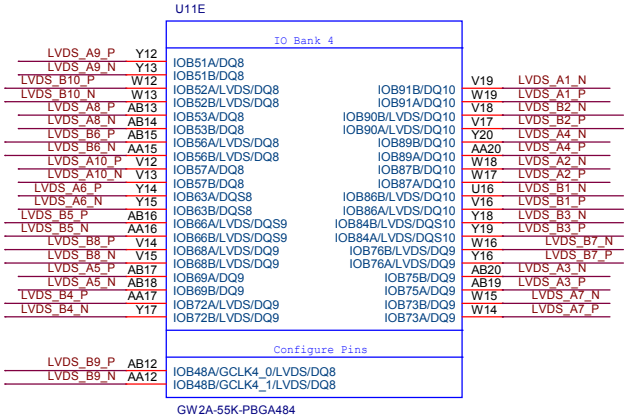

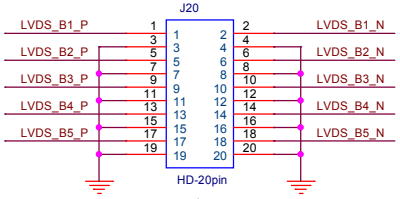

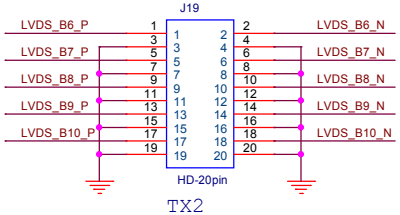

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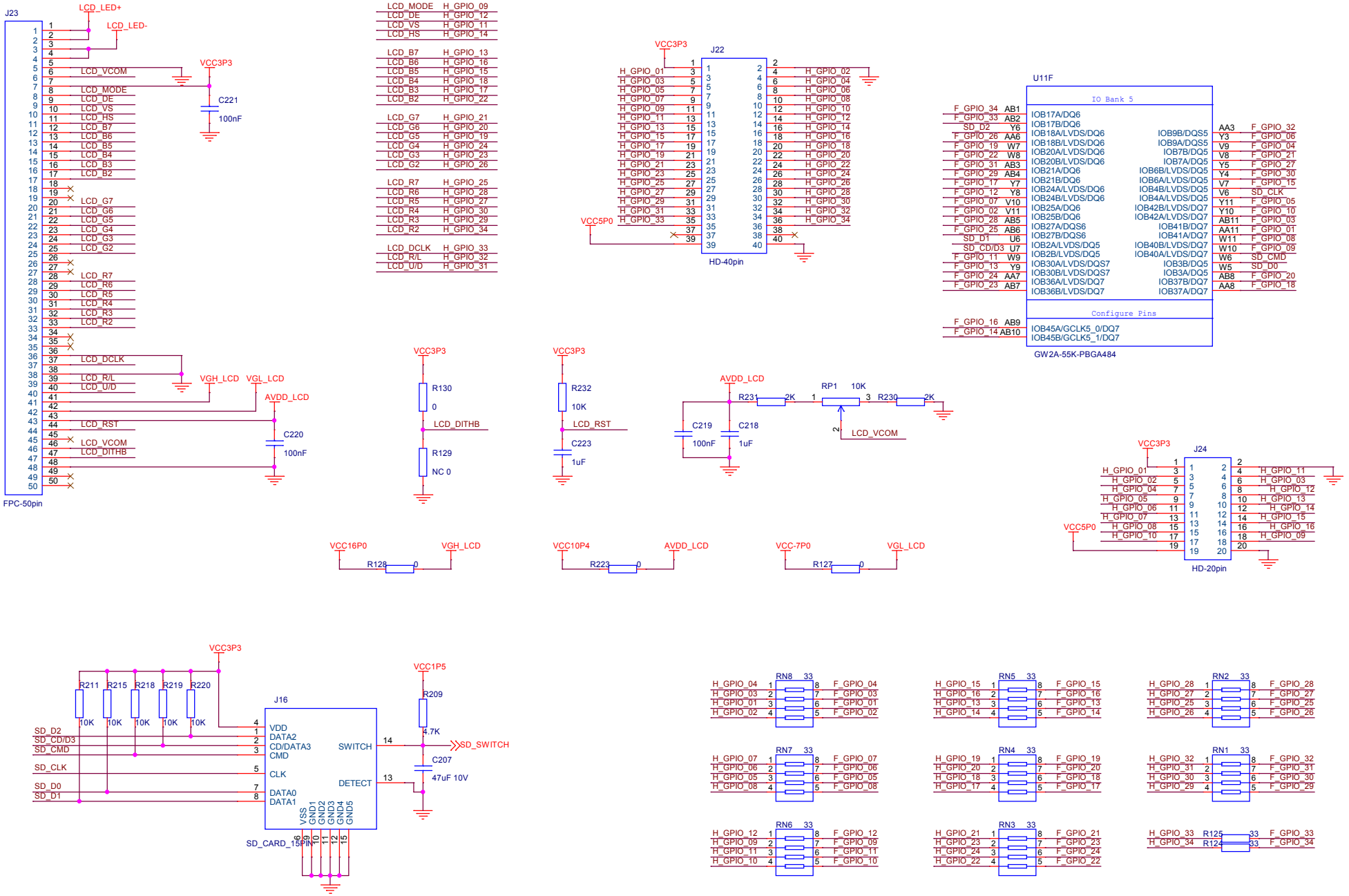

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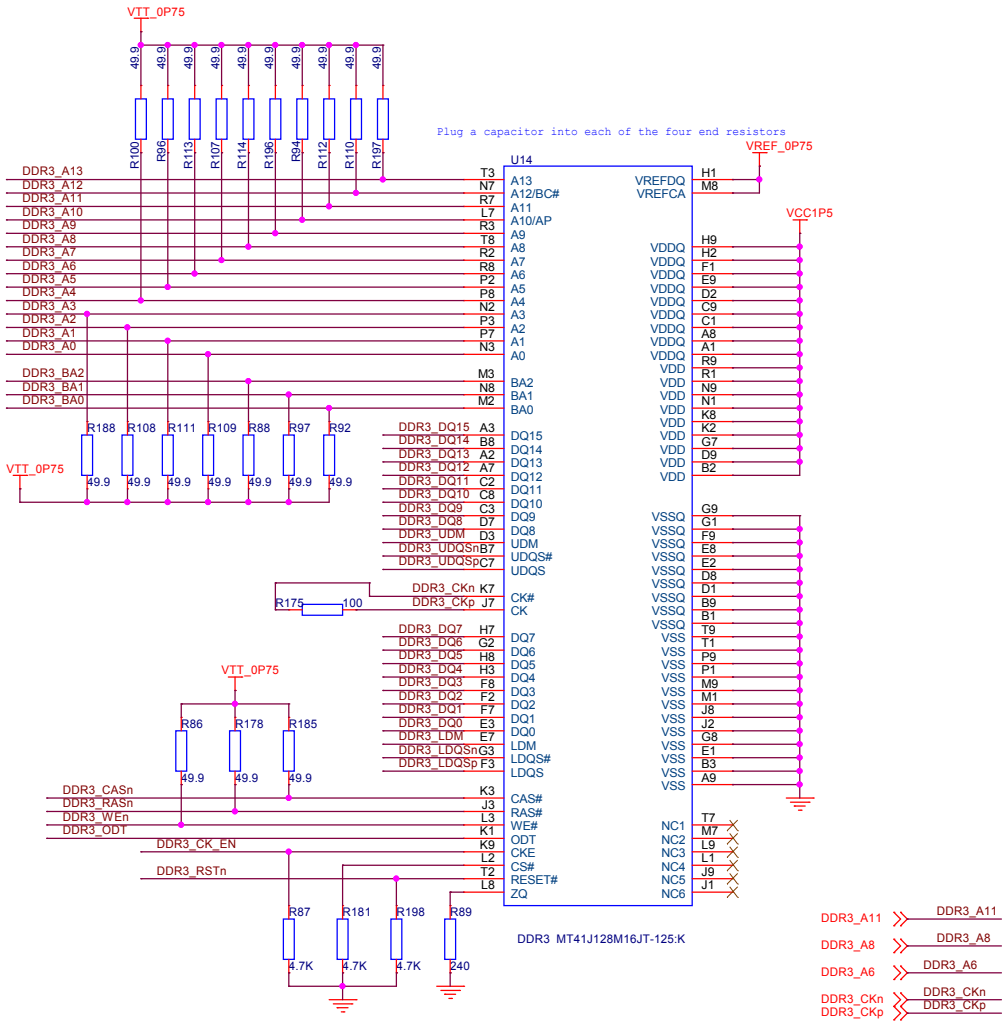
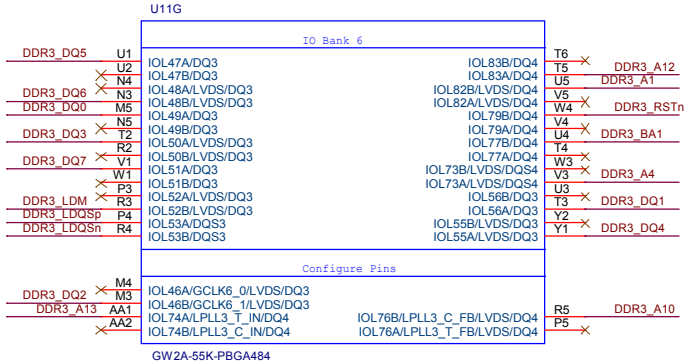
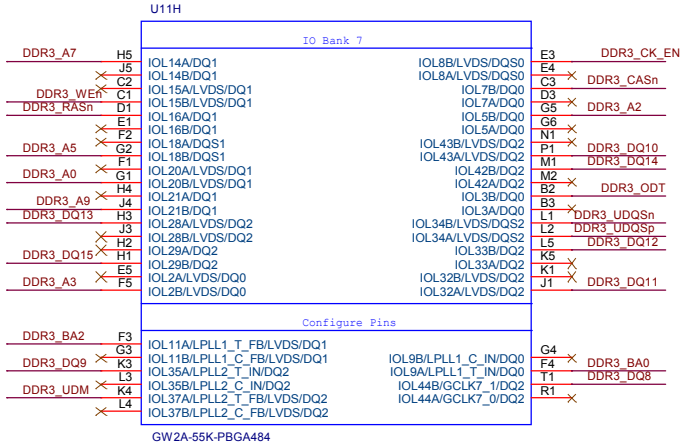




DQ[7:0]、LDQSn、LDQSp&LDM is placed on the DQ3 cluster of Bank6

DQ15:8]、UDQSn、UDQSp&UDM is placed on the DQ2 cluster of Bank7



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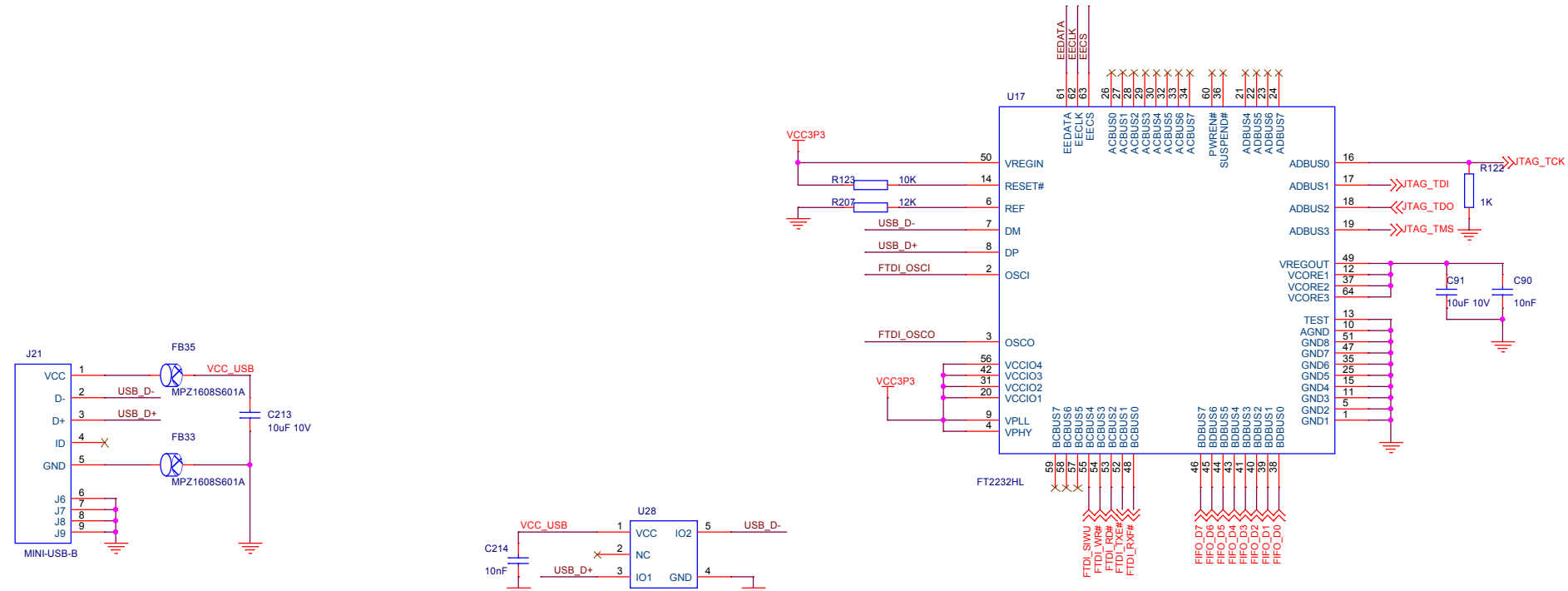

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