Gowin LVDS 7to1 TX RX IP

User Guide

IPUG771-1.0E, 02/26/2021

Disclaimer

Revision History

Date	Version	Description
02/26/2021	1.0E	Initial version published.

Contents

List of Figures

List of Tables

1 About This Guide

1.1 Purpose

The purpose of Gowin LVDS 7to1 TX RX IP is to help you learn the features and usage of Gowin LVDS 7to1 TX RX IP by providing the descriptions of features, functions, ports, timing, GUI and reference design, etc.

1.2 Related Documents

You can find the related documents at www.gowinsemi.com:

- DS100, GW1N series of FPGA Products Data Sheet
- DS117, GW1NR series of FPGA Products Data Sheet
- DS821, GW1NS series of FPGA Products Data Sheet
- DS861, GW1NSR series of FPGA Products Data Sheet
- DS871, GW1NSE series of FPGA Products Data Sheet
- DS881, GW1NSER series of FPGA Products Data Sheet
- DS891, GW1NRF series of FPGA Products Data Sheet
- DS841, GW1NZ series of FPGA Products Data Sheet
- DS102,GW2A series of FPGA Products Data Sheet
- DS226, GW2AR series of FPGA Products Data Sheet
- DS961, GW2ANR series of FPGA Products Data Sheet
- DS976, GW2A-55 Data Sheet
- SUG100, Gowin Software User Guide

1.3 Terminology and Abbreviations

Table 1-1 shows the abbreviations and terminology used in this manual.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
FPGA	Field Programmable Gate Array
LVDS	Low-Voltage Differential Signaling
VESA	Video Electronics Standards Association
JEIDA	Japan Electronic Industry Development Association
VS	Vertical Sync
HS	Horizontal Sync
DE	Data Enable
IP	Intellectual Property

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

2.1 Overview

LVDS 7:1 video interface is mainly used in LCD panel driver products. The LVDS 7to1 TX IP is used to receive parallel video signals and then convert them to LVDS signals for output. LVDS 7to1 RX IP is used to receive LVDS signals and then convert them into parallel video signals.

Table 2-1 Gowin LVDS 7to1 TX RX IP

Gowin LVDS 7to1 TX RX IP	
Logic Resource	Please refer to Table 2-2 and Table 2-3.
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software

2.2 Features

- Supports VESA and JEIDA standards.
- Supports RGB888 and RGB666.
- Supports one channel, two channels and 4 lanes/channels.
- The data rate of single lane supports 80Mb/s~700Mb/s.

2.3 Resource Utilization

Gowin 7to1 DVI 7to1 TX RX can be implemented by Verilog. Its performance and resource utilization may vary when the design is employed in different devices, or at different densities, speeds, or grades. Take GW1N-4 as an instance, and the resource utilization is as shown in Table 2-2 and Table 2-3.

Table 2-2 LVDS 7to1 TX Resource Utilization

Device Series	Speed Grade	Name	Resource Utilization	Remarks
GW1N-4	-6	-LUT	1	Configure internal PLL, RGB888, and One Channel.
		REG	0	
		PLL	1	
		OVIDEO	5	

Table 2-3 LVDS 7to1 RX Resource Utilization

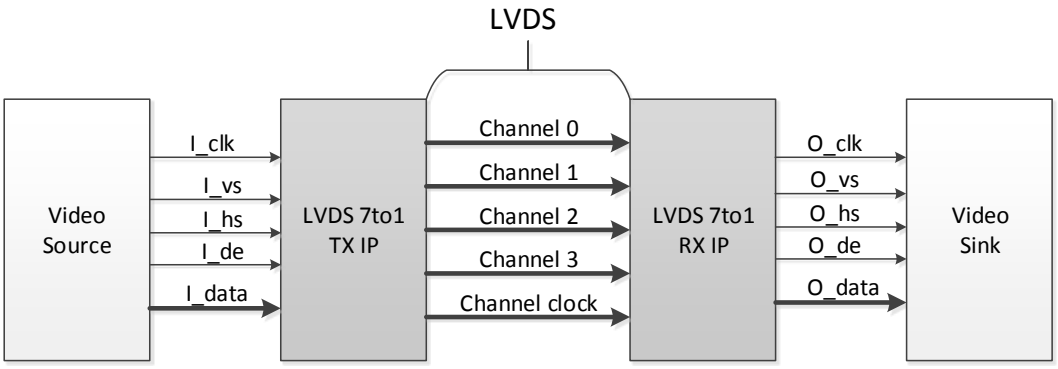
Device Series	Speed Grade	Name	Resource Utilization	Remarks
GW1N-4	-6	LUT	245	Configure internal PLL, Auto Phase, RGB888, and One Channel.
		REG	130	
		PLL	1	
		CLKDIV	1	
		IODELAY	4	
		IVIDEO	5	

3 Functional Description

3.1 System Block Diagram

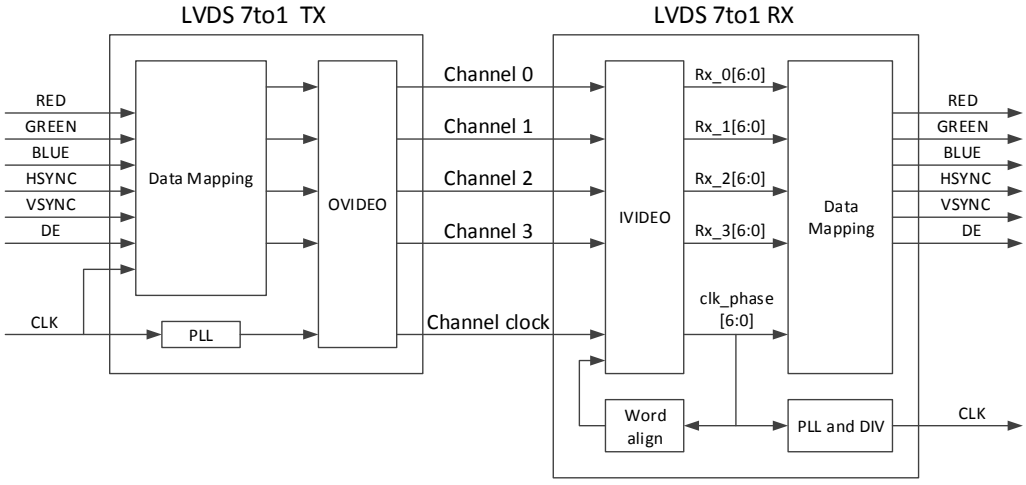
Gowin LVDS 7to1 TX RX IP includes LVDS 7to1 TX IP and LVDS 7to1 RX IP, and its block diagram is as shown in Figure 3-1.

Figure 3-1 Block Diagram



3.2 Implementation Diagram

Figure 3-2 Implementation Diagram



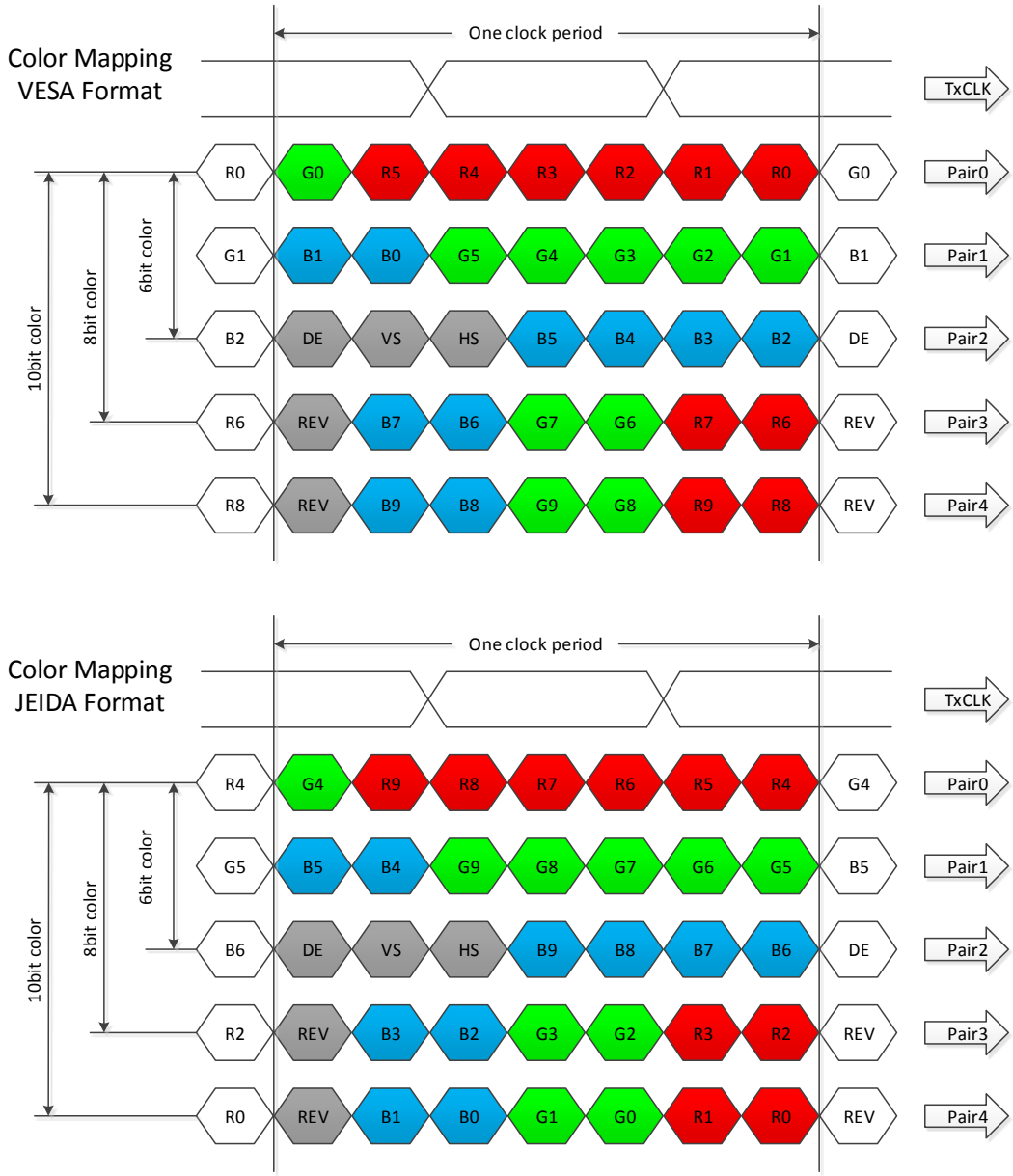
LVDS 7to1 TX IP mainly includes Data Mapping and OVIDEO modules. LVDS 7to1 RX IP mainly includes IVIDEO, Word align and Data Mapping modules.

3.2.1 LVDS 7to1 TX

The LVDS 7to1 TX completes the mapping and serial-to-parallel conversion of video data and includes Data Mapping and OVIDEO.

- Data Mapping Module
  Maps the video RGB data and HS/VS signals based on VESA or JEIDA standards, and the data mapping standard diagram is shown in Figure 3-3.

Figure 3-3 Data Mapping Standard Diagram



- OVIDEO Module
  Converts 7-bit parallel data to serial data for output.

3.2.2 LVDS 7to1 RX

The LVDS 7to1 RX completes the deserialization and data mapping of the LVDS signals, and it mainly consists of IVIDEO, Word align and Data Mapping, and finally outputs RGB data and HS/VS signals.

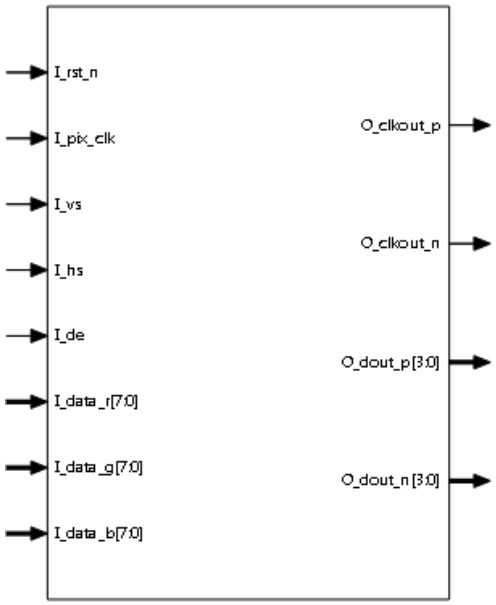
- IVIDEO Module
  Converts LVDS serial data into 7-bit parallel data.
- Word align Module
  Generates slip signal to control the IVIDEO bit shift until 7'b1100011 appears in the clk_phase[6:0] data.
- Data Mapping Module
  Remaps the 7-bit parallel data of each channel and converts it into RGB data and HS/VS signals.

3.3 Port List

3.3.1 LVDS 7to1 TX Port

The I/O ports of the Gowin LVDS 7to1 TX IP are shown in Figure 3-4.

Figure 3-4 LVDS 7to1 TX IO Diagram



Ports vary slightly depending on the parameters.

The details of I/O ports of Gowin LVDS 7to1 TX IP are shown in Table 3-1.

Table 3-1 I/O List of Gowin LVDS 7to1 TX IP

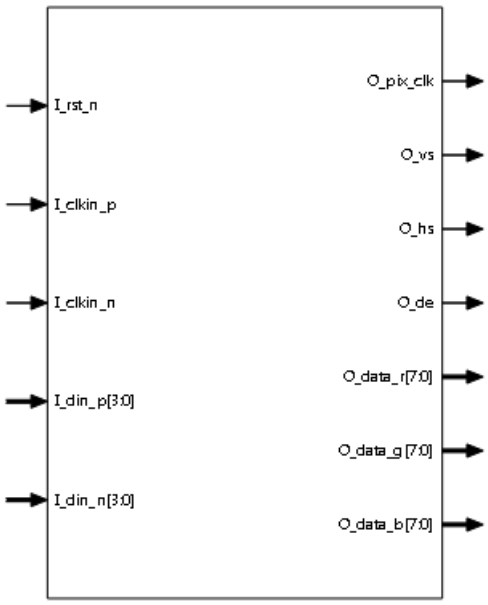
No.	Signal Name	I/O	Description	Remarks
1	I_rst_n	I	Reset signal, active-low	The I/O of all the signals takes LVDS 7to1 TX IP as reference.
2	I_serial_clk	I	This signal is valid when using external clock. I_serial_clk = I_pix_clk * 3.5	
3	I_pix_clk	I	Video input pixel clock	
4	I_vs	I	Video input vs signal	
5	I_hs	I	Video input hs signal	
6	I_de	I	Video input de signal	
One Channel				
7	I_data_r	I	Video input R component	

No.	Signal Name	I/O	Description	Remarks
8	I_data_g	I	Video input G component	
9	I_data_b	I	Video input B component	
10	O_clkout_p	O	Output clock positive of LVDS differential signal	
11	O_clkout_n	O	Output clock negative of LVDS differential signal	
12	O_dout_p	O	Output data positive of LVDS differential signal	
13	O_dout_n	O	Output data negative of LVDS differential signal	
Two Channel				
14	I_data_ro	I	Video input data odd pixel R component	
15	I_data_go	I	Video input data odd pixel G component	
16	I_data_bo	I	Video input data odd pixel B component	
17	I_data_re	I	Video input data even pixel R component	
18	I_data_ge	I	Video input data even pixel G component	
19	I_data_be	I	Video input data even pixel B component	
20	O_clkouto_p	O	Output clock odd channel positive of LVDS differential signal	
21	O_clkouto_n	O	Output clock odd channel negative of LVDS differential signal	
22	O_clkoute_p	O	Output clock even channel positive of LVDS differential signal	
23	O_clkoute_n	O	Output clock even channel negative of LVDS differential signal	
24	O_douto_p	O	Output data odd channel positive of LVDS differential signal	
25	O_douto_n	O	Output data odd channel negative of LVDS differential signal	
26	O_doute_p	O	Output data even channel positive of LVDS differential signal	
27	O_doute_n	O	Output data even channel negative of LVDS differential signal	

3.3.2 LVDS 7to1 RX Port

The I/O ports of the Gowin LVDS 7to1 RX are shown in Figure 3-5.

Figure 3-5 LVDS 7to1 RX I/O Diagram



Ports vary slightly depending on the parameters.

The details of I/O ports of Gowin LVDS 7to1 RX IP are shown in Table 3-2.

Table 3-2 I/O List of Gowin LVDS 7to1 RX IP

No.	Signal Name	I/O	Description	Remarks
1	I_rst_n	I	Reset signal, active-low.	The I/O of all the signals takes LVDS 7to1 RX IP as reference.
2	O_pix_clk	O	Output pixel clock	
3	O_vs	O	Video output vs signal	
4	O_hs	O	Video output hs signal	
5	O_de	O	Video output de signal	
6	I_clkin_p		Input clock positive of LVDS differential signal	
7	I_clkin_n		Input clock negative of LVDS differential signal	
One Channel				
8	I_din_p		Input data positive of LVDS differential signal	
9	I_din_n		Input data negative of LVDS differential signal	
10	O_data_r		Video output data R component	
11	O_data_g		Video output data G component	
12	O_data_b		Video output data B component	
Two Channel				
13	I_dino_p		Input data odd channel positive	

No.	Signal Name	I/O	Description	Remarks
			of LVDS differential signal	
14	I_dino_n		Input data odd channel negative of LVDS differential signal	
15	I_dine_p		Input data even channel positive of LVDS differential signal	
16	I_dine_n		Input data even channel negative of LVDS differential signal	
17	O_data_ro		Video output data odd pixel R component	
18	O_data_go		Video output data odd pixel G component	
19	O_data_bo		Video output data odd pixel B component	
20	O_data_re		Video output data even pixel R component	
21	O_data_ge		Video output data odd pixel G component	
22	O_data_be		Video output data odd pixel B component	

3.4 Parameter Configuration

3.4.1 LVDS 7to1 TX Parameters

Table 3-1 LVDS 7to1 TX Parameters

No.	Name	Range	Default	Description
1	Using External Clock	Yes/No	No	If this parameter is configured, the external serial clock I_serial_clk is used; Or it will be generated by PLL.
2	TX Clock In Frequency	10.0~110.0	74.250MHz	Input clock frequency value
3	Data Channels	One/Two	One	Number of LVDS channels
4	Clock Numbers	One/Two	One	Number of LVDS clock
5	Data Mapping Standard	VESA/JEIDA	VESA	Data Mapping Standard
6	Video Data Format	RGB888/RGB666	RGB888	RGB Data Format
7	OBUF Type	TLVDS/ELVDS	TLVDS	I/O Buffer Type

3.4.2 LVDS 7to1 RX Parameters

Table 3-4 LVDS 7to1 RX Parameters

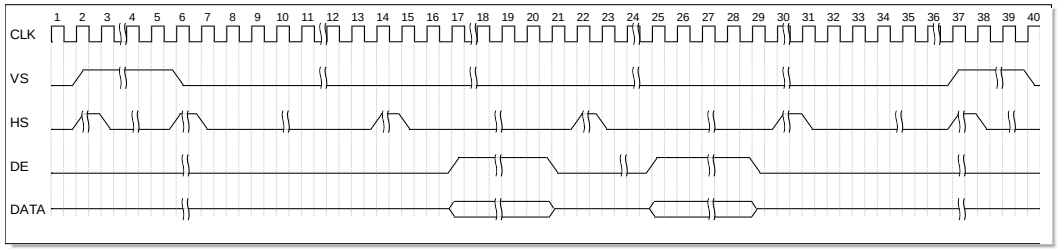
No.	Name	Range	Default	Description
1	RX Clock In Frequency	10.0~110.0	74.250MHz	Input clock frequency value
2	Phase Search Mode	Auto/Manual	Auto	Phase Search Mode
3	Initial Phase	0.0/180	0.0	Initial phase value
4	RX Clock Out Phase	0.0/22.5/45/67.5/90/112.5/135/157.5/180/202.5/225/247.5/270/292.5/315/337.5	0.0	Output phase value of serial clock
5	Data Channels	One/Two	One	Number of LVDS channels
6	Data Mapping Standard	VESA/JEIDA	VESA	Data Mapping Standard
7	Video Data Format	RGB888/RGB666	RGB888	RGB data format
8	Data0 IO Delay Value	0~127	0ps	Data0 IO Delay Control
9	Data1 IO Delay Value	0~127	0ps	Data1 IO Delay Control
10	Data2 IO Delay Value	0~127	0ps	Data2 IO Delay Control
11	Data3 IO Delay Value	0~127	0ps	Data3 IO Delay Control
12	Odd Data0 IO Delay Value	0~127	0ps	Odd Data0 IO Delay Control
13	Odd Data1 IO Delay Value	0~127	0ps	Odd Data1 IO Delay Control
14	Odd Data2 IO Delay Value	0~127	0ps	Odd Data2 IO Delay Control
15	Odd Data3 IO Delay Value	0~127	0ps	Odd Data3 IO Delay Control
16	Even Data0 IO Delay Value	0~127	0ps	Even Data0 IO Delay Control
17	Even Data1 IO Delay Value	0~127	0ps	Even Data1 IO Delay Control
18	Even Data2 IO Delay Value	0~127	0ps	Even Data2 IO Delay Control
19	Even dd Data3 IO Delay Value	0~127	0ps	Even Data3 IO Delay Control

3.5 Timing Description

This section describes the timing of Gowin LVDS 7to1 TX RX IP.

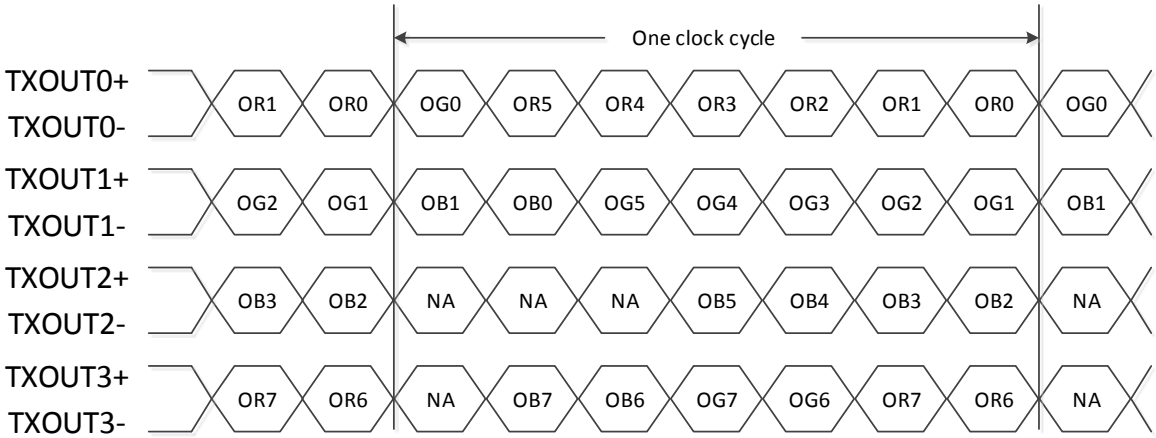
The timing diagram of is as shown in Figure 3-6.

Figure 3-6 Timing Diagram of Video Interface



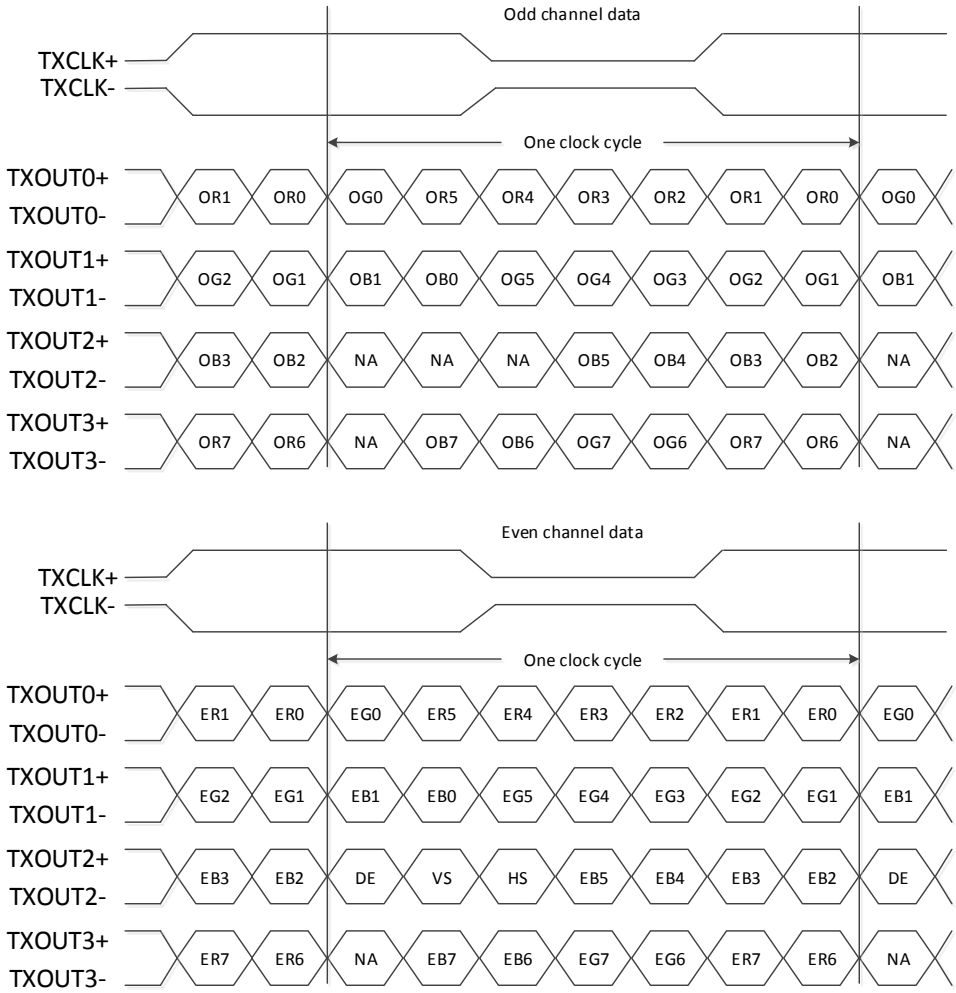
The timing diagram of one channel LVDS is as shown in Figure 3-7.

Figure 3-7 Timing Diagram of One Channel LVDS



The timing diagram of two-channel LVDS is as shown in Figure 3-8.

Figure 3-8 Timing Diagram of Two-channel LVDS



4 GUI

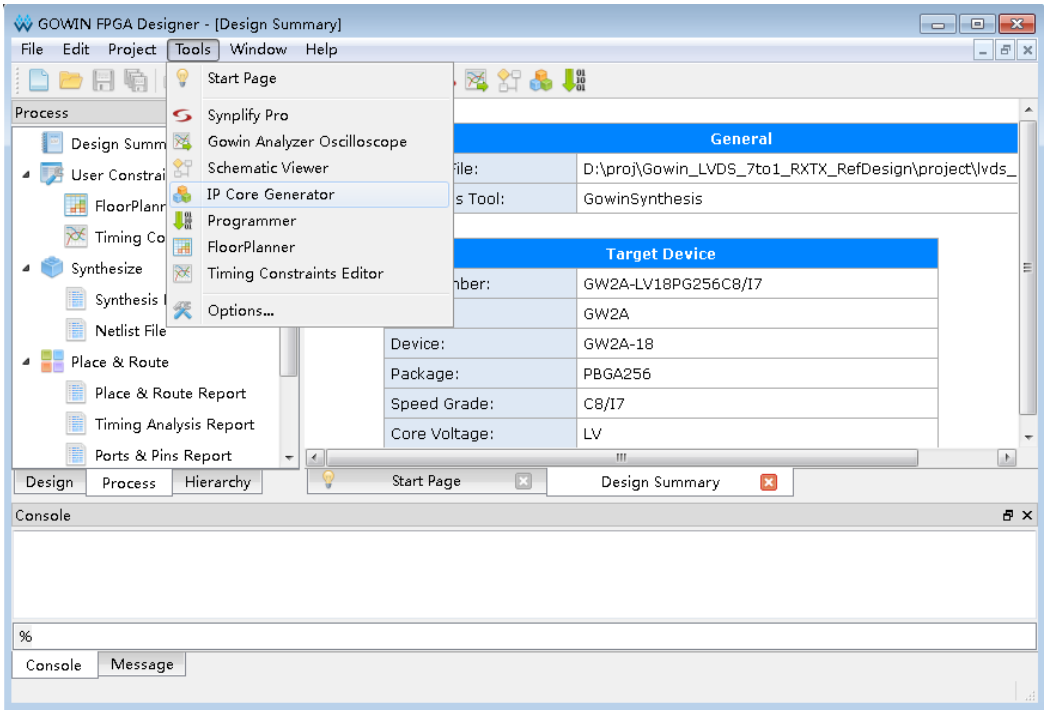
You can use IP core generator in the IDE to call and configure Gowin LVDS 7to1 TX RX IP.

4.1 LVDS 7to1 TX IP Configuration

1. Open IP Core Generator

After creating the project, click the "Tools" tab in the upper left, select and open the IP Core Generater from the drop-down list, as shown in Figure 4-1.

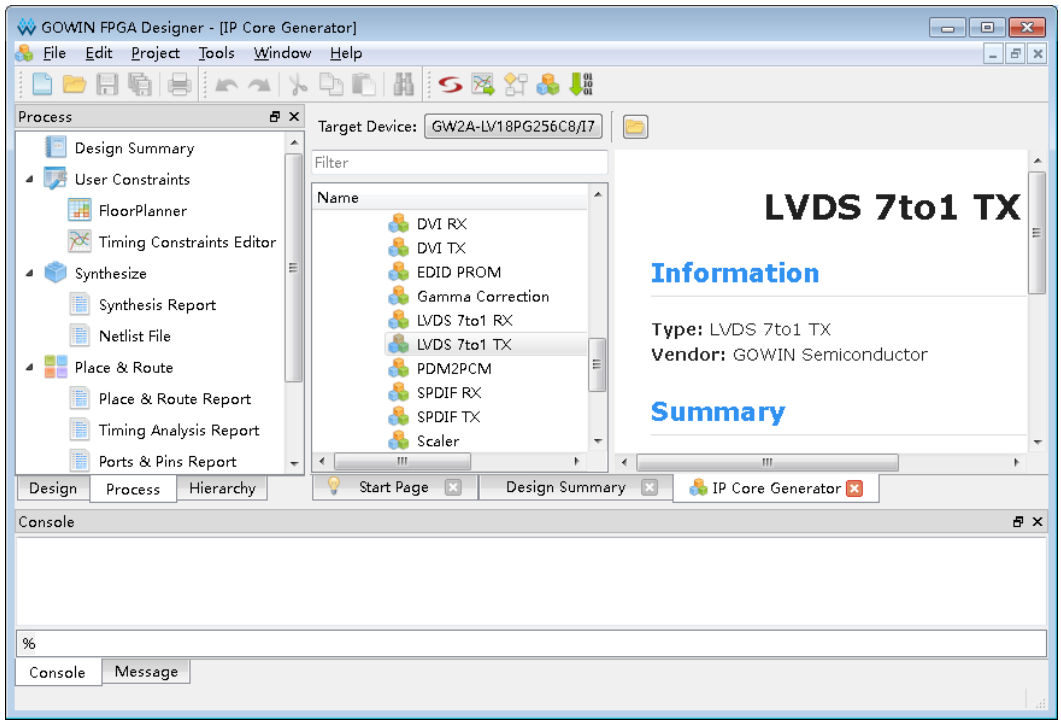
Figure 4-1 Open IP Core Generator



2. Open LVDS 7to1 TX IP core

Click "Multimedia" and double click "LVDS 7to1 TX" to open the configuration interface, as shown in Figure 4-2.

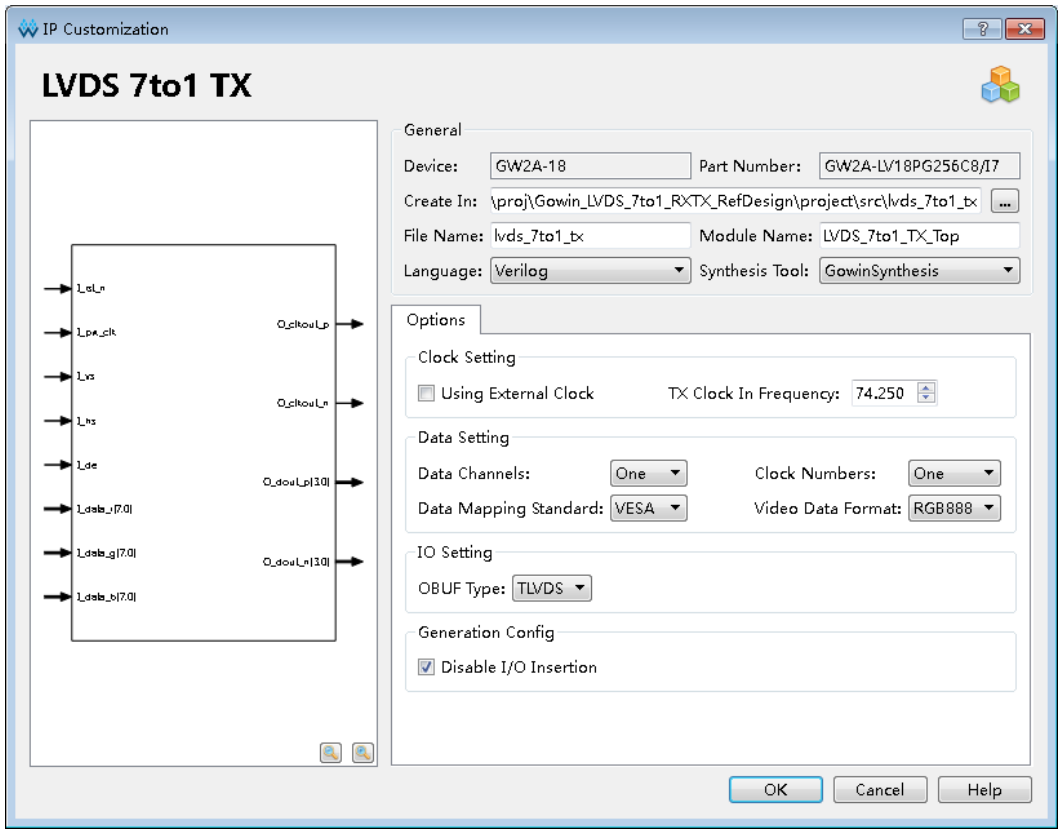
Figure 4-2 Open LVDS 7to1 TX IP Core



3. LVDS 7to1 TX IP Core Port Diagram

On the left of the configuration interface is the port diagram of LVDS 7to1 TX IP, as shown in Figure 4-3.

Figure 4-3 Port Diagram of LVDS 7to1 TX IP



4. Open the Help file

Click "Help" button in the right lower corner of Figure 4-3 to learn the simple English introduction to options in the configuration interface, so as to help you quickly complete the configuration of IP core. The order of options in Help is the same as the one in the interface, as shown in Figure 4-4.

Figure 4-4 Help

LVDS 7to1 TX

Information

Type: LVDS 7to1 TX
Vendor: GOWIN Semiconductor
Summary: The LVDS 7to1 TX IP is used to transmit the video timing signals and data into LVDS signals.

Options & Description

Clock Setting

Using External Clock :

- The choice of whether using external clock.

TX Clock In Frequency :

- The pixel clock frequency of LVDS 7to1 TX.

Data Setting

Data Channels :

- The number of LVDS Channels.

Clock Numbers :

- The number of clock port, when data dhannels are two.

Data Mapping Standard :

- The LVDS data mapping standard, VESA or JEIDA.

Video Data Format :

- The video data format, RGB888 or RGB666.

IO Setting

OBUF Type :

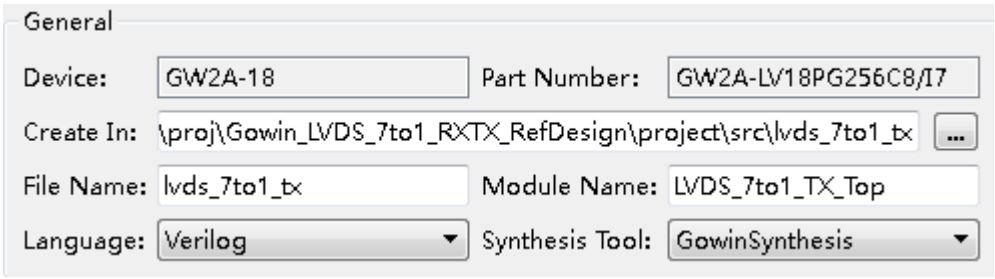
- The choice of OBUF Type, TLVDS_OBUF or ELVDS_OBUF.

5. Configure Basic Information

See the project basic information in the configuration interface. Take GW2A-18 and PBGA484 package as an example. The Module Name option displays the top-level file name of the generated project, and the default is "LVDS_7to1_TX_Top". You can modify the name. The File Name option displays the folder generated by the IP core , which contains the files required by LVDS 7to1 TX IP core, and the default is "lvds_7to1_tx". You

can modify the path. "Creat In" displays the path of IP core folder. The default is "\project path\src\lvds_7to1_tx" . You can modify the path.

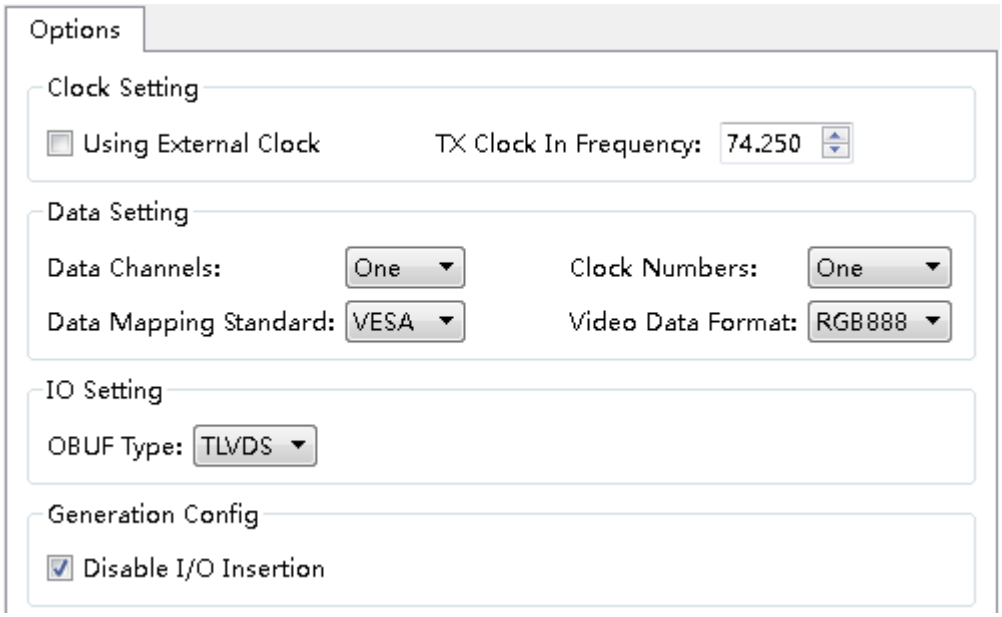
Figure 4-5 Basic Information Configuration Interface



6. Options

You can configure clock and data format in the Options.

Figure 4-6 Options

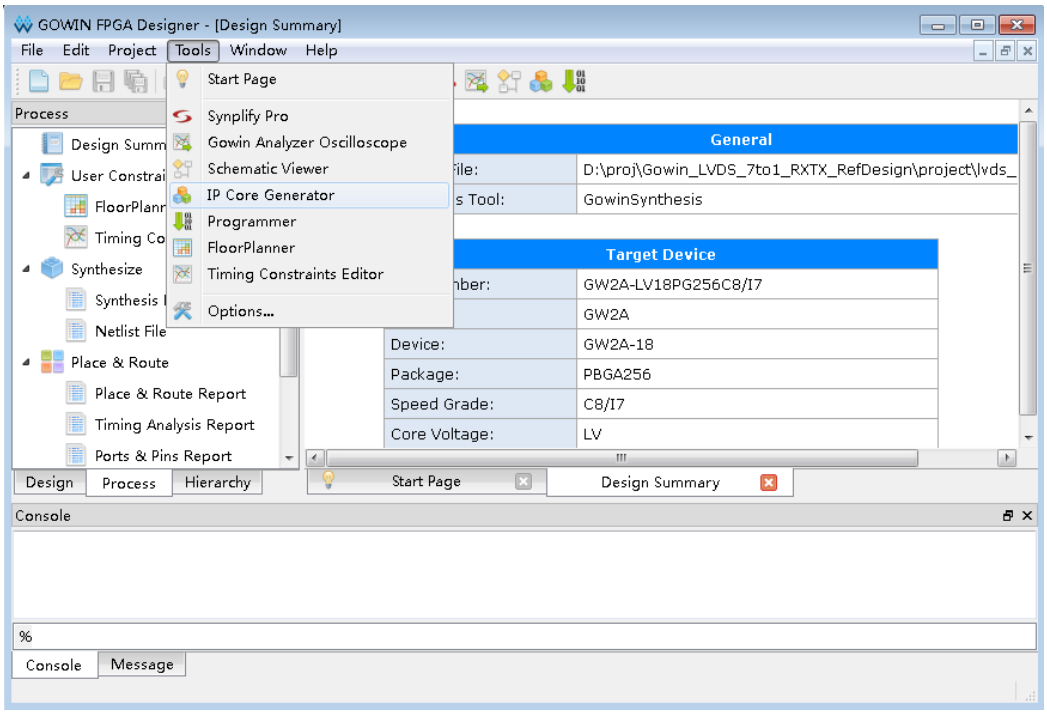


4.2 LVDS 7to1 RX IP Configuration

1. Open IP Core Generator

After creating the project, click the "Tools" tab in the upper left, select and open the IP Core Generater from the drop-down list, as shown in Figure 4-7.

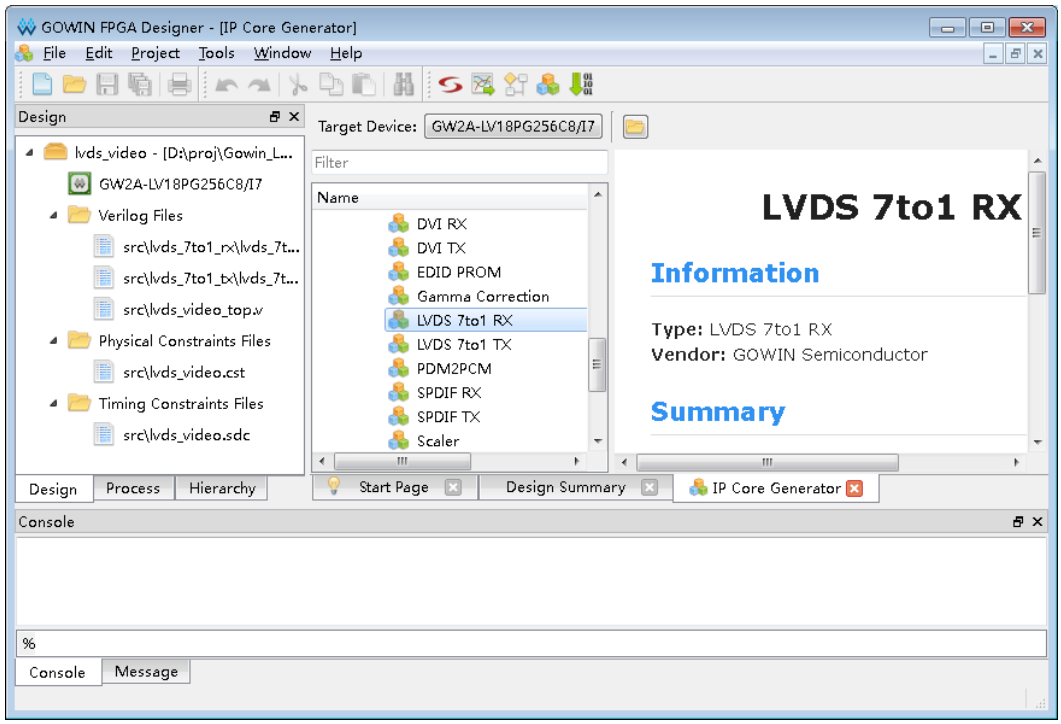
Figure 4-7 Open IP Core Generator



2. Open LVDS 7to1 RX IP core

Click "Multimedia" and double click "LVDS 7to1 RX" to open the configuration interface, as shown in Figure 4-8.

Figure 4-8 Open LVDS 7to1 RX IP Core

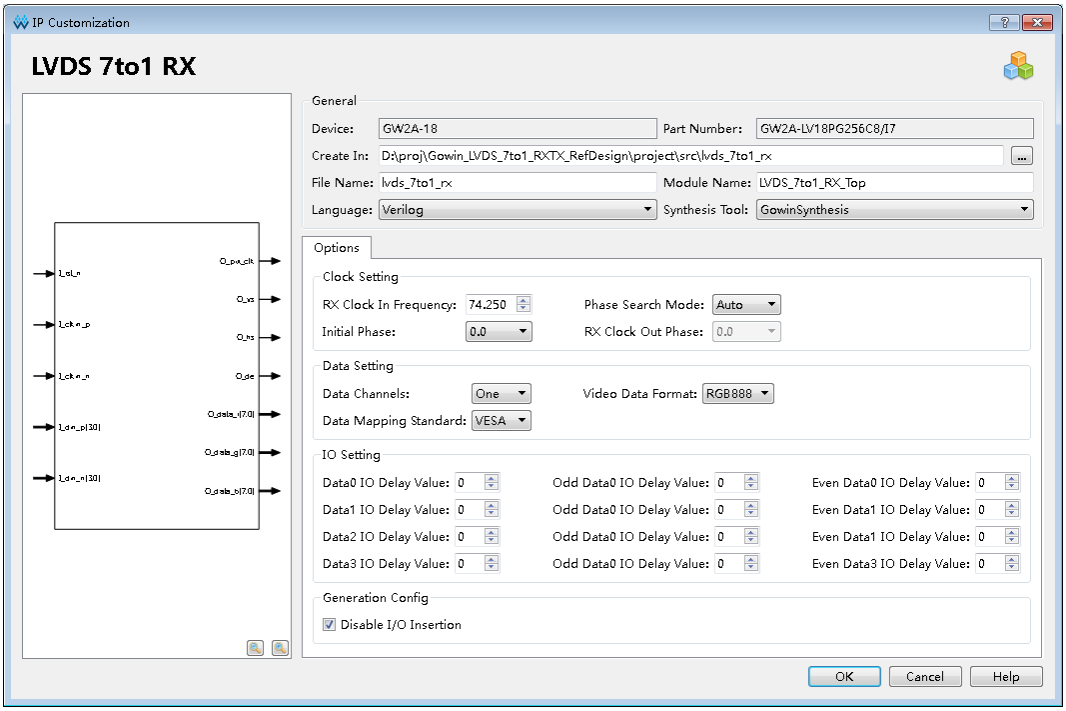


3. LVDS 7to1 RX IP Core Port Diagram

On the left of the configuration interface is the port diagram of LVDS

7to1 RX IP, as shown in Figure 4-9.

Figure 4-9 LVDS 7to1 RX IP



4. Open the Help file

Click "Help" button in the right lower corner of Figure 4-9 to learn the simple English introduction to options in the configuration interface, so as to help you quickly complete the configuration of IP core. The order of options in Help is the same as the one in the interface, as shown in Figure 4-10.

Figure 4-10 Help

LVDS 7to1 RX

Information

Type: LVDS 7to1 RX
Vendor: GOWIN Semiconductor
Summary: The LVDS 7to1 RX IP is used to receive LVDS signals and transmit it into the video timing signals and data.

Options & Description

Clock Setting

RX Clock In Frequency :

- The pixel clock frequency of LVDS 7to1 RX.

Phase Search Mode :

- The RX clock out phase search mode, Auto or Manual.

Initial Phase :

- The initial phase of output serial clock in Auto mode.

RX Clock Out Phase :

- The phase of output serial clock in Manual mode.

Data Setting

Data Channels :

- The number of LVDS Channels.

Data Mapping Standard :

- The LVDS data mapping standard, VESA or JEIDA.

Video Data Format :

- The video data format, RGB888 or RGB666.

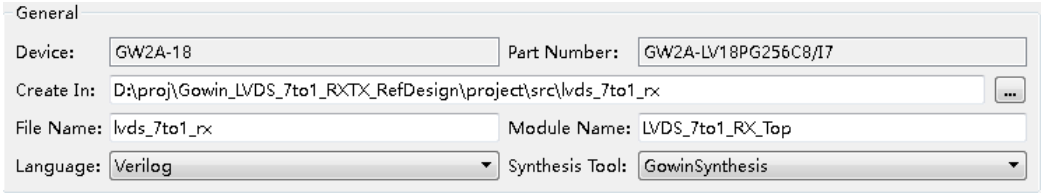
IO Setting

Data0 IO Delay Value :

5. Configure Basic Information

See the project basic information in the configuration interface. Take GW2A-18 and PBGA484 package as an example. The Module Name option displays the top-level file name of the generated project, and the default is "LVDS_7to1_RX_Top". You can modify the name. The File Name option displays the folder generated by the IP core, which contains the files required by LVDS 7to1 RX IP core, and the default is "lvds_7to1_rx". You can modify the path. Creat In" displays the path of IP core folder. The default is "\project path\src\lvds_7to1_rx" . You can modify the path.

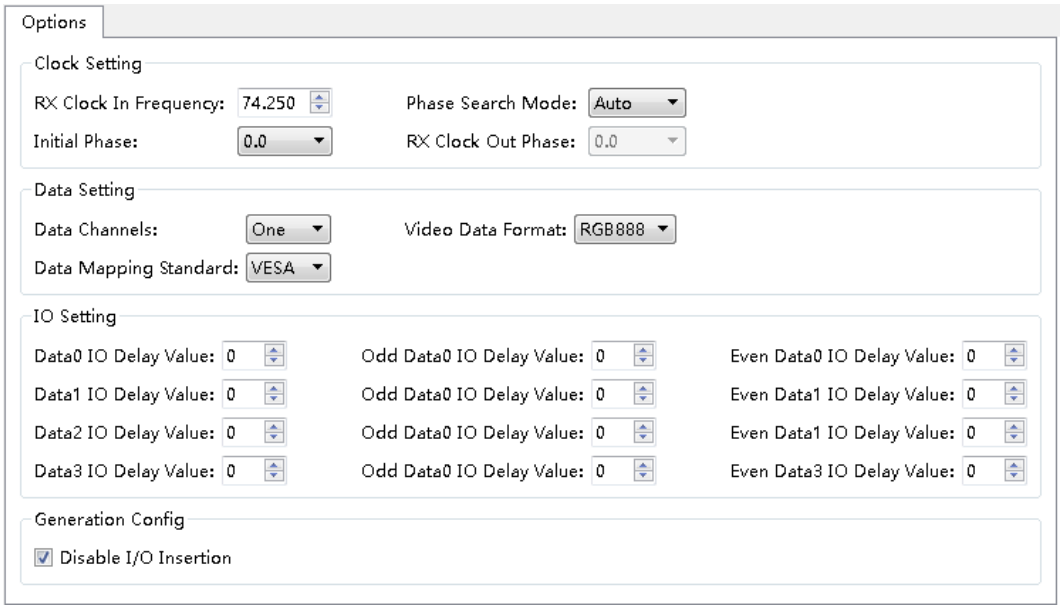
Figure 4-11 Basic Information Configuration Interface



6. Options

You can configure clock, data format in the Options.

Figure 4-12 Options



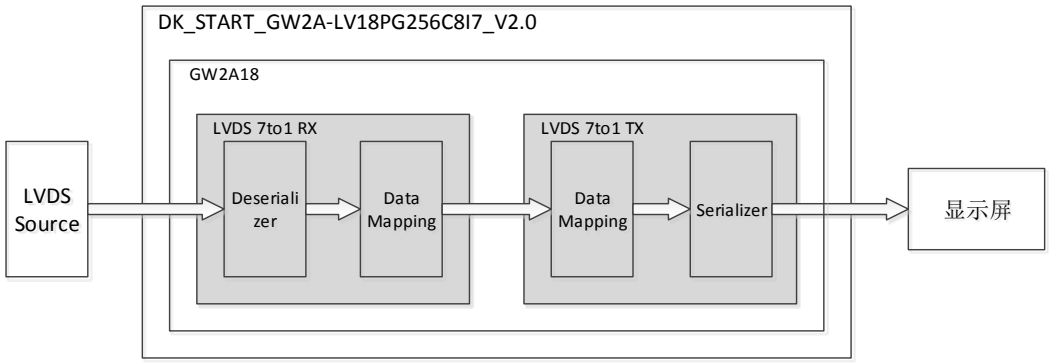
5 Reference Design

This chapter introduces the usage and structure of the reference design instance of Gowin LVDS 7to1 TX RX IP. Please see LVDS 7to1 Reference Design for details at Gowinsemi website.

5.1 Design Instance 1

Take DK_START_GW2A-LV18PG256C8I7_V2.0 as an example, and the diagram is as shown in Figure 5-1. For the details of DK_START_GW2A-LV18PG256C8I7_V2.0, you can click here.

Figure 5-1 Reference Design Diagram



In this instance, there are LVDS 7to1RX IP and LVDS 7to1 TX IP, and the steps are as follows:

1. Receive LVDS 7:1 format video data with 1280x800 resolution via LVDS RX interface.
2. The LVDS 7to1 RX IP module is used to deserialize the LVDS signal and to map the data.
3. The LVDS 7to1 TX IP module is then used to map the parallel video data, serialize it, and then convert it to LVDS signals.
4. It is then output through the LVDS TX interface and connected to the display, where the input LVDS signal can be displayed.

When the reference design is applied to board-level test, you can output signal to the display and also can analyze with the on-line logic analyzer or oscilloscope.

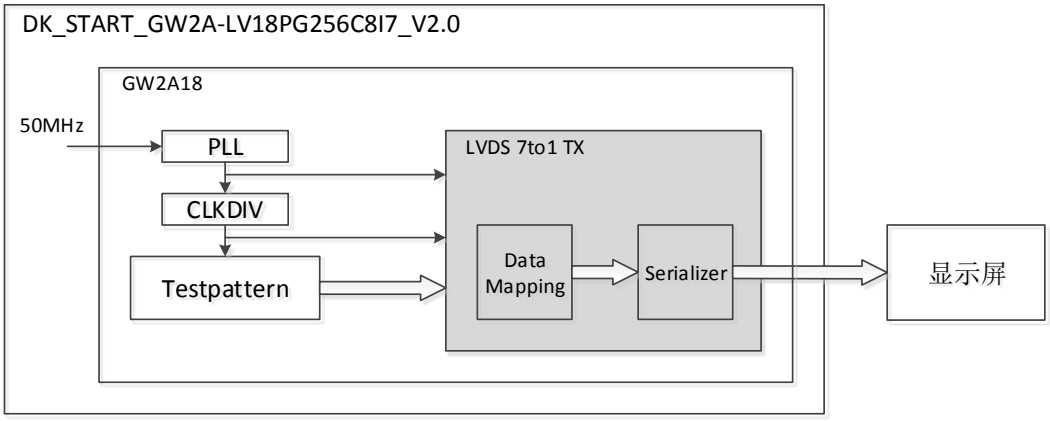
In the simulation project provided by the reference design, bmp bitmap

is used as the test excitation source, and tb_top is the top-level module of the simulation project. The simulation results can be compared with the output figures.

5.2 Design Instance 2

Take DK_START_GW2A-LV18PG256C8I7_V2.0 as an example, and the diagram is as shown in Figure 5-2.

Figure 5-2 Reference Design Diagram



In this reference design, there is only LVDS 7to1 TX IP, and its steps are as follows:

1. The pixel clock and serial clock required by LVDS 7to1 TX IP is generated from 50MHz reference clock.
2. Test data with 1280x800 resolution video format is output by the Testpattern module.
3. The LVDS 7to1 TX IP is used to map the parallel video data , serialize and convert to LVDS signals.
4. It is then output through the LVDS TX interface and connected to the display, where the test pattern can be displayed. Test pattern includes color pattern, grid pattern, grayscale pattern and pure color pattern.

In the simulation project provided by the reference design, bmp bitmap is used as the test excitation source, and tb_top is the top-level module of the simulation project. The simulation results can be compared with the output figures.

6 File Delivery

The delivery file of Gowin LVDS 7to1 TX RX IP includes file, source code and reference design.

6.1 Documents

The document mainly contains the user guide in PDF.

Table 6-1 Document List

Name	Description
IPUG771, Gowin LVDS 7to1 TX RX IP User Guide	Gowin LVDS 7to1 TX RX IP, namely this one.

6.2 Design Source Code (Encryption)

The encrypted code file contains RTL encrypted code, which is used for GUI in order to generate IP core required by users.

Table 6-2 LVDS 7to1 TX Design Source Code List

Name	Description
lvds_7to1_tx.v	The top-level file of the IP core, which provides you with interface information, encrypted.

Table 6-3 LVDS 7to1 RX Design Source Code List

Name	Description
lvds_7to1_rx.v	The top-level file of the IP core, which provides you with interface information, encrypted.

6.3 Reference Design

The Ref. Design folder contains the netlist file, user reference design, constraints file, top-level file and the project file, etc.

Table 6-4 Flie List

Name	Description
lvds_video_top.v	The top module of reference design
lvds_video.cst	Project physical constraints file
lvds_video.sdc	Project timing constraints file
lvds_7to1_tx	LVDS 7to1 TX IP project folder

Name	Description
lvds_7to1_rx	LVDS 7to1 RX IP project file

The Ref. Design folder contains the netlist file, user reference design, constraints file, top-level file and the project file, etc.

Table 6-5 File List

Name	Description
lvds_video_top.v	The top module of reference design
lvds_video.cst	Project physical constraints file
lvds_video.sdc	Project timing constraints file
testpattern.v	Reference Design file
lvds_7to1_tx	LVDS 7to1 TX IP project folder
gowin_rpll	PLL project file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