PROJECT REPORT

24 HOUR DIGITAL CLOCK

Student Name: Shoaib Asghar 19I-0406

Introduction:

The clock consists of three stages - seconds, minutes, hours after reading time 23 hours 59 minutes 59 seconds then repeat back 00.00.00, better called 0^{th} hour. we use the Push Button to set the clock zero or at any time. We know that 60 seconds equals 1 minute and 60 minutes equals 1 hour. Hence the minute section is derived by second section and hour section derived by the minute section. Each of the minute and second section has been designed to give a count from 00 to 59 after which it resets to 00. And the hour section to give a count from 00 to 24 hours after which it resets to 00. For each cycle of 00 to 59 in second section the minute section increases its count by 1. Similarly for each cycle of 00 to 59 in minute section the hour section increases its count by 1. In this way when the clock reaches 23hrs. 59mins. 59secs.each of the section resets to 00 giving us a display 00.00.00 known as the 0^{th} hour.

Working:

The whole project is divided into four modules. These are following:

555 IC Timer Section:

The 555 Timer IC is an integrated circuit (chip) used in various time zones, pulse generation, and oscillator applications. 555 timer gives 1 Hz frequency to JK Flip Flop.

Second section:

We used eight JK Flip Flop IC (4027) and one IC contains two flip flops. We use four JK flip flop IC which give 0 to 15 outputs of the flip flop and the other four JK flip flop IC also give 0 to 15 count. But we know that digital clock always display 5 and 9 in Second, instead of this we required 0 to 5 output in one seven segment display so we connect the AND gate which gave low logic to JK flip flop and not allow it to exceed from 5 digit numbers which is our requirement on one seven segment display. On the other hand the remaining four JK flip flops which also give 0 to 15 count but our requirement is that it should display 0 to 9 count not to exceed from it so we use AND gate to stop it and give us our requirement which is 0 to 9 count on single 7 segment display. Now the circuit will Display Successfully 5 and 9 in each 7 segments display with the help of IC 74LS248 then it gives clock pulse to minute section.

Minute section:

Repeat the same operation which we had previously use for the seconds section but this part active when second section more than from 59 second display. We use total eight JK Flip Flop IC (4027) and one IC contains two JK flip flops. We use four JK flip flop IC which give 0 to 15 outputs of the flip flop and the other four JK flip flop IC also give 0 to 15 count. But we know that digital clock always display 5 and 9 in minute, instead of this we required 0 to 5 output in one seven segment display so we connect the AND gate which gave low logic to JK flip flop and not allow it to exceed from 5 digit numbers which is our requirement on one seven segment display.

On the other hand the remaining four JK flip flops which also give 0 to 15 count but our requirement is that it should display 0 to 9 count not to exceed from it so we use AND gate to stop it and give us our requirement which is 0 to 9 count on single 7 segment display. Then the circuit will Display Successfully 5 & 9 in each 7 segments display with the help of IC 74LS248 then it gives clock pulse to hour section.

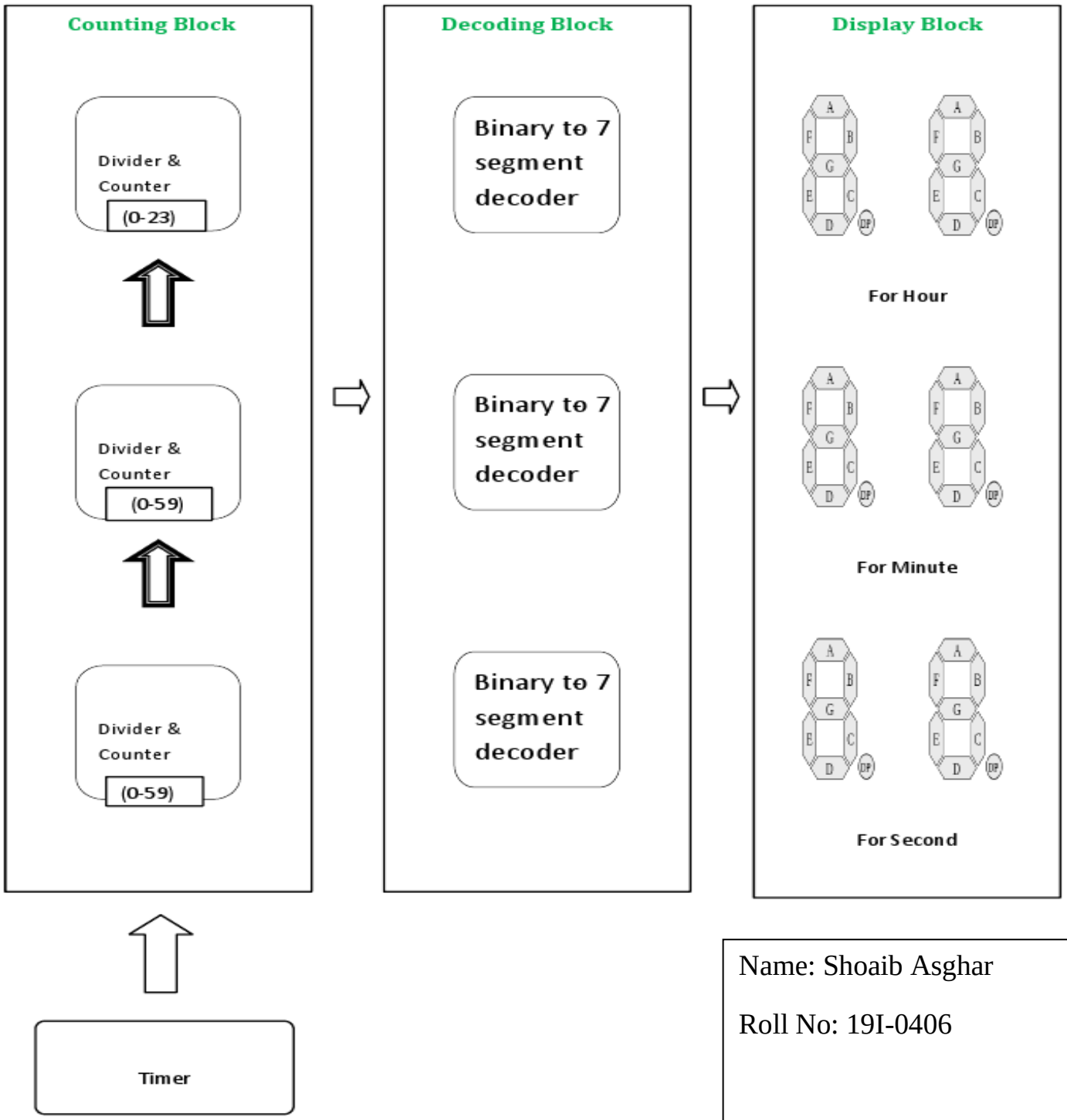
Hour section:

Design the circuit in a way so that the output resets to 00 00 00 automatically when display 11.59.59 in whole 7segement display. The counting process with a frequency of 1 pulse per hour coming from minute section. We used four JK flip flop IC (4027) and in a one JK Flip Flop IC it contain two flip flop function. We also know that hour section would show 2&4 in each 7 segment display not great than this number. So we need 0 to 2 displays count on first 7 segment and 0 to 4 counts on other 7 segment. In hour section same as previous operation we use Jk Flip flop to connect all needy component we need 0 to 2 display on 1 seven segment display due to prevent it from exceed we use NAND operation to clear the two flip flop which they want to show 0 to 4 count but our requirement is to display 0 to 2. On other hand remaining flip flop which would like to show 0 to 15 counting but our required to display only 0 to 9 count on single 7segment display so we use NAND gate to clear when it want to increase but our goal display only 0 to 2 and 0 to 4 on each seven segment only, not above than that.

COMPONENT USED

Material	Quantity
IC 7408	7(2 for min & sec and 3 for hrs)
IC 7400	2(1 for min & hrs section)
IC 7432	4(1 for min and 3 for hrs section)
IC 74LS248	6(2 for each section)
IC 4027	24(8 for sec,8for min 8 for hrs)
IC 555	1
7-segment display(common Cathode Type)	6(2 for each section)
Push Button	2(1 for min and 1 for hrs)
Resistances 470Ω, 470k Ω, 10k Ω	1, 1, 2
Capacitor 1uf	1

Block Diagram

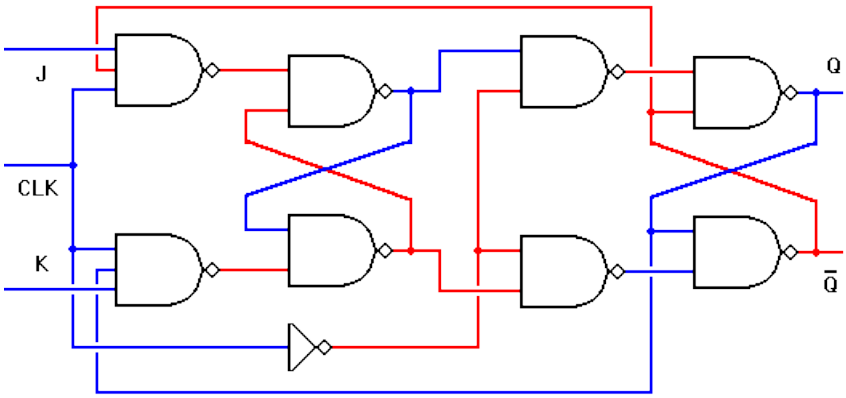


Name: Shoaib Asghar

Roll No: 19I-0406

JK – flip-flop:

JK-flip-flop with reset function is the most important basic block used to create counters. The JK flip-flop added the behavior of the SR flip-flop (J=SET, K=RESET) by interpret JK flip-flop as S=R=1 condition as change or toggle command. Generally it has different combination as, the combination J=1, k=0 is a command to set the flip flop; the combination J=K=1 is a toggle command of the flip-flop i.e. change its output to the logical complement of its current value. This flip flop is negative edge triggered flip flop as bellow.



0-5 Counter:

0-5 counter acts as a digital output for ten's digit of minutes. The main idea of using 0-5 counter is based on JK flip flop to ripple the digits. Digit starts from 00 when it reaches to 5 and then it again start from 00. To design 0-5 counter we used 3 JK flip flops, Inverters, and NAND gates. The truth table of 0-5 counter is following.

	OUTPUT		COUNT
C	B	A	
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5

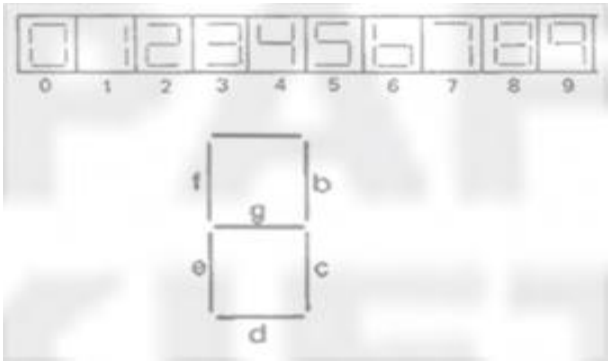
0-9 counter:

0-9 counter is a inhanced version of 0-5 counter. 0-9 acts as a digital output for units of minute. The main idea of using 0-9 counter is based on JK flipflop to ripple the digits. Digits start from 00, when they reach 9 in decimal and then then it again start from 00. The truth table of 0-9 counter is following.

OUTPUT			COUNT	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

Seven Segment Decoder :

7 segment Decoder is used for output binary digits of Second Minutes and Hours in LEDs display. Normally, LEDs Display has the function as following in the table below. We usually use the previous 10 output from 0 to 9 counter. To implement this function, we generate the truth table for a Seven Segment decoder as below and get its corresponding seven segment output and Convert them into decimal which is display on 7 Segment display.



Function Table of 74LS248 IC:

Decimal or function	Input						BI/RBO	Outputs							Note
	LT	RBI	D	C	B	A	1	a	b	c	d	e	f	g	1
0	1	1	0	0	0	0	1	1	1	1	1	1	1	0	1
1	1	X	0	0	0	1	1	0	1	1	0	0	0	0	
2	1	X	0	0	1	0	1	1	1	0	1	1	1	0	
3	1	X	0	0	1	1	1	1	1	1	1	0	1	0	
4	1	X	0	1	0	0	1	0	1	1	0	0	1	1	
5	1	X	0	1	0	1	1	1	0	1	1	0	1	1	
6	1	X	0	1	1	0	1	1	0	1	1	1	1	1	
7	1	X	0	1	1	1	1	1	1	1	0	0	0	0	1
8	1	X	1	0	0	0	1	1	1	1	1	1	1	1	
9	1	X	1	0	0	1	1	1	1	1	1	0	1	1	
10	1	X	1	0	1	0	1	0	0	0	1	1	0	1	
11	1	X	1	0	1	1	1	0	0	1	1	0	0	1	
12	1	X	1	1	0	0	1	0	1	0	0	0	1	1	
13	1	X	1	1	0	1	1	1	0	0	1	0	1	1	
14	1	X	1	1	1	0	1	0	0	0	1	1	1	1	
15	1	X	1	1	1	1	1	0	0	0	0	0	0	0	
BI	X	X	X	X	X	X	0	0	0	0	0	0	0	0	2
RBI	1	0	L	0	0	0	0	0	0	0	0	0	0	0	3
LT	0	X	X	X	X	X	1	1	1	1	1	1	1	1	4

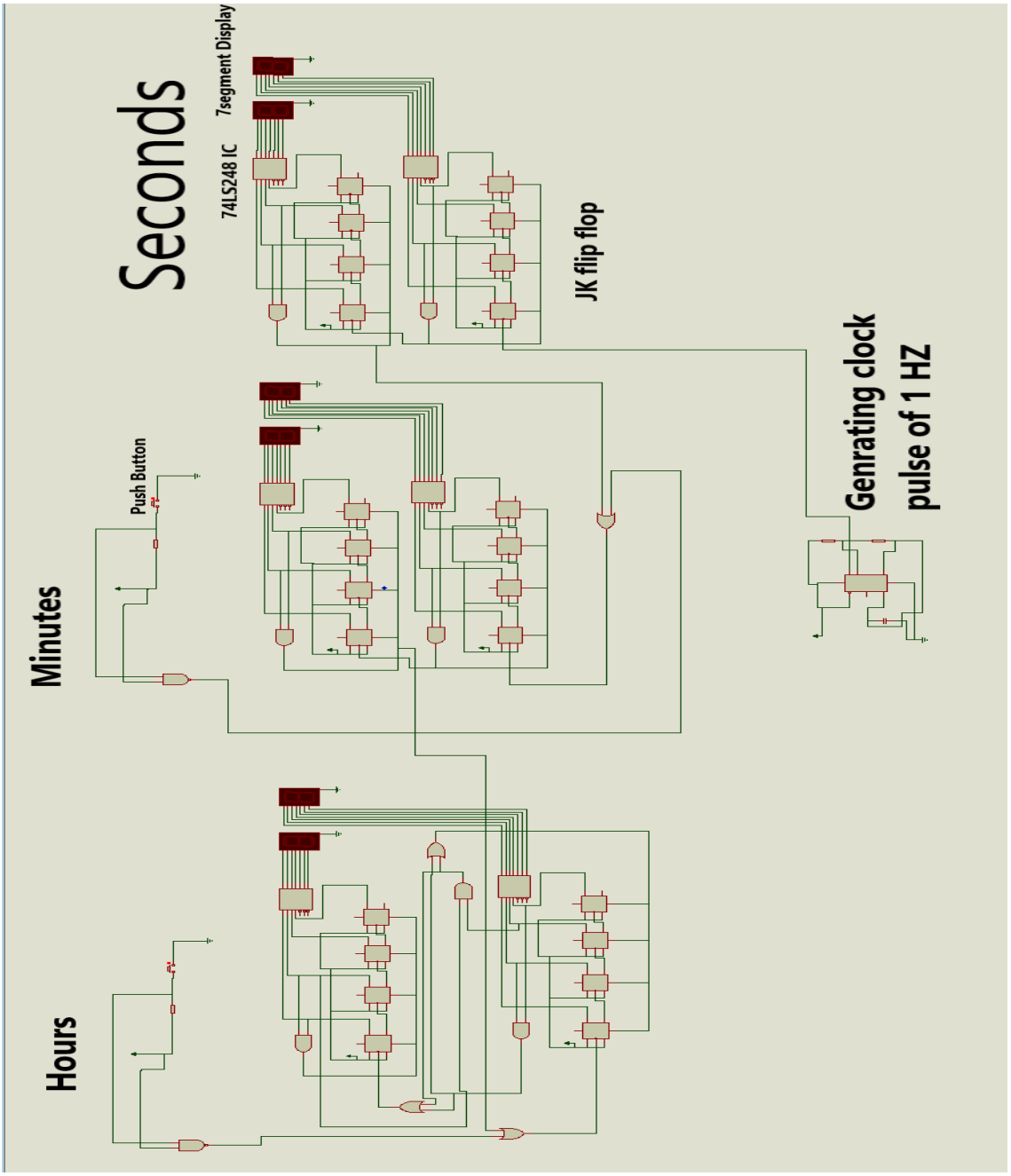
Calculation 555 timer IC:

$F = \frac{1.44}{(R1+2R2)C}$ $\qquad R1 = 470\ \Omega \quad , \ R2 = 470\ k\Omega$

$F = \frac{1.44}{(470 + 2(470*1000))*(1*10^{-6})}$ $\qquad C = 1\ \mu F$

F=1 Hz

Circuit Diagram:



Assembling the whole sections:

Now the circuit is completely design. we Design the three sections (seconds, minute and hour) to get the “Digital Clock” with the supply connected to power source, we operate the clock to check the output many times. By using push button we set the time as we want and Reset the clock to 00 00 00 (initial state). The clock was found to operate correctly and satisfy all the condition which we were given.

Conclusion :

The Degital Clock is purely designed with the basic knowledge on sequential circuit designing and with the components which we use in the Lab. The Clock is operate smoothly with desired accuracy.

Figure 1