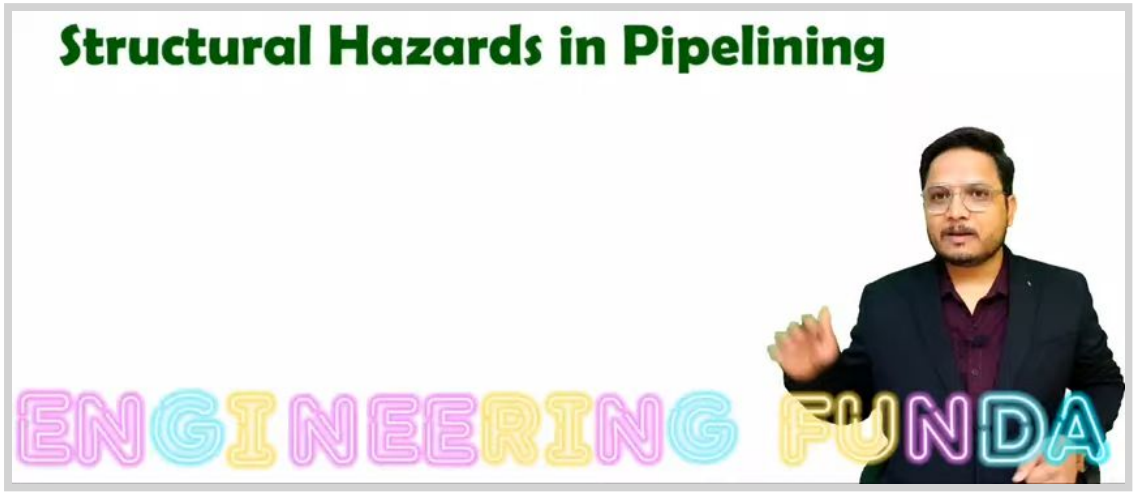
←

00:00



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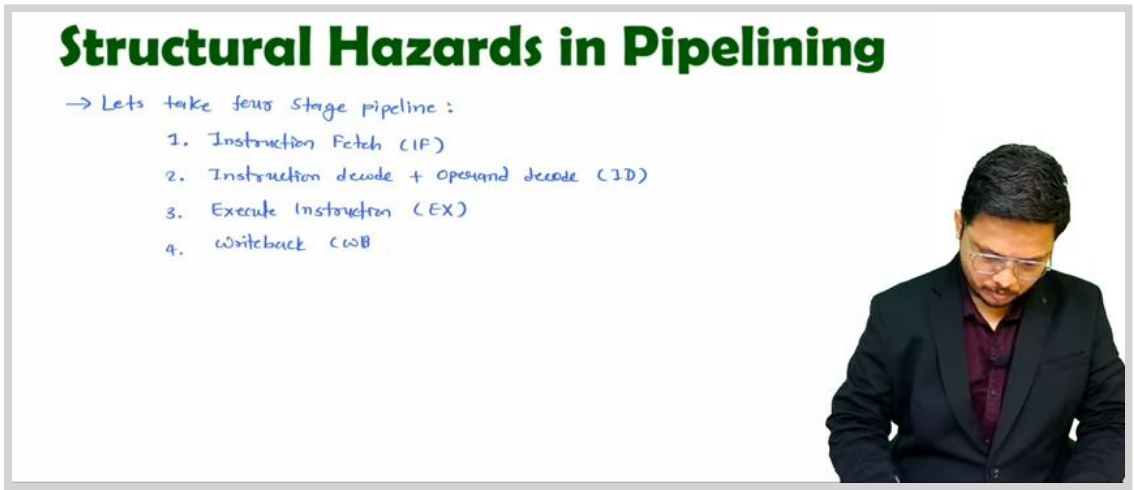

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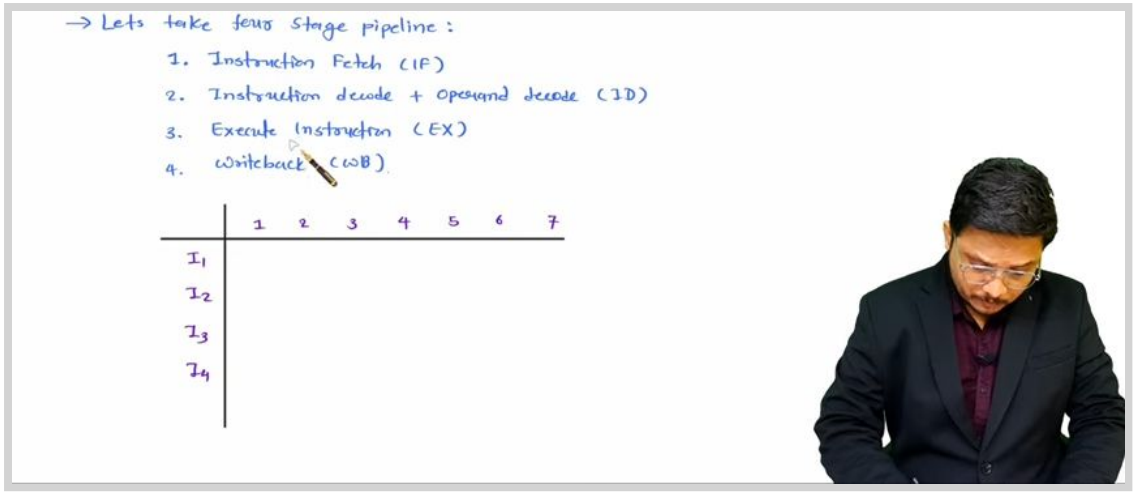

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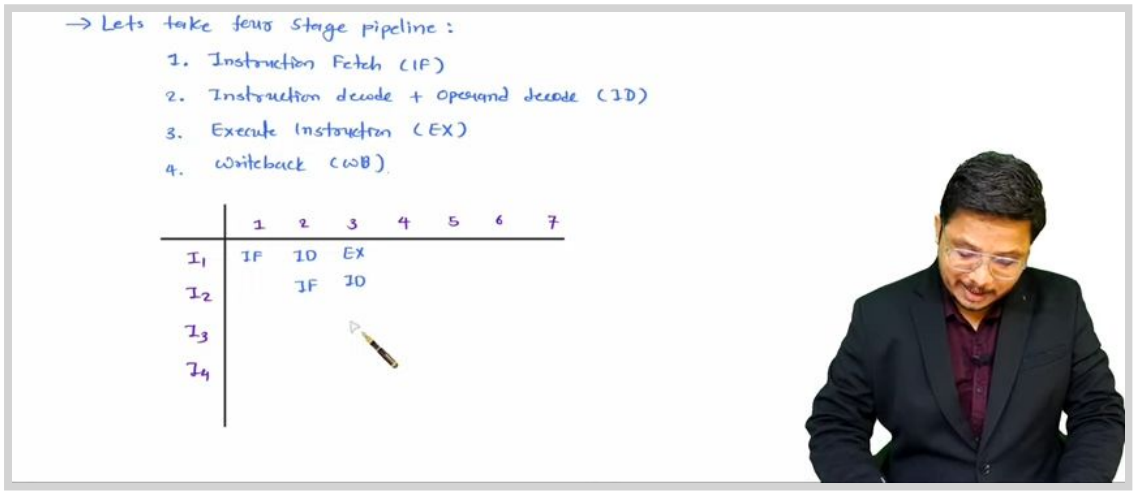

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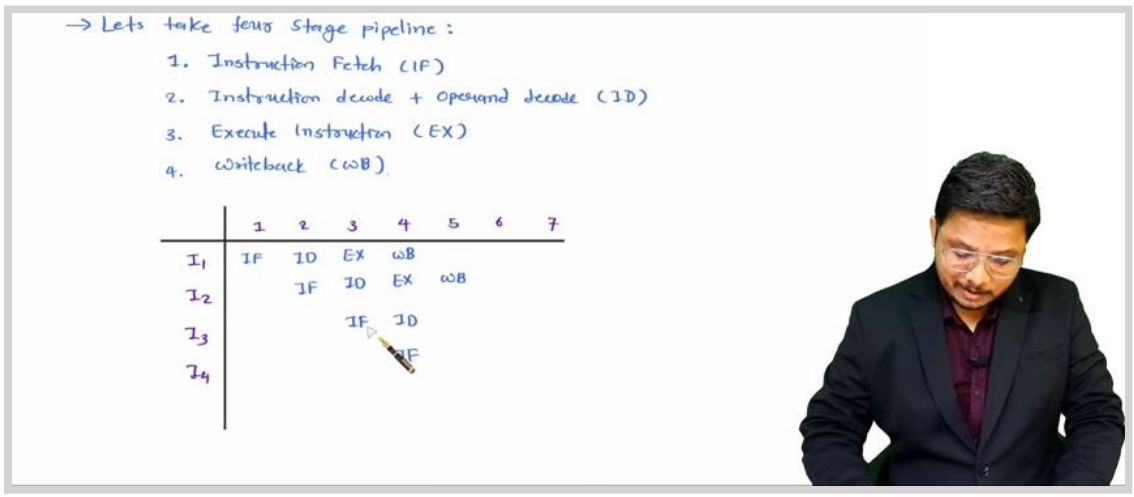

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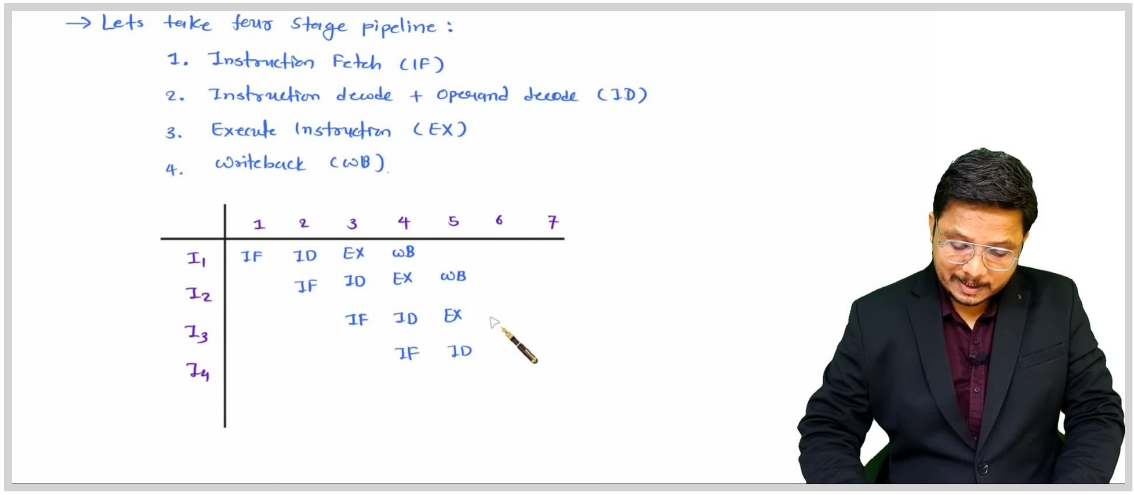

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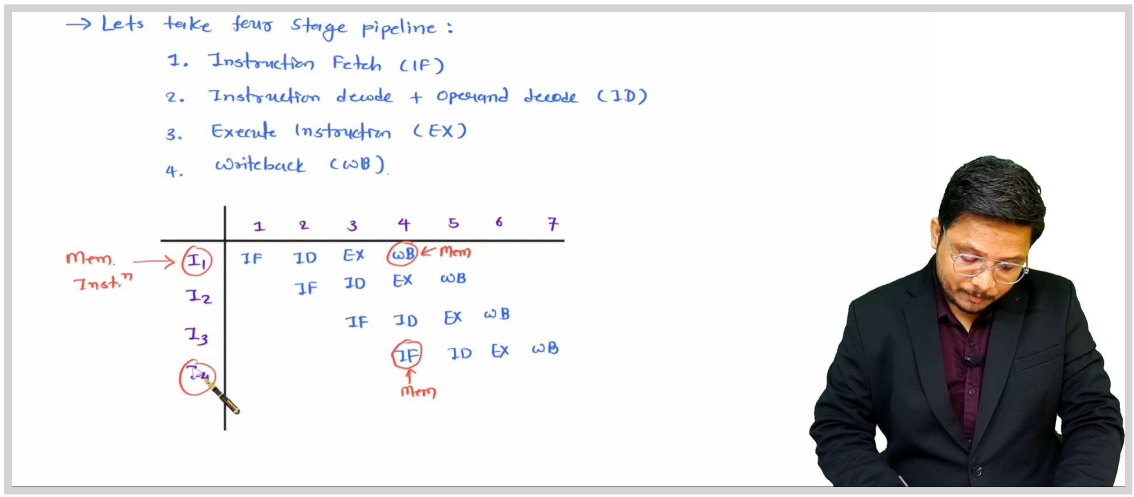

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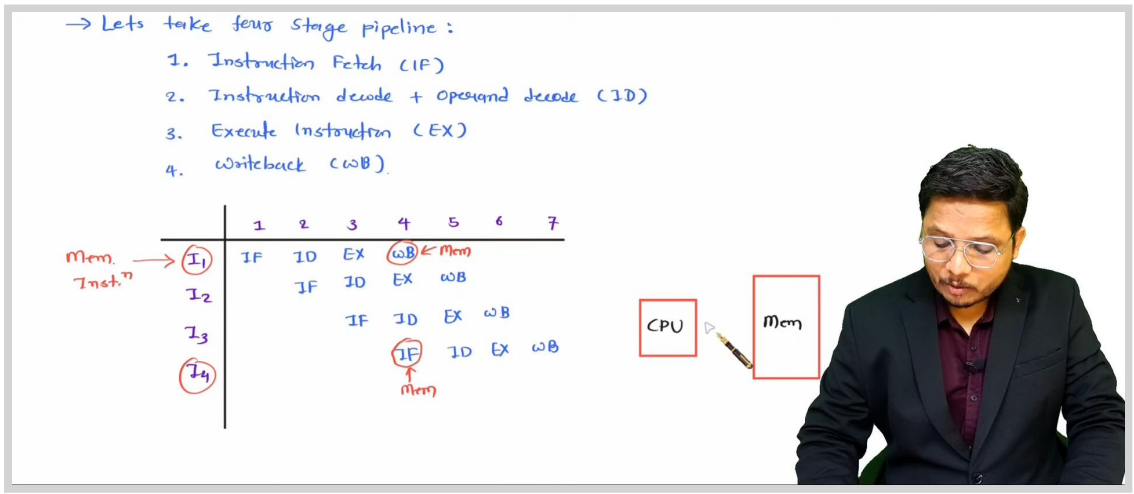
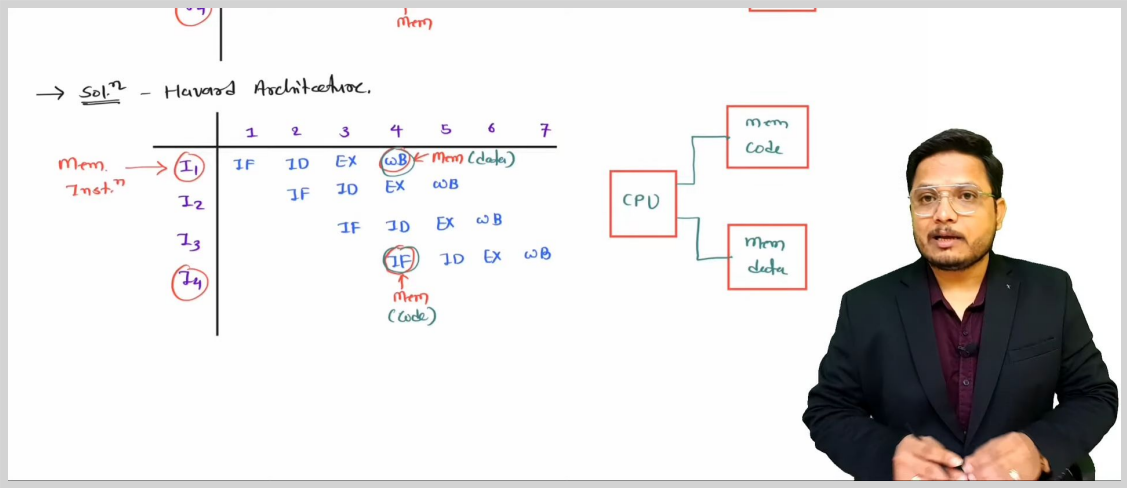


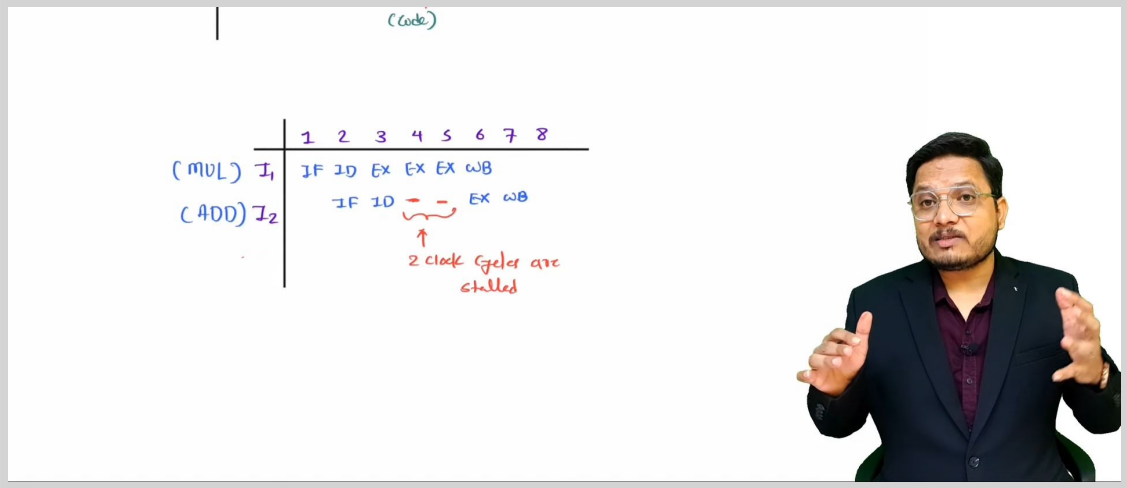
structural hazard basically means that we can't use the same resource agar ek fetch mei memory use kr rhi hai and ek write

back mei

05:14



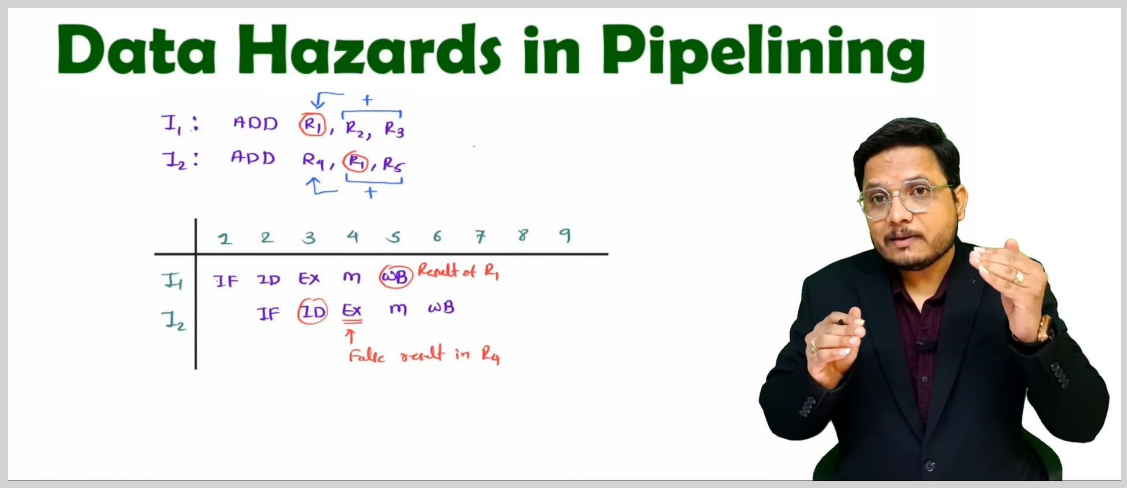
07:39



multiplication takes more time for execution as compared to addition so addition wali instruction have to wait for the multiplication to free up execution unit to proceed hence adding a stall

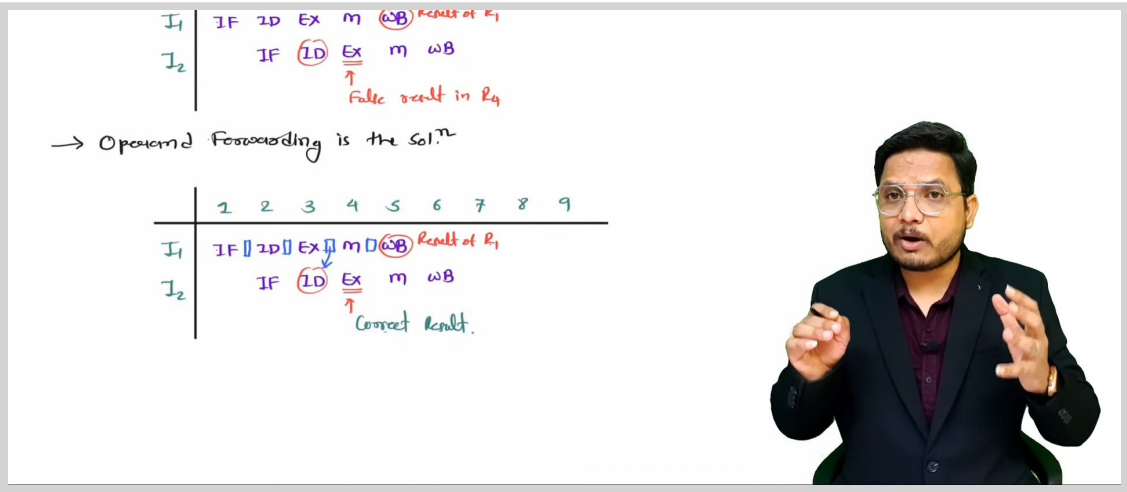
Data Hazard

03:31

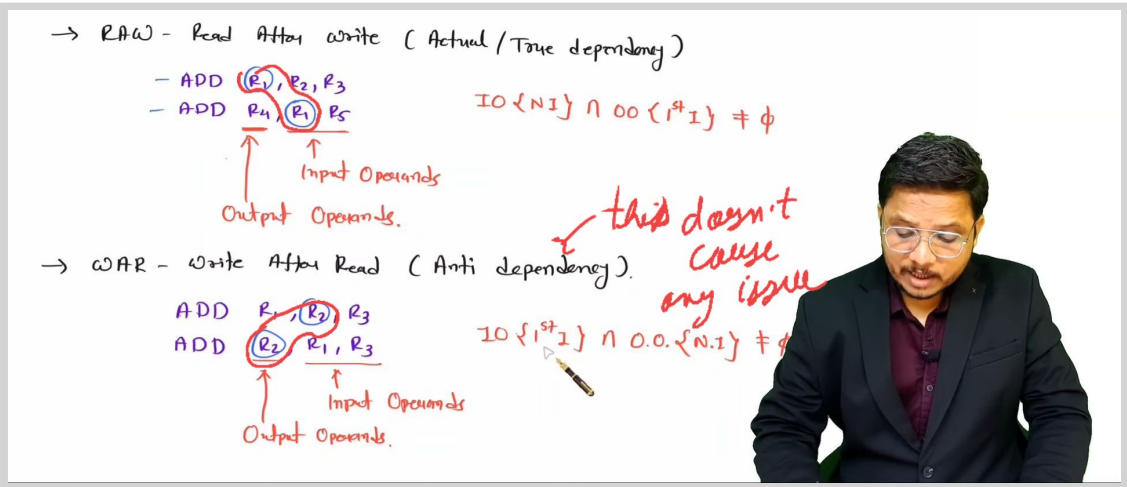


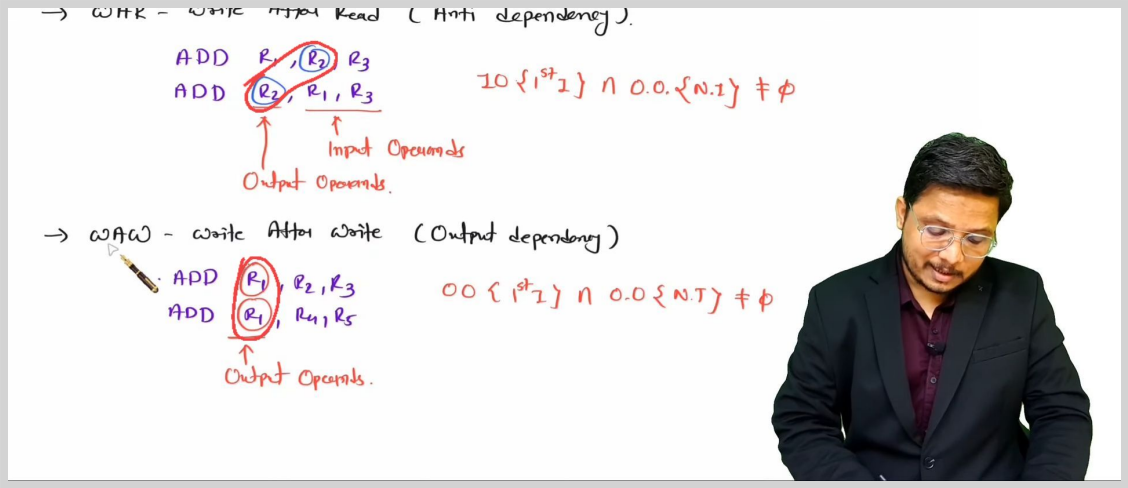
I2 decode stage will take the not updated value of R1 and create false result

[06:23](#)



basically buffer register is used to fetch the value in operator forwarding instead of the actual memory location





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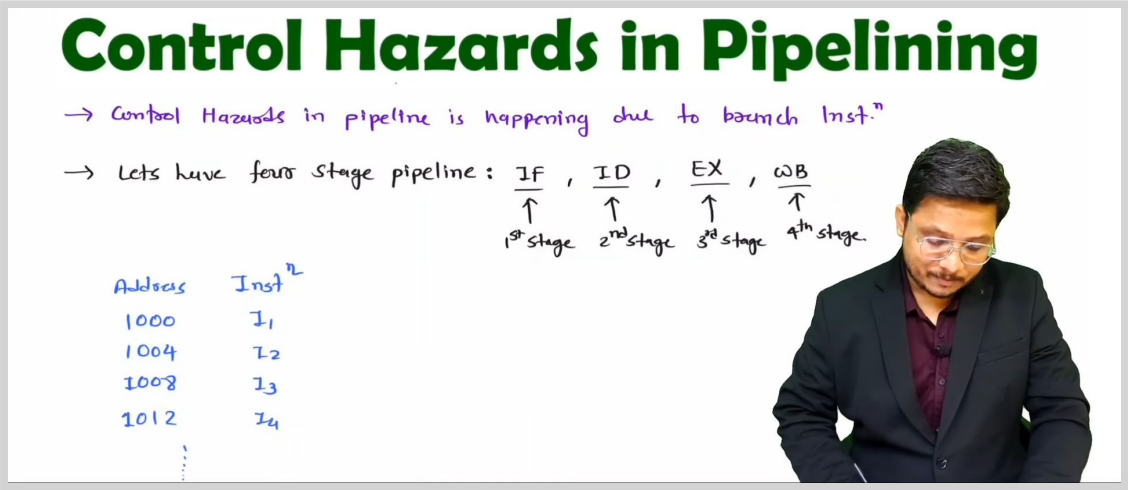
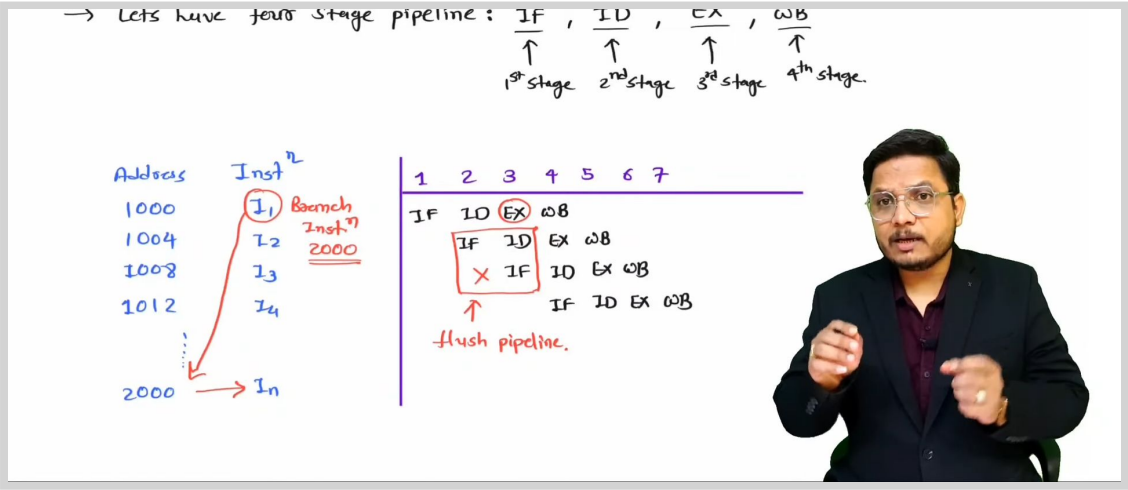
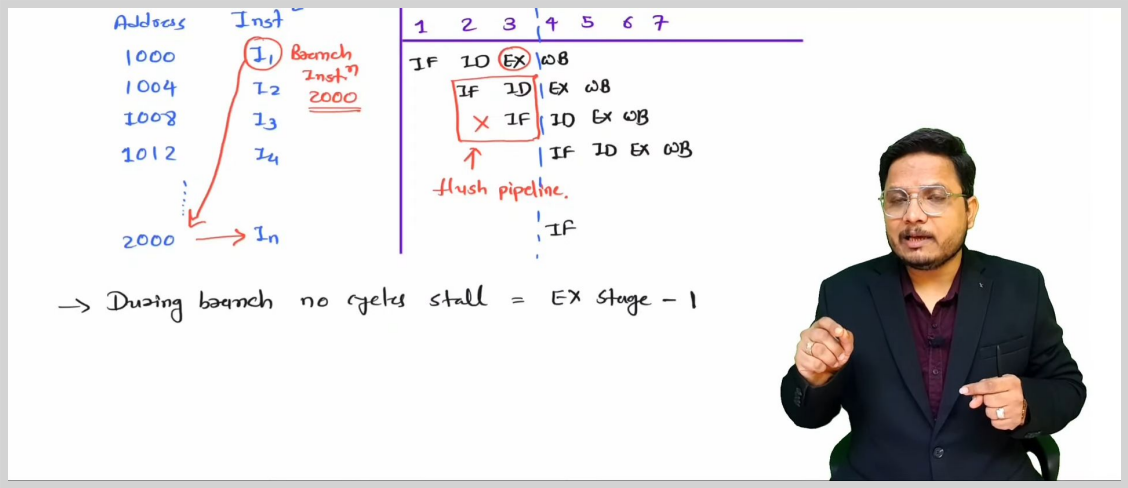


[04:40](#)



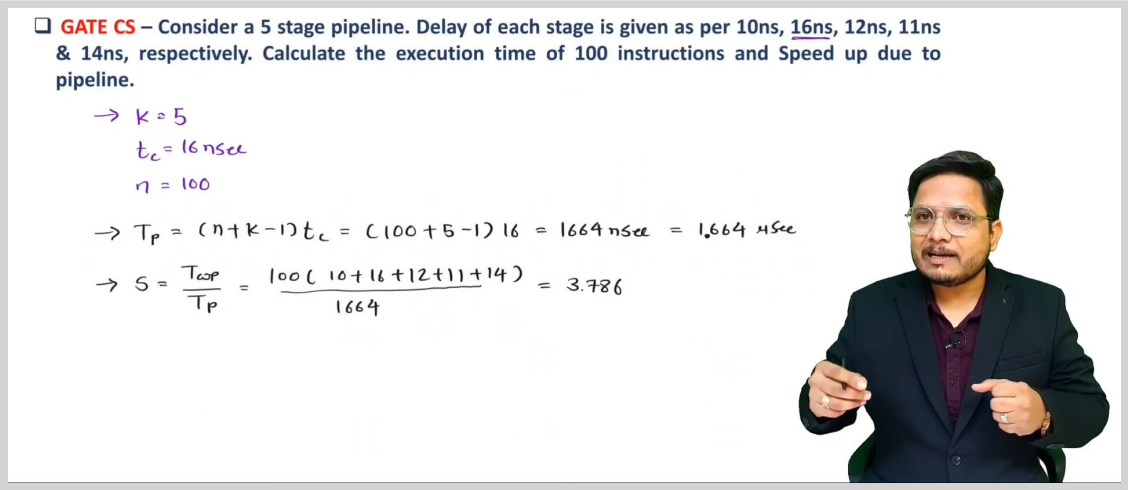
during branch instruction we get to know where to jump (that is the address of jump location) during execution stage

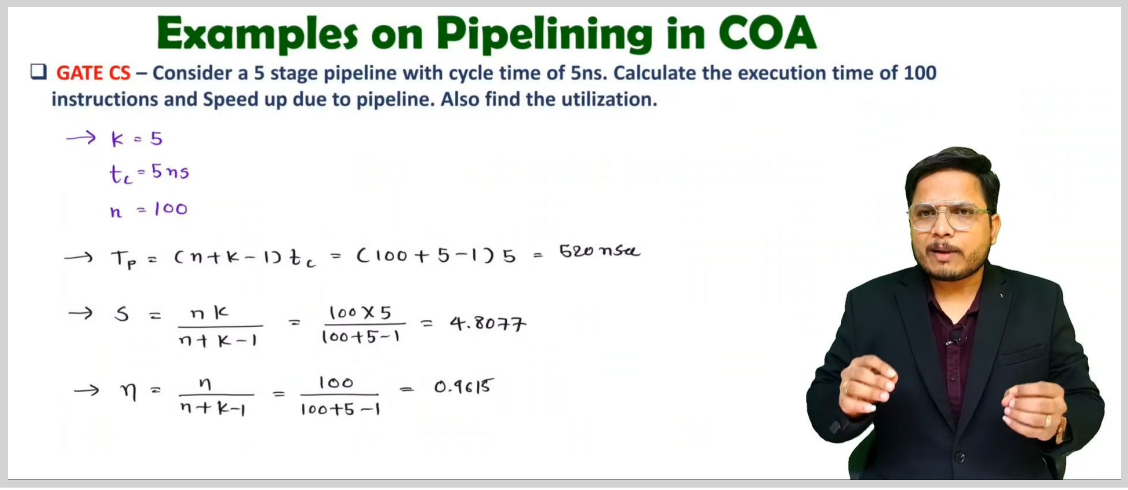
[07:40](#)


Address
Inst
1000
1004
1008
1012
2000
Branch Inst.ⁿ
2000
1 2 3 4 5 6 7
IF ID EX WB
IF ID EX WB
IF ID EX WB
IF ID EX WB
IF
flush pipeline.
→ During branch no cycles stall = EX stage − 1

[03:54]

[07:52]


GATE CS – Consider a 5 stage pipeline. Delay of each stage is given as per 10ns, 16ns, 12ns, 11ns & 14ns, respectively. Calculate the execution time of 100 instructions and Speed up due to pipeline.
→ k = 5
tc = 16 nsec
n = 100
→ Tp = (n+k−1)tc = (100+5−1)16 = 1664 nsec = 1.664 μsec
→ S = Tnop / Tp = 100(10+16+12+11+14) / 1664 = 3.786


Examples on Pipelining in COA
GATE CS – Consider a 5 stage pipeline with cycle time of 5ns. Calculate the execution time of 100 instructions and Speed up due to pipeline. Also find the utilization.
→ k = 5
tc = 5ns
n = 100
→ Tp = (n+k−1)tc = (100+5−1)5 = 520 nsec
→ S = nk/(n+k−1) = 100×5/(100+5−1) = 4.8077
→ η = n/(n+k−1) = 100/(100+5−1) = 0.9615

❑ **GATE 2011 CS** – Consider an instruction pipeline with four stages (S1, S2, S3 & S4) each with combinational circuit only. The pipeline registers are required between each stage and at the end of the last stage. Delay for the stages and for the pipeline registers are as given in the figure.

❑ What is the approximate speed up of the pipeline in steady state under ideal conditions w
compared to the corresponding non pipeline implementation?

$$S = \frac{T_{wp}}{T_p} = \frac{[5+6+11+8]}{[11+1]} = 2.5$$

[01:53](#)

Examples on Pipelining in COA

❑ **GATE CS** – Consider a pipeline having 5 stages with duration 10ns, 30ns, 45ns, 80ns and 35ns. If the buffer delay is 20ns, calculate the speed up of pipelined processor.

$$S = \frac{T_{wp}}{T_p} = \frac{[10+30+45+80+35]}{[80+20]}$$

[05:50](#)

❑ **GATE CS** – Assume we have two pipelines P1 and P2, respectively. P1 has 6 stages, having execution time of 12ns, 14ns, 19ns, 20ns, 22ns and 25ns. P2 has 4 stages each having execution time of 10ns. Calculate the time that can be saved while using P2 pipeline over P1 pipeline, If 2000 instructions are executed.

→ P_1, $K_1 = 6$, $t_{c_1} = 25$ nsec
→ P_2, $K_2 = 4$, $t_{c_2} = 10$ nsec
→ $n = 2000$
→ $T_{P_1} = (n + K_1 - 1)\, t_{c_1} = (2000 + 6 - 1)\, 25 = 50125$ nsec
→ $T_{P_2} = (n + K_2 - 1)\, t_{c_2} = (2000 + 4 - 1)\, 10 = 20030$ nsec
→ $\Delta T = T_{P_1} - T_{P_2} = 50125 - 20030 = 30095$ nsec

[07:53](#)

❑ **GATE CS – Assume a pipeline P which operates at 3GHz clock rate. It has a speed up factor of 10 and efficiency of 40%. Calculate the number of stages in the above pipeline.**

→ $f_{clock} = 3\,GHz$

$S = 10$

$\eta = 40\% = 0.4$

→ $S = k\eta \Rightarrow k = \frac{10}{0.4} = 25$

03:21

Examples on Pipelining in COA

❑ **GATE 2015 CS – Consider a non pipelined processor with a clock rate of 2.5GHz and average cycles per instruction of four. The same processor is upgraded to a pipelined processor with five stages; but due to internal pipeline delay, the clock speed is reduced to 2GHz. Assume that there are no stalls in the pipeline. The speed up achieved in this pipelined processor is .....**

→ $f_{c_1} = 2.5\,GHz$, $CPI = 4$

→ $k = 5$, $f_{c_2} = 2\,GHz$

→ $S = \frac{T_{nP}}{T_P} = \frac{4/2.5\times10^{9}}{1/2\times10^{9}} = \frac{8}{2.5} = 3.2$

10:14

❑ **GATE CS – The stage delays in a 4 stage pipeline are 5ns, 6ns, 4ns and 5ns. The second stage is replaced with a functionally equivalent design involving two stages with respective delays 4ns and 5ns. The throughput increase of the pipeline is ....20..... %**

→ P-1 {5ns, 6ns, 4ns, 5ns} → P-2 {5ns, 4ns, 5ns, 4ns, 5ns}.

→ Throughput $= \frac{\eta}{(n+k-1)t_c} = \frac{1}{t_c}$ ← Ideally.

→ $t_{c_1} = 6ns$, $t_{c_2} = 5ns$

→ $TP_1 = \frac{1}{t_{c_1}} = \frac{1}{6ns}$

→ $TP_2 = \frac{1}{t_{c_2}} = \frac{1}{5ns}$.

→ $\%\uparrow_a = \frac{TP_2 - TP_1}{TP_1} \times 100$

$= \frac{1/5 - 1/6}{1/6} \times 100$

$= \frac{6}{5} - 1 = 0.2 \times 100 = 20\%$

12:26

❑ **GATE 2004 CS** – A 4 stage pipeline has the stage delays as 150, 120, 160 and 140 nanoseconds, respectively. Registers that are used between the stages have a delay of 5 ns each. Assuming constant clock rate, the total time taken to process 1000 data items on this pipeline will be ..... Microseconds

$n = 1000$
$k = 4$
$t_c = 160 + 5 = 165$ nsec

$\rightarrow T_p = (n+k-1)t_c$
$= (1000+4-1)165$
$= 165995$ nsec
$= 165995$ usec

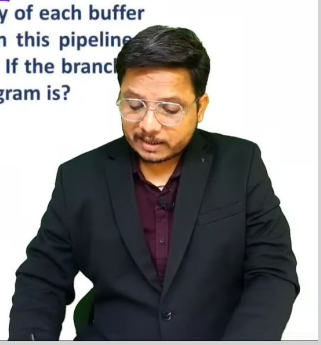
[05:53](#)

Examples on Pipelining in COA

❑ **GATE 2009 CS** – Consider an instruction pipeline with five stages without any branch prediction: Fetch Instruction (FI), Decode Instruction (DI), Fetch Operand (FO), Execute Instruction (EI) and Write Operand (WO). The stage delay for FI, DI, FO, EI and WO are 5ns, 7ns, 10ns, 8ns and 6ns, respectively. There are intermediate storage buffer after each stage and the delay of each buffer is 1ns. A program consisting of 12 instructions I1, I2, I3, ... , I12 is executed in this pipelined processor. Instruction I4 is only the branch instruction and its branch target is I9. If the branch is taken during the execution of this program, the time needed to complete the program is?

- $\frac{I_1, I_2, I_3, I_4, I_9, I_{10}, I_{11}, I_{12}}{n = 8}$
- FI, DI, FO, EI, WO
  ↑ 4th Stage.
- No of stalled cycles = 4 − 1 = 3

- $T_p = t_p + t_s$
  $= (n+k-1)t_c + x t_c$
  $= (8+5-1)11 + 3\times 11$
  $=$



[10:01](#)

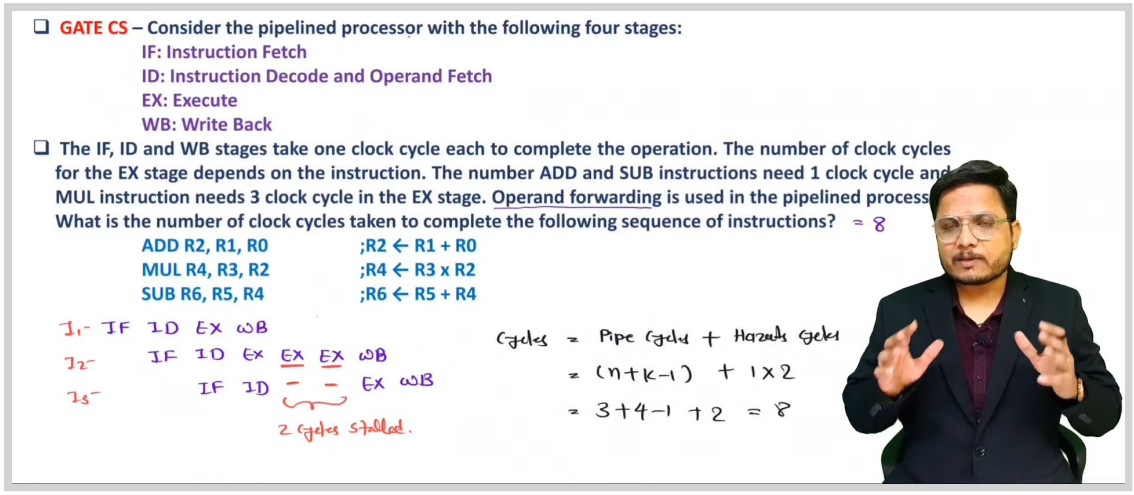
❑ **GATE CS** – Consider the pipelined processor with the following four stages:
IF: Instruction Fetch
ID: Instruction Decode and Operand Fetch
EX: Execute
WB: Write Back

❑ The IF, ID and WB stages take one clock cycle each to complete the operation. The number of clock cycles for the EX stage depends on the instruction. The number ADD and SUB instructions need 1 clock cycle and MUL instruction needs 3 clock cycle in the EX stage. Operand forwarding is used in the pipelined processor. What is the number of clock cycles taken to complete the following sequence of instructions? = 8

```
ADD R2, R1, R0      ;R2 ← R1 + R0
MUL R4, R3, R2      ;R4 ← R3 x R2
SUB R6, R5, R4      ;R6 ← R5 + R4
```

I_1- IF ID EX WB
I_2- IF ID EX EX EX WB
I_3- IF ID – – EX WB
2 cycles stalled.

[11:18](#)



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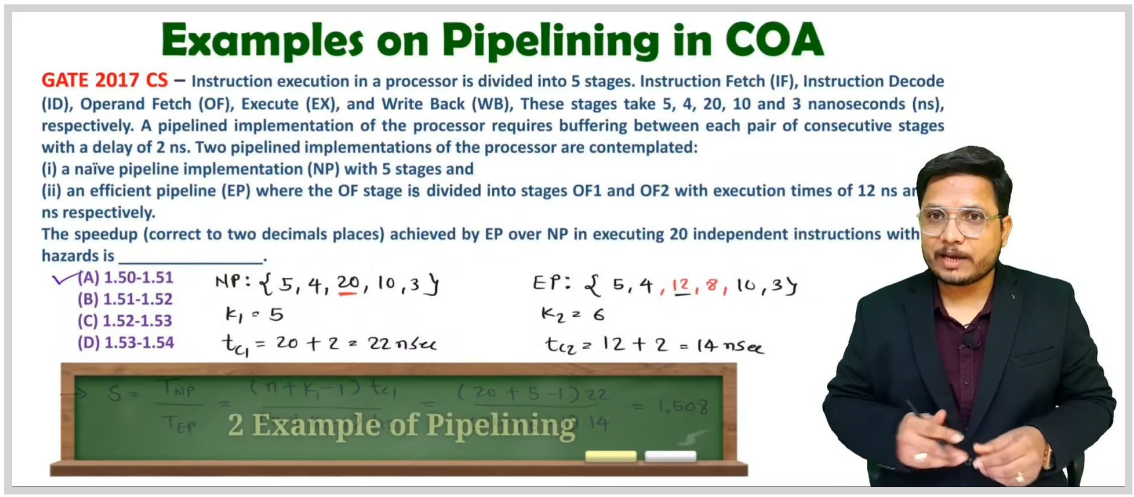

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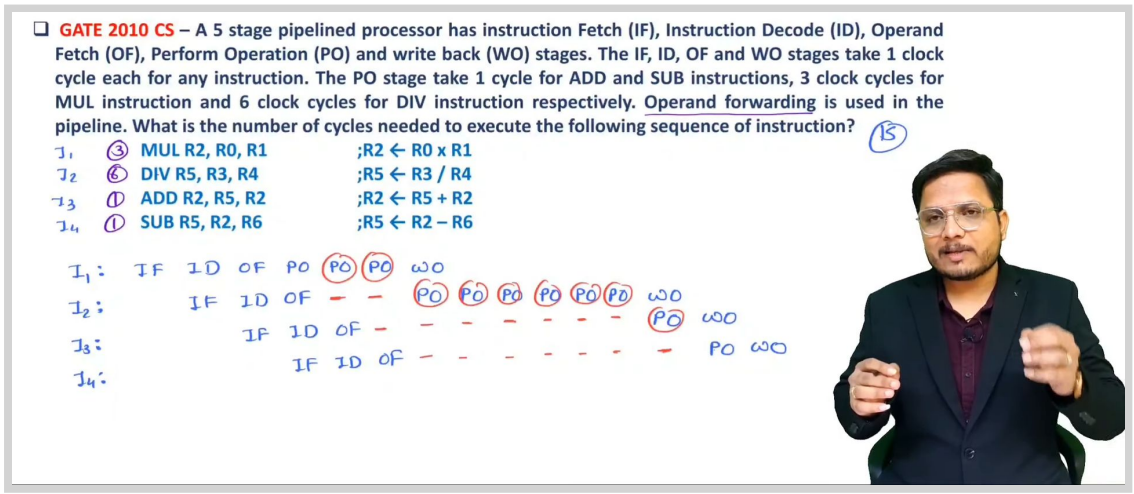
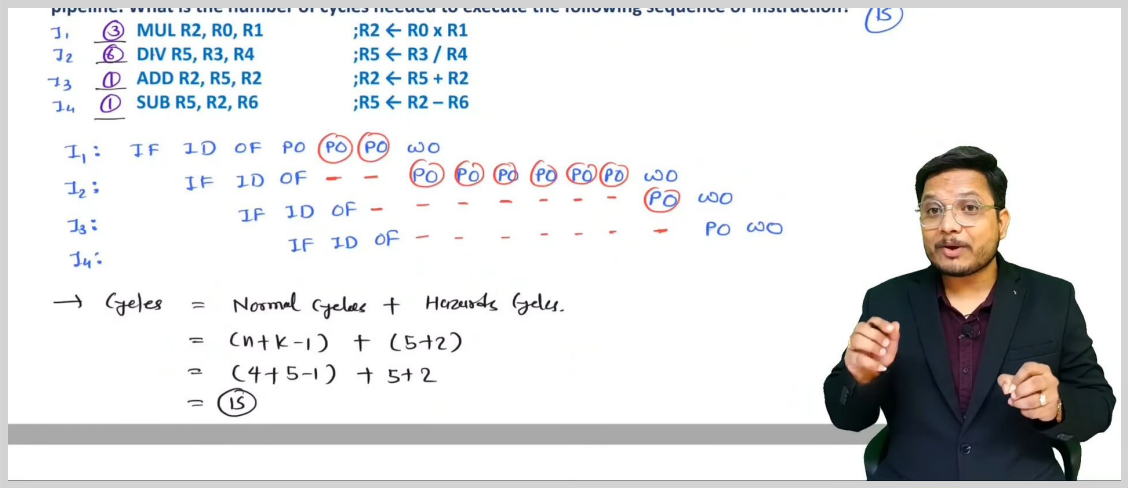
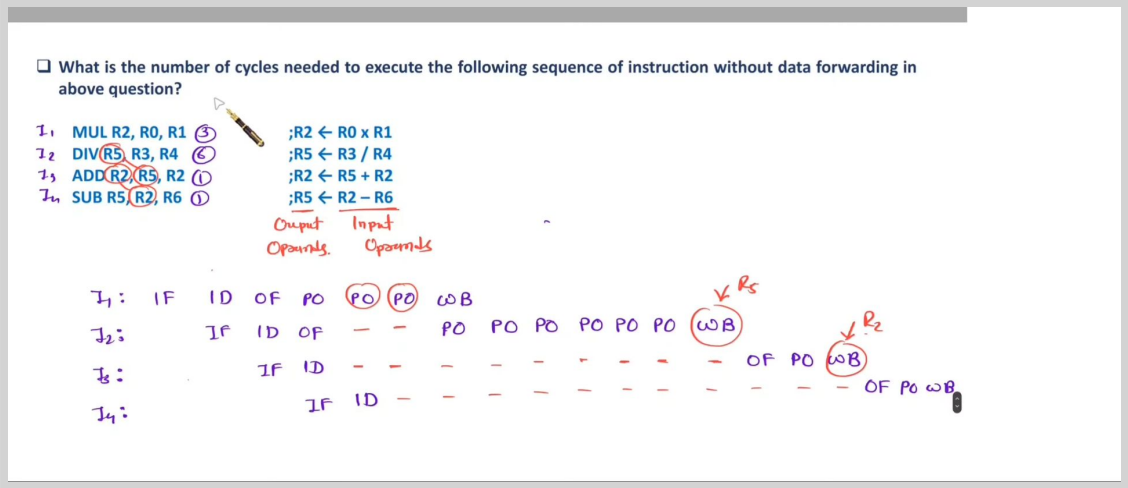


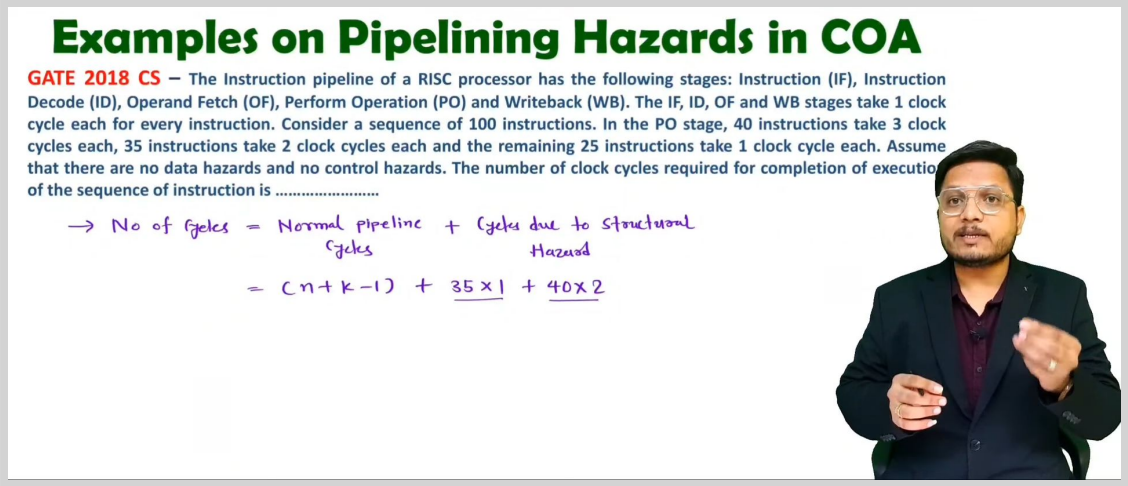
[11:12](#)



16:35



03:38



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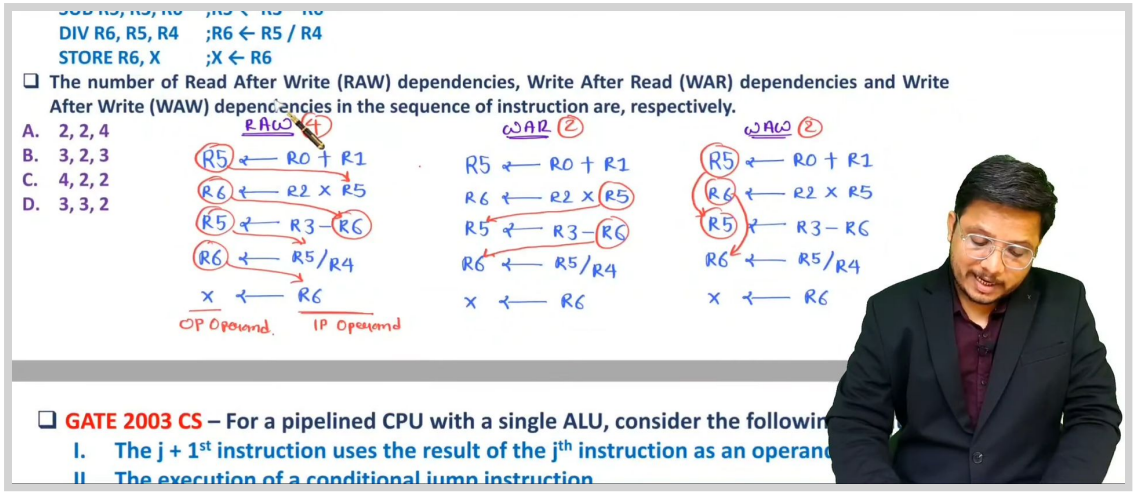
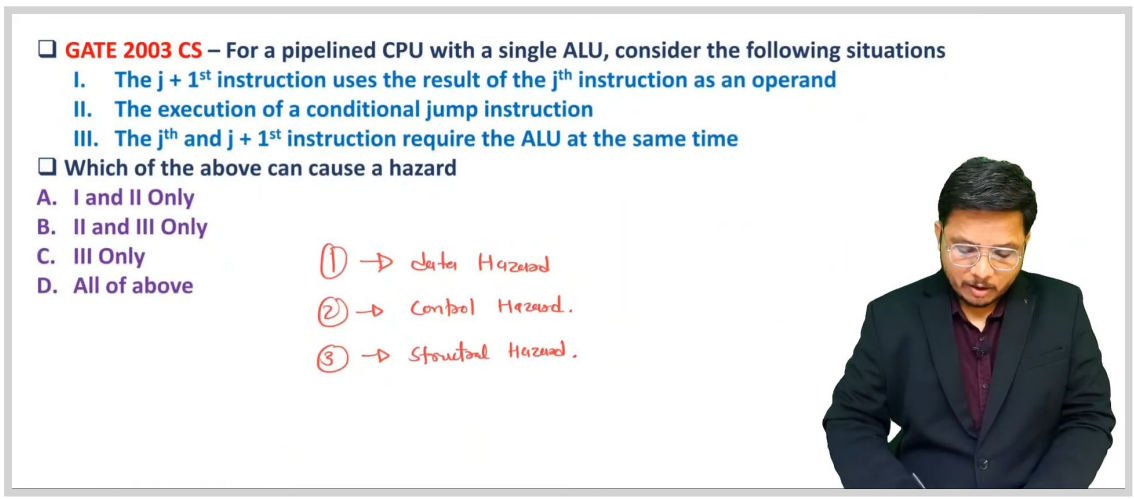
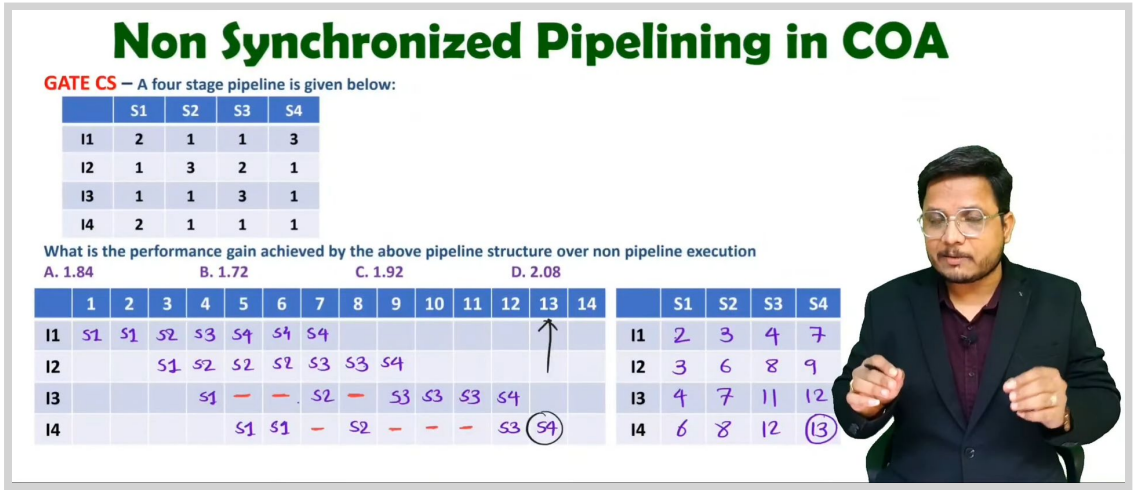

DIV R6, R5, R4 ;R6 ← R5 / R4
STORE R6, X ;X ← R6
The number of Read After Write (RAW) dependencies, Write After Read (WAR) dependencies and Write After Write (WAW) dependencies in the sequence of instruction are, respectively.
A. 2, 2, 4
B. 3, 2, 3
C. 4, 2, 2
D. 3, 3, 2
RAW 4
R5 ← R0 + R1
R6 ← R2 x R5
R5 ← R3 − R6
R6 ← R5/R4
X ← R6
OP Operand
IP Operand
WAR 2
WAW 2
GATE 2003 CS – For a pipelined CPU with a single ALU, consider the followin
I. The j + 1st instruction uses the result of the jth instruction as an operan

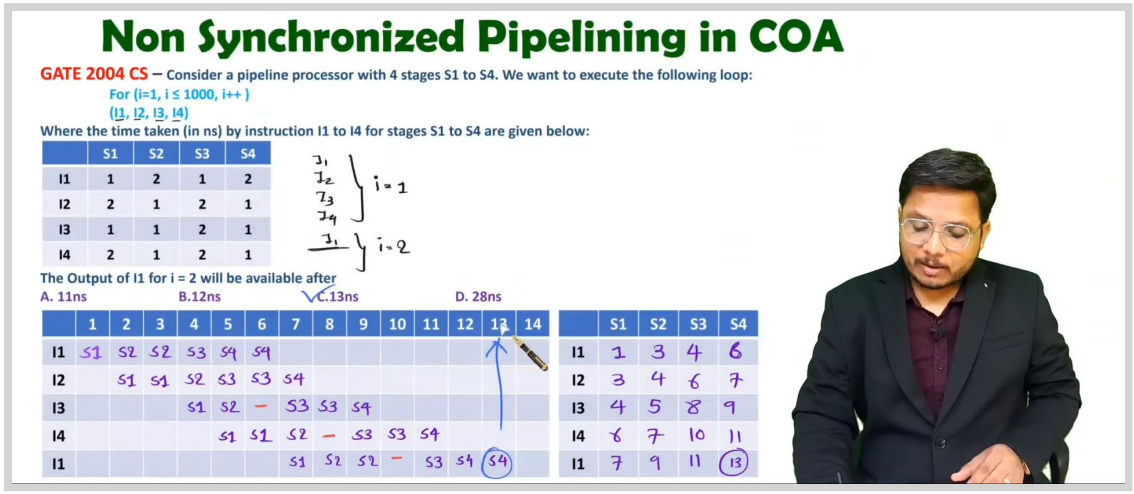
[12:08](#)


GATE 2003 CS – For a pipelined CPU with a single ALU, consider the following situations
I. The j + 1st instruction uses the result of the jth instruction as an operand
II. The execution of a conditional jump instruction
III. The jth and j + 1st instruction require the ALU at the same time
Which of the above can cause a hazard
A. I and II Only
B. II and III Only
C. III Only
D. All of above
1 → Data Hazard
2 → Control Hazard.
3 → Structural Hazard.

[08:30](#)


Non Synchronized Pipelining in COA
GATE CS – A four stage pipeline is given below:
What is the performance gain achieved by the above pipeline structure over non pipeline execution
A. 1.84
B. 1.72
C. 1.92
D. 2.08

09:14



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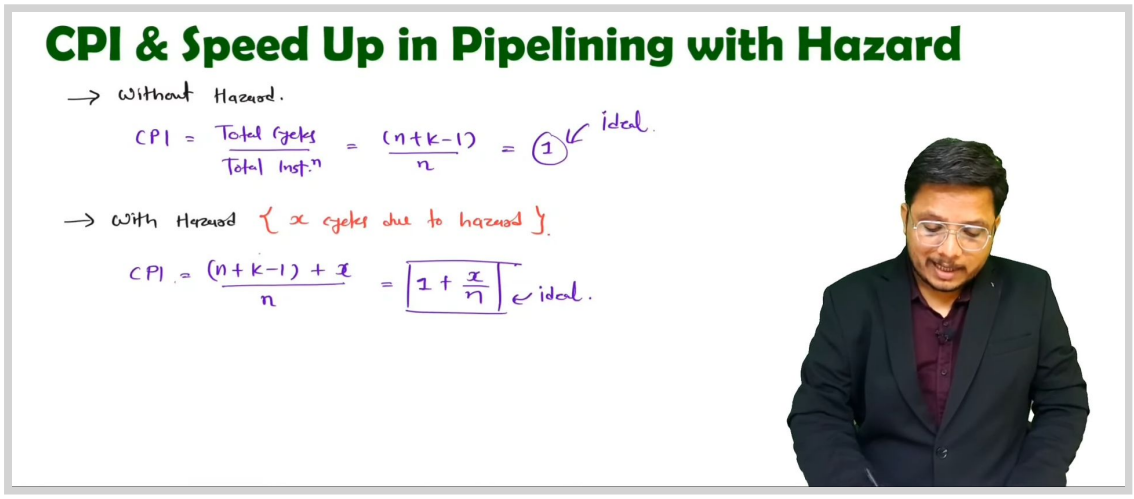

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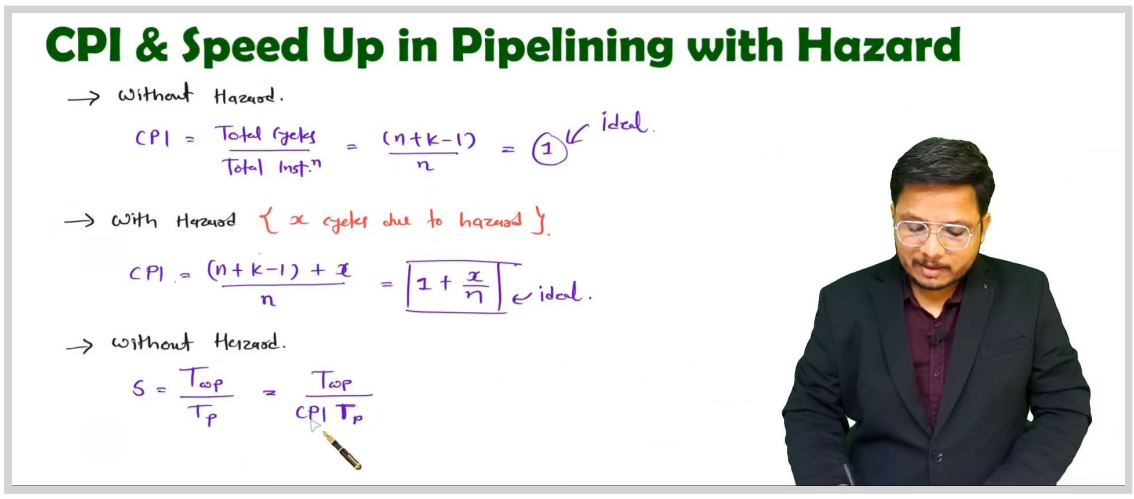

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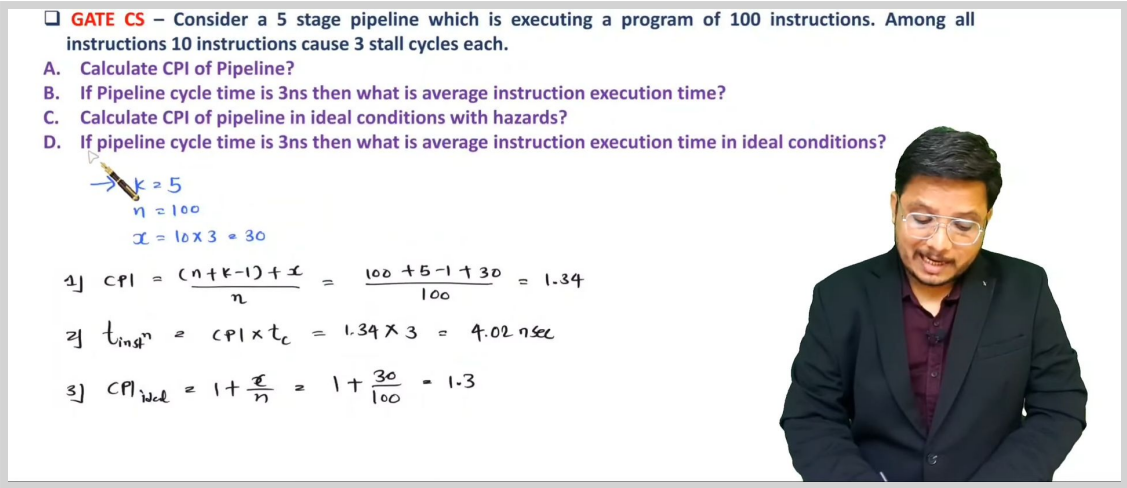

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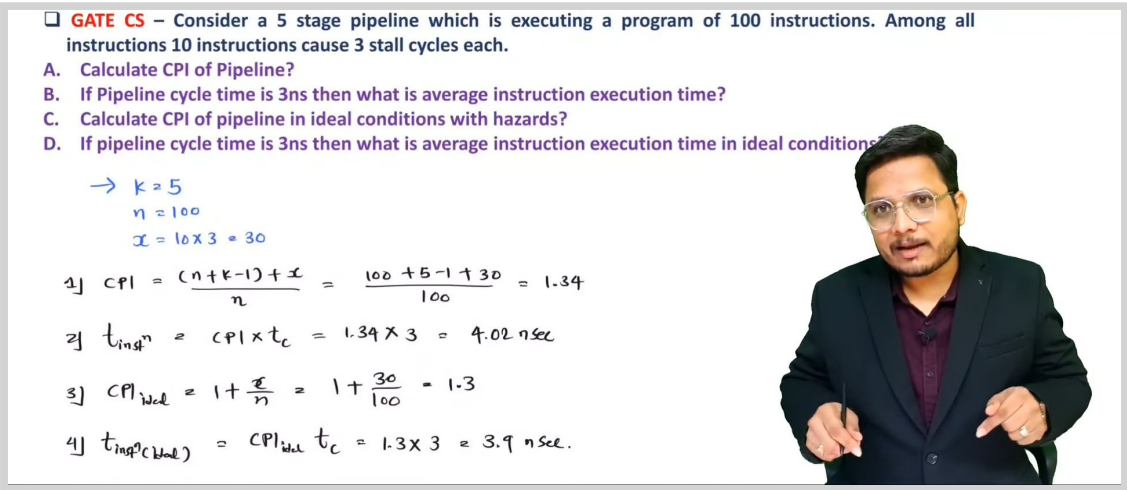
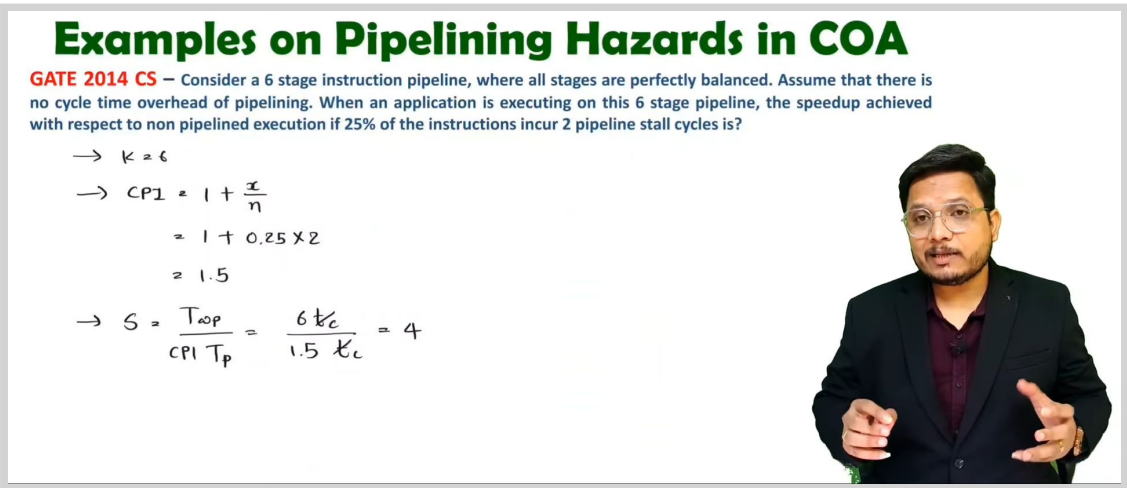


03:13



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