Superscalar Processor

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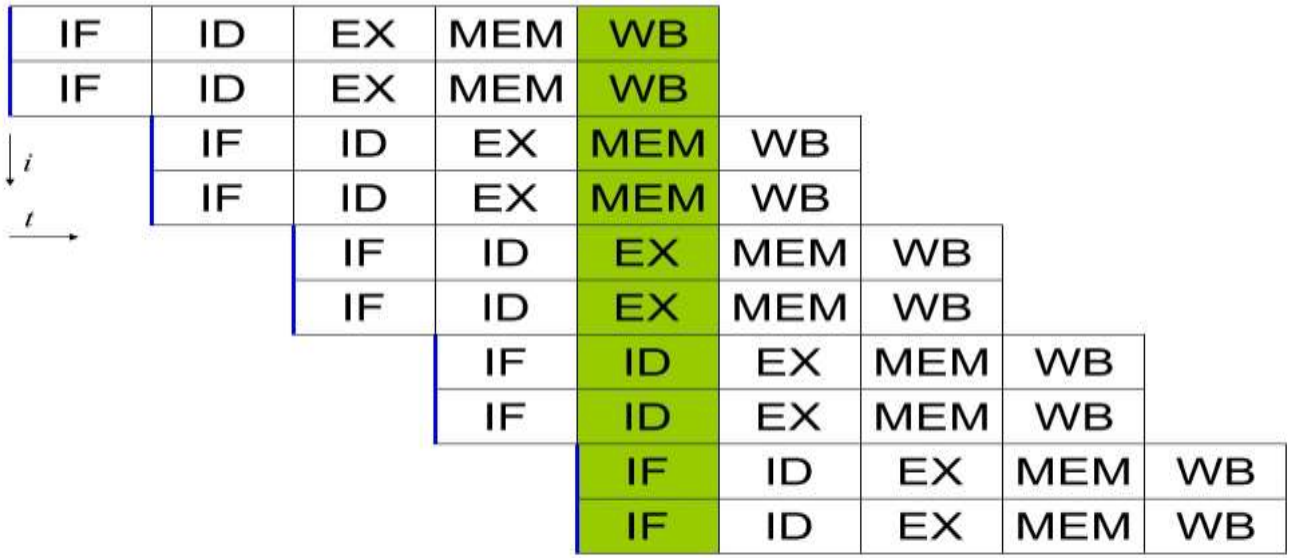
Supersalar processor

A superscalar processor is a CPU that implements a form of parallelism called instruction-level parallelism within a single processor.

Simple superscalar pipeline

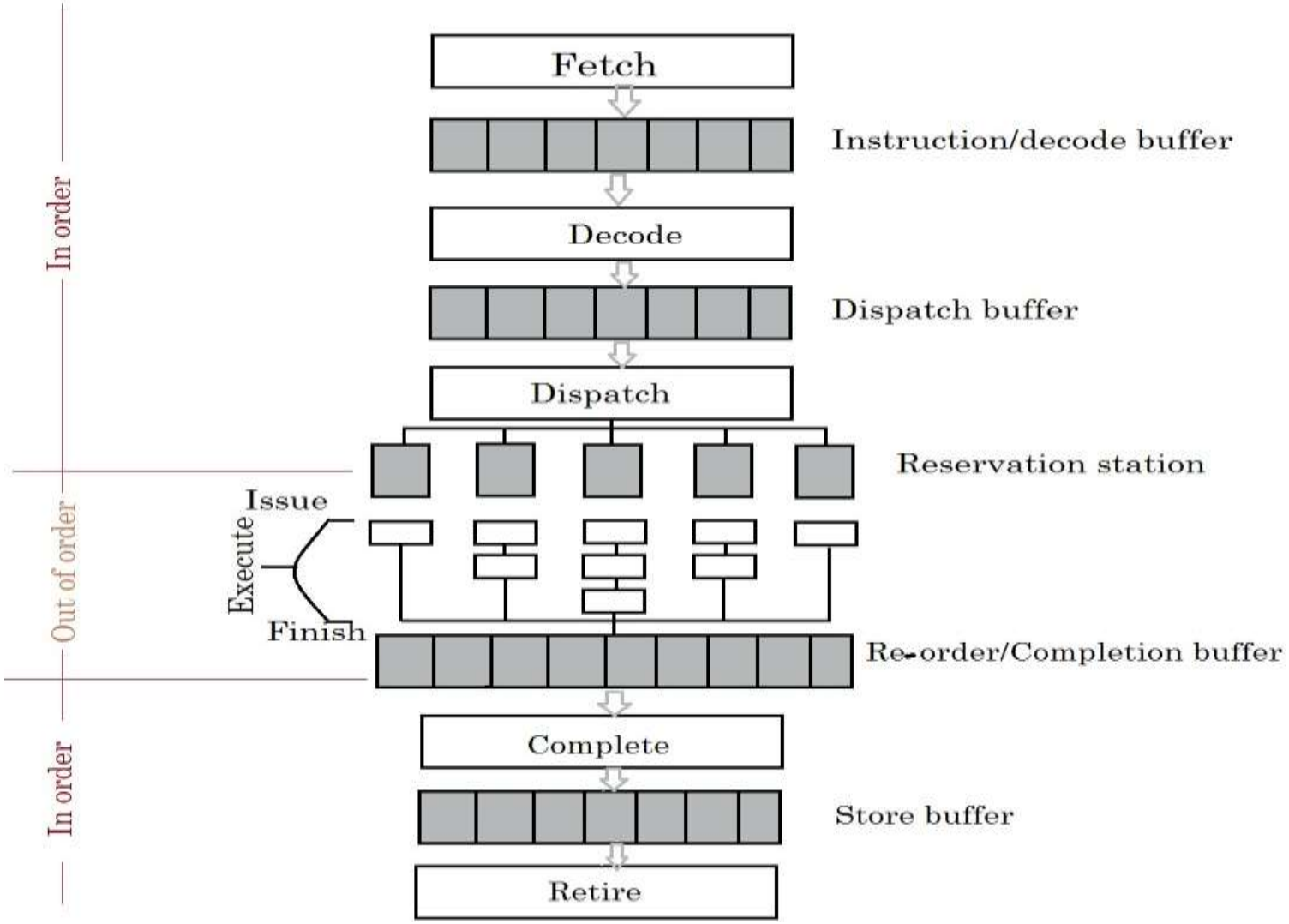


By fetching and dispatching two instructions at a time, a maximum of two instructions per cycle can be completed. (IF = Instruction Fetch, ID = Instruction Decode, EX = Execute, MEM = Memory access, WB = Register write back, i = Instruction number, t = Clock cycle [i.e., time])

Why superscalar?

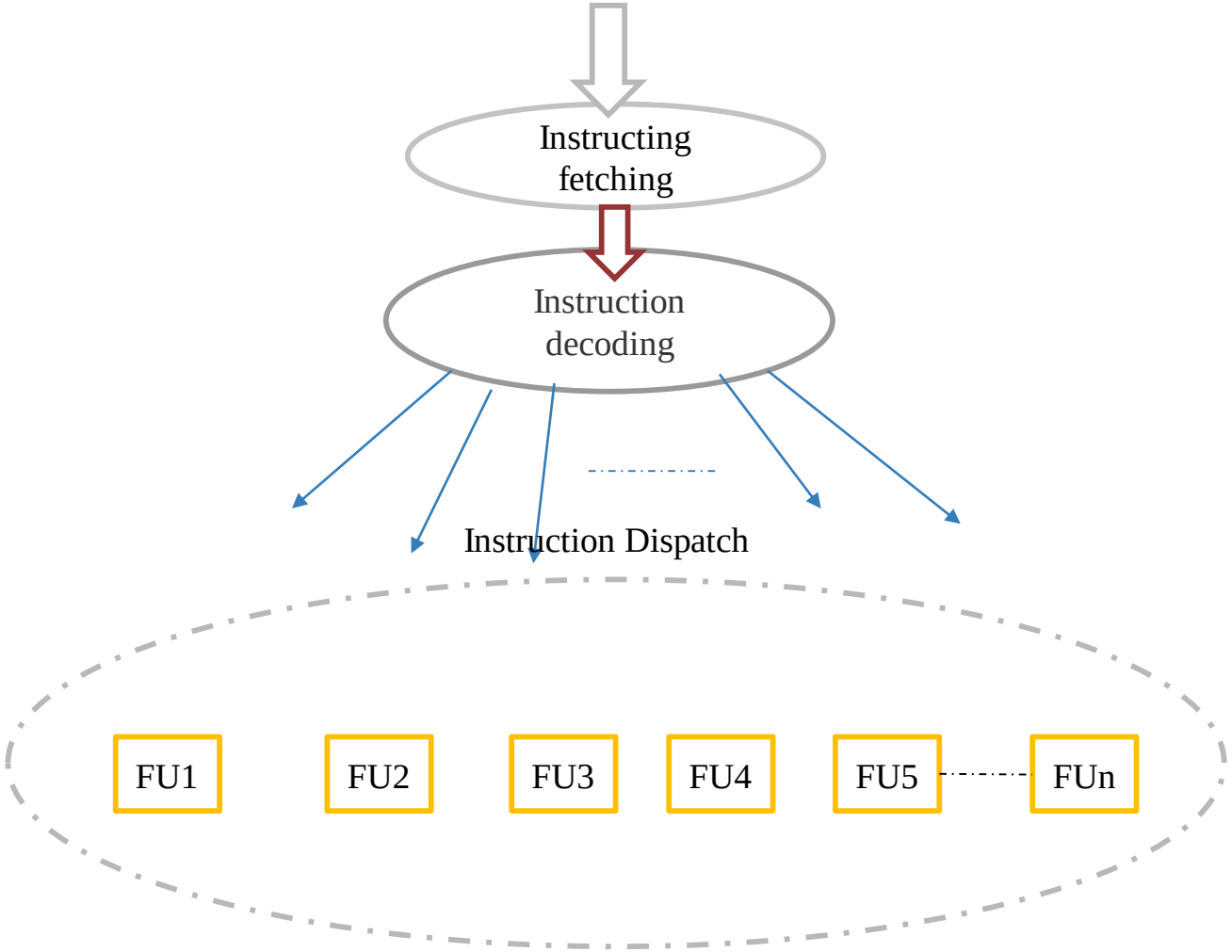
- Most operations are on scalar quantities
- Improve these operations to get an overall improvement
- Superscalar processor executes multiple independent instructions in parallel.

Superscalar Organization



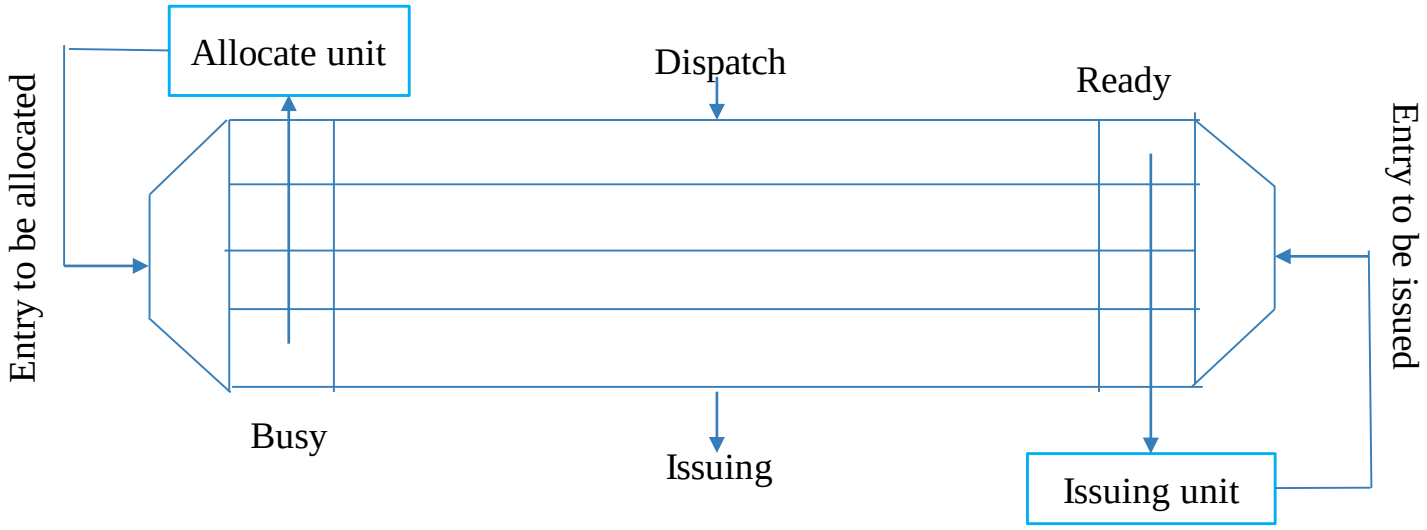
Instruction Dispatch

- Route decoded instructions to appropriate functional units



Reservation Station

- Reservation station decouple instruction decoding and instruction execution .
- Main task: *Dispatching* -- *Waiting* --*Issuing*



Reservation station

Reservation station: Centralised Vs Distributed

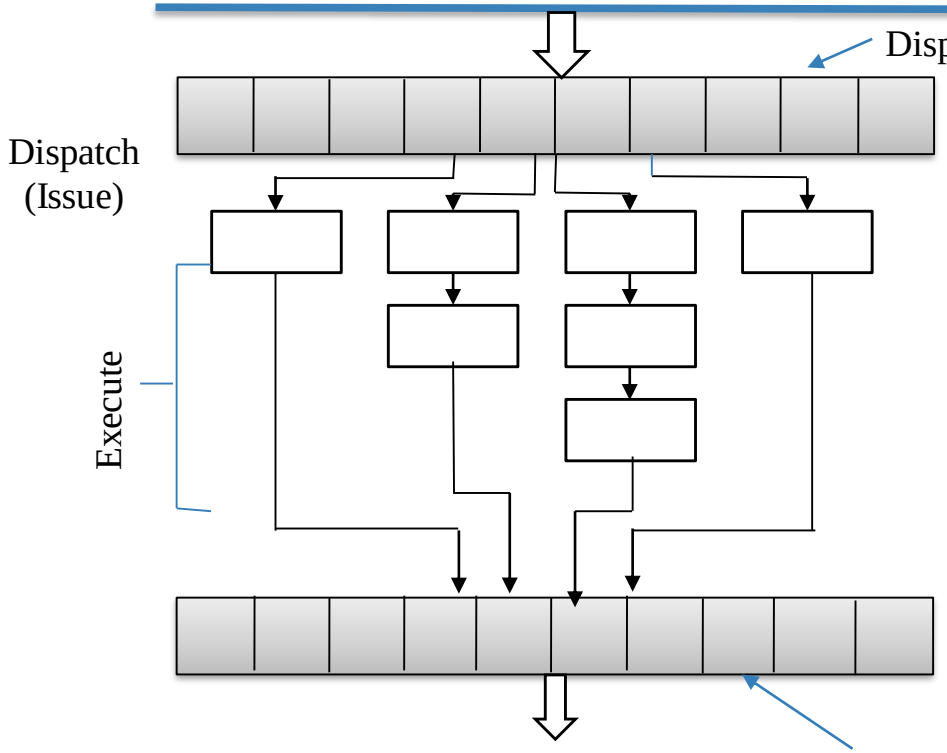


Fig: Centralize reservation station (Intel P6)

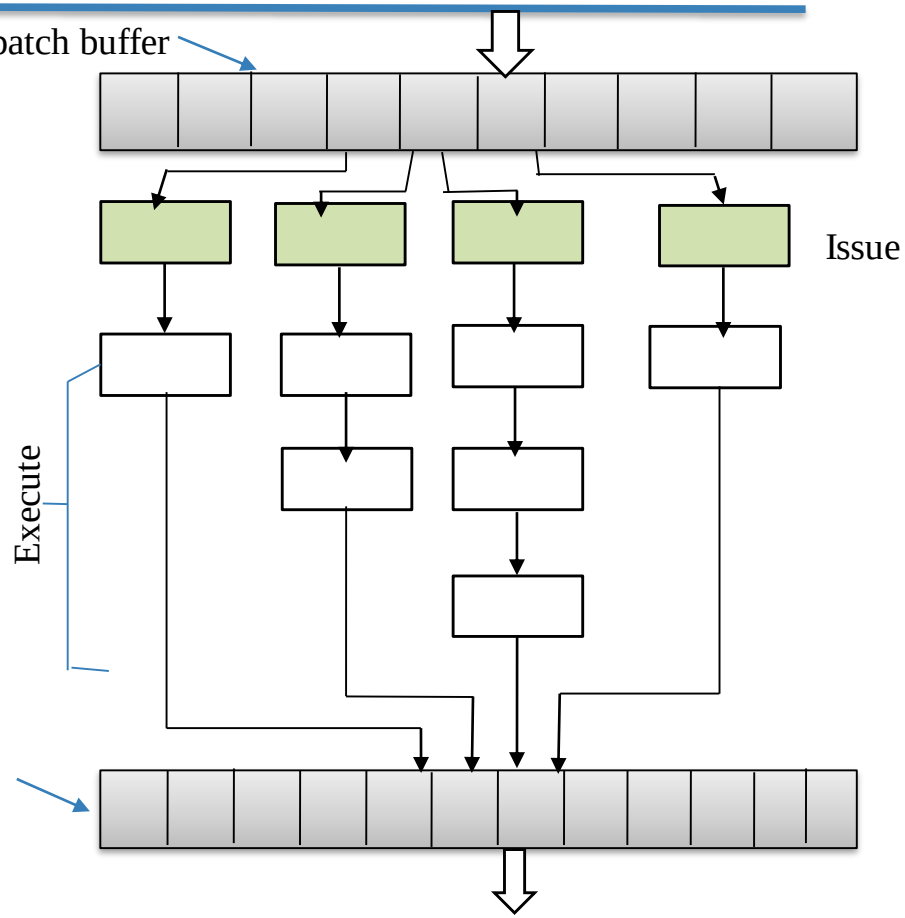


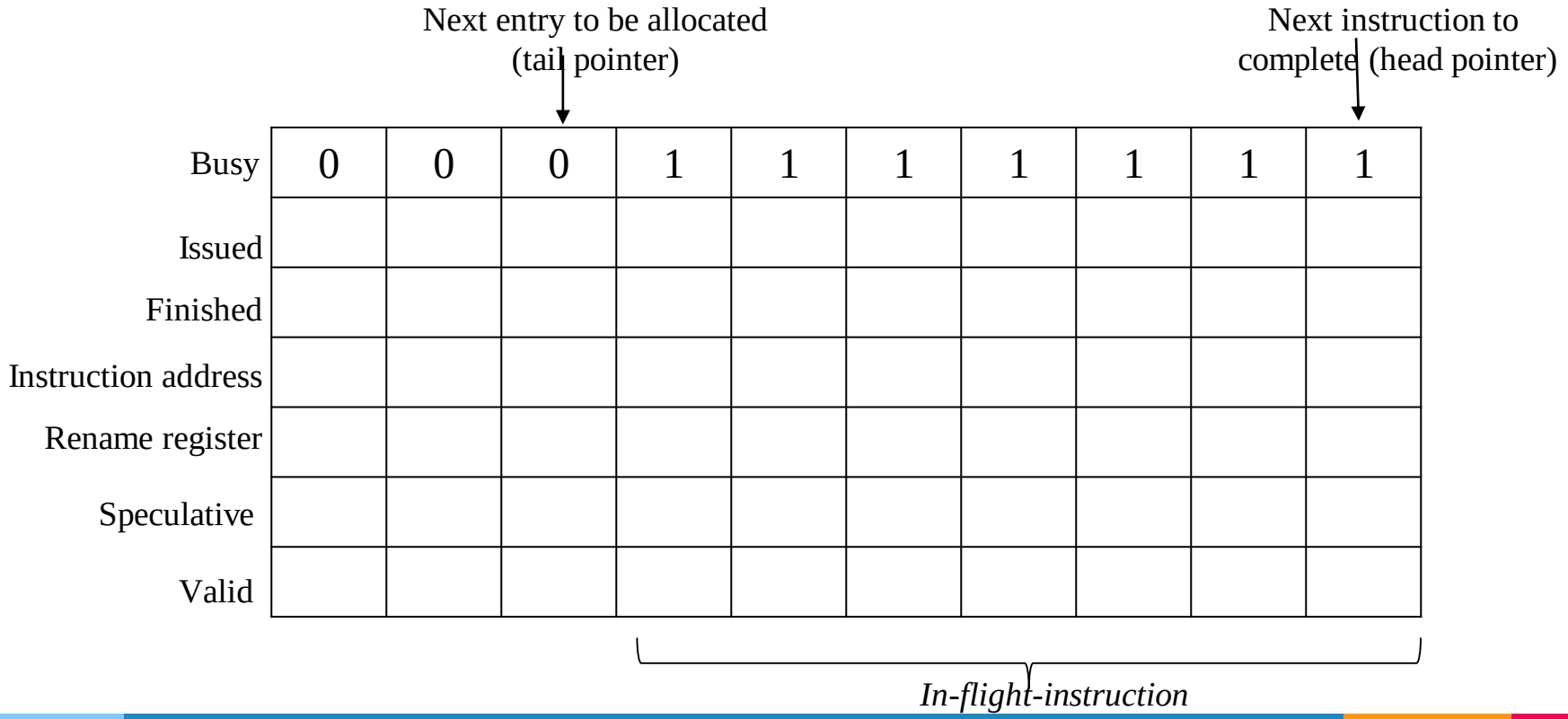
Fig: Distributed reservation station (Power PC 620)

Reorder Buffer

- Contain all *in–flight* instruction

  Includes instruction in RS + instruction executing in FUs + instruction which are finished execution but waiting to be completed in program order

- Only finished and non-speculative instructions can be completed



Instruction completion and Retire

- Completion – finish the execution and update the machine state
- Retire - update the memory
  - A store may complete by writing to store buffer, but it retire only when the data is written into the memory
- When an interrupt occurs, stop fetching new instructions and finish the execution of all-in-flight instructions
- When an exception occurs, the result of the completion may no longer be valid.

Limitation of superscalar processor

Instruction-fetch inefficiencies caused by both branch delays and instruction misalignment

- not worthwhile to explore highly- concurrent execution hardware, rather, it is more appropriate to explore economical execution hardware
- degree of intrinsic parallelism in the instruction stream (instructions requiring the same computational resources from the CPU)
- complexity and time cost of the dispatcher and associated dependency checking logic
- branch instruction processing.

References

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Thank you !