END SEMESTER EXAMINATION – APR - MAY 2022
B. TECH. – 6th Sem

Course Code: COCSC18, CACSC20 ✓	Course Title: High Performance Computing
Time: 3.0 Hours	Max. Marks: 40

Note: Attempt all the five questions. Missing data / information if any, may be suitably assumed & mentioned in the answer. All questions are of equal marks.

Q. No.	Question	Marks	CO
Q1	**Attempt any 2 parts of the following.**		
1a	Explain temporal and data parallelism with suitable example. In addition, consider the execution of an object code with $2 * 10^5$ instructions on a 400 Mhz processor. The program consists of four major types of instructions. The instruction mix and the number of cycles [CPI] needed for each instruction type are given below based on the result of a program trace experiment: **Instruction type / CPI / Instruction mix** Arithmetic and logic — 1 — 60% Load/store with cache hit — 2 — 18% Branch — 4 — 12% Memory reference with cache miss — 8 — 10% (a) Calculate the average CPI when the program is executed on a uniprocessor with the above trace results. (b) Calculate the corresponding MIPS rate based on the CPI obtained in part (a).	4	CO1
1b	Characterize the architectural operations of SIMD and MIMD computers. Distinguish between multiprocessors and multicomputers based on their structures, resource sharing, and interprocessor communications. Also, explain the differences among UMA, NUMA, COMA, and NORMA computers	4	CO1
1c	Compare the PRAM models with physical models of real parallel computers in each of the following categories: (a) Which PRAM variant can best model SIMD machines and how? (b) Repeat the question in part (a) for shared memory MIMD machines.	4	CO2
Q2	**Attempt any 2 parts of the following.**		
2a	Develop two algorithms for fast multiplication of two $n * n$ matrices with a system of p processors. where $1 <= p <= n^3/\log n$. Choose an appropriate PRAM machine model to prove that the matrix multiplication can be done in $T = O(n^3/p)$ time. (a) Prove that $T = O(n^2)$ if $p = n$. The corresponding algorithm must be shown (b) Show the parallel algorithm with $T = O(n)$ if $p = n^2$	4	CO2
2b	Write the pseudocode of adding all elements of an array using p=process in shared memory computer.	4	CO3

Q. No.	Question	Marks	CO
2c	Write the pseudocode for addition of an array using Single Program multiple data (SPMD) message passing model.	4	CO3
Q3	**Attempt any 2 parts of the following.**		
3a	Explain all types of delays in pipeline execution. Determine the time taken with and without pipelining during the loss of speedup due to resource non-availability. Further, use the following code fragment: Loop: LD R1,0(R2) load R1 from address 0+R2 DADDI R1, R1, #1 R1=R1+1 SD R1, 0, (R2) store R1 at address 0+R2 DADDI R2, R2, #4 R2=R2+4 DSUB R4, R3, R2 R4=R3-R2 BNEZ R4, Loop branch to Loop if R4!= 0 Data hazards are caused by data dependences in the code. Whether a dependency causes a hazard depends on the machine implementation (i.e., number of pipeline stages). List all of the data dependences in the code above. Record the register, source instruction, and destination instruction.	4	CO4
3b	Explain data flow steps while executing an instruction. In addition, draw consolidated data flow showing all the steps in instruction execution in detail?	4	CO4
3c	Explain the concept of delay, locking and out-of-order completion in detail using diagrams or examples. The following assembly code is to be executed in a three-stage pipelined processor with hazard detection and resolution in each stage. The stages are instruction fetch. operand fetch (one or more as required), and execution [including a write-back operation]. Explain all possible hazards in the execution of the code. Inc R0 /R0 ← (R0) + 1/ Mul ACC, R0 /ACC ← (ACC) × (R0)/ Store R1, ACC /R1 ← (ACC)/ Add ACC, R0 /ACC ← (ACC) + (R0)/ Store M,ACC /M ← (ACC)/	4	CO3
Q4	**Attempt any 2 parts of the following.**		
4a	Why does a cache read, write miss happen? Explain all the possible reasons for a single processor system? You have an L1 data cache, L2 cache, and main memory. The hit rates and hit times for each are: 50% hit rate, 2 cycle hit time to L1. 70% hit rate, 15 cycle hit time to L2. 100% hit rate, 200 cycle hit time to main memory. A) What fraction of accesses are serviced from L2? From main memory? B) What is the miss rate and miss time for the L2 cache? C) What is the miss rate and miss time for the L1 cache?	4	CO3
4b	Explain two major relaxed consistency models in detail. Describe what happens in the MESI protocol (bus traffic, state changes) if a processor experiences: 1. a local read miss, while another cache holds a copy. in exclusive state 2. a local read miss, while another cache has a copy in modified state 3. a local write hit, while the cacheline is in modified state 4. a local write hit, while the cacheline is in exclusive state 5. a local write hit, while the cacheline is in shared state in several caches	4	CO4
4c	Explain shared bus multiprocessor with write buffers in detail with the help of a diagram. Consider the following sequence of operations by two processors for a block that starts at address B. Determine the state of that block in the caches of both the processors after each	4	CO5

operation in the sequence for the MOESI protocol. Both caches are initially empty and all lines are in the I state. The table below is provided to help organize your answer.

No.	Operation	MOESI	
		P1	P2
1	P1 reads B		I
2	P1 writes B		I
3	P2 writes B		
4	P1 reads B		
5	P1 writes B		
6	P2 reads B		

Q5	Attempt any 2 parts of the following.		
5a	Explain the energy-efficient computing on many-core processor of Amdahl's law in detail. Assuming a program consists of 50% non-parallelizable code. A) Compute the speed-up when using 2 and 4 processors according to Amdahl's law. B) Now assume that the parallel work per processor is fixed. Compute the speed-up when using 2 and 4 processors according to Gustafson's law. C) Explain why both speed-up results are different.	4	CO4
5b	What is Gustafson's Law? Illustrate the speedup expression of Gustafson's law in detail. The analysis of a program has shown a speedup of 3 when running on 4 cores. What is the serial fraction according to Gustafson's law? In addition, the analysis of a program has shown a speedup of 3 when running on 4 cores. What is the serial fraction according to Amdahl's law (assuming best possible speedup)?	4	CO5
5c	Explain at least three hardware related, and software related factors that affect parallel program's performance in detail. Explain all the special cases of G(n) in detail?	4	CO5

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B. Tech. VIth Sem
END-SEMESTER EXAMINATION, May 2022

Course Code: Internet of Things
Course Title: COCSC20

Time: 3 Hours

Max. Marks: 50

Note: - **Attempt all the five questions. Missing data / information if any, may be suitably assumed & mentioned in the answer. Write as precise as possible, do not write unnecessarily.**

Q. No.	Question	Marks	CO
Q1	**Attempt any 2 parts of the following.**		
1a	Consumer is providing following different Analog values for encoding it into **Digital values.** Provide the solution using SAM approach. The signal for 5 bits registers with a full-scale range of 100 Volts. a) 14.5 V b) 74 V	5	2
1b	Define an embedded **system** in IoT device and provide the **functions** used to read analog and digital data from a sensor in Arduino.	5	1
1c	Provide the **difference** between IoT and IIoT. Explain various wireless communications boards available in Raspberry Pi.	5	1
Q2	**Attempt any 2 parts of the following.**		
2a	Delhi NCR pollution index is increasing day by day from Average to Severe; Prof NAO from NSUT want to update people every minute about change in Pollution Index to their subscribers. And you know Delhi-NCR population is around 10 million. Please help to clear his **doubts** regarding implementation of MQTT protocol with the following points: a) Who will be subscriber, who will be publisher and where the broker will be placed? b) Which QoS reliability will work fine with this case, explain? c) Is there any better solution then MQTT protocol for this use-case scenario, explain. d) What could be the formatting or allocation of Topic, so that subscriber can easily choose the nearest publisher.	5	2, 5
2b	Mention any **two** commonly used water **sensors** and their pin configuration	5	2
2c	Write **five major comparisons** in MQTT and CoAP web protocols. (Hint: Architecture, Size, QoS, Transport Protocol, port, methods).	5	2, 3
Q3	**Attempt any 2 parts of the following.**		
3a	How many **types of messages** are existing in CoAP protocol, **explain** each with diagrammatical representation?	5	3
3b	Explain the following abbreviations: a) ESC.	5	2, 3, 4

	b) 6LoWPAN			
	c) CoAP			
	d) LWT			
	e) PAN ID in ZIGBEE			
3c	Explain the requirement/working of **Fragmentations** over IEEE 802.15.4 standard using IPv6 with Example	5	3, 4	
Q4	**Attempt any 2 parts of the following.**			
4a	What are the **challenges** in IoT network which can be addresses using SDN and how?	5	4	
4b	Explain the **preliminary sensors** required to fly the drones in any flight controllers	5	4, 5	
4c	What are the security **issues** and possible **attacks** over IoT networks, explain in the bullet points?	5	5	
Q5	**Attempt any 2 parts of the following.**			
5a	How **blockchain** helps to make reliable IoT networks, explain with one case study.	5	4, 5	
5b	Write brief about **five** applications of Drones, where IoT can be applicable.	5	4	
5c	Explain the major components of 5G. What are the benefits for applying **5G technology** for IoT networks?	5	4	

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B.TECH- CSAI (6th SEMESTER)
END-SEMESTER EXAMINATION (MAY 2022)

Course Code: CACSC19
Course Title: AI Hardware and Tools Workshop

Time: 3 Hours

Max. Marks: 20

Note: - Attempt all the five questions. Missing data/ information if any, may be suitably assumed & mentioned in the answer.

Q. No.	Question	Marks	CO
Q1	**Attempt any 2 parts of the following.**		
1a	What do you understand by TinyML? What is difference between TinyML and ML? Discuss the challenges of low-power ML applications.	2	CO1
1b	What are the advantages of TinyML? Why microcontrollers for TinyML, not CPU? Explain with suitable example.	2	CO1
1c	Briefly explain a Capstone Project one can implement utilizing TinyML on a microcontroller.	2	CO5
Q2	**Attempt any 2 parts of the following.**		
2a	Explain the Statistical and Programming features of R Programming Language.	2	CO2
2b	What are the different data structures in R? What are the uses of the following R Packages- ggplot2, dplyr, dygraphs, leaflet?	2	CO2
2c	Briefly explain a Capstone Project one can develop utilizing R library on data visualization and analytics.	2	CO5
Q3	**Attempt any 2 parts of the following.**		
3a	What is Data Visualization? Why is it important in business? What are its advantages?	2	CO2
3b	What is Power BI ? How Power BI helps in providing an effective solution for businesses?	2	CO3
3c	Briefly explain a Capstone Project one can develop using Power BI for data visualization and analytics.	2	CO5

Q4	Attempt any 2 parts of the following.		
4a	How is distributed database processed using AI? How can you achieve machine learning in Spark?	2	CO4
4b	Which tools Spark's Machine Learning library (MLlib) provide? Highlight their basic features/uses.	2	CO4
4c	Briefly explain a Capstone Project one can develop using Apache Spark on distributed databases.	2	CO5
Q5	Attempt any 2 parts of the following.		
5a	What is DevOps lifecycle? Explain how the DevOps lifecycle works at every stage with an illustrated infinite loop diagram with the related tools.	2	CO5
5b	What are the benefits and challenges of DevOps?	2	CO5
5c	Explain a Capstone Project one can develop using an Open Source framework focused on DevOps for AI deployment.	2	CO5

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B.TECH- MAC (6th SEMESTER)
END-SEMESTER EXAMINATION (MAY 2022)

Course Code: CMCSC19
Course Title: Computing Tools Workshop

Time: 3 Hours

Max. Marks: 20

Note: - Attempt all the five questions. Missing data/ information if any, may be suitably assumed & mentioned in the answer.

Q. No.	Question	Marks	CO
Q1	Attempt any 2 parts of the following.		
1a	What do you understand by TinyML? What is difference between TinyML and ML? Discuss the challenges of low-power ML applications.	2	CO1
1b	What are the advantages of TinyML? Why microcontrollers for TinyML, not CPU? Explain with suitable example.	2	CO1
1c	Briefly explain a Capstone Project one can implement utilizing TinyML on a microcontroller.	2	CO5
Q2	Attempt any 2 parts of the following.		
2a	Explain the Statistical and Programming features of R Programming Language.	2	CO2
2b	What are the different data structures in R? What are the uses of the following R Packages- ggplot2, dplyr, dygraphs, leaflet?	2	CO2
2c	Briefly explain a Capstone Project one can develop utilizing R library on data visualization and analytics.	2	CO5
Q3	Attempt any 2 parts of the following.		
3a	What is Data Visualization? Why is it important in business? What are its advantages?	2	CO2
3b	What is Power BI ? How Power BI helps in providing an effective solution for businesses?	2	CO3
3c	Briefly explain a Capstone Project one can develop using Power BI for data visualization and analytics.	2	CO5

Q4	Attempt any 2 parts of the following.	2	CO4
4a	How is distributed database processed using AI? How can you achieve machine learning in Spark?	2	CO4
4b	Which tools Spark's Machine Learning library (MLlib) provide? Highlight their basic features/uses.	2	CO5
4c	Briefly explain a Capstone Project one can develop using Apache Spark on distributed databases.		
Q5	Attempt any 2 parts of the following.	2	CO5
5a	What is DevOps lifecycle? Explain how the DevOps lifecycle works at every stage with an illustrated infinite loop diagram with the related tools.	2	CO5
5b	What are the benefits and challenges of DevOps?	2	CO5
5c	Explain a Capstone Project one can develop using an Open Source framework focused on DevOps for AI deployment.		