

**MID-SEMESTER EXAMINATION
(CO & IT)**

Time: 1:30

Max. Marks 25

Note: All Questions carry equal marks
Assume suitable missing data, if any

Q. 1: Write in brief, about two of the following:

- a) Domain Analysis
- b) Two different Elicitation Techniques
- c) Scenario-Based Analysis

Q. 2: Describe two of the following:

- a) What you understand by "Use Cases", and write how the user will use the system?
- b) Why and when we go for Prioritizing requirements?
- c) A note on Managing Changing Requirements.

Q. 3: Write in brief about any two of the following:

- a) Validation of Requirements
- b) Aids for Validation of Requirements
- c) Write a checklist for Requirements Review

Q. 4: Write in brief about any two of the following:

- a) Two different ways of Partitioning
- b) Two different approaches to Problem Analysis
- c) Different characteristics of SRS document

Q. 5: Write in brief about any two of the following:

- a) Design constraints
- b) Reliability and Fault tolerance
- c) SRS specifications Language

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Total No. of pages: 01

B.Tech. (CSE), Sem. 06

Roll No. _____

MID SEMESTER EXAMINATION

February-2022

Course Code: COCSC20

Course Title: Internet of Things

Time: 1:30 Hours

Max Marks: 25

Note: Attempt all questions.

Assume suitable missing data if any.

No.	Question(s)	CO	Marks												
1 (a)	Explain the format of HTTP request and response line with an example.	1	2												
1 (b)	What is Axiom 0 by Tim Berners-Lee, director W3C? What are the key considerations for IoT architecture?	3	3												
2 (a)	Explain the following abbreviations: a) URI b) JSON c) NFC d) MANET e) Name one of ADC approach	1	2.5												
2 (b)	Explain the uses/applicability of cloud, fog, and edge computing in terms of an IoT application.	4	2.5												
3 (a)	Write any five differences between Active and passive RFID Tags. Active Tag Passive Tag	3	2												
3 (b)	Explain the usecase of RFID technology at Airport. What could be the pros and cons using RFID.	5	3												
4 (a)	Write and explain an algorithm of DSR protocol with an example (routing process over a network).	2	2												
4 (b)	Explain the most suitable architecture for IoT networks in a diagrammatical representation.	2	3												
5 (a)	Match the following: <table style="width: 100%; border-collapse: collapse;"><thead><tr><th style="text-align: center; width: 30%;">Layer(s)</th><th style="text-align: center; width: 30%;">Protocol</th></tr></thead><tbody><tr><td style="text-align: center;">Link Layer</td><td style="text-align: center;">UDP</td></tr><tr><td style="text-align: center;">Application Layer</td><td style="text-align: center;">6LoWPAN</td></tr><tr><td style="text-align: center;">Application Layer</td><td style="text-align: center;">COAP</td></tr><tr><td style="text-align: center;">Internet Layer</td><td style="text-align: center;">HTTP</td></tr><tr><td style="text-align: center;">Transport Layer</td><td style="text-align: center;">IEEE 802.15.4</td></tr></tbody></table> What are pin configurations of the ultrasonic sensor?	Layer(s)	Protocol	Link Layer	UDP	Application Layer	6LoWPAN	Application Layer	COAP	Internet Layer	HTTP	Transport Layer	IEEE 802.15.4	1, 3	3
Layer(s)	Protocol														
Link Layer	UDP														
Application Layer	6LoWPAN														
Application Layer	COAP														
Internet Layer	HTTP														
Transport Layer	IEEE 802.15.4														
5 (b)	What are the enablers for the IoT Technology, explain with example?	1	2												

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Total No. of Page: 2

Roll No.

MID SEMESTER EXAMINATION – FEB - MAR 2022
B. TECH. - 6th Sem

Course Code: COCSC18, CACSC20

Course Title: High Performance Computing

Time: 1.5 Hours

Max. Marks: 15

Note: Attempt all the five questions. Missing data / information if any, may be suitably assumed & mentioned in the answer. All questions are of equal marks.

Q. No.	Question	Marks	CO
1a	Explain Flynn's classification of parallel architecture with diagram.	2	1
1b	Define granularity.	1	2
2a	State any four application areas of parallel computing.	2	3
2b	Explain recursive decomposition with an example.	1	2

Q3	S1: Load R1, 1024 /R1 ← 1024/ S2: Load R2, M(10) /R2 ← Memory(10)/ S3: Add R1, R2 /R1 ← (R1) + (R2)/ S4: Store M(1024), R1 /Memory(1024) ← (R1)/ S5: Store M((R2)), 1024 /Memory(64) ← 1024/ where (R _i) means the content of register R _i and Memory(10) contains 64 initially.		
3a	Draw the dependency graph to show all the dependencies.	2	3
3b	Are there any resource dependencies if only one copy of each functional unit is available in CPU?	1	1
4a	Explain MPI_Send() primitive in message passing using MPI.	2	4
4b	Explain PRAM models in brief	1	5

P.T.O.

Total No. of Pages: 2

Roll Number:

B.E. (COE) 5th SemesterEND SEMESTER EXAMINATION
CEC16 – HIGH PERFORMANCE COMPUTING

NOV 2019

TIME: 3 HOURS

MAX. MARKS: 40

NOTE: Attempt any FIVE questions. Attempt all parts of each question together. Assume suitable missing data, if any and specify it clearly.

[4 + 4 = 8]

Question 1

(a) Are the following two loops vectorizable? If yes, show the vectorized code, else, give justification in support of your answer.

i) Do I = 1, N

$$A(I) = A(I+1) + 10$$

End Do

ii) Do I = 1, N-1

$$A(I) = B(I) + C(I)$$

$$B(I+1) = D(I) + 10$$

End Do

(b) Explain the actions taken in Goodman's write-once cache coherence protocol for different type of cache events with the help of suitable state transition diagram.

[4 + 4 = 8]

Question 2

(a) Explain the various types of dependence test applicable for SIV category subscripts. How does these tests help in loop parallelization? Explain with examples.

(b) Look at the two loops: Original loop and Transformed loop. Transformed loop has been obtained after applying loop reversal on the i loop. Verify and explain, whether it is legal to apply loop reversal here.

Original Loop

```
for (j = 0 ; j < N; j++)
    for (i = 0 ; i < N; i++)
        a[i+1][j+1] = a[i][j] + c;
```

Transformed Loop

```
for (j = 0; j < N; j++)
    for (i = N-1; i >= 0; i--)
        a[i+1][j+1] = a[i][j] + c;
```

[4 + 4 = 8]

Question 3

(a) A pipelined processor has a cycle time of 10 ns and a program exhibits an average CPI of 1.6 on this. 10% of the instructions in this program are branches and branch prediction scheme is 90% accurate. Every branch misprediction costs 2 cycles of delay in this processor. Consider a modification in the processor design due to which the cycle time is decreased to 9 ns by increasing the depth of the pipeline. However, the cost of a misprediction will become 7 clock cycles but everything else will stay the same. Compute the average CPI on the modified processor design for the program. Will this program run faster or slower on this new processor? Show your work.

(b) Describe the properties of a Unimodular Matrix. Explain the following loop transformations by choosing the appropriate unimodular matrices: Permutation, Reversal, Skewing.

[2 + 6 = 8]

Question 4

(a) Look at the following segment of C code. Loop Nest is desired to be parallelized. Is parallelization possible or not. If yes, which loop can be parallelized. Do we need any loop transformation? Explore.

```
#define M 100
#define N 200
int i,j;
float sf, a[M,N];
for (i=2; i<M; i++){
    for (j=0; j<N; j++){
        sf=i*j+(N-j);
        a[i,j]=sf*a[i-2,j];
    }
}
```

- (b) Draw the fine grain program flow graph for computing sum of all elements of resultant matrix C which is obtained by matrix multiplication of two 2×2 matrices A and B. A multiplication node has a grain size of 101 CPU cycles, addition node has a grain size of 8 CPU cycles and inter-node communication delay scheduled on two different processors is 8 CPU cycles. Draw a sequential schedule and a 4-processor parallel schedule for the above program flow graph. Also, perform grain packing and show the 4-processor parallel schedule for packed program.

Question 5

- (a) Categorize and explain the different Directory based protocols for cache coherence protocols.
 (b) The instruction pipeline of a RISC processor has the following stages: Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Perform Operation (PO) and Writeback (WB). The IF, ID, OF and WB stages take 1 clock cycle each for every instruction. Consider a sequence of 100 instructions. In the PO stage, 50 instructions take 3 clock cycles each, 25 instructions take 2 clock cycles each, and the remaining 25 instructions take 1 clock cycle each. Compute the speedup obtained due to pipelined execution w.r.t. sequential execution. Assume that there are no data hazards and no control hazards.

$$[4 + 4 = 8]$$

Question 6

- (a) A programmer has parallelized a program such that 1% of the total time is spent in serial code of the program. The problem size can expand as the number of processors increases. What is the expected speedup on 20 processors?
 (b) A program written in C is executed on two different computers: Computer A and Computer B. Both have a processor that implements the x86 ISA and 3 GHz clock frequency. During execution of this program, we measure cycles per instruction (CPI) that is found to be 10 on Computer A and 8 on Computer B. On which computer (A or B) this program runs faster? Explain.
 (c) Test for dependences on S. Which dependence test would you apply to each subscript position? Explain.

```
for (k=0; k<100; k++) {
    for (j=0; j<100; j++) {
        for (i=0; i<100; i++) {
            A[i+1,j+1,k+1] = A[i,j,1] + c; // S
        }
    }
}
```

- (d) How do the following techniques affect the different parameters of processor performance: Pipelining, Compiler Optimizations, Multi-level Memory, Branch Predictor?

Question 7

- (a)

```
for( i =1;i<50; i++)
    a[2*i] = a[(100 *i)+1];
```

 Does the GCD test detect any dependency? Is there a loop-carried true dependency in this loop, explain?
 (b) Which type of branch predictors (1-bit or 2-bits for branch history) performs best in predicting the direction of a branch that changes its direction after every two executions? Show your work.
 (c) In a 3-stage pipelined processor, S1 stage is used in clock cycle 1, 6, 8; S2 stage is used in clock cycles 2, 4, 6, 8. S3 stage is used in clock cycles 3, 5, 7. Verify theoretical values of lower bound and upper bound on the MAL for this processor with the ones obtained from collision state diagram.

	1	2	3	4	5	6	7	8
S1	X					X		X
S2		X		X				
S3			X		X		X	

-----X-----X-----X-----

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Roll No. _____

B. Tech. VIth Sem
END-SEMESTER EXAMINATION, May 2022

Course Code: Internet of Things
Course Title: COCSC20

Time: 3 Hours

Max. Marks: 50

Note: - Attempt all the five questions. Missing data / information if any, may be suitably assumed & mentioned in the answer. Write as precise as possible, do not write unnecessarily.

Q. No.	Question	Marks	CO
Q1	Attempt any 2 parts of the following.		
1a	Consumer is providing following different Analog values for encoding it into Digital values. Provide the solution using SAM approach. The signal for 5 bits registers with a full-scale range of 100 Volts. a) 14.5 V b) 74 V	5	2
1b	Define an embedded system in IoT device and provide the functions used to read analog and digital data from a sensor in Arduino.	5	1
1c	Provide the difference between IoT and IIoT. Explain various wireless communications boards available in Raspberry Pi.	5	1
Q2	Attempt any 2 parts of the following.		
2a	Delhi NCR pollution index is increasing day by day from Average to Severe; Prof NAO from NSUT want to update people every minute about change in Pollution Index to their subscribers. And you know Delhi-NCR population is around 10 million. Please help to clear his doubts regarding implementation of MQTT protocol with the following points: a) Who will be subscriber, who will be publisher and where the broker will be placed? b) Which QoS reliability will work fine with this case, explain? c) Is there any better solution than MQTT protocol for this use-case scenario, explain. d) What could be the formatting or allocation of Topic, so that subscriber can easily choose the nearest publisher.	5	2, 5
2b	Mention any two commonly used water sensors and their pin configuration	5	2
2c	Write five major comparisons in MQTT and CoAP web protocols. (Hint: Architecture, Size, QoS, Transport Protocol, port, methods).	5	2, 3
Q3	Attempt any 2 parts of the following.		
3a	How many types of messages are existing in CoAP protocol, explain each with diagrammatical representation?	5	3
3b	Explain the following abbreviations: a) ESC.	5	2, 3, 4

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	b) 6LoWPAN. c) CoAP d) LWT e) PAN ID in ZIGBEE		
3c	Explain the requirement/working of Fragmentations over IEEE 802.15.4 standard using IPv6 with Example	5	3, 4
Q4	Attempt any 2 parts of the following.		
4a	What are the challenges in IoT network which can be addressed using SDN and how?	5	4
4b	Explain the preliminary sensors required to fly the drones in any flight controllers	5	4, 5
4c	What are the security issues and possible attacks over IoT networks, explain in the bullet points?	5	5
Q5	Attempt any 2 parts of the following.		
5a	How blockchain helps to make reliable IoT networks, explain with one case study.	5	4, 5
5b	Write brief about five applications of Drones, where IoT can be applicable.	5	4
5c	Explain the major components of 5G. What are the benefits for applying 5G technology for IoT networks?	5	4

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Total No. of Pages: 1

Roll Number:

B.E. (COE) 5th Semester

MID SEMESTER EXAMINATION - SEP 2019

TIME: 1.5 HOURS

CEC16 – HIGH PERFORMANCE COMPUTING

MAX. MARKS: 15

NOTE: Attempt ALL questions. Attempt all parts of each question together. Assume suitable missing data, if any and specify it clearly.

Question 1

- a) Hazards do not occur due to false dependencies in scalar pipelines. Explain. [1 x 4 = 4]
- b) What is the effect on Clock frequency and CPI on converting a scalar processor superscalar? Briefly explain your reasoning.
- c) A non-pipelined processor has a cycle time of 100 ns. When it is pipelined into 5 stages, individual stage delays are 10 ns, 15 ns, 40 ns, 20 ns, and 15 ns. If each pipeline stage added also adds 2 ns due to latch delay, what is the best speedup you can get from pipelined processor compared to the original processor?
- d) A program which has 4000 instructions has 20% branch instructions, 32% load-store instructions and the rest are ALU instructions. The program is running on a processor operating at 2 GHz. The CPI of branch, load-store and ALU instructions are 2, 2.5, and 1.25, respectively. Compute the execution time of this program.

Question 2

- a) A processor with 10-stage instruction pipeline incurs three stalls due to data hazards for every 7 instructions. In addition to it, branch mis-prediction causes 5 cycles stall. If branches constitute 40% of the instructions, and branch mis-prediction rate is 10%, what is the effective CPI considering both data hazards and branch mis-predictions? [1 x 3 = 4]
- b) Give an example in which a static predictor will perform better than a 1-bit dynamic branch predictor.
- c) A linear pipeline operating at 400 MHz has a speedup factor of 6 and operating at 70% efficiency. How many stages are there in the pipeline?
- d) Write the diameter and bisection width of following networks: A hypercube with 512 processors; A 2-D Mesh with 256 processors.

Question 3

Explain the functioning of a branch handling technique with example that will result in conditional branches going to target as zero delay. [2]

Question 4

For a 4-stage non-linear pipelined processor, collision vector is 1000 and clock period is 20 ns. Determine the maximum throughput of this pipeline. [2]

Question 5

- a) Consider a multiprocessor system with 3 processors P1, P2 and P3. Assume that they are connected through a static network. At time instant 1, all three processors would like to send a message: P1 should send to P2, P2 to P3, and P3 to P1. How many time units does this communication take and why on following network topologies: (1) Bus (2) Linear Array (3) Ring [1.5 x 2 = 3]
- b) Draw 8x8 Omega Network. Check whether the switches can be configured to connect node 0 to node 6 and node 4 to node 7 without conflict.

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Total No. of Page: 3	Roll No.
END SEMESTER EXAMINATION - APR - MAY 2022 B. TECH. - 6 th Sem	
Course Code: COCSC18, CACSC20 ✓	Course Title: High Performance Computing
Time: 3.0 Hours	Max. Marks: 40
Note: Attempt all the five questions. Missing data / information if any, may be suitably assumed & mentioned in the answer. All questions are of equal marks.	

Q. No.	Question	Marks	CO															
Q1	Attempt any 2 parts of the following.																	
1a	Explain temporal and data parallelism with suitable example. In addition, consider the execution of an object code with 2×10^4 instructions on a 400 MHz processor. The program consists of four major types of instructions. The instruction mix and the number of cycles [CPI] needed for each instruction type are given below based on the result of a program trace experiment:																	
	<table border="1"> <thead> <tr> <th>Instruction type</th> <th>CPI</th> <th>Instruction mix</th> </tr> </thead> <tbody> <tr> <td>Arithmetic and logic</td> <td>1</td> <td>60%</td> </tr> <tr> <td>Load/store with cache hit</td> <td>2</td> <td>15%</td> </tr> <tr> <td>Branch</td> <td>4</td> <td>12%</td> </tr> <tr> <td>Memory reference with cache miss</td> <td>8</td> <td>10%</td> </tr> </tbody> </table> <p>(a) Calculate the average CPI when the program is executed on a uniprocessor with the above trace results. (b) Calculate the corresponding MIPS rate based on the CPI obtained in part (a).</p>	Instruction type	CPI	Instruction mix	Arithmetic and logic	1	60%	Load/store with cache hit	2	15%	Branch	4	12%	Memory reference with cache miss	8	10%	4	CO1
Instruction type	CPI	Instruction mix																
Arithmetic and logic	1	60%																
Load/store with cache hit	2	15%																
Branch	4	12%																
Memory reference with cache miss	8	10%																
1b	Characterize the architectural operations of SIMD and MIMD computers. Distinguish between multiprocessors and multic平ers based on their structures, resource sharing, and interprocessor communications. Also, explain the differences among UMA, NUMA, COMA, and NORMA computers.	4	CO1															
1c	Compare the PRAM models with physical models of real parallel computers in each of the following categories: (a) Which PRAM variant can best model SIMD machines and how? (b) Repeat the question in part (a) for shared memory MIMD machines.	4	CO2															
Q2	Attempt any 2 parts of the following.																	
2a	Develop two algorithms for fast multiplication of two $n \times n$ matrices with a system of p processors, where $1 \leq p \leq n/\log n$. Choose an appropriate PRAM machine model to prove that the matrix multiplication can be done in $T = O(n^2/p)$ time. (a) Prove that $T = O(n^2)$ if $p = n$. The corresponding algorithm must be shown (b) Show the parallel algorithm with $T = O(n)$ if $p = n^2$	4	CO2															
2b	Write the pseudocode of adding all elements of an array using p=process in shared memory computer.	4	CO3															

2c	Write the pseudocode for addition of an array using Single Program multiple data (SPMD) message passing model.	4	CO3
Q3	Attempt any 2 parts of the following.		
3a	<p>Explain all types of delays in pipeline execution. Determine the time taken with and without pipelining during the loss of speeding due to resource non-availability. Further, use the following code fragment:</p> <pre> Loop: LD R1,0(R2) load R1 from address 0+R2 ADDI R1, R1, #2 R1=R1+1 SD R1, 0, (R2) store R1 at address 0+R2 DADDI R2, R2, #4 R2=R2+4 DSUB R4, R3, R2 R4=R3-R2 BNEZ R4, Loop branch to Loop if R4!=0 </pre> <p>Data hazards are caused by data dependences in the code. Whether a dependency causes a hazard depends on the machine implementation (i.e., number of pipeline stages). List all of the data dependences in the code above. Record the register, source instruction, and destination instruction.</p>	4	CO4
3b	Explain data flow steps while executing an instruction. In addition, draw consolidated data flow showing all the steps in instruction execution in detail?	4	CO4
3c	<p>Explain the concept of delay, locking and out-of-order completion in detail using diagrams or examples. The following assembly code is to be executed in a three-stage pipelined processor with hazard detection and resolution in each stage. The stages are instruction fetch, operand fetch (one or more as required), and execution (including a write-back operation). Explain all possible hazards in the execution of the code.</p> <pre> Inc R0 /R0 ← (R0) + 1 Mul ACC, R0 /ACC ← (ACC) × (R0) Store R1, ACC /R1 ← (ACC) Add ACC, R0 /ACC ← (ACC) + (R0) Store M, ACC /M ← (ACC) </pre>	4	CO3
Q4	Attempt any 2 parts of the following.		
4a	Why does a cache read, write miss happen? Explain all the possible reasons for a single-processor system? You have an L1 data cache, L2 cache, and main memory. The hit rates and hit times for each are: 50% hit rate, 2 cycle hit time to L1, 70% hit rate, 15 cycle hit time to L2, 100% hit rate, 200 cycle hit time to main memory. A) What fraction of accesses are serviced from L2? From main memory? B) What is the miss rate and miss time for the L2 cache? C) What is the miss rate and miss time for the L1 cache?	4	CO3
4b	Explain two major relaxed consistency models in detail. Describe what happens in the MESI protocol (bus traffic, state changes) if a processor experiences: 1. a local read miss, while another cache holds a copy in exclusive state 2. a local read miss, while another cache has a copy in modified state 3. a local write hit, while the cache line is in modified state 4. a local write hit, while the cache line is in exclusive state 5. a local write hit, while the cache line is in shared state in several caches	4	CO4
4c	Explain shared bus multiprocessor with write buffers in detail with the help of a diagram. Consider the following sequence of operations by two processors for a block that starts at address B. Determine the state of that block in the caches of both the processors after each	4	CO5

(10)

operation in the sequence for the MOESI protocol. Both caches are initially empty and all lines are in the I state. The table below is provided to help organize your answer.

No.	Operation	MOESI	
		P1	P2
1	P1 reads B		I
2	P1 writes B		I
3	P2 writes B		
4	P1 reads B		
5	P1 writes B		
6	P2 reads B		

Q5

Attempt any 2 parts of the following.

5a

Explain the energy-efficient computing on many-core processor of Amdahl's law in detail. Assuming a program consists of 50% non-parallelizable code. A) Compute the speed-up when using 2 and 4 processors according to Amdahl's law. B) Now assume that the parallel work per processor is fixed. Compute the speed-up when using 2 and 4 processors according to Gustafson's law. C) Explain why both speed-up results are different.

4

C04

5b

What is Gustafson's Law? Illustrate the speedup expression of Gustafson's law in detail. The analysis of a program has shown a speedup of 3 when running on 4 cores. What is the serial fraction according to Gustafson's law? In addition, the analysis of a program has shown a speedup of 3 when running on 4 cores. What is the serial fraction according to Amdahl's law (assuming best possible speedup)?

4

C05

5c

Explain at least three hardware related, and software related factors that affect parallel program's performance in detail. Explain all the special cases of G(n) in detail?

4

C05