VE311 RC4 MOSFET

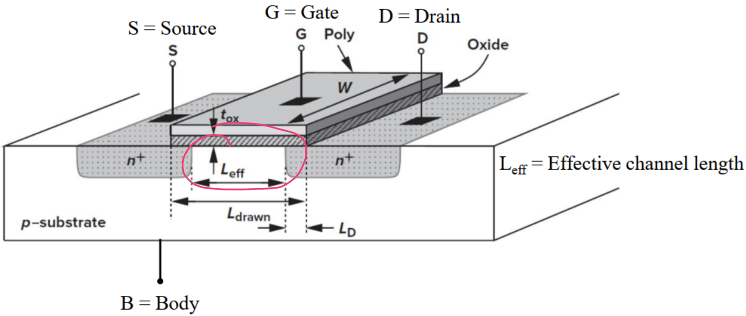
Yian HU

University of Michigan-Shanghai Jiao Tong University Joint Institute

November 7, 2024

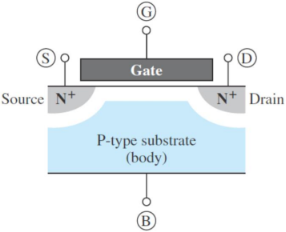
Overview

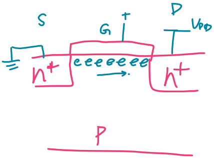
NMOS



- $L_{eff} = L_{drawn} - 2L_D$
- If not specify L, we assume it is L_{eff}

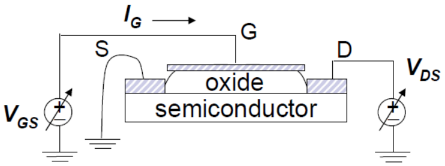
NMOS

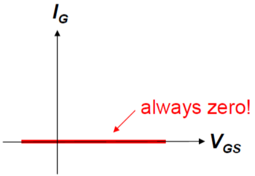




- $V_{GS} < 0$, attract holes to surface: Accumulation, not we want
- $V_{GS} > V_T$, induce electrons: Inversion, form channel
- If not apply V_{DS}, no current
- How to distinct Source (S) and Drain (D)
  - Since both S and D are doped with same concentration, it depends on how you apply voltage
  - Electrons flow from source to drain. Current I_{DS} or I_D, drain to source
  - Positive voltage: Drain. $V_{DS} > 0$
  - S and D can switch by changing voltage

NMOS - I_G



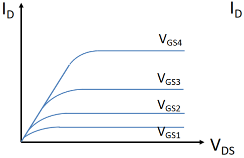


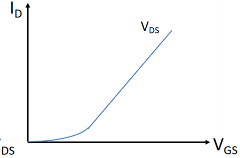
- Gate is insulated from the semiconductor, always 0

NMOS - I_D

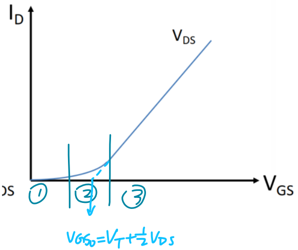
$$I_D = \begin{cases} 0 & V_{GS} - V_T < 0 \\ \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_T)^2 & 0 \le V_{GS} - V_T < V_{DS} \\ \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_T - \frac{1}{2}V_{DS})V_{DS} & V_{GS} - V_T \ge V_{DS} \end{cases}$$

Summary of I_D





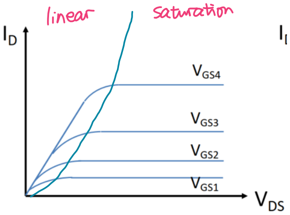
$I_D - V_{GS}$



- Fixed V_{DS}

1. When $V_{GS} < V_T$, no current, $I_D = 0$
2. When $0 < V_{GS} - V_T < V_{DS}$, $I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_T)^2$, I_D and V_{GS} follows **quadratic** relation.
3. When $V_{GS} - V_T > V_{DS}$, $I_D = \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_T - \frac{1}{2}V_{DS})V_{DS}$, I_D and V_{GS} follows **linear** relation, the interception with x axis is $V_T + \frac{1}{2}V_{DS}$

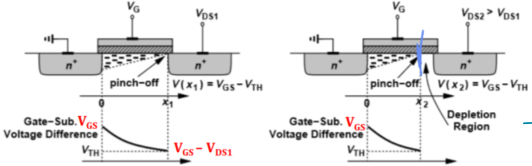
$I_D - V_{DS}$

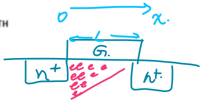


- Fixed V_{GS} for each curve

1. When $0 < V_{DS} < V_{GS} - V_T$, $I_D = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T - \frac{1}{2}V_{DS})V_{DS}$
   - When $0 < V_{DS} << 2(V_{GS} - V_T)$, V_{DS}^2 can be ignored. Then $I_D = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)V_{DS}$, I_D and V_{DS} follows **linear** relationship. We call this **Linear/ Triode/ Resistive** region
   - S to D can be represented by a linear $R_o = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)}$
2. When $V_{DS} > V_{GS} - V_T$, $I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)^2$,$I_D$ has no relation with V_{DS}, current saturate. We call this **Saturation** region.

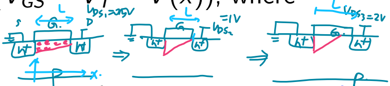
*How does saturation happen - Pinch off





- $I_D = WQ_n(x)v$. $Q_n(x)$ is charge per unit area. $v = \mu_n E$
- Inversion layer charge density $|Q_n(x)| = C_{ox}(V_{GS} - V_T - V(x))$, where $V(x) = \frac{V_{DS}}{L}x$
- When x increases, $|Q_n(x)|$ decreases

$V_{GS}-V_T=1V$ $V_{DS_1}=0.5V$ $V_{DS_2}=1V$ $V_{DS_3}=2V$

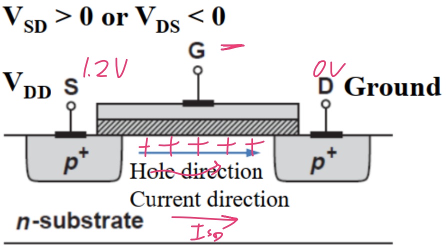


1. When $0 < V_{DS} < V_{GS} - V_T$: At L, $|Q_n(x)| > 0$, still has electrons, no pinch off
2. When $V_{DS} = V_{GS} - V_T$: At L, $|Q_n(x)| = 0$, start to pinch off
3. When $V_{DS} > V_{GS} - V_T$: Before L, $|Q_n(x)| = 0$, pinch off. MOSFET reaches saturation region, even if we increase V_D, I_D will not change since $|Q_n(x)|$ will not change.

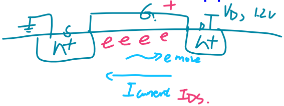
- Electrons can still pass through the pinch-off region because of E_{bi}

PMOS

PMOS!



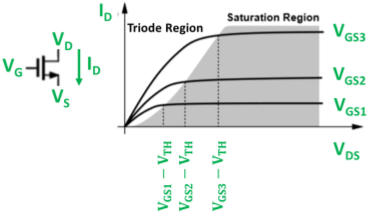
- $V_{GS} < 0$, attract holes as channel.
  - In PMOS, V_T is usually smaller than 0. To turn on the device, $V_{GS} < V_T$
- Holes from source to drain. Current I_{SD}, source to drain
- Positive voltage: Source. $V_{SD} > 0$. Current direction is opposite from NMOS (I_{DS})



NMOS and PMOS

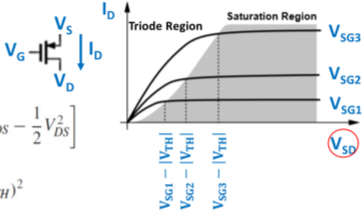
From slides

NMOS *vs* PMOS



Triode region: $I_D = \mu_n C_{ox} \frac{W}{L_{eff}} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} {V_{DS}}^2 \right]$

Saturation region: $I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L'} (V_{GS} - V_{TH})^2$



Triode region: $I_D = -\mu_p C_{ox} \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$

Saturation region: $I_D = -\frac{1}{2} \mu_p C_{ox} \frac{W}{L'} (V_{GS} - V_{TH})^2$

NMOS and PMOS IMPORTANT!

To simplify the equation, we can use the following universal formula by simply adding $|\quad|$ on I_D, $V_{GS} - VT$, and V_{DS}.
This equation is valid for both NMOS and PMOS, and either V_T is positive or negative.

$$I_D = \begin{cases} 0 & |V_{GS}| - |V_T| < 0 \\ \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(|V_{GS} - V_T|)^2 & 0 \leq |V_{GS} - V_T| < |V_{DS}| \\ \mu_n C_{ox}\frac{W}{L}\left(|V_{GS} - V_T| - \frac{1}{2}|V_{DS}|\right)|V_{DS}| & |V_{GS} - V_T| \geq |V_{DS}| \end{cases}$$

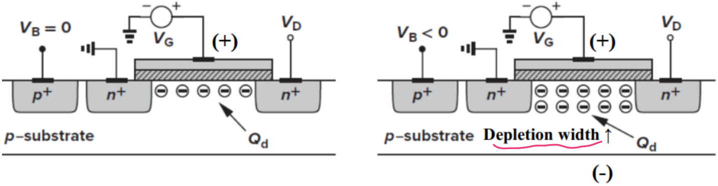
Universal Formula

Transconductance g_m

- Usually defined in saturation region. $I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_T)^2$
- $g_m = \frac{dI_D}{dV_{GS}} = \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_T) = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D} = \frac{2I_D}{V_{GS} - V_T}$
- High g_m, small change in V_{GS} will lead to large change in I_D. High sensitivity.

Overview

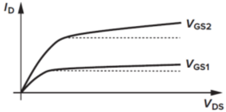
Second Order Effects - Body Effect

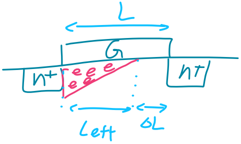


- Initially $V_B = 0$, now $V_B < 0$. Attract more holes to bottom, leaving more electrons to surface. Wider depletion region. V_{TH} increases.
- $V_{TH} = V_{TH0} + \gamma(\sqrt{|2\Phi_F + V_{SB}|} - 2\sqrt{|2\Phi_F|})$
  - $\gamma = 0$, no body effect

define:
- $g_{mb} = \frac{dI_D}{dV_{BS}} = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)\frac{\gamma}{2}\frac{1}{\sqrt{|2\Phi_F + V_{SB}|}} = g_m \eta.$
  - $\Delta I_D = \Delta V_{BS} * g_{mb}$, when $V_{BS}(> 0)$ increases (V_{SB} becoming more negative), I_D increases
- $g_m = \frac{dI_D}{dV_{GS}} = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T) = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} = \frac{2I_D}{V_{GS} - V_T}.$
  - $\Delta I_D = \Delta V_{GS} * g_m$, when $V_{GS}(> 0)$ increases, I_D increases

Second Order Effects - Channel Length Modulation





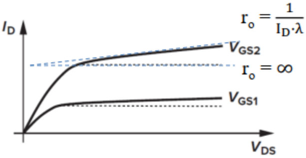
- After reaching saturation region, when $\Delta L << L_{eff}$ is not satisfied, the effect of V_{DS} on I_D cannot be ignored. Now we use $L' = L_{eff} - \Delta L$, where ΔL is the pinch-off length.
- $I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L'}(V_{GS} - V_T)^2 = \frac{1}{2}\mu_n C_{ox}\frac{W}{L_{eff}}(V_{GS} - V_T)^2(1 + \frac{\Delta L}{L_{eff}}) = \frac{1}{2}\mu_n C_{ox}\frac{W}{L_{eff}}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$, λ is the slope

With the channel-length modulation,

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})$$

$$\mathbf{g_m} = \frac{\partial \mathbf{I_D}}{\partial \mathbf{V_{GS}}} = \mu_n C_{ox}\frac{W}{L_{eff}}(V_{GS} - V_{TH})(1 + \lambda V_{DS})$$

$$\mathbf{r_o} = \frac{\partial V_{DS}}{\partial I_D} = 1\Big/\frac{\partial I_D}{\partial V_{DS}} = \frac{1}{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \cdot \lambda} \approx \frac{\mathbf{1}}{\mathbf{I_D \cdot \lambda}}$$

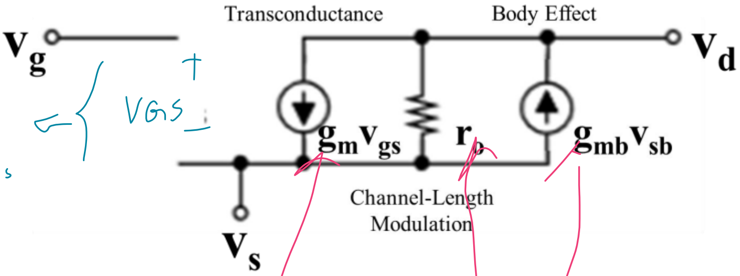


Channel-length modulation is reflected in g_m and r_o by λ

Overview

Small-Singal Model

don't connect!
no I_{GS}



- $\Delta I_D = g_m \Delta V_{GS} \rightarrow i_d = g_m V_{gs}$, add voltage controlled current source
- Consider channel length modulation ($\lambda \neq 0$): $r_o = \frac{dV_{DS}}{dI_D} \rightarrow i_d = \frac{v_{DS}}{r_o}$, add a resistor r_o
- Consider body effect ($\gamma \neq 0$): $g_{mb} = \frac{dI_D}{dV_{BS}} \rightarrow i_d = g_{mb} v_{bs}$, add voltage controlled current source. If $V_{SB} > 0$, we reverse the direction of the current source to make each term positive value
- This small-signal diagram is the same for PMOS

How to solve problems

- For DC analysis, we are required to calculate I or V.
- If the question specify which region the MOSFET is now working in, apply the equation for I directly
- If not, assume the MOSFET is in saturation region, because the equation for I is much easier. $|V_{DS}| > |V_{GS} - V_T|$ ← PMOS.
- Apply the formula $I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_T)^2$ to calculate I and V
- Check whether $|V_{DS}| > |V_{GS} - V_T|$ is indeed true
  - If indeed true, then it is in saturation region, you get the answer
  - If not, it is in linear region, and use $I_D = \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_T)V_{DS}$ to calculate I and V again

Overview

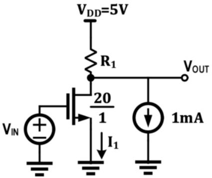
Exercise 1

See solution.

For the following problems, assume: $\mu_n C_{ox}$ = 100 μA/V², V_{TH} = 1 V.

Problem 1: For the circuit below, perform the following calculations:

a) Find I_1 when V_{IN} =1.2 V and R_1 =2 kΩ.
b) If W/L of the transistor is changed to W/L = 80/1, compute the new value of overdrive voltage (V_{OV}) such the current I_1 remains the same as in part (a).
c) Find the maximum value of R_1 which ensures that the transistor remains in saturation.
d) Determine the minimum value of supply voltage V_{DD} to bias the transistor in saturation.



- b): $V_{ov} = V_{GS} - V_{TH}$
- c): $V_{IN} = 1.2V$
- d): $V_{IN} = 1.2V,\ R_1 = 2k\Omega$

EX1 ANS

ANS

$$\mu_n C_{ox} = 100\mu A/V^2,\ V_{TH} = 1V$$

Problem 2: Consider the circuit below. For R_D = 5 kΩ and R_S = 1 kΩ, find I_D, V_D, and V_S.

Step 1. Suppose it is in saturation.

$V_{DS} > V_{GS} - V_{th}$

$V_D > V_G - 1. = 1V$

$$\begin{cases} I = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{th})^2. \\ I = \frac{V_S}{R_S}. \end{cases}$$

V_S unknown.

V_S = 1.25V or 0.8V.

Device on:
$V_{GS} - V_{th} > 0$.
$2 - V_S - 1 > 0$
$V_S < 1V$

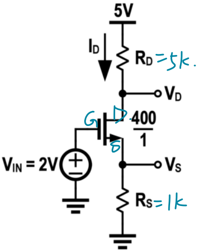
$$I = \frac{V_S}{R_S} = \frac{0.8}{1k} = 0.8mA.$$

$$V_D = 5 - I \cdot R_D = 5 - 0.8m \times 5k. = 1V$$

Step2. check.

$\Downarrow$

indeed in saturation.



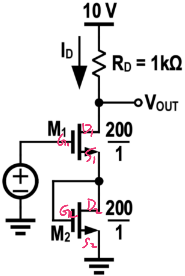
EX2 ANS

ANS

Exercise 3

$$\mu_n C_{ox} = 100\mu A/V^2,\ V_{TH} = 1V$$

Problem 3: For the circuit below V_{IN} = 2.8 V, find the value of I_D and V_{OUT}.



☆ self-bias first. M2:

$V_{D2} = V_{G2}$.

$V_{DS2} > V_{GS2} - V_{th}$.

must in saturation.

$I_2 = \frac{1}{2}\mu_n C_{ox}(\frac{W}{L})_2 . (V_{GS2} - V_{th})^2$ ①

step1. suppose M1 is in saturation

$V_{DS1} > V_{GS1} - V_T$.

$V_D > V_{G1} - V_T = 2.8 - 1 = 1.8V$

$I_1 = \frac{1}{2}\mu_n C_{ox}(\frac{W}{L})_1 (V_{GS1} - V_{th})^2$ ②

① = ②

$V_{GS2} - \cancel{V_{th}} = V_{GS1} - \cancel{V_{th}}$

$V_{G2} - \cancel{V_{S2}}^{0} = \underbrace{V_{G1}}_{2.8} - V_{S1}$

$V_{S1} = V_{D2} = V_{G2}$.

$V_{G2} = 2.8 - V_{G2}$.

$V_{G2} = 1.4V = V_{D2} = V_{S1}$

$I_1 = 1.6mA$.

$V_{D1} = V_{DD} - I_1 R_D = 10 - 1.6m \times 1k = 8.4V$. ⇒ indeed in saturation.

$\|$ Vout.

Step2 check.

EX3 ANS

ANS

- Analyze the self-bias stage M2 first