VE311 Electronic Circuit Homework 6

Due: **Jul 8th 11:59a.m.**

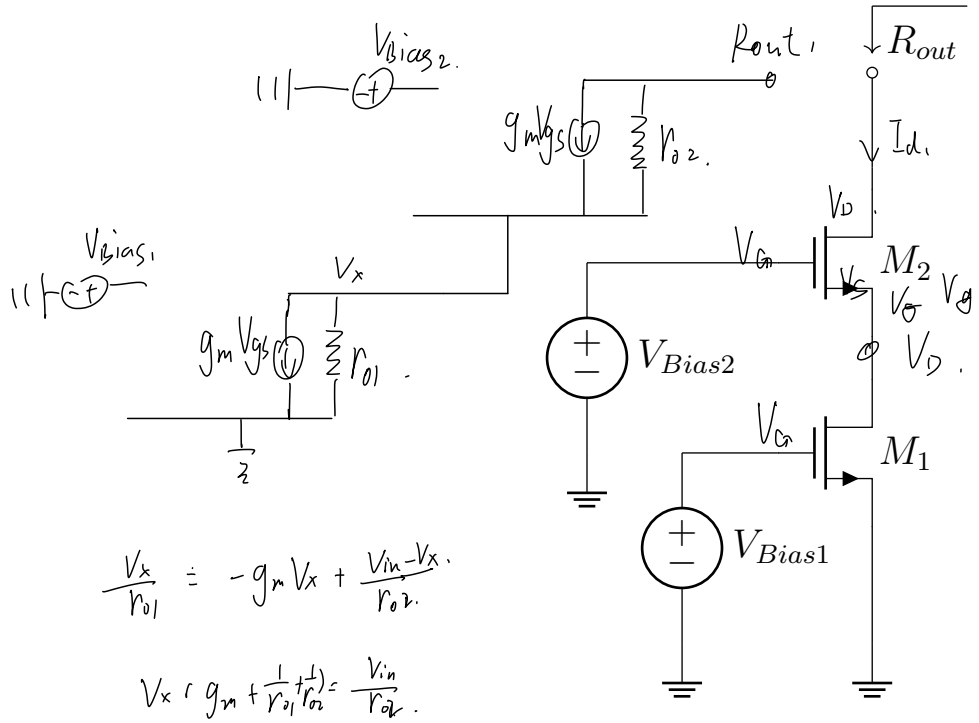
Note:

1) Please use A4 size paper or page.
2) Please clearly state out your final result for each question.
3) Please attach the screenshot of Pspice simulation result if necessary.

Peilin has become proficient in understanding the large-signal model of the MOSFET. However, to fully grasp the behavior of electronic circuits, Peilin needs to extend his knowledge to include the small-signal model. This is crucial for analyzing how the output signal reacts to variations in the input signal. This transition marks Peilin's next challenge in the homework.

Question 1. Small Signal of MOSFET

Initially, Peilin needed to learn to draw small-signal circuits and understand the parameters of their components. The circuit shown below is a MOSFET cascode amplifier. The next challenge Xuyang hands Peilin is to draw the small signal model and derive R_{out} for the amplifier. Assume transistors M_1 and M_2 are in saturation and include r_O in the calculation.



$$\frac{V_x}{r_{o1}} = -g_m V_x + \frac{V_{in}-V_x}{r_{o2}}$$

$$V_x\left(g_m + \frac{1}{r_{o1}} + \frac{1}{r_{o2}}\right) = \frac{V_{in}}{r_{o2}}$$

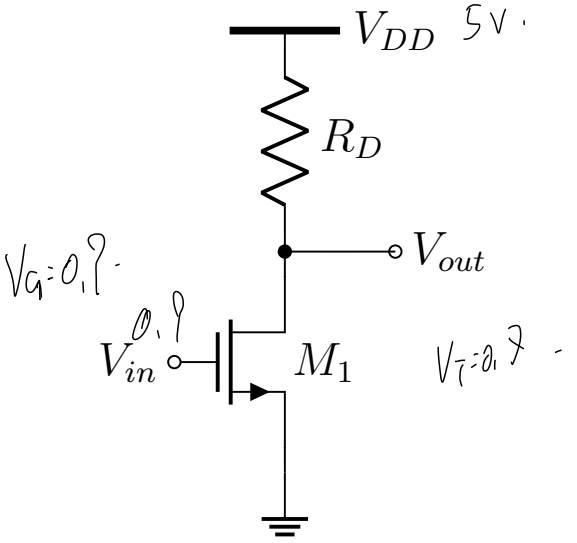
$$V_x = \frac{V_{in}}{r_{o2}} \cdot \frac{1}{g_m + \frac{1}{r_{o1}} + \frac{1}{r_{o2}}}$$

$$R_{out} = \frac{V_{in}}{\frac{V_x}{r_{o1}}} = \frac{V_{in}}{V_x} \cdot r_{o1} = r_{o2}\left(g_m + \frac{1}{r_{o1}} + \frac{1}{r_{o2}}\right) \cdot r_{o1}$$

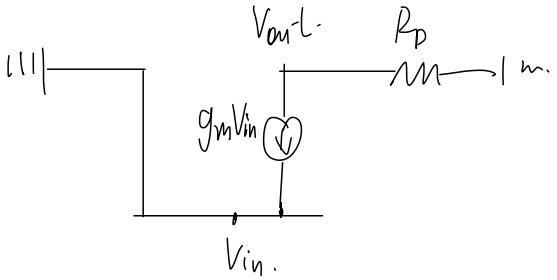
$$= g_m r_{o1} r_{o2} + r_{o1} + r_{o2}$$

Question 2. Common-Source with Resistive Load

When dealing with weak signals, such as microphone amplifiers or signal conditioning circuits for other sensing devices, common-source MOSFET amplifiers are often used as the first stage of amplification because of the high voltage gain they can provide. In his final task, Peilin must optimize a common-source amplifier with a resistive load. Assume $\lambda = 0$ and $\gamma = 0$. For $V_{DD} = 5V$, $V_{in} = 0.9$ V + small signal, $R_D = 15k\Omega$ and $L_{drawn} = 2\mu m$, find out the value W_{drawn} to obtain a voltage gain $|A_v| > 10$ and V_{OUT} (the DC biasing voltage at the output) close to $2.5V$ as much as possible.



$$\begin{cases} I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_T)^2 \\ I_D = \frac{V_{DD}-V_{out}}{R_D} \end{cases}$$



$W = 1.24\times10^{-4}$ m.

$g_m = \mu_n C_{ox}\frac{W}{L}(V_{GS}-V_T) = 1.67\times10^{-3}$

$\frac{0-V_{out}}{g_m V_{in}} = R_D$.

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$|V_{out}| = |g_m V_{in} R_D|$.

$\left|\frac{V_{out}}{V_{in}}\right| = |g_m R_D| = 25 > 10$.

Therefore, it's valid.

NMOS Model			
LEVEL=1	VTO=0.7	GAMMA=0.45	PHI=0.9
NSUB=9e+14	LD=0.08e-6	UO=350	LAMBDA=0.1
TOX=9e-9	PB=0.9	CJ=0.56e-3	CJSW=0.35e-11
MJ=0.45	MJSW=0.2	CGDO=0.4e-9	JS=1.0e-8
PMOS Model			
LEVEL=1	VTO=-0.8	GAMMA=0.4	PHI=0.8
NSUB=5e+14	LD=0.09e-6	UO=100	LAMBDA=0.2
TOX=9e-9	PB=0.9	CJ=0.94e-3	CJSW=0.32e-11
MJ=0.5	MJSW=0.3	CGDO=0.3e-9	JS=0.5e-8

VTO : threshold voltage with zero V_{SB} (unit : V)
GAMMA : body effect coefficient (unit : $V^{1/2}$)
PHI : $2\Phi_F$ (unit : V)
TOX : gate oxide thickness (unit : m)
NSUB : substrate doping (unit : cm^{-3})
LD : source/drain side diffusion (unit : m)
UO : channel mobility (unit : $cm^2/V/s$)
LAMBDA : channel-length modulation coefficient (unit : V^{-1})
CJ : source/drain bottom-plate junction capacitance per unit area (unit : F/m^2)
CJSW : source/drain sidewall junction capacitance per unit length (unit : F/m)
PB : source / drain junction built-in potential (unit : V)
MJ : exponent in CJ equation (unitless)
MJSW : exponent in CJSW equation (unitless)
CGDO: gate-drain overlap capacitance per unit width (unit : F/m)
CGSO : gate-source overlap capacitance per unit width (unit : F/m)
JS : source/drain leakage current per unit area (unit A/m^2)
Vacuum permittivity (ϵ_o) = 8.85×10^{-12}(F/m)
Silicon oxide dielectric constant (ϵ_r) = 3.9

After days of intense focus, Peilin finally submitted his solutions for the small-signal MOSFET models and the common-source amplifier. He had met all the challenges Xuyang had thrown at him, from understanding MOSFET biasing in Homework 5 to mastering the intricacies of small-signal analysis and amplifier optimization in Homework 6.

In a brief yet significant meeting, Xuyang reviewed Peilin's work. "Excellent job, Peilin," Xuyang said with a nod of approval. "Your understanding of MOSFET technology is impressive, and your solutions demonstrate both precision and creativity."

Peilin felt a surge of pride. He had not only completed the tasks but had also deepened his understanding of crucial electronic concepts. More importantly, he had proven his value to Blue Tiger Electronics.

As Peilin left Xuyang's office, he looked forward to the new challenges ahead. With a renewed sense of confidence, he knew he was ready to tackle whatever came next in his journey as an engineer at Blue Tiger Electronics.