UM-SJTU Joint Institute

VE311

Laboratory Report

Excercise 3

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[rev4.1]

1 Objective

Study the Common-Source amplifier, and factors that may affect the voltage gain.

2 Common-Source with NMOS Diode-Connected Load

2.1

Using Proteus, we get the following simulation result.

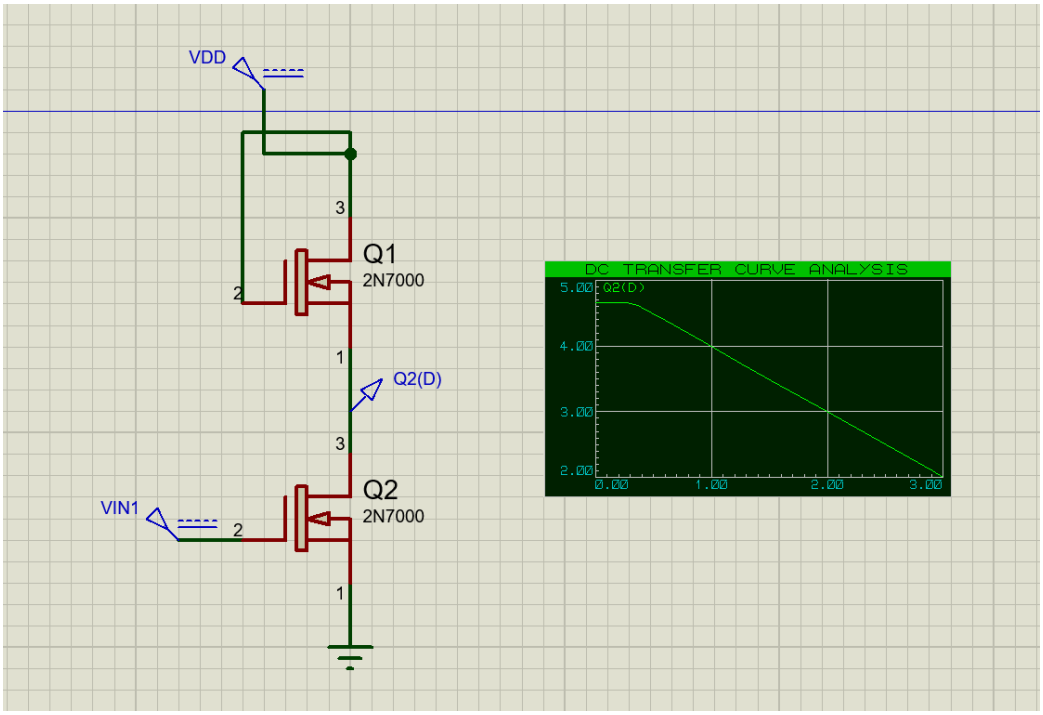

Figure 1: Simulation Circuit & Result

According to the slope of the figure, $A_v = \frac{0.637}{0.54} = 1.0$.

2.2

Using Proteus, we get the following simulation result.

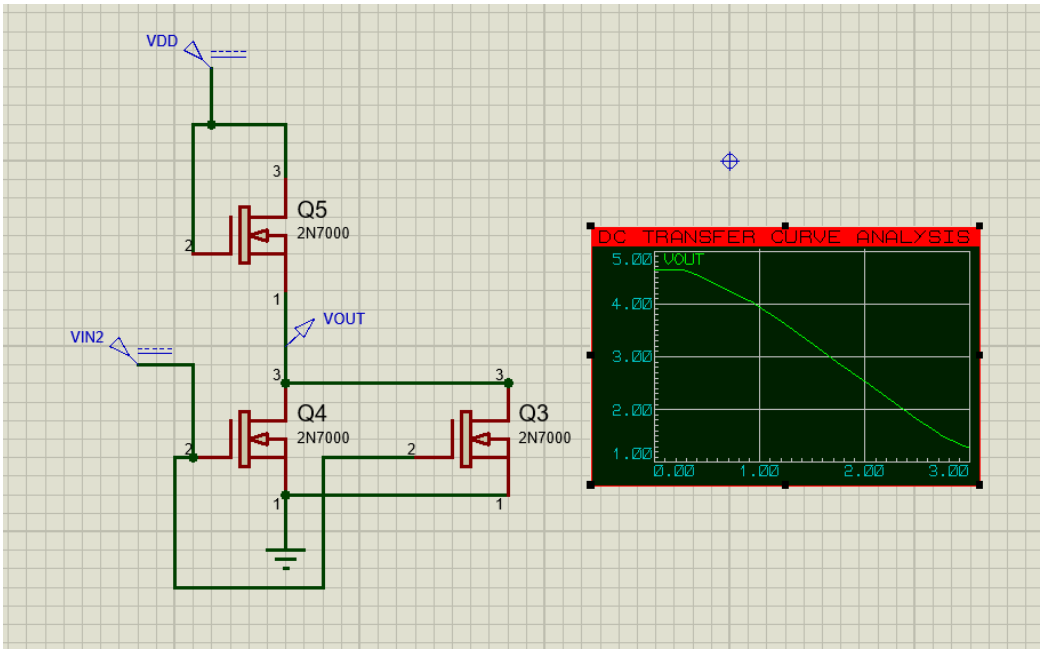

Figure 2: Simulation Circuit & Result

According to the slope of the figure, $A_v = \frac{2.07}{1.46} = 1.42$.

$$A_v = -\frac{\sqrt{2k_n'(W/L)_1 I_D}}{\sqrt{2k_p'(W/L)_2 I_D}} = -\sqrt{\frac{k_n'(W/L)_1}{k_p'(W/L)_2}}$$

$$A_v' = -\sqrt{\frac{k_n'(2(W/L)_1)}{k_p'(W/L)_2}} = \sqrt{2}\left(-\sqrt{\frac{k_n'(W/L)_1}{k_p'(W/L)_2}}\right)$$

$$A_v' = \sqrt{2} \cdot A_v$$

Therefore, $A_{v1} \neq A_{v2}$.

2.3

Using Proteus, we get the following simulation result. What's more, we have built the circuit and get the corresponding figure.

According to that, $A_v = \frac{0.237}{0.225} = 1.05$, which is in align with the theoretical value, verifying that our result is correct.

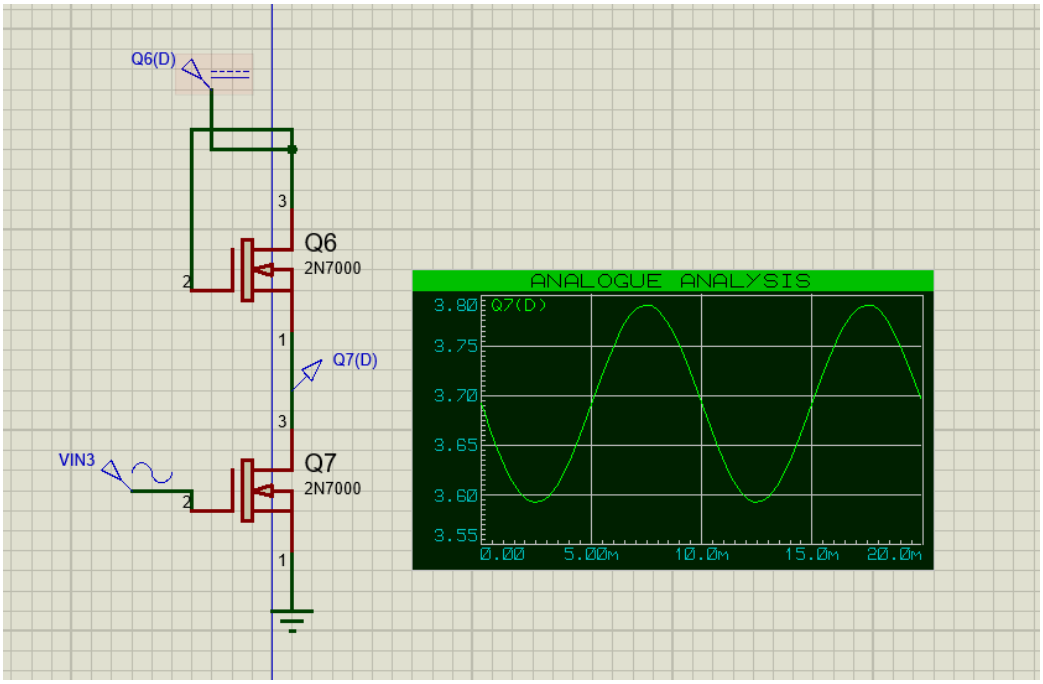

Figure 3: Simulation Circuit & Result

3 Common-Source with PMOS Diode-Connected Load

3.1

Using Proteus, we get the following simulation result.
According to the slope of the figure, $A_v = \frac{0.162}{0.225} = 0.64$.

3.2

Using Proteus, we get the following simulation result. According to the slope of the figure, $A_v = \frac{0.183}{0.544} = 0.33$. Reason: As we have added a PMOS, we can assume we have added a resistance, therefore, the gain will be smaller.

3.3

Using Proteus, we get the following simulation result.
What's more, we have built the circuit and get the corresponding figure.

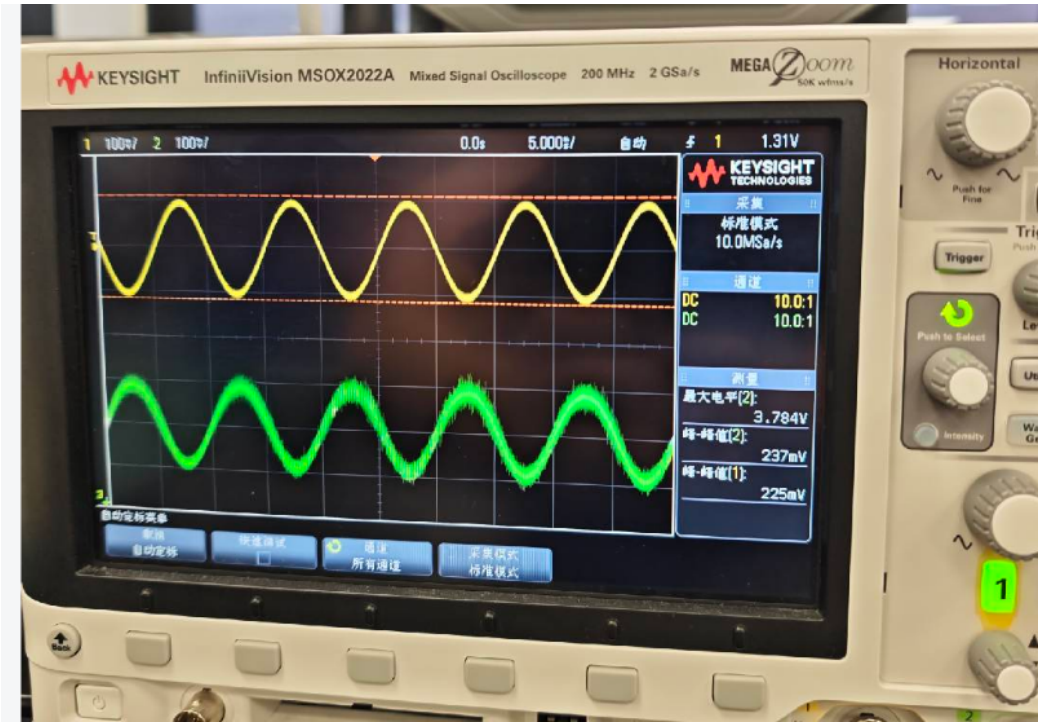

Figure 4: Lab Result

According to that, $A_v = \frac{0.221}{0.293} = 0/75$, which is in align with the theoretical value, verifying that our result is correct.

4 Error Analysis

4.1 Errors Introduced by Measuring Instruments and Methods

The measurement process in this experiment is subject to instrumental errors. Systematic errors stem from the digital multimeter's finite internal resistance, which creates a loading effect that can inaccurately lower voltage readings at high-impedance points, and from the oscilloscope probe's intrinsic capacitance, which alters the circuit's frequency response and reduces the measured -3dB cutoff frequency. Additionally, random errors were introduced into dynamic signal measurements by power line noise and ambient electromagnetic interference, which appeared as small fluctuations on the oscilloscope waveform.

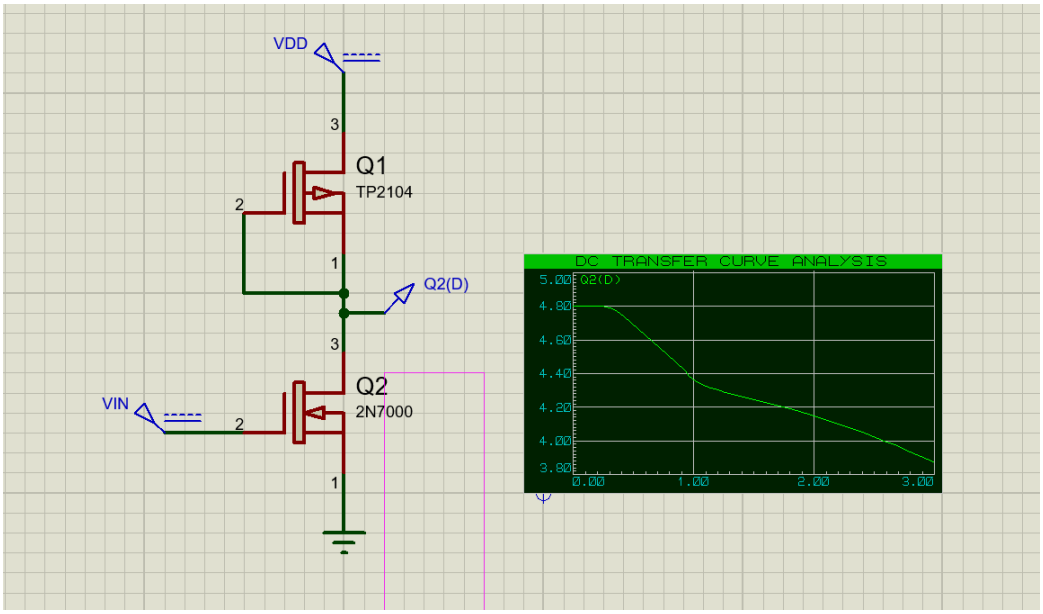

Figure 5: Simulation Circuit & Result

4.2 Errors from Circuit Construction and Environmental Factors

The circuit's performance is impacted by both the prototyping medium and thermal effects. The breadboard introduces issues like contact resistance and unreliability, which can cause intermittent connection failures, while long wires add parasitic inductance and capacitance that degrade high-frequency performance. Additionally, as the transistor heats up during operation, its material properties (carrier mobility and threshold voltage) change. This thermal effect causes the DC operating point to drift, leading to inconsistent measurements as the circuit warms up to a stable temperature.

5 Conclusion

Valuable insights into amplifier behavior using MOSFET configurations were gained from the experiments, despite the challenges encountered. The process highlighted the critical importance of integrating theoretical knowledge with hands-on experience to optimize circuit design and measurement methodologies.

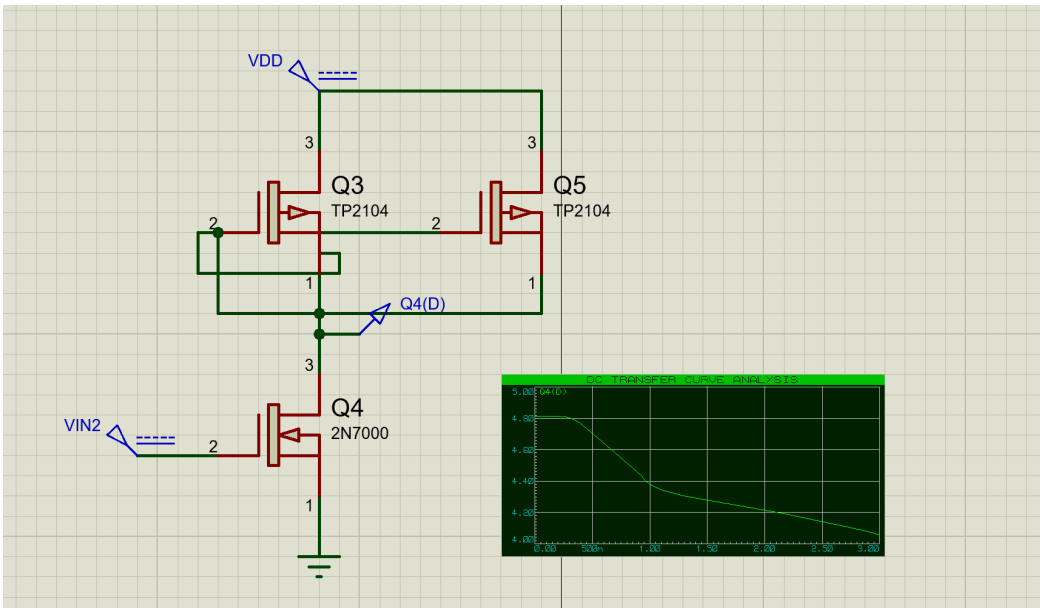

Figure 6: Simulation Circuit & Result

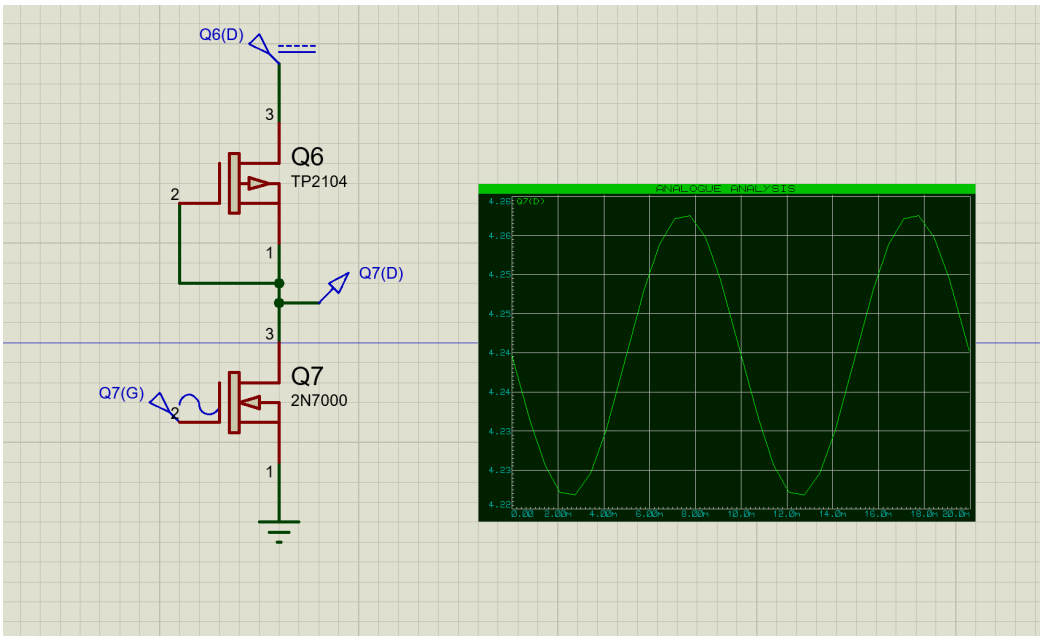

Figure 7: Simulation Circuit & Result

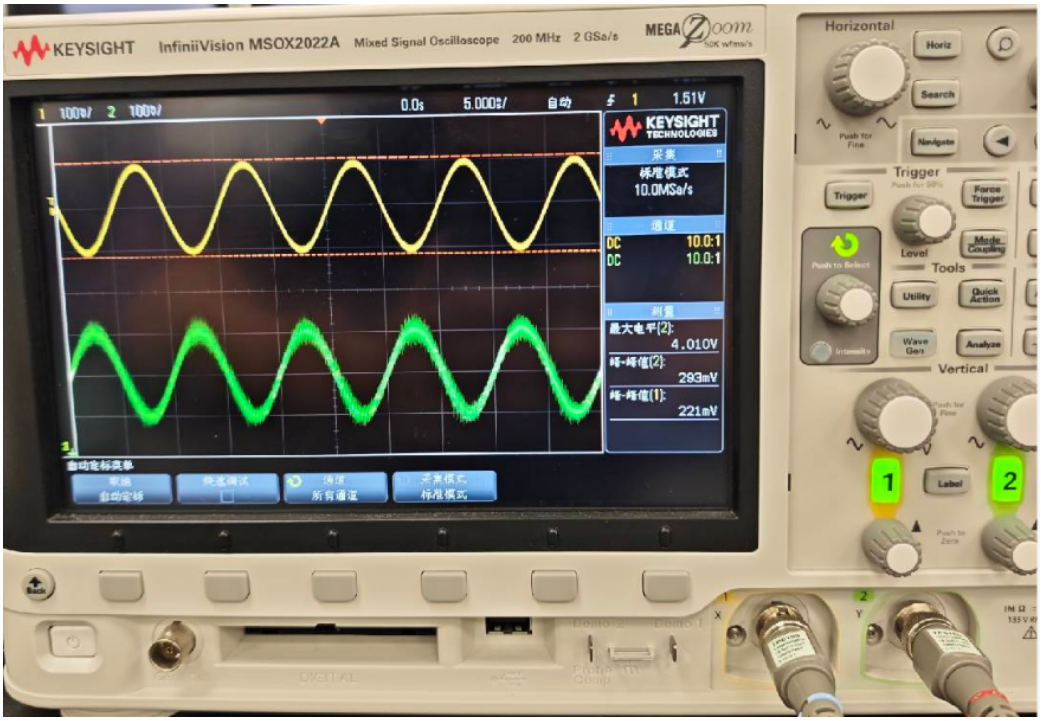

Figure 8: Lab Result