
DEPLOYING A TASK-BASED RUNTIME SYSTEM ON RASPBERRY PI CLUSTERS

A PREPRINT

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ABSTRACT

Arm[®] technology is becoming increasingly important in HPC. Recently, Fugaku, an Arm[®]-based system, was awarded the number one place in the Top500 list. Raspberry Pis provide an inexpensive platform to become familiar with this architecture. However, Pis can also be useful on their own. Here we describe our efforts to configure and benchmark the use of a Raspberry Pi cluster with the HPX/Phylanx platform (normally intended for use with HPC applications) and document the lessons we learned. First, we highlight the required changes in the configuration of the Pi to gain performance. Second, we explore how limited memory bandwidth limits the use of all cores in our shared memory benchmarks. Third, we evaluate whether low network bandwidth affects distributed performance. Fourth, we discuss the power consumption and the resulting trade-off in cost of operation and performance.

Keywords Arm[®], asynchronous manytask system · Raspberry Pi · HPX · vectorization

1 Introduction

The Arm[®] architecture is becoming increasingly important in the high-performance computing (HPC) and server world. Not only is the fastest super computer in the *Top500*, Fugaku, an Arm[®]-based system, but Sandia National Labs has announced the Arm[®]-based Astra prototype cluster. One reason for the rising interest is energy efficiency, since it is one of the most significant costs for any supercomputer and a critical factor for building a petaflops cluster.

The Raspberry Pi is based on the Arm[®] architecture and follows the Arm[®] ISA. It has a single pipeline, Neon, to enable support for vectorization, which potentially increases its computing power by a factor of four. Furthermore, Raspberry Pis are portable and many times more efficient than most CPUs, allowing them to be used in places where traditional computers can't exist (e.g. remote sensor devices).

The message passing interface (MPI) is a common paradigm for parallel distributed applications on supercomputers and was studied on Arm[®]-based clusters. See Section 2. An alternative to MPI and the message passing paradigm is the task-based paradigm, also called asynchronous many-task (AMT). One example for AMT is the C++ standard library for concurrency and parallelism (HPX) [1], but there are many others [2–4]. A comparative review is given in [5].

This study uses the three most recent Raspberry Pi models (Model 3 B, Model 3 B+, and Model 4) for a set of various benchmarks: a stencil-based one-dimensional heat equation solver (for distributed memory analysis), a stencil-based two-dimension Jacobi method solver (for shared memory and vectorization analysis), and the alternating least square (ALS) algorithm. First, the scaling on shared and distributed memory is investigated. Second, the energy consumption is compared against one of the conventional x86 architecture.

1.1 Our Contribution

In this paper, we present the first overview of porting and evaluating an AMT (HPX) to Raspberry Pis. We investigate the performances on all fronts, i.e. vectorization, shared memory, and distributed memory. We further investigate the distributed machine learning potential of Raspberry Pis using Phylanx, a distributed array processing toolkit that utilizes HPX for distributed memory tasks. We conclude the paper with the energy consumption benefits of Raspberry Pis.

2 Related Work

Works using cloud training and Pis for evaluating neural nets [6] show that Raspberry Pis can be very effective. Raspberry Pis are also efficient at pre-processing data that can later be fed to a machine learning model. Collecting and pre-processing images on Raspberry Pis has been proven useful by Wang et al [7]. Raspberry Pis are also helpful for scenarios where portability is the key. For instance, machine learning applications within a vehicle [8], at face detection and tracking [9], and in botany [10]. Other similar works taking advantage of Raspberry Pis have also been explored [11–17].

While we could not find any papers on porting HPC applications to the Raspberry Pi, there many ports of HPC applications to the Arm[®] ecosystem. S. McIntosh-Smith et al [18, 19] were among the first to measure performance on mainstream Arm[®] HPC systems. Later, Jackson et al [20] investigated the performance of distributed memory communications (MPI) through a benchmark suite utilizing MPI on ThunderX2. The energy consumption of these Arm[®] processors has been investigated by the Mont-Blanc project [21].

3 Tools

3.1 HPX

HPX [1, 22–24] is based on the theoretical ParalleX [25] execution model. HPX is an asynchronous many-task runtime system with an API that closely adheres to the ISO C++ standard that enables wait-free asynchronous parallel programming including futures, channels and other synchronization primitives. Conforming with the C++ standard makes it possible for HPX code to be deployed on virtually any machine. Figure 1 shows the architecture of HPX.

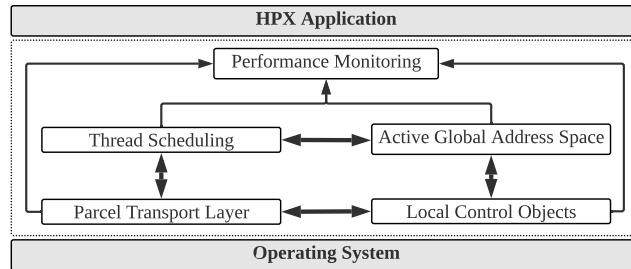


Figure 1: The architecture of HPX: Tasks, or HPX-threads, are run on top of operating system threads. A global view of the application is made possible using Active Global Address Space (AGAS). The Network Layer manages communication between tasks on different nodes.

Tasks in HPX, also called *HPX-threads*, are lightweight threads that are scheduled on top of the underlying operating system threads. Asynchronous execution in HPX is achieved through *futures* [26] (which are placeholders for the result of a computation that has not yet been completed), *continuations* (a function which is invoked when a future becomes ready), and *dataflow* (which are functions that don't begin execution until their arguments are ready). These mechanisms enable HPX programmers to write fully asynchronous code. The tasks generated by the application are synchronized by Local Control Objects (LCOs), which are a family of synchronization primitives.

The parcel [27] subsystem is an active-message networking layer that ships functions to the objects they operate on. Because HPX is designed for use with distributed memory, HPX utilizes Active Global Address Space (AGAS) to track remote objects. This is achieved by assigning each object a unique Global Identifier (GID) that persists till object destruction.

A performance counter layer sits on top of these four subsystems, providing feedback to developers.

In the context of this work, HPX is used as a backend for Phylanx that is described in section 3.2.

3.2 Phylanx

Phylanx [28] is an HPX-based distributed array processing toolkit. The architecture of Phylanx is shown in Fig. 2.

Phylanx provides a function decorator which access the function’s abstract syntax tree and reinterprets it. While Phylanx supports a substantial subset of Python functionality, it is not intended to be a substitute for the Python interpreter. Instead, it is only a means to allow the analysis and evaluation mathematical kernels.

Phylanx works by translating Python code into a tree of phylanx objects (*primitives*) connected by futures known as the execution tree. Each phylanx *primitive* waits for its input futures to become ready before executing, then sets a future to convey its result to the next primitive(s).

Phylanx uses an intermediate language called Phylanx Specification Language (PhySL) which is similar to Lisp. Programs can be written in Python or in this intermediate language.

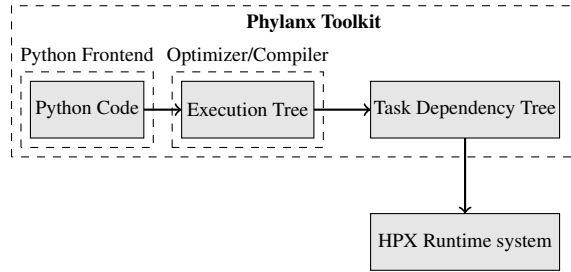


Figure 2: The architecture of Phylanx: Python code is compiled into a tree of phylanx objects called the execution tree. The execution tree is traversed, resulting in a task graph of *futures* which are executed by HPX.

4 Benchmarks

This section explains the benchmarks and the parameters used to run them. Furthermore, we give a brief description of the system configuration and software versions.

4.1 2D Jacobi Solver (Shared Memory)

For shared memory performance, we implement a 2D stencil based on the Jacobi method. To fully exploit the Neon pipeline, we add explicit vectorization. As vectorizing a standard grid layout of a stencil is non-trivial, we changed the data layout to Virtual Node Scheme [29]. The changed data layout allows us to trivially vectorize the code in a cache friendly manner. We do not change the data layout for non-vectorized code to test GCC’s ability to autovectorize a non-trivial layout.

Stencil codes are known to be memory bound due to their low Arithmetic Intensity (AI). Therefore, we do not expect many-fold increase in performance by utilizing explicit vectorization. Furthermore, we expect the compiler to auto vectorize the base code, which may limit the additional benefits of explicit vectorization.

The application is tested using strong scaling. All benchmarks are run with a grid size of 4096×4096 iterating over a 100 time steps. The benchmark achieves parallelism by dividing the grid into smaller grids of sizes $4096 \times y$ and working on the smaller grids in parallel. Therefore, the number 4096 is chosen such that three rows of the grid fits in the caches. This reduces the number of memory transfers per iteration to three. The arithmetic intensity for such

a scenario is given by $1/24$ for double precision, and $1/12$ for single precision respectively. Using the principles of the roofline model [30], one can now calculate the optimal performance using the following formula:

$$P_{optimal} = Memory\ Bandwidth \times AI \quad (1)$$

We use the STREAM benchmark [31] to compute the memory bandwidth. All performance numbers are provided in Million Lattice site Updates Per Second (MLUPs/s). For our case, 1 lattice site update corresponds to 4 floating point operations. Therefore, one can convert the performance from MLUPs/s to FLOPs/s by multiplying by 4.

4.2 ALS

ALS or “Alternating Least Squares” is a matrix factorization algorithm widely employed for computing recommendations in streaming services, online stores, etc.

The idea behind ALS is that we factor a ratings matrix R_{ij} where i runs over users and j runs over items, into a user matrix U_{ik} and an item matrix, V_{kj} , and the k values represent “latent factors.”

The word *alternating* is in the name because the solver alternately minimizes the least squares error arising from the values in U and V .

For our benchmark, we use the first two hundred thousand lines of the MovieLens 20m database¹

4.3 1D Heat Equation solver (Distributed memory)

For distributed memory performance, we use HPX’s optimized in-house stencil benchmark. This benchmark uses a single partition per locality, exchanges data from a single cell during halo exchange, and the exchange is made asynchronously via dataflow (allowing overlap of computation and communication).

For benchmarking, we use a heat transfer coefficient of $k = 0.5$, a time step of $dt = 1$, and a grid spacing of $dx = 1$. For strong scaling, we use 30 million and 60 million stencil points iterating for 100 or 500 time steps. For weak scaling, we start with 30 million stencil points and another 30 million stencil points are added for each node. The benchmark iterates over 100 time steps.

4.4 System Setup

The CPU models Cortex-A53 and Cortex-A72 are capable of running both 32-bit (armv7l) and 64-bit (aarch64) instruction sets. On the Raspberry Pi model 3, there is no benefit in using a 64-bit operating system since there is only 1GB of memory available. Also, a 64-bit application is going to use more memory simply because variables take up more space—although this increase in memory usage is negligible in most cases. On the other hand, the Raspberry Pi 4 potentially has more memory and could benefit from a 64-bit operating system. To compensate the memory limitation imposed by hardware, all installations include 8GB swap space (which was needed by the gnu C++ compiler to compile HPX and Phylanx).

The 64-bit version of the official operating system from the Raspberry Pi Foundation is still in development. So far, the foundation has only released the 32-bit version. However, there are third party distributions which provide both versions, but many on those lack support for relatively newer Raspberry Pi 4. In our search, we found that Ubuntu Server 2020 is the only distribution that supports all three versions of boards, has both 32-bit and 64-bit release, and has a relatively up-to-date development library.

We understand that the Ubuntu distribution is an unusual choice for our experiment. Ubuntu, while very popular among developers and Linux enthusiasts, is rarely used in an HPC environment. As a result, many default settings are tuned toward desktop usage. By tweaking those settings, the desired performance can be achieved. For example, the default CPU profile is set to “*ondemand*,” which means the Linux kernel will keep the CPU frequency at lowest level allowed by hardware and only increase the frequency in response to system load. Although this setting may be acceptable for a single user, it could have significant impact on application performance, especially at startup. Throughout these tests, the CPU frequency is always kept at highest level allowed by hardware (using the CPU profile “*performances*”).

Although the Arm® processors are praised for their low power consumption, they are not entirely immune to the problem of power consumption and heat generation. Like any other contemporary microprocessor, the power consumption happens during the switching time in logic gates. Therefore, the amount of heat produced is directly related to CPU

¹<http://dx.doi.org/10.17632/n6sjkpy87f.5>

Table 1: Specification/Architecture of the three nodes utilised in the benchmarks.

Model	Raspberry Pi 3B	Raspberry Pi 3B+	Raspberry Pi 4B
Micro-architecture	Arm [®] v8-A	Arm [®] v8-A	Arm [®] v8
Processor Model	Cortex-A53	Cortex-A53	Cortex-A72
Number of CPUs	1	1	1
Cores per CPU	4	4	4
Total Cores	4	4	4
Frequency	1.2GHz	1.4GHz	1.5GHz
Memory	1GB	1GB	4GB

Operating System	Ubuntu 20.04 LTS for Arm [®]	Kernel blaze ²	5.4 75179e6
Compilers	gcc 9.30.1	boost	1.71
hwloc	2.1.0	gperftools	2.7
lapack	3.8	HPX ³	5b9de48ab1

Table 2: Overview of the compilers, software, and operating system used.

frequency. Raspberry Pis do not have an active cooling system. To avoid any damage to the processor, the firmware will reduce the CPU frequency to reduce amount of heat production when a certain high temperature reached. The process is called *thermal throttling* and it could cause inconsistency in the performance results. To avoid thermal throttling, a small aluminium heat-sink was installed on all processors and boards were transferred to our data-center which as well regulated air temperature and better air flow.

Distributed computing on the Raspberry Pi board isn't without challenges, since the performance of these distributed applications is heavily influenced by network speed and latency. Although all model B Raspberry Pis provide an Ethernet interface, the earlier models lack a dedicated network controller. Raspberry Pis model 3B and 3B+ use the USB controller to provide Ethernet interface, therefore the performance network interface is bound to the performance of USB interface. On the Raspberry Pi 3B, the network interface works at a speed of 100 Mb/s. On the Raspberry Pi model 3B+ the network interface establishes a 1 Gb/s link, but the underlying USB cannot transfer the data faster than 300 Mb/s, therefore, the actual data transfer rate is limited to that speed. Only on the Raspberry Pi Model 4B is this issue addressed, and a dedicated network controller capable of transferring data at the speed of 1 Gb/s is installed on the board.

Table 2 shows the libraries and compiler used to build HPX, Phylax, and the benchmarks. Table 1 specifies the hardware. For the distributed memory benchmark, we used the network latency hiding 1D stencil 8 benchmark from HPX's in-house benchmark suite. For the shared memory benchmark, we wrote a 2D stencil Jacobi solver with explicit vectorization. For Phylax, the in-house benchmark ALS Python script was used.

5 Results

5.1 2D stencil (Shared Memory)

Figure 3 depicts the STREAM TRIAD results. It can be seen that the Raspberry Pi 3B and 3B+ have very low memory bandwidth. The memory bandwidth is almost fully saturated by a single PU, and decreases with the number of PUs. For the Raspberry Pi 4, we observe a similar behavior. Memory bandwidth is expected to increase or be the same (if saturation is achieved) on a single NUMA domain. Here we see a sharp decline as we increase the number of PUs. The memory bus and controllers can only handle a certain amount of memory bandwidth and concurrency at the same time. This can be a possible reason behind the decline.

Using Equation 1, we find the expected peak performance. We use the Linux `perf` utility to retrieve performance counters. The Gnu compiler was readily able to auto vectorize our 2D stencil with minimal differences in instruction counts. Visible improvements, however, were seen in cache-references and cache-misses. This means that the approach taken by GCC to auto vectorize the code differs in data layout.

For the Raspberry Pi 4, the best recorded performance is for a core count of 2 and 3. This is because the memory bandwidth decreases with the core count. Our measurements are on par with the expected peak performance.

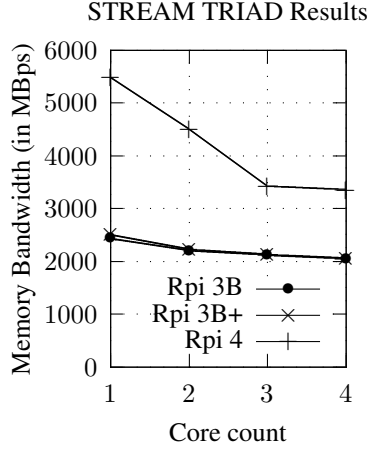


Figure 3: Memory Bandwidth results using the STREAM TRIAD Benchmark with an array size of 10M elements

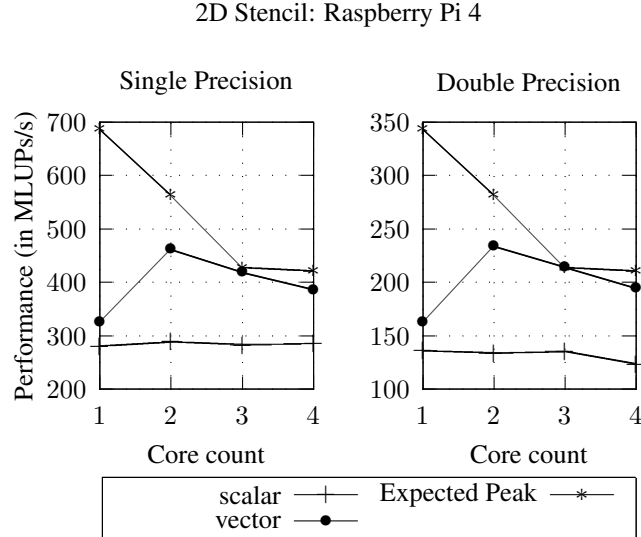


Figure 4: 2D stencil (Raspberry Pi 4): Grid size of 4096×4096 iterated over a 100 time steps.

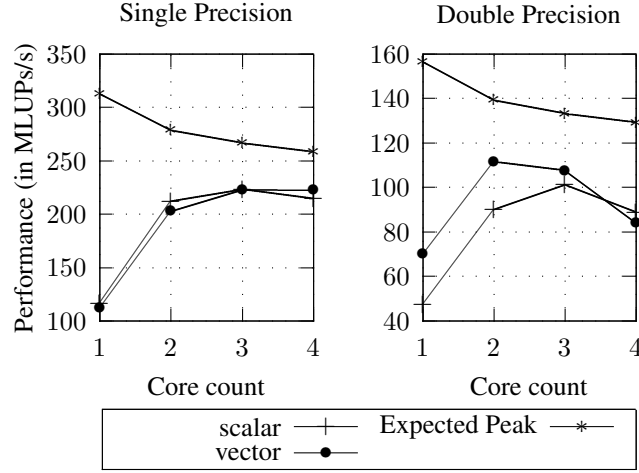
Table 3 shows the hardware counter values we measured. Our perf results show similar instruction counts, but about 50% less cache misses for explicitly vectorized codes. This shows that our Virtual Node Scheme [29] is more cache-friendly compared to the autovectorization layout utilized by GCC.

Table 3: Hardware counters for Raspberry Pi4

Data Type	Instructions	Cache-Misses
float	6,168,850,721	288,165,018
nsimd float	5,858,534,460	210,042,447
double	11,553,460,548	641,066,436
nsimd double	11,147,560,795	411,352,041

For the Raspberry Pi 3B+ and 3B, we see very similar performance. This is because the two models differ only in the clock speeds. The Raspberry Pi 3B clocks at 1.2GHz whereas 3B+ clocks at 1.4GHz. This allows for a 16% improvement in performance, which is noticeable at lower thread counts. At a core count of 1 and 2, 3B+ performs noticeably better than 3B. At higher core counts, the performance is almost the same. For both these processors, we are not able to achieve the expected peak performance. Explicit vectorization is not able to help boost the performance

2D Stencil: Raspberry Pi 3B+

Figure 5: 2D stencil (Raspberry Pi 3B+): Grid size of 4096×4096 iterated over a 100 time steps.

either. While 1 core performance can be attributed to the limited compute, many core performance is sub par. Table 4 describes the major contributing hardware counters when all four cores were used. From the instruction count, it is clear that GCC does well at auto vectorization. However, similar to the Raspberry Pi 4, GCC fails to exploit the data layout resulting in a higher cache-miss count. While Raspberry Pis do not allow access to hardware stall counters, we believe that explicit vectorization gains from having lower number of memory transactions in-flight. This explains why the explicitly vectorized results are sub par as well. A redesign of vectorized elements should help alleviate the problems given the small cache size and higher instruction count.

5.2 ALS

For the ALS benchmark, the performance of the Pi4 is nearly double the value obtained for the Pi3 and Pi3+, despite the modest difference in clock speed.

Because this application, as it is written, is fairly memory intensive, the larger memory bandwidth and larger L2 cache of the Pi4 (1mb vs. 512kb) are the significant factors here.

2D Stencil: Raspberry Pi 3B

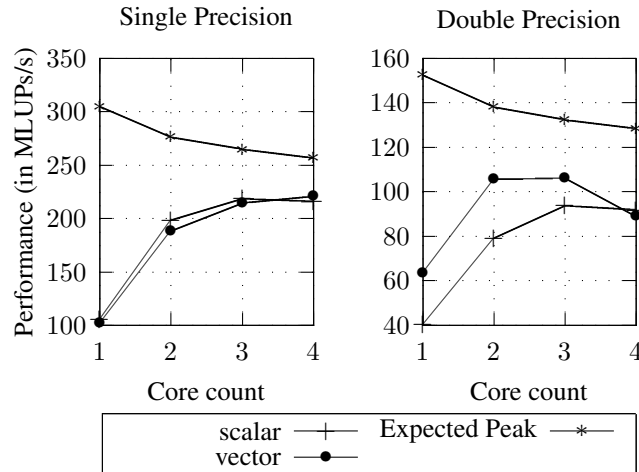
Figure 6: 2D stencil (Raspberry Pi 3B): Grid size of 4096×4096 iterated over a 100 time steps

Table 4: Hardware counters for Raspberry Pi3B+

Data Type	Instructions	Cache-Misses
float	8,973,631,540	147,993,989
nsimd float	13,484,044,923	133,391,170
double	22,009,615,376	296,496,230
nsimd double	23,158,335,089	279,417,800

Performance of the ALS Benchmark

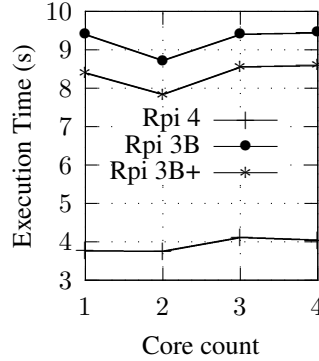


Figure 7: Here we see the performance of the ALS benchmark on the Pi3, the Pi3B+ and the Pi4. The Pi4 provides almost twice the performance.

Our ALS application receives little benefit from parallelism. We believe that, with future effort at improving the code, we will be able to get better parallel speedup.

5.3 1D stencil (Distributed Memory)

Strong scaling results are provided in Figure 8. The benchmark was designed to hide latency and allow for an almost linear scaling. One interesting point to note is that the benchmark fails to run with 60 million stencil point configuration on Raspberry Pi 3B and 3B+ because memory is insufficient.

We see a behavior similar to what was observed to the 2D stencil (Sec. 5.1) while observing strong scaling for different threads/node. For the Raspberry Pi 4, single threaded runs resulted in the best performance, and all other multi-threaded variations resulted in a similar lower performance. For the Raspberry Pi 3B and 3B+, we see improvements in result as we progress to all threads per node. A significant difference can be observed going from single core to two cores per node. Moving from two to three cores provide an additional 15% improvement. No noticeable difference is observed thereafter. The additional clock speed helps Raspberry Pi 3B+ to perform about 12% faster than 3B.

For all the Raspberry Pi models, we see a slight rise in execution time going from one to many nodes. The rise in execution time is attributed to the initialization time of the communication protocol and are not a result of increased execution times of the kernel. Again, we see the Raspberry Pi 3B+ showing better performances compared to 3B due to the higher clock speed.

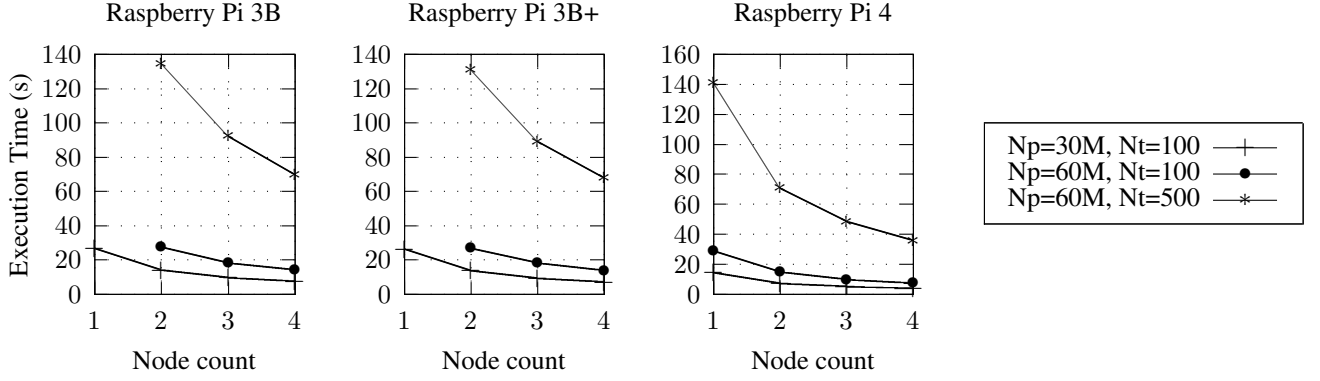
6 Energy consumption

One interesting aspect of this kind of hardware is the energy consumption [32–34]. We compute the cost for the simulations in US dollars for the 1D stencil benchmark using HPX and for the ALS benchmark using Phylanx.

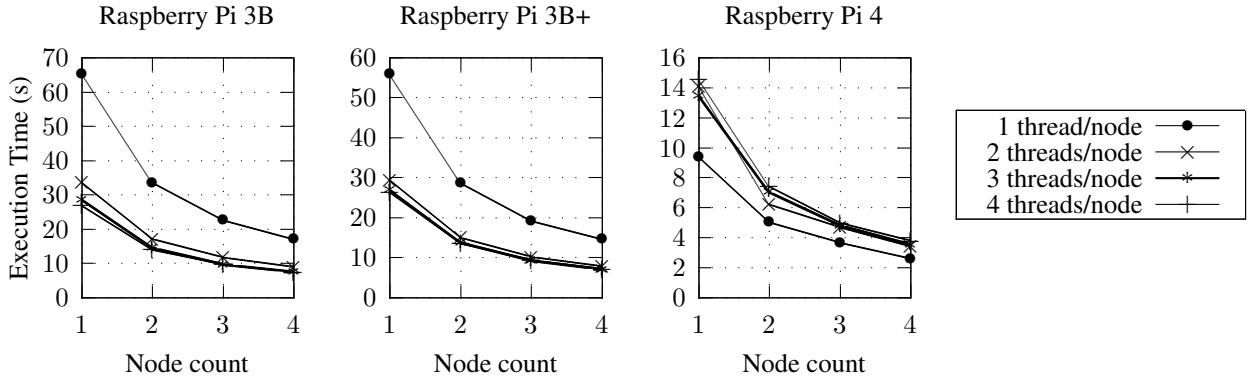
For the power consumption, we used the measurements obtained by the Linux command⁴ `stress --cpu 4` in Table 5 which were provided by Jeff Geerling⁵. Note that the Raspberry Pi device does not provide a hardware-enabled power

⁴<https://linux.die.net/man/1/stress>

⁵<https://www.pidramble.com/wiki/benchmarks/power-consumption>



(a) 1D stencil: Strong scaling results (ran on all threads per node) for different stencil points and iterations.



(b) 1D stencil: Strong scaling results (ran on all threads per node) for 30 million stencil points iterated over a 100 time steps.

Figure 8: 1D stencil: Strong Scaling results for different combinations of stencil points and iterations, and threads per node.

measurement, and we could not use the PAPI or APEX library to obtain these values. For the price per kWh, we use the average residential electricity rate in Baton Rouge is 8.2¢/kWh⁶, since the hardware is located there.

Table 5: Power consumption of various Raspberry Pi models using all four cores obtained by running the Linux command `stress --cpu 4`.

Model	Watt	milli Ampere
PI 3B	3.7	730
PI 3B+	5.1	980
PI 4	6.4	1280

First, the cost in US ¢ per iteration for the 1D stencil using 30 million stencil points, see Figure 8b was calculated. Figure 10a shows that the cost per iteration is very low for all models, the PI 4 has the lowest cost of all, because the computation time is around five times less. The PI 3B+ has the highest cost, since the time difference to the PI 3 is close, but the power consumption is around one third more.

Second, the cost in US ¢ for the ALS benchmark is shown in Figure 10b. Again, the PI 4 has the lowest cost since the computation finished in half of the time. For the PI 3B+, the cost is the highest again for the same reason as above.

⁶<https://www.electricitylocal.com/states/louisiana/baton-rouge/>

1D stencil: Weak Scaling (All threads)

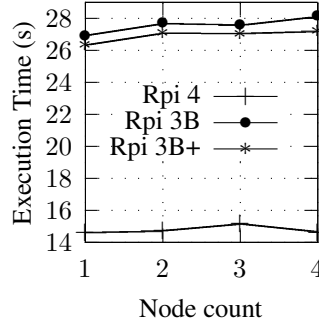
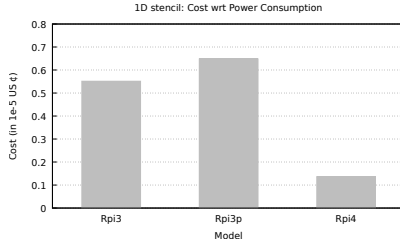
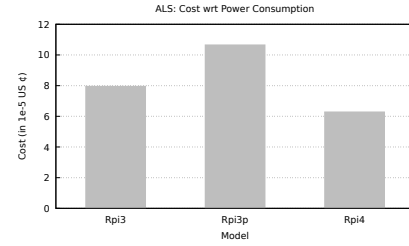


Figure 9: 1D stencil: weak scaling results (ran on all threads per node) for 30M stencil points iterated over 100 time steps.



(a) Cost with respect to power consumption for the 1D stencil code using 30 million stencil points per iteration and a total of 100 iterations.



(b) Cost with respect to power consumption for the ALS benchmark.

Figure 10: Cost with respect to power consumption for (a) 1D stencil and (b) ALS benchmark. The power consumption for all models was obtained using the Linux command `stress` for all four cores. The costs are for the state of Louisiana, since the PI cluster was located there.

However, the trade-off for energy consumption is clearly performance, as one can see in the previous section for comparing the computation time. This aligns with the references in the related work section for running other parallel and distributed application on Raspberry Pis.

7 Conclusion and Outlook

In this paper we have described how to use a cluster of Raspberry Pi (32-bit and 64-bit) for a number of small benchmarks that are part of the HPX and Phylax toolkit. To support 32-bit and 64-bit options, using the Ubuntu Server 2020 operating system is the best option. However, we examined performance issues related to vectorization, threading, clock frequency settings, and operating system choice. We note that, for purposes of benchmarking, an appropriate CPU profile needs to be set instead of the default option. In our case, we used *performance*.

We found that, due to the limited memory bandwidth, Pis are often unable to make use of all four cores. The STREAM TRIAD benchmark shows that memory bandwidth decreases for the Raspberry Pi 4 as threads are added. This is probably why performance peaks with 2 or 3 cores. Extending the observation to a distributed scale, we find that our 1D stencil benchmark scales almost linearly on a distributed scale while worsening as more threads are added per node.

In terms of energy consumption, we observed that for both benchmarks the Raspberry Pi 4 had the lowest power consumption and thus the lowest costs. However, clearly trade-off is the computational time for all three models. Furthermore, limited scalability was observed for the Raspberry Pi 3. In short, with some effort at configuration, a Raspberry Pi cluster can provide modest performance at a reasonable cost.

7.1 Outlook

From our experience, two possible use cases of the Raspberry Pi cluster can be considered. First, for the Raspberry Pi 4 cluster, an application in teaching parallel and distributing computing is imaginable. The students can see the behavior of adding threads or multiple nodes to the performance of the application. Thus, the students do not occupy more performant nodes which might be required for other valuable research.

Second, the Raspberry Pi devices provide interfaces to attach sensors such as temperature and humidity sensors. Raspberry Pis are used in field studies to collect sensor data and offloading them to a more powerful device to carry analysis over the data. Phylanx can help in such scenarios by processing data at the Pi's end before offloading.

8 Acknowledgments

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