Chapter 1
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Digital I/O Module

NOTE: This chapter is an excerpt from the *MSP430x5xx and MSP430x6xx Family User's Guide*. The latest version of the full user's guide can be downloaded from http://www.ti.com/lit/pdf/slau208.

This chapter describes the operation of the digital I/O ports in all devices.

Topic **Page**

1.1 Digital I/O Introduction

The digital I/O features include:

- Independently programmable individual I/Os
- Any combination of input or output
- Individually configurable P1 and P2 interrupts. Some devices may include additional port interrupts.
- Independent input and output data registers
- Individually configurable pullup or pulldown resistors

Devices within the family may have up to twelve digital I/O ports implemented (P1 to P11 and PJ). Most ports contain eight I/O lines; however, some ports may contain less (see the device-specific data sheet for ports available). Each I/O line is individually configurable for input or output direction, and each can be individually read or written. Each I/O line is individually configurable for pullup or pulldown resistors, as well as, configurable drive strength, full or reduced.

Ports P1 and P2 always have interrupt capability. Each interrupt for the P1 and P2 I/O lines can be individually enabled and configured to provide an interrupt on a rising or falling edge of an input signal. All P1 I/O lines source a single interrupt vector P1IV, and all P2 I/O lines source a different, single interrupt vector P2IV. On some devices, additional ports with interrupt capability may be available (see the device-specific data sheet for details) and contain their own respective interrupt vectors.

Individual ports can be accessed as byte-wide ports or can be combined into word-wide ports and accessed in word formats. Port pairs P1 and P2, P3 and P4, P5 and P6, and so on, are associated with the names PA, PB, PC, and so on, respectively. All port registers are handled in this manner with this naming convention except for the interrupt vector registers; for example, PAIV does not exist for P1IV and P2IV.

When writing to port PA with word operations, all 16 bits are written to the port. When writing to the lower byte of the PA port using byte operations, the upper byte remains unchanged. Similarly, writing to the upper byte of the PA port using byte instructions leaves the lower byte unchanged. When writing to a port that contains less than the maximum number of bits possible, the unused bits are a "don't care". Ports PB, PC, PD, PE, and PF behave similarly.

Reading of the PA port using word operations causes all 16 bits to be transferred to the destination. Reading the lower or upper byte of the PA port (P1 or P2) and storing to memory using byte operations causes only the lower or upper byte to be transferred to the destination, respectively. Reading of the PA port and storing to a general-purpose register using byte operations causes the byte transferred to be written to the least significant byte of the register. The upper significant byte of the destination register is cleared automatically. Ports PB, PC, PD, PE, and PF behave similarly. When reading from ports that contain less than the maximum bits possible, unused bits are read as zeros (similarly for port PJ).

1.2 Digital I/O Operation

The digital I/O are configured with user software. The setup and operation of the digital I/O are discussed in the following sections.

1.2.1 Input Registers (PxIN)

Each bit in each PxIN register reflects the value of the input signal at the corresponding I/O pin when the pin is configured as I/O function. These registers are read only.

- Bit = 0: Input is low
- Bit = 1: Input is high

NOTE: Writing to read-only registers PxIN

Writing to these read-only registers results in increased current consumption while the write attempt is active.

1.2.2 Output Registers (PxOUT)

Each bit in each PxOUT register is the value to be output on the corresponding I/O pin when the pin is configured as I/O function, output direction.

- Bit = 0: Output is low
- Bit = 1: Output is high

If the pin is configured as I/O function, input direction and the pullup or pulldown resistor are enabled; the corresponding bit in the PxOUT register selects pullup or pulldown.

- Bit = 0: Pin is pulled down
- Bit = 1: Pin is pulled up

1.2.3 Direction Registers (PxDIR)

Each bit in each PxDIR register selects the direction of the corresponding I/O pin, regardless of the selected function for the pin. PxDIR bits for I/O pins that are selected for other functions must be set as required by the other function.

- Bit = 0: Port pin is switched to input direction
- Bit = 1: Port pin is switched to output direction

1.2.4 Pullup or Pulldown Resistor Enable Registers (PxREN)

Each bit in each PxREN register enables or disables the pullup or pulldown resistor of the corresponding I/O pin. The corresponding bit in the PxOUT register selects if the pin contains a pullup or pulldown.

- Bit = 0: Pullup or pulldown resistor disabled
- Bit = 1: Pullup or pulldown resistor enabled

Table 1-1 summarizes the usage of PxDIR, PxREN, and PxOUT for proper I/O configuration.

Table 1-1. I/O Configuration

PxDIR	PxREN	PxOUT	I/O Configuration
0	0	x	Input
0	1	0	Input with pulldown resistor
0	1	1	Input with pullup resistor
1	x	x	Output

1.2.5 Output Drive Strength Registers (PxDS)

Each bit in each PxDS register selects either full drive or reduced drive strength. Default is reduced drive strength.

- Bit = 0: Reduced drive strength
- Bit = 1: Full drive strength

NOTE: Drive strength and EMI

All outputs default to reduced drive strength to reduce EMI. Using full drive strength can result in increased EMI.

1.2.6 Function Select Registers (PxSEL)

Port pins are often multiplexed with other peripheral module functions. See the device-specific data sheet to determine pin functions. Each PxSEL bit is used to select the pin function – I/O port or peripheral module function.

- Bit = 0: I/O Function is selected for the pin
- Bit = 1: Peripheral module function is selected for the pin

Setting PxSEL = 1 does not automatically set the pin direction. Other peripheral module functions may require the PxDIR bits to be configured according to the direction needed for the module function. See the pin schematics in the device-specific data sheet.

NOTE: P1 and P2 interrupts are disabled when PxSEL = 1

When any PxSEL bit is set, the corresponding pin's interrupt function is disabled. Therefore, signals on these pins does not generate P1 or P2 interrupts, regardless of the state of the corresponding P1IE or P2IE bit.

When a port pin is selected as an input to a peripheral, the input signal to the peripheral is a latched representation of the signal at the device pin. While its corresponding PxSEL = 1, the internal input signal follows the signal at the pin. However, if its PxSEL = 0, the input to the peripheral maintains the value of the input signal at the device pin before its corresponding PxSEL bit was reset.

1.2.7 Port Interrupts

Each pin in ports P1 and P2 has interrupt capability, configured with the PxIFG, PxIE, and PxIES registers. On some devices, additional ports have interrupt capability (see the device-specific data sheet). All P1 interrupt flags are prioritized, with P1IFG.0 being the highest, and combined to source a single interrupt vector. The highest priority enabled interrupt generates a number in the P1IV register. This number can be evaluated or added to the program counter to automatically enter the appropriate software routine. Disabled P1 interrupts do not affect the P1IV value. The same functionality exists for P2. Some devices may contain additional port interrupts besides P1 and P2. See the device specific data sheet to determine which port interrupts are available.

Each PxIFG bit is the interrupt flag for its corresponding I/O pin and is set when the selected input signal edge occurs at the pin. All PxIFG interrupt flags request an interrupt when their corresponding PxIE bit and the GIE bit are set. Software can also set each PxIFG flag, providing a way to generate a software-initiated interrupt.

- Bit = 0: No interrupt is pending
- Bit = 1: An interrupt is pending

Only transitions, not static levels, cause interrupts. If any PxIFG flag becomes set during a Px interrupt service routine, or is set after the RETI instruction of a Px interrupt service routine is executed, the set PxIFG flag generates another interrupt. This ensures that each transition is acknowledged.

NOTE: PxIFG flags when changing PxOUT, PxDIR, or PxREN

Writing to P1OUT, P1DIR, P1REN, P2OUT, P2DIR, or P2REN can result in setting the corresponding P1IFG or P2IFG flags.

Any access (read or write) of the lower byte of the P1IV register, either word or byte access, automatically resets the highest pending interrupt flag. If another interrupt flag is set, another interrupt is immediately generated after servicing the initial interrupt. For example, assume that P1IFG.0 has the highest priority. If the P1IFG.0 and P1IFG.2 flags are set when the interrupt service routine accesses the P1IV register, P1IFG.0 is reset automatically. After the RETI instruction of the interrupt service routine is executed, the P1IFG.2 generates another interrupt.

Port P2 interrupts behave similarly, and source a separate single interrupt vector and utilize the P2IV register.

1.2.7.1 Port Interrupt Software Example

The following software example shows the recommended use of P1IV and the handling overhead. The P1IV value is added to the PC to automatically jump to the appropriate routine. The P2IV is similar.

The numbers at the right margin show the necessary CPU cycles for each instruction. The software overhead for different interrupt sources includes interrupt latency and return-from-interrupt cycles, but not the task handling itself.

```
;Interrupt handler for P1                                  Cycles
P1_HND   ...                 ; Interrupt latency             6
         ADD      &P1IV,PC   ; Add offset to Jump table      3
         RETI                ; Vector  0: No interrupt       5
         JMP      P1_0_HND   ; Vector  2: Port 1 bit 0       2
         JMP      P1_1_HND   ; Vector  4: Port 1 bit 1       2
         JMP      P1_2_HND   ; Vector  6: Port 1 bit 2       2
         JMP      P1_3_HND   ; Vector  8: Port 1 bit 3       2
         JMP      P1_4_HND   ; Vector 10: Port 1 bit 4       2
         JMP      P1_5_HND   ; Vector 12: Port 1 bit 5       2
         JMP      P1_6_HND   ; Vector 14: Port 1 bit 6       2
         JMP      P1_7_HND   ; Vector 16: Port 1 bit 7       2

P1_7_HND                    ; Vector 16: Port 1 bit 7
         ...                ; Task starts here
         RETI               ; Back to main program          5

P1_6_HND                    ; Vector 14: Port 1 bit 6
         ...                ; Task starts here
         RETI               ; Back to main program          5

P1_5_HND                    ; Vector 12: Port 1 bit 5
         ...                ; Task starts here
         RETI               ; Back to main program          5

P1_4_HND                    ; Vector 10: Port 1 bit 4
         ...                ; Task starts here
         RETI               ; Back to main program          5

P1_3_HND                    ; Vector 8: Port 1 bit 3
         ...                ; Task starts here
         RETI               ; Back to main program          5

P1_2_HND                    ; Vector 6: Port 1 bit 2
         ...                ; Task starts here
         RETI               ; Back to main program          5

P1_1_HND                    ; Vector 4: Port 1 bit 1
         ...                ; Task starts here
         RETI               ; Back to main program          5
P1_0_HND                    ; Vector 2: Port 1 bit 0
```

```
...                 ; Task starts here
RETI                ; Back to main program        5
```

1.2.7.2 Interrupt Edge Select Registers (PxIES)

Each PxIES bit selects the interrupt edge for the corresponding I/O pin.

- Bit = 0: Respective PxIFG flag is set with a low-to-high transition
- Bit = 1: Respective PxIFG flag is set with a high-to-low transition

NOTE: Writing to PxIES

Writing to P1IES or P2IES for each corresponding I/O can result in setting the corresponding interrupt flags.

PxIES	PxIN	PxIFG
0 → 1	0	Will be set
0 → 1	1	Unchanged
1 → 0	0	Unchanged
1 → 0	1	Will be set

1.2.7.3 Interrupt Enable Registers (PxIE)

Each PxIE bit enables the associated PxIFG interrupt flag.

- Bit = 0: The interrupt is disabled
- Bit = 1: The interrupt is enabled

1.2.8 Configuring Unused Port Pins

Unused I/O pins should be configured as I/O function, output direction, and left unconnected on the PC board, to prevent a floating input and reduce power consumption. The value of the PxOUT bit is don't care, because the pin is unconnected. Alternatively, the integrated pullup or pulldown resistor can be enabled by setting the PxREN bit of the unused pin to prevent the floating input. See the SYS chapter for termination of unused pins.

NOTE: Configuring port J and shared JTAG pins:

Application should ensure that port PJ is configured properly to prevent a floating input. Because port PJ is shared with the JTAG function, floating inputs may not be noticed when in an emulation environment. Port J is initialized to high-impedance inputs by default.

1.3 I/O Configuration and LPMx.5 Low-Power Modes

NOTE: The LPMx.5 low-power modes may not be available on all devices. The LPM4.5 power mode allows for lowest power consumption and no clocks are available. The LPM3.5 power mode allows for RTC mode operation at the lowest power consumption available. See the SYS chapter for details; also see the device-specific datasheet for LPMx.5 low-power modes that are available. With respect to the digital I/O, this section is applicable for both LPM3.5 and LPM4.5.

The regulator of the Power Management Module (PMM) is disabled upon entering LPMx.5 (LPM3.5 or LPM4.5), which causes all I/O register configurations to be lost. Because the I/O register configurations are lost, the configuration of I/O pins must be handled differently to ensure that all pins in the application behave in a controlled manner upon entering and exiting LPMx.5. Properly setting the I/O pins is critical to achieving the lowest possible power consumption in LPMx.5, as well as preventing any possible uncontrolled input or output I/O state in the application. The application has complete control of the I/O pin conditions preventing the possibility of unwanted spurious activity upon entry and exit from LPMx.5. The detailed flow for entering and exiting LPMx.5 with respect to the I/O operation is as follows:

1. Set all I/Os to general-purpose I/Os and configure as needed. Each I/O can be set to input high impedance, input with pulldown, input with pullup, output high (low or high drive strength), or output low (low or high drive strength). It is critical that no inputs are left floating in the application, otherwise excess current may be drawn in LPMx.5. Configuring the I/O in this manner ensures that each pin is in a safe condition before entering LPMx.5.

   Optionally, configure input interrupt pins for wakeup from LPMx.5. To wake the device from LPMx.5, a general-purpose I/O port must contain an input port with interrupt capability. Not all devices include wakeup from LPMx.5 by I/O, and not all inputs with interrupt capability offer wakeup from LPMx.5. See the device-specific data sheet for availability. To configure a port to wake the device, the I/O should be configured properly before entering LPMx.5. Each port should be configured as general-purpose input. Pulldowns or pullups can be applied if required. Setting the PxIES bit of the corresponding register determines the edge transition that wakes the device. Last, the PxIE for the port must be enabled, as well as the general interrupt enable.

   NOTE: It is not possible to wake from LPMx.5 if the respective I/O interrupt flag is already asserted. It is recommended that the respective flag be cleared before entering LPMx.5. It is also recommended that GIE = 1 be set before entry into LPMx.5. Any pending flags in this case could then be serviced before LPMx.5 entry.

   Although it is recommended to set GIE = 1 before entering LPMx.5, it is not required. Device wakeup from LPMx.5 with an enabled wake-up function still causes the device to wake from LPMx.5 even with GIE = 0. If GIE = 0 before LPMx.5, additional care may be required. If the respective interrupt event occurs during LPMx.5 entry, the device may not recognize this or any future interrupt wakeup event on this function.

2. Enter LPMx.5 with LPMx.5 entry sequence, enable general interrupts for wakeup:

```
MOV.B #PMMPW_H, &PMMCTL0_H                ; Open PMM registers for write
BIS.B #PMMREGOFF, &PMMCTL0_L              ;
BIS   #GIE+CPUOFF+OSCOFF+SCG1+SCG0,SR     ; Enter LPMx.5 when PMMREGOFF is set
```

3. Upon entry into LPMx.5, the LOCKLPM5 bit in the PM5CTL0 register of the PMM module is set automatically. The I/O pin states are held and locked based on the settings before LPMx.5 entry. Note that only the pin conditions are retained. All other port configuration register settings such as PxDIR, PxREN, PxOUT, PxDS, PxIES, and PxIE contents are lost.
4. An LPMx.5 wake-up event (for example, an edge on a configured wake-up input pin) starts the BOR entry sequence together with the regulator. All peripheral registers are set to their default conditions. Upon exit from LPMx.5, the I/O pins remain locked while LOCKLPM5 remains set. Keeping the I/O pins locked ensures that all pin conditions remain stable upon entering the active mode regardless of the default I/O register settings.
5. When in active mode, the I/O configuration and I/O interrupt configuration that was not retained during LPMx.5 should be restored to the values before entering LPMx.5. It is recommended to reconfigure the PxIES and PxIE to their previous settings to prevent a false port interrupt from occurring. The LOCKLPM5 bit can then be cleared, which releases the I/O pin conditions and I/O interrupt configuration. Any changes to the port configuration registers while LOCKLPM5 is set have no effect on the I/O pins.
6. After enabling the I/O interrupts, the I/O interrupt that caused the wakeup can be serviced indicated by the PxIFG flags. These flags can be used directly, or the corresponding PxIV register may be used. Note that the PxIFG flag cannot be cleared until the LOCKLPM5 bit has been cleared.

NOTE: It is possible that multiple events occurred on various ports. In these cases, multiple PxIFG flags will be set, and it cannot be determined which port has caused the I/O wakeup.

1.4 Digital I/O Registers

The digital I/O registers are listed in Table 1-2. The base addresses can be found in the device-specific data sheet. Each port grouping begins at its base address. The address offsets are given in Table 1-2.

NOTE: All registers have word or byte register access. For a generic register *ANYREG*, the suffix "_L" (*ANYREG_L*) refers to the lower byte of the register (bits 0 through 7). The suffix "_H" (*ANYREG_H*) refers to the upper byte of the register (bits 8 through 15).

Table 1-2. Digital I/O Registers

Offset	Acronym	Register Name	Type	Access	Reset	Section
0Eh	P1IV	Port 1 Interrupt Vector	Read only	Word	0000h	Section 1.4.1
0Eh	P1IV_L		Read only	Byte	00h	
0Fh	P1IV_H		Read only	Byte	00h	
1Eh	P2IV	Port 2 Interrupt Vector	Read only	Word	0000h	Section 1.4.2
1Eh	P2IV_L		Read only	Byte	00h	
1Fh	P2IV_H		Read only	Byte	00h	
00h	P1IN or PAIN_L	Port 1 Input	Read only	Byte		Section 1.4.9
02h	P1OUT or PAOUT_L	Port 1 Output	Read/write	Byte	undefined	Section 1.4.10
04h	P1DIR or PADIR_L	Port 1 Direction	Read/write	Byte	00h	Section 1.4.11
06h	P1REN or PAREN_L	Port 1 Resistor Enable	Read/write	Byte	00h	Section 1.4.12
08h	P1DS or PADS_L	Port 1 Drive Strength	Read/write	Byte	00h	Section 1.4.13
0Ah	P1SEL or PASEL_L	Port 1 Port Select	Read/write	Byte	00h	Section 1.4.14
18h	P1IES or PAIES_L	Port 1 Interrupt Edge Select	Read/write	Byte	undefined	Section 1.4.3
1Ah	P1IE or PAIE_L	Port 1 Interrupt Enable	Read/write	Byte	00h	Section 1.4.4
1Ch	P1IFG or PAIFG_L	Port 1 Interrupt Flag	Read/write	Byte	00h	Section 1.4.5
01h	P2IN or PAIN_H	Port 2 Input	Read only	Byte		Section 1.4.9
03h	P2OUT or PAOUT_H	Port 2 Output	Read/write	Byte	undefined	Section 1.4.10
05h	P2DIR or PADIR_H	Port 2 Direction	Read/write	Byte	00h	Section 1.4.11
07h	P2REN or PAREN_H	Port 2 Resistor Enable	Read/write	Byte	00h	Section 1.4.12
09h	P2DS or PADS_H	Port 2 Drive Strength	Read/write	Byte	00h	Section 1.4.13
0Bh	P2SEL or PASEL_H	Port 2 Port Select	Read/write	Byte	00h	Section 1.4.14
19h	P2IES or PAIES_H	Port 2 Interrupt Edge Select	Read/write	Byte	undefined	Section 1.4.6
1Bh	P2IE or PAIE_H	Port 2 Interrupt Enable	Read/write	Byte	00h	Section 1.4.7
1Dh	P2IFG or PAIFG_H	Port 2 Interrupt Flag	Read/write	Byte	00h	Section 1.4.8
00h	P3IN or PBIN_L	Port 3 Input	Read only	Byte		Section 1.4.9
02h	P3OUT or PBOUT_L	Port 3 Output	Read/write	Byte	undefined	Section 1.4.10

Table 1-2. Digital I/O Registers (continued)

Offset	Acronym	Register Name	Type	Access	Reset	Section
04h	P3DIR or PBDIR_L	Port 3 Direction	Read/write	Byte	00h	Section 1.4.11
06h	P3REN or PBREN_L	Port 3 Resistor Enable	Read/write	Byte	00h	Section 1.4.12
08h	P3DS or PBDS_L	Port 3 Drive Strength	Read/write	Byte	00h	Section 1.4.13
0Ah	P3SEL or PBSEL_L	Port 3 Port Select	Read/write	Byte	00h	Section 1.4.14
01h	P4IN or PBIN_H	Port 4 Input	Read only	Byte		Section 1.4.9
03h	P4OUT or PBOUT_H	Port 4 Output	Read/write	Byte	undefined	Section 1.4.10
05h	P4DIR or PBDIR_H	Port 4 Direction	Read/write	Byte	00h	Section 1.4.11
07h	P4REN or PBREN_H	Port 4 Resistor Enable	Read/write	Byte	00h	Section 1.4.12
09h	P4DS or PBDS_H	Port 4 Drive Strength	Read/write	Byte	00h	Section 1.4.13
0Bh	P4SEL or PBSEL_H	Port 4 Port Select	Read/write	Byte	00h	Section 1.4.14
00h	P5IN or PCIN_L	Port 5 Input	Read only	Byte		Section 1.4.9
02h	P5OUT or PCOUT_L	Port 5 Output	Read/write	Byte	undefined	Section 1.4.10
04h	P5DIR or PCDIR_L	Port 5 Direction	Read/write	Byte	00h	Section 1.4.11
06h	P5REN or PCREN_L	Port 5 Resistor Enable	Read/write	Byte	00h	Section 1.4.12
08h	P5DS or PCDS_L	Port 5 Drive Strength	Read/write	Byte	00h	Section 1.4.13
0Ah	P5SEL or PCSEL_L	Port 5 Port Select	Read/write	Byte	00h	Section 1.4.14
01h	P6IN or PCIN_H	Port 6 Input	Read only	Byte		Section 1.4.9
03h	P6OUT or PCOUT_H	Port 6 Output	Read/write	Byte	undefined	Section 1.4.10
05h	P6DIR or PCDIR_H	Port 6 Direction	Read/write	Byte	00h	Section 1.4.11
07h	P6REN or PCREN_H	Port 6 Resistor Enable	Read/write	Byte	00h	Section 1.4.12
09h	P6DS or PCDS_H	Port 6 Drive Strength	Read/write	Byte	00h	Section 1.4.13
0Bh	P6SEL or PCSEL_H	Port 6 Port Select	Read/write	Byte	00h	Section 1.4.14
00h	P7IN or PDIN_L	Port 7 Input	Read only	Byte		Section 1.4.9
02h	P7OUT or PDOUT_L	Port 7 Output	Read/write	Byte	undefined	Section 1.4.10
04h	P7DIR or PDDIR_L	Port 7 Direction	Read/write	Byte	00h	Section 1.4.11
06h	P7REN or PDREN_L	Port 7 Resistor Enable	Read/write	Byte	00h	Section 1.4.12
08h	P7DS or PDDS_L	Port 7 Drive Strength	Read/write	Byte	00h	Section 1.4.13
0Ah	P7SEL or PDSEL_L	Port 7 Port Select	Read/write	Byte	00h	Section 1.4.14

Table 1-2. Digital I/O Registers (continued)

Offset	Acronym	Register Name	Type	Access	Reset	Section
01h	P8IN or PDIN_H	Port 8 Input	Read only	Byte		Section 1.4.9
03h	P8OUT or PDOUT_H	Port 8 Output	Read/write	Byte	undefined	Section 1.4.10
05h	P8DIR or PDDIR_H	Port 8 Direction	Read/write	Byte	00h	Section 1.4.11
07h	P8REN or PDREN_H	Port 8 Resistor Enable	Read/write	Byte	00h	Section 1.4.12
09h	P8DS or PDDS_H	Port 8 Drive Strength	Read/write	Byte	00h	Section 1.4.13
0Bh	P8SEL or PDSEL_H	Port 8 Port Select	Read/write	Byte	00h	Section 1.4.14
00h	P9IN or PEIN_L	Port 9 Input	Read only	Byte		Section 1.4.9
02h	P9OUT or PEOUT_L	Port 9 Output	Read/write	Byte	undefined	Section 1.4.10
04h	P9DIR or PEDIR_L	Port 9 Direction	Read/write	Byte	00h	Section 1.4.11
06h	P9REN or PEREN_L	Port 9 Resistor Enable	Read/write	Byte	00h	Section 1.4.12
08h	P9DS or PEDS_L	Port 9 Drive Strength	Read/write	Byte	00h	Section 1.4.13
0Ah	P9SEL or PESEL_L	Port 9 Port Select	Read/write	Byte	00h	Section 1.4.14
01h	P10IN or PEIN_H	Port 10 Input	Read only	Byte		Section 1.4.9
03h	P10OUT or PEOUT_H	Port 10 Output	Read/write	Byte	undefined	Section 1.4.10
05h	P10DIR or PEDIR_H	Port 10 Direction	Read/write	Byte	00h	Section 1.4.11
07h	P10REN or PEREN_H	Port 10 Resistor Enable	Read/write	Byte	00h	Section 1.4.12
09h	P10DS or PEDS_H	Port 10 Drive Strength	Read/write	Byte	00h	Section 1.4.13
0Bh	P10SEL or PESEL_H	Port 10 Port Select	Read/write	Byte	00h	Section 1.4.14
00h	P11IN or PFIN_L	Port 11 Input	Read only	Byte		Section 1.4.9
02h	P11OUT or PFOUT_L	Port 11 Output	Read/write	Byte	undefined	Section 1.4.10
04h	P11DIR or PFDIR_L	Port 11 Direction	Read/write	Byte	00h	Section 1.4.11
06h	P11REN or PFREN_L	Port 11 Resistor Enable	Read/write	Byte	00h	Section 1.4.12
08h	P11DS or PFDS_L	Port 11 Drive Strength	Read/write	Byte	00h	Section 1.4.13
0Ah	P11SEL or PFSEL_L	Port 11 Port Select	Read/write	Byte	00h	Section 1.4.14
00h	PAIN	Port A Input	Read only	Word		
00h	PAIN_L		Read only	Byte		
01h	PAIN_H		Read only	Byte		
02h	PAOUT	Port A Output	Read/write	Word	undefined	
02h	PAOUT_L		Read/write	Byte	undefined	
03h	PAOUT_H		Read/write	Byte	undefined	
04h	PADIR	Port A Direction	Read/write	Word	0000h	

Table 1-2. Digital I/O Registers (continued)

Offset	Acronym	Register Name	Type	Access	Reset	Section
04h	PADIR_L		Read/write	Byte	00h	
05h	PADIR_H		Read/write	Byte	00h	
06h	PAREN	Port A Resistor Enable	Read/write	Word	0000h	
06h	PAREN_L		Read/write	Byte	00h	
07h	PAREN_H		Read/write	Byte	00h	
08h	PADS	Port A Drive Strength	Read/write	Word	0000h	
08h	PADS_L		Read/write	Byte	00h	
09h	PADS_H		Read/write	Byte	00h	
0Ah	PASEL	Port A Port Select	Read/write	Word	0000h	
0Ah	PASEL_L		Read/write	Byte	00h	
0Bh	PASEL_H		Read/write	Byte	00h	
18h	PAIES	Port A Interrupt Edge Select	Read/write	Word	undefined	
18h	PAIES_L		Read/write	Byte	undefined	
19h	PAIES_H		Read/write	Byte	undefined	
1Ah	PAIE	Port A Interrupt Enable	Read/write	Word	0000h	
1Ah	PAIE_L		Read/write	Byte	00h	
1Bh	PAIE_H		Read/write	Byte	00h	
1Ch	PAIFG	Port A Interrupt Flag	Read/write	Word	0000h	
1Ch	PAIFG_L		Read/write	Byte	00h	
1Dh	PAIFG_H		Read/write	Byte	00h	
00h	PBIN	Port B Input	Read only	Word		
00h	PBIN_L		Read only	Byte		
01h	PBIN_H		Read only	Byte		
02h	PBOUT	Port B Output	Read/write	Word	undefined	
02h	PBOUT_L		Read/write	Byte	undefined	
03h	PBOUT_H		Read/write	Byte	undefined	
04h	PBDIR	Port B Direction	Read/write	Word	0000h	
04h	PBDIR_L		Read/write	Byte	00h	
05h	PBDIR_H		Read/write	Byte	00h	
06h	PBREN	Port B Resistor Enable	Read/write	Word	0000h	
06h	PBREN_L		Read/write	Byte	00h	
07h	PBREN_H		Read/write	Byte	00h	
08h	PBDS	Port B Drive Strength	Read/write	Word	0000h	
08h	PBDS_L		Read/write	Byte	00h	
09h	PBDS_H		Read/write	Byte	00h	
0Ah	PBSEL	Port B Port Select	Read/write	Word	0000h	
0Ah	PBSEL_L		Read/write	Byte	00h	
0Bh	PBSEL_H		Read/write	Byte	00h	
00h	PCIN	Port C Input	Read only	Word		
00h	PCIN_L		Read only	Byte		
01h	PCIN_H		Read only	Byte		
02h	PCOUT	Port C Output	Read/write	Word	undefined	
02h	PCOUT_L		Read/write	Byte	undefined	
03h	PCOUT_H		Read/write	Byte	undefined	
04h	PCDIR	Port C Direction	Read/write	Word	0000h	
04h	PCDIR_L		Read/write	Byte	00h	
05h	PCDIR_H		Read/write	Byte	00h	

Table 1-2. Digital I/O Registers (continued)

Offset	Acronym	Register Name	Type	Access	Reset	Section
06h	PCREN	Port C Resistor Enable	Read/write	Word	0000h	
06h	PCREN_L		Read/write	Byte	00h	
07h	PCREN_H		Read/write	Byte	00h	
08h	PCDS	Port C Drive Strength	Read/write	Word	0000h	
08h	PCDS_L		Read/write	Byte	00h	
09h	PCDS_H		Read/write	Byte	00h	
0Ah	PCSEL	Port C Port Select	Read/write	Word	0000h	
0Ah	PCSEL_L		Read/write	Byte	00h	
0Bh	PCSEL_H		Read/write	Byte	00h	
00h	PDIN	Port D Input	Read only	Word		
00h	PDIN_L		Read only	Byte		
01h	PDIN_H		Read only	Byte		
02h	PDOUT	Port D Output	Read/write	Word	undefined	
02h	PDOUT_L		Read/write	Byte	undefined	
03h	PDOUT_H		Read/write	Byte	undefined	
04h	PDDIR	Port D Direction	Read/write	Word	0000h	
04h	PDDIR_L		Read/write	Byte	00h	
05h	PDDIR_H		Read/write	Byte	00h	
06h	PDREN	Port D Resistor Enable	Read/write	Word	0000h	
06h	PDREN_L		Read/write	Byte	00h	
07h	PDREN_H		Read/write	Byte	00h	
08h	PDDS	Port D Drive Strength	Read/write	Word	0000h	
08h	PDDS_L		Read/write	Byte	00h	
09h	PDDS_H		Read/write	Byte	00h	
0Ah	PDSEL	Port D Port Select	Read/write	Word	0000h	
0Ah	PDSEL_L		Read/write	Byte	00h	
0Bh	PDSEL_H		Read/write	Byte	00h	
00h	PEIN	Port E Input	Read only	Word		
00h	PEIN_L		Read only	Byte		
01h	PEIN_H		Read only	Byte		
02h	PEOUT	Port E Output	Read/write	Word	undefined	
02h	PEOUT_L		Read/write	Byte	undefined	
03h	PEOUT_H		Read/write	Byte	undefined	
04h	PEDIR	Port E Direction	Read/write	Word	0000h	
04h	PEDIR_L		Read/write	Byte	00h	
05h	PEDIR_H		Read/write	Byte	00h	
06h	PEREN	Port E Resistor Enable	Read/write	Word	0000h	
06h	PEREN_L		Read/write	Byte	00h	
07h	PEREN_H		Read/write	Byte	00h	
08h	PEDS	Port E Drive Strength	Read/write	Word	0000h	
08h	PEDS_L		Read/write	Byte	00h	
09h	PEDS_H		Read/write	Byte	00h	
0Ah	PESEL	Port E Port Select	Read/write	Word	0000h	
0Ah	PESEL_L		Read/write	Byte	00h	
0Bh	PESEL_H		Read/write	Byte	00h	
00h	PFIN	Port F Input	Read only	Word		
00h	PFIN_L		Read only	Byte		

Table 1-2. Digital I/O Registers (continued)

Offset	Acronym	Register Name	Type	Access	Reset	Section
01h	PFIN_H		Read only	Byte		
02h	PFOUT	Port F Output	Read/write	Word	undefined	
02h	PFOUT_L		Read/write	Byte	undefined	
03h	PFOUT_H		Read/write	Byte	undefined	
04h	PFDIR	Port F Direction	Read/write	Word	0000h	
04h	PFDIR_L		Read/write	Byte	00h	
05h	PFDIR_H		Read/write	Byte	00h	
06h	PFREN	Port F Resistor Enable	Read/write	Word	0000h	
06h	PFREN_L		Read/write	Byte	00h	
07h	PFREN_H		Read/write	Byte	00h	
08h	PFDS	Port F Drive Strength	Read/write	Word	0000h	
08h	PFDS_L		Read/write	Byte	00h	
09h	PFDS_H		Read/write	Byte	00h	
0Ah	PFSEL	Port F Port Select	Read/write	Word	0000h	
0Ah	PFSEL_L		Read/write	Byte	00h	
0Bh	PFSEL_H		Read/write	Byte	00h	
00h	PJIN	Port J Input	Read only	Word		
00h	PJIN_L		Read only	Byte		
01h	PJIN_H		Read only	Byte		
02h	PJOUT	Port J Output	Read/write	Word	undefined	
02h	PJOUT_L		Read/write	Byte	undefined	
03h	PJOUT_H		Read/write	Byte	undefined	
04h	PJDIR	Port J Direction	Read/write	Word	0000h	
04h	PJDIR_L		Read/write	Byte	00h	
05h	PJDIR_H		Read/write	Byte	00h	
06h	PJREN	Port J Resistor Enable	Read/write	Word	0000h	
06h	PJREN_L		Read/write	Byte	00h	
07h	PJREN_H		Read/write	Byte	00h	
08h	PJDS	Port J Drive Strength	Read/write	Word	0000h	
08h	PJDS_L		Read/write	Byte	00h	
09h	PJDS_H		Read/write	Byte	00h	
0Ah	PJSEL	Port J Port Select	Read/write	Word	0000h	
0Ah	PJSEL_L		Read/write	Byte	00h	
0Bh	PJSEL_H		Read/write	Byte	00h	

1.4.1 P1IV Register

Port 1 Interrupt Vector Register

Figure 1-1. P1IV Register

15	14	13	12	11	10	9	8
P1IV							
r0	r0	r0	r0	r0	r0	r0	r0
7	6	5	4	3	2	1	0
P1IV							
r0	r0	r0	r-0	r-0	r-0	r-0	r0

Table 1-3. P1IV Register Description

Bit	Field	Type	Reset	Description
15-0	P1IV	R	0h	Port 1 interrupt vector value 00h = No interrupt pending 02h = Interrupt Source: Port 1.0 interrupt; Interrupt Flag: P1IFG.0; Interrupt Priority: Highest 04h = Interrupt Source: Port 1.1 interrupt; Interrupt Flag: P1IFG.1 06h = Interrupt Source: Port 1.2 interrupt; Interrupt Flag: P1IFG.2 08h = Interrupt Source: Port 1.3 interrupt; Interrupt Flag: P1IFG.3 0Ah = Interrupt Source: Port 1.4 interrupt; Interrupt Flag: P1IFG.4 0Ch = Interrupt Source: Port 1.5 interrupt; Interrupt Flag: P1IFG.5 0Eh = Interrupt Source: Port 1.6 interrupt; Interrupt Flag: P1IFG.6 10h = Interrupt Source: Port 1.7 interrupt; Interrupt Flag: P1IFG.7; Interrupt Priority: Lowest

1.4.2 P2IV Register

Port 2 Interrupt Vector Register

Figure 1-2. P2IV Register

15	14	13	12	11	10	9	8
P2IV							
r0	r0	r0	r0	r0	r0	r0	r0
7	6	5	4	3	2	1	0
P2IV							
r0	r0	r0	r-0	r-0	r-0	r-0	r0

Table 1-4. P2IV Register Description

Bit	Field	Type	Reset	Description
15-0	P2IV	R	0h	Port 2 interrupt vector value 00h = No interrupt pending 02h = Interrupt Source: Port 2.0 interrupt; Interrupt Flag: P2IFG.0; Interrupt Priority: Highest 04h = Interrupt Source: Port 2.1 interrupt; Interrupt Flag: P2IFG.1 06h = Interrupt Source: Port 2.2 interrupt; Interrupt Flag: P2IFG.2 08h = Interrupt Source: Port 2.3 interrupt; Interrupt Flag: P2IFG.3 0Ah = Interrupt Source: Port 2.4 interrupt; Interrupt Flag: P2IFG.4 0Ch = Interrupt Source: Port 2.5 interrupt; Interrupt Flag: P2IFG.5 0Eh = Interrupt Source: Port 2.6 interrupt; Interrupt Flag: P2IFG.6 10h = Interrupt Source: Port 2.7 interrupt; Interrupt Flag: P2IFG.7; Interrupt Priority: Lowest

1.4.3 P1IES Register

Port 1 Interrupt Edge Select Register

Figure 1-3. P1IES Register

7	6	5	4	3	2	1	0
P1IES							
rw	rw	rw	rw	rw	rw	rw	rw

Table 1-5. P1IES Register Description

Bit	Field	Type	Reset	Description
7-0	P1IES	RW	undefined	Port 1 interrupt edge select 0b = P1IFG flag is set with a low-to-high transition. 1b = P1IFG flag is set with a high-to-low transition.

1.4.4 P1IE Register

Port 1 Interrupt Enable Register

Figure 1-4. P1IE Register

7	6	5	4	3	2	1	0
P1IE							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 1-6. P1IE Register Description

Bit	Field	Type	Reset	Description
7-0	P1IE	RW	0h	Port 1 interrupt enable 0b = Corresponding port interrupt disabled 1b = Corresponding port interrupt enabled

1.4.5 P1IFG Register

Port 1 Interrupt Flag Register

Figure 1-5. P1IFG Register

7	6	5	4	3	2	1	0
P1IFG							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 1-7. P1IFG Register Description

Bit	Field	Type	Reset	Description
7-0	P1IFG	RW	0h	Port 1 interrupt flag 0b = No interrupt is pending 1b = Interrupt is pending

1.4.6 P2IES Register

Port 2 Interrupt Edge Select Register

Figure 1-6. P2IES Register

7	6	5	4	3	2	1	0
P2IES							
rw	rw	rw	rw	rw	rw	rw	rw

Table 1-8. P2IES Register Description

Bit	Field	Type	Reset	Description
7-0	P2IES	RW	undefined	Port 2 interrupt edge select 0b = P2IFG flag is set with a low-to-high transition. 1b = P2IFG flag is set with a high-to-low transition.

1.4.7 P2IE Register

Port 2 Interrupt Enable Register

Figure 1-7. P2IE Register

7	6	5	4	3	2	1	0
P2IE							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 1-9. P2IE Register Description

Bit	Field	Type	Reset	Description
7-0	P2IE	RW	0h	Port 2 interrupt enable 0b = Corresponding port interrupt disabled 1b = Corresponding port interrupt enabled

1.4.8 P2IFG Register

Port 2 Interrupt Flag Register

Figure 1-8. P2IFG Register

7	6	5	4	3	2	1	0
P2IFG							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 1-10. P2IFG Register Description

Bit	Field	Type	Reset	Description
7-0	P2IFG	RW	0h	Port 2 interrupt flag 0b = No interrupt is pending 1b = Interrupt is pending

1.4.9 PxIN Register

Port x Input Register

Figure 1-9. PxIN Register

7	6	5	4	3	2	1	0
PxIN							
r	r	r	r	r	r	r	r

Table 1-11. PxIN Register Description

Bit	Field	Type	Reset	Description
7-0	PxIN	R	undefined	Port x input. Read only.

1.4.10 PxOUT Register

Port x Output Register

Figure 1-10. PxOUT Register

7	6	5	4	3	2	1	0
PxOUT							
rw	rw	rw	rw	rw	rw	rw	rw

Table 1-12. PxOUT Register Description

Bit	Field	Type	Reset	Description
7-0	PxOUT	RW	undefined	Port x output When I/O configured to output mode: 0b = Output is low 1b = Output is high When I/O configured to input mode and pullups/pulldowns enabled: 0b = Pulldown selected 1b = Pullup selected

1.4.11 PxDIR Register

Port x Direction Register

Figure 1-11. PxDIR Register

7	6	5	4	3	2	1	0
PxDIR							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 1-13. PxDIR Register Description

Bit	Field	Type	Reset	Description
7-0	PxDIR	RW	0h	Port x direction 0b = Port configured as input 1b = Port configured as output

1.4.12 PxREN Register

Port x Pullup/Pulldown Resistor Enable Register

Figure 1-12. PxREN Register

7	6	5	4	3	2	1	0
PxREN							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 1-14. PxREN Register Description

Bit	Field	Type	Reset	Description
7-0	PxREN	RW	0h	Port x pullup or pulldown resistor enable. When respective port is configured as input, setting this bit will enable the pullup or pulldown. See Table 1-1 0b = Pullup or pulldown disabled 1b = Pullup or pulldown enabled

1.4.13 PxDS Register

Port x Drive Strength Register

Figure 1-13. PxDS Register

7	6	5	4	3	2	1	0
PxDS							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 1-15. PxDS Register Description

Bit	Field	Type	Reset	Description
7-0	PxDS	RW	0h	Port x drive strength 0b = Reduced output drive strength 1b = Full output drive strength

1.4.14 PxSEL Register

Port x Port Select Register

Figure 1-14. PxSEL Register

7	6	5	4	3	2	1	0
PxSEL							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 1-16. PxSEL Register Description

Bit	Field	Type	Reset	Description
7-0	PxSEL	RW	0h	Port x function selection 0b = I/O function is selected 1b = Peripheral module function is selected

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