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Lockdown Period
Open Practice Test Series
(Also useful for ESE & Other Exams)

EE : ELECTRICAL ENGINEERING
TEST No. - 10 | DIGITAL ELECTRONICS

Read the following instructions carefully

1. This question paper contains 33 MCQ's & NAQ's. Bifurcation of the questions are given below:

Subjectwise Test Pattern

Questions	Question Type	No. of Questions	Marks	Total Marks	Negative Marking
1 to 9	Multiple Choice Ques.	9	1	9	0.33
10 to 16	Numerical Answer Type Ques.	7	1	7	None
17 to 25	Multiple Choice Ques.	9	2	18	0.66
26 to 33	Numerical Answer Type Ques.	8	2	16	None
Total Questions : 33		**Total Marks : 50**		**Total Duration : 90 min**	

2. Choose the closest numerical answer among the choices given.

Multiple Choice Questions : Q.1 to Q.9 carry 1 mark each

Q.1 Which one of the following is the correct sequence of numbers (in base 10) represented in the series $(2)_3$, $(5)_6$, $(13)_5$, $(15)_6$?

(a) 2, 5, 10, 12 (b) 2, 5, 8, 11

(c) 3, 7, 10, 14 (d) 3, 8, 13, 17

1. (b)

Converting into decimal,

$$(2)_3 = 2 \times 3^0 = 2$$
$$(5)_6 = 5 \times 6^0 = 5$$
$$(13)_5 = 1 \times 5^1 + 3 \times 5^0 = 8$$
$$(15)_6 = 1 \times 6^1 + 5 \times 6^0 = 11$$

Q.2 Let $F(A,B) = \overline{A} + \overline{B}$, then the value of $f(f(x + y, y), z)$ = ?

(a) $\overline{y} + z$ (b) $\overline{y} + \overline{z}$

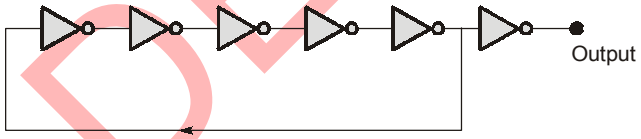
(c) $y + \overline{z}$ (d) $\overline{y + z}$

2. (c)

$$A = x + y$$
$$B = y$$
$$f(x + y, y) = \left(\overline{x + y}\right) + \overline{y} = \overline{x}.\overline{y} + \overline{y}$$

So, $$f(\overline{y},z) = \overline{\overline{y}} + \overline{z} = y + \overline{z}$$

Q.3 In the circuit shown below, the propagation delay of each NOT gate is 2 nsec (2 nano sec), then the time period of generated square wave at output is –



(a) 10 nsec (b) 14 nsec

(c) 18 nsec (d) 20 nsec

3. (d)

$$N = 5,$$
$$t_{pd} = 2 \text{ nsec}$$
$$T = 2 N t_{pd}$$
$$\Rightarrow \quad T = 2 \times 5 \times 2 \times 10^{-9}$$
$$= 20 \text{ nsec}$$

Q.4 For a 4-bit addition, loop ahead carrry generator requires.

(a) 4-OR, 5-AND (b) 4-OR, 10-AND

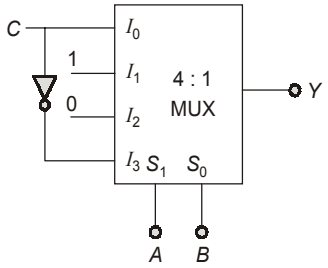
(c) 2-OR, 4-AND (d) 5-OR, 7-AND

4. (b)

For n bits,

$$\text{No. of OR gates} = n$$
$$= 4$$
$$\text{No. of AND Gates} = \frac{n(n+1)}{2} = \frac{4 \times 5}{2} = 10$$

Q.5 The output of the given 4 : 1 MUX will be



(a) $\Sigma m\,(1,2,3,6)$ (b) $\Sigma m\,(2,4,5,7)$

(c) $\Sigma m\,(1,3,4,7)$ (d) $\Sigma m\,(1,2,6,7)$

5. (a)

$$\begin{aligned} Y &= \bar{S}_0\bar{S}_1I_0 + S_0\bar{S}_1I_1 + \bar{S}_0S_1I_2 + S_0S_1I_3 \\ &= \bar{A}\bar{B}C + \bar{A}B\cdot 1 + A\bar{B}\cdot 0 + AB\cdot\bar{C} \\ &= \bar{A}\bar{B}C + \bar{A}B\cdot(C+\bar{C}) + AB\bar{C} \\ &= \bar{A}\bar{B}C + \bar{A}BC + \bar{A}B\bar{C} + AB\bar{C} \\ &\approx 001, 011, 010, 110 \\ Y(A, B, C) &= \Sigma m\,(1,2,3,6) \end{aligned}$$

Q.6 How many numbers of 8 : 1 MUX is required to implement 256 : 1 MUX ?

(a) 25 (b) 31

(c) 37 (d) 40

6. (c)

$$\text{Number of MUX} = \frac{256}{8} = 32 \quad \Rightarrow \frac{32}{8} = 4 \Rightarrow \frac{4}{8} = 1$$

$$\text{Total} = 32 + 4 + 1 = 37$$

Q.7 If M represents total number of states and n represents total no. of FFs, then for a nonbinary counter, which relation holds true ?

(a) $M < 2^n$ (b) $M = 2^n$

(c) $M > 2^{n+1}$ (d) $M = 2^{2n}$

7. (a)

M = total number of states

n = total number of FF's

$M = 2^n$; Binary counter

$M < 2^n$; Non-Binary counter

Q.8 A logic family has the following specifications

$I_{OH_{max}} = 0.8$ mA, $I_{OL_{max}} = 10$ mA,

$I_{IH_{max}} = 20\,\mu$A $I_{IL_{max}} = 0.2$ mA

The fan out based on the given data will be

(a) 30 (b) 40

(c) 50 (d) 60

8. **(b)**

$$(\text{Fan out})_H = \frac{I_{OH_{max}}}{I_{IH_{max}}} = \frac{0.8\times10^{-3}}{20\times10^{-6}} = 40$$

$$(\text{Fan out})_L = \frac{I_{OL_{max}}}{I_{IL_{max}}} = \frac{10\times10^{-3}}{0.2\times10^{-3}} = 50$$

$$\text{Fan out} = \text{minimum of } [(F.0)_H, (F.0)_L]$$
$$= \text{minimum of } (40, 50) = 40$$

Q.9 In which of the following programmable logic device, Both AND and OR arrays are programmable?

(a) PROM (b) PAL

(c) EPROM (d) PLA

9. **(d)**

PROM – AND array is fixed and OR array is programmable.

PLA – Both AND and OR arrays are programmable.

PAL – OR array is fixed and AND array is programmable.

Numerical Answer Type Questions : Q. 10 to Q. 16 carry 1 mark each

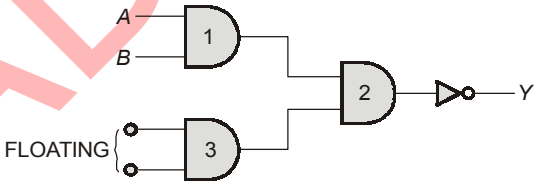
Q.10 The base of the number system for the addition 13 + 24 = 42 to be true will be

10. **5 (4.50 to 5.50)**

Let base be x, then

$$(13)_x + (24)_x = (42)_x$$
$$(1x^2 + 3x) + (2x^2 + 4x) = 4x^2 + 2x$$
$$3x^2 + 7x = 4x^2 + 2x$$
$$x^2 = 5x$$
$$x = 5$$

Q.11 The circuit shown below is an ECL circuit. The output of the circuit is_____



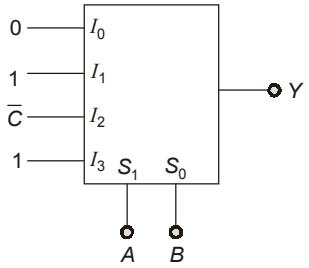
11. **1 (0.80 to 1.20)**

Floating inputs are considered as 0 in ECL circuit.

So, input to 2nd AND gate is AB and 0.

So output of 2nd AND gate is 0 and this OUTPUT of NOT gate is 1.

Q.12 The output of the given MUX contains _____ number of min-terms.



12. 5 (4.5 to 5.5)

As *A*, *B* is the select line and *C* is the input,

	I_0	I_1	I_2	I_3
$\overline{C}$	0	②	④	⑥
C	1	③	5	⑦
	0	1	$\overline{C}$	1

So, $\Sigma m\,(2, 3, 4, 6, 7)$ = Total no. of min-terms = 5

Q.13 If a 6 MHz clock frequency is applied to a cascaded counter of modulus – 2 counter and modulus – 3 counter, then lowest frequency is _____ kHz.

13. 1000 (999 to 1001)

Resulting mode in cascade counter

$$= M \times N = 2 \times 3 = 6$$

$$\text{Lowest output frequency} = \frac{6 \times 10^6}{6} = 1000 \text{ kHz}$$

Q.14 For a logic family –

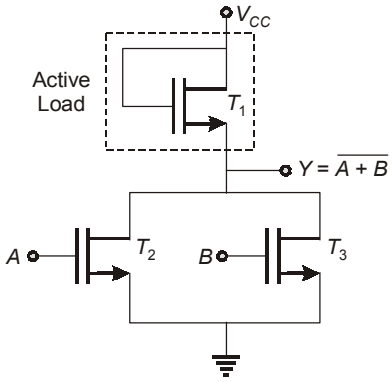
minimum guaranteed output high voltage	$V_{OH} = 4$ V
minimum accepted input high voltage	$V_{IH} = 3$ V
maximum guaranteed output output voltage	$V_{OL} = 1.5$ V
maximum accepted input low voltage	$V_{IL} = 2.5$ V

Its noise margin will be _____ V.

14. 1 (0.8 to 1.2)

$$(NM)_H = V_{OH} - V_{IH} = 4 - 3 = 1 \text{ V}$$
$$(NM)L = V_{IL} - V_{OL} = 2.5 - 1.5 = 1 \text{ V}$$

Q.15 For the figure shown below,



Out of all the combination of input (A, B), Output will be low for _____ combination of (A, B)

15. (3)

It is two input NOR gate using MOS transistors connected in parallel.

Input		NMOS			Output	
A	B	T_1	T_2	T_3	Y	
0	0	ON	OFF	OFF	V_{CC}	
0	1	ON	OFF	ON	0	3
1	0	ON	ON	OFF	0	
1	1	ON	ON	ON	0	

Q.16 The resolution required is 3 mV for full scale input voltage of 9 V in ADC. This ADC can have minimum no. of bits _____

16. 12 (11 to 13)

$$\text{Resolution} = \frac{\text{Full scale voltage}}{2^n - 1}$$

$$3 \times 10^{-3} = \frac{9}{2^n - 1}$$

$$2^n - 1 = 3000$$

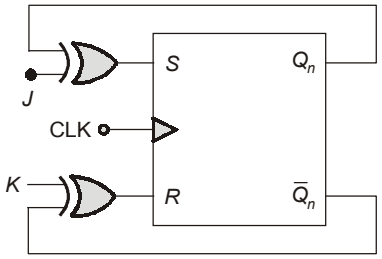
$$2^n = 3001$$

$$n = 12$$

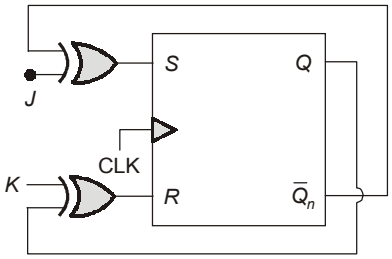
Multiple Choice Questions : Q.17 to Q.25 carry 2 marks each

Q.17 Which of the following circuit connection represents $J-K$ Flip-Flop ?

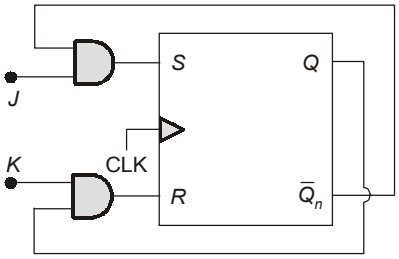
(a)



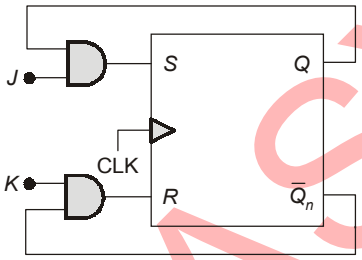
(b)



(c)



(d)



17. (c)

The characteristics tabel with J, K, Q_n, Q_{n+1} and the excitation table for S and R is shown below –

J	K	Q_n	Q_{n+1}	S	R
0	0	0	0	0	×
0	0	1	1	×	0
0	1	0	0	0	×
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	×	0
1	1	0	1	1	0
1	1	1	0	0	1

The K-map for S and R is shown as –

For S,

J \ KQ_n	00	01	11	10
0		×		
1	1	×		1

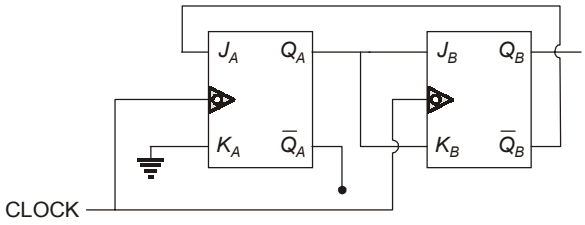
$$S = J\overline{Q}_n$$

For R,

J \ KQ_n	00	01	11	10
0	×		1	×
1			1	

$$R = KQ_n$$

Q.18 A circuit is designed with 2 – J-K FF's. If the output $Q_A\,Q_B = 10$ at starting, what will be the output ($Q_A\,Q_B$) after 13th clock pulse will be



(a) 0 0 (b) 1 0
(c) 1 1 (d) 0 1

18. (c)

	Q_A	Q_B
Initial	1	0
after 1st clock pulse	1	1
after 2nd clock pulse	1	0
after 3rd clock pulse	1	1
after 4th clock pulse	1	0
.		
.		
.		
after 13th clock pulse	1	1

So, after 13th clock pulse, output will be 1 1.

Q.19 Decimal equivalent of $(1000)_2 = -2^n$
Decimal equivalent of $(10000)_2 = -2^m$
So, $(n + m)_2$ would be
(a) 1 1 1 (b) 0 1 1
(c) 0 0 1 (d) 1 0 1

19. (a)

Decimal equivalent of $(1000)_2 = -2^3$
$\Rightarrow \quad n = 3$
Decimal equivalent of $(10000)_2 = -2^4$
$\Rightarrow \quad m = 4$
So, $(n + m)_2 = (3 + 4)_2 = (7)_2 = 111$

Q.20 The Boolean function can be expressed in canonical SOP and POS forms. So, for $Y = A\overline{B} + B\overline{C}$, the SOP and POS forms will be –
(a) $Y = \Sigma\,(0, 2, 4, 6);\ Y = \pi\,(1, 3, 7)$ (b) $Y = \Sigma\,(1, 2, 5, 7);\ Y = \pi\,(0, 3, 4, 6)$
(c) $Y = \Sigma\,(2, 4, 5, 6);\ Y = \pi\,(0, 1, 3, 7)$ (d) $Y = \Sigma\,(1, 2, 4, 5);\ Y = \pi\,(0, 3, 6)$

20. (c)

Plotting the K-map for $Y = A\overline{B} + B\overline{C}$

	$\overline{B}\overline{C}$	$\overline{B}C$	BC	$B\overline{C}$
$\overline{A}$	0	1	3	1 2
A	1 4	1 5	7	1 6

So, $\Sigma m\,(2, 4, 5, 6) =$ SOP
$\Sigma\pi\,(0, 1, 3, 7) =$ POS

Q.21 A 8-bit ADC with full scale output voltage of 10.00 V is designed to have a $\pm\frac{LSB}{2}$ accuracy. If the ADC is calibrated at 20° C and the operating temperature range from 0° C to 50° C, then the maximum net temperature coefficient of ADC should not exceed

(a) ± 650 μV (b) ± 700 μV

(c) ± 800 μV (d) 1 ± 850 μV

21. (a)

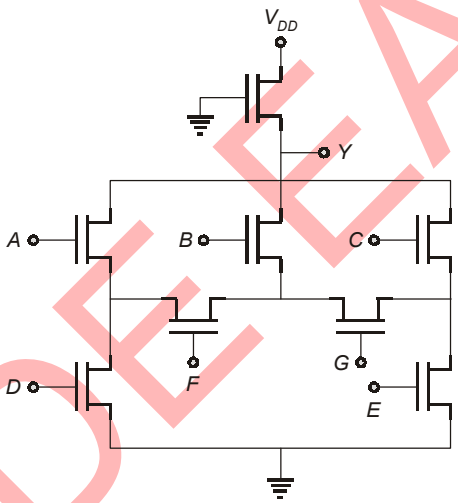
$$\text{Resolution} = \frac{\text{Full scale voltage}}{2^n} = \frac{10}{2^8} = 0.039$$

$$\pm\frac{LSB}{2} = T_{coeff} \times (50 - 20)$$

$$\pm\frac{0.039}{2} = 30 \times T_{coeff.}$$

$$T_{coeff} = \pm 650\,\mu V$$

Q.22 An NMOS circuit is shown below. The logic function for the output will be –



(a) (AFGE + AD + BFD + BGE + CE + CFGD)′

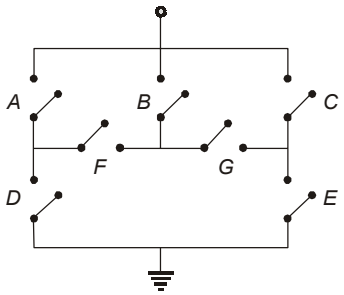
(b) ((AB + BC) . (DE + FG))′

(c) (AFGE + AD + BFD + BGE + CE + CFGD)

(d) ((AB + BC) . (DE + FG))

22. (a)

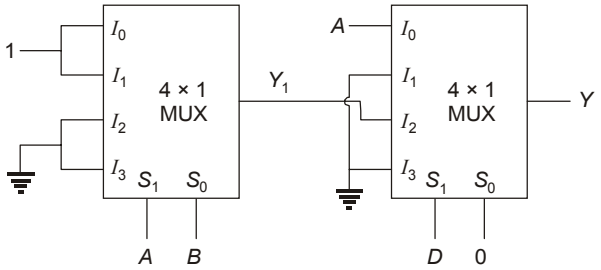
Drawing switch equivalent



The number of parallel paths to go from output to the ground are AFGE or AD or BFD or BGE or CE or CFGD.

As it is a NMOS logic circuit, the output for this logic function will be (AFGE + AD + BFD + BGE + CE + CFGD)′

Q.23 What will be the output of multiplexer shown below –



(a) $A \oplus D$ (b) $A \odot D \odot B$

(c) $A + D + \bar{B}$ (d) $A \,.\, D$

23. (a)

For 1st 4 × 1 MUX –

$$Y_1 = \bar{A}\bar{B}.I_0 + \bar{A}B.I_1 + 0 + 0$$

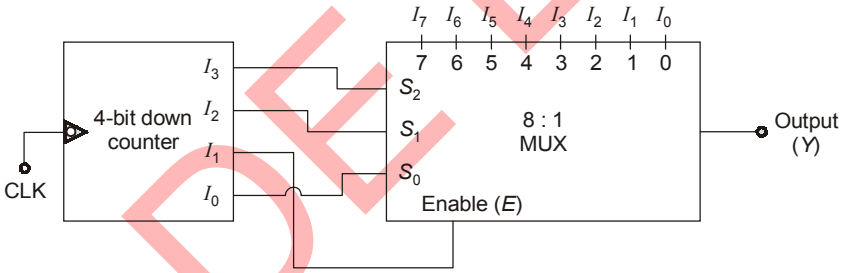
$$\Rightarrow \quad \bar{A}\bar{B}.1 + \bar{A}B.1 = \bar{A}(B + \bar{B}) = \bar{A}$$

For 2nd 4 × 1 MUX –

$$= \bar{D}.1.A + D.1.Y_1$$

$$= A\bar{D} + \bar{A}D = A \oplus D$$

Q.24 A 4-bit down counter is used to control the output of the multiplexer as shown in figure. The counter is initially at $(1111)_2$, then the output of the multiplexer will follow the sequence –



(a) $I_7, 0, I_6, 0, I_5, 0 \ldots$ (b) $I_7, 0, 0, I_6, 0, 0, I_5 \ldots$

(c) $I_7, I_6, I_5, I_4, I_3 \ldots$ (d) $I_7, I_6, 0, 0, I_5, I_4, 0, 0 \ldots$

24. (d)

Counter output =

	I_3	I_2	I_1	I_0	
1st clock	1	1	1	1	– 15
2nd	1	1	1	0	– 14
3rd	1	1	0	1	– 13
4th	1	1	0	0	– 12
5th	1	0	1	1	– 11
6th	1	0	1	0	– 10

So it can be seen that

$$S_2 = I_3,\ S_1 = I_2,\ S_0 = I_0 \text{ and } E = I_1$$

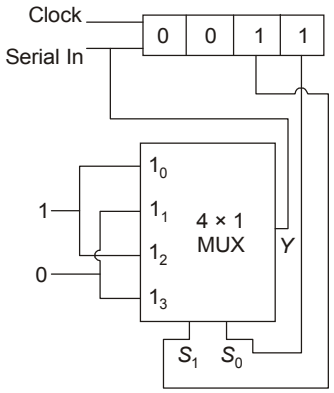
For 1st and 2nd clock pulses, enable (E) is 1

	S_2	S_1	S_0		
1st clock pulse –	1	1	1	→	I_7
2nd clock pulse –	1	1	0	→	I_6

For 3rd and 4th clock pulse, enable (E) is 0, so, Y is 0

Similarly, for 5th and 6th clock pulse enable (E) is 1 so output will be I_5, I_4.

Q.25 The initial content of serial IN parallel OUT, right shift, shift register shown below is 0011. After how many clock pulses, the content of register will return to its initial value.



(a) 7 (b) 8
(c) 11 (d) 13

25. (b)

Clock Pulses	Register Content	Output of 4 × 1 MUX
	0 0 1 1	→ 0
1	0 0 0 1	→ 0
2	0 0 0 0	→ 1
3	1 0 0 0	→ 1
4	1 1 0 0	→ 1
5	1 1 1 0	→ 1
6	1 1 1 1	→ 0
7	0 1 1 1	→ 0
8	0 0 1 1	

Numerical Answer Type Questions : Q. 26 to Q. 33 carry 2 marks each

Q.26 Number of '1' in 2's complement representation of $(-89)_{10}$ is _____

26. (5)

Binary representation of $(89)_{10}$ = (01011001)
$(-89)_{10}$ = 2's compliment of (01011001)
So, 2's complement of (01011001) = (10100110) + (1)
sum of bits = 5

Q.27 A system has resolution of 30.52 μV for maximum output voltage of 2 V, then the dynamic range of the system will be _____ dB. (answer to 2 decimal places)

27. 97.76 (97 to 98)

$$\text{Resolution} = \frac{\text{Maximum output voltage}}{2^N}$$

$$30.52 \times 10^{-6} = \frac{2}{2^N}$$

$\Rightarrow N = 16$

Dynamic range = (1.76 + 6 N) dB
= 97.76 dB

Q.28 For a Mod-10 counter, Jhonson counter uses X flip flops, ring counter uses y flip flops, and ripple counter uses Z flip flops. Then $X + Y + Z$ will _____ .

28. 19 (18 to 20)

For MOD - 10 counter –

X = Jhonson counter required = 5 flip flops

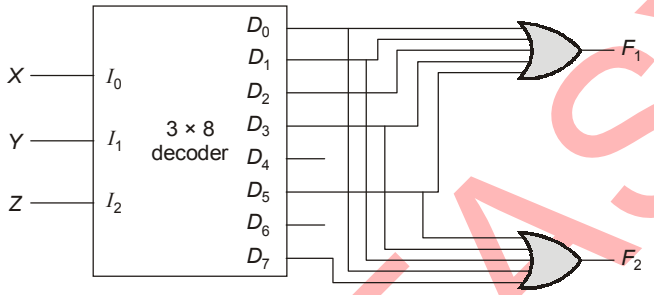
Y = ring counter required = 10 flip flops

Z = ripple counter required = 4 flip flops

$X + Y + Z = 5 + 10 + 4$

$= 19$ flip flops

Q.29 Two functions $F_1(x, y, z)$ and $F_2(x, y, z)$ are implemented using a 3 × 8 decoder as shown in figure below.



The number of essential prime implicants of function F_1F_2 is _____ .

29. 3 (2 to 4)

Min-terms common to both F_1 and F_2 will be min-terms of F_1F_2.

D_0, D_1, D_3, D_5 min-terms are common to F_1 and F_2.

$\Sigma_m(0, 1, 3, 5)$

K-Map

	$\bar{Y}\bar{Z}$	$\bar{Y}Z$	YZ	$Y\bar{Z}$
$\bar{X}$	1_0	1_1	1_3	2
X	4	1_5	7	6

So,

Essential prime implicants = 3

Q.30 An ADC has to total conversion time of 300 μ sec. The highest frequency of analog input signal is ___ kHz.

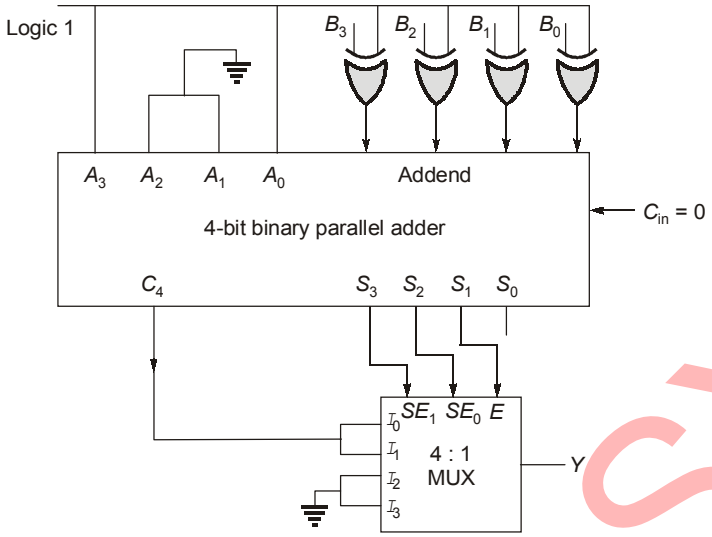
30. 1.67 (1.50 to 2.00)

Highest frequency that the analog signal can contain is –

$$fc_{(max)} = \frac{1}{2 \times \text{Average conversion time}}$$

$$= \frac{1}{2 \times 300\,\mu\text{sec}} = 1.67 \text{ kHz}$$

Q.31 Consider the digital circuit shown below. What will be the output Y, if the number $B_3\ B_2\ B_1\ B_0 = 0101$



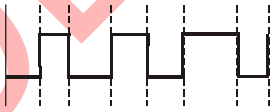
31. (1)

$$\text{Addend will be} = 1010$$
$$S_3\ S_2\ S_1\ S_0 = 1010 + A_3\ A_2\ A_1\ A_0 + C_{in}$$
$$= 1010 + 1001$$
$$= 0011 \qquad (C_4 = 1)$$
$$SE_1\ SE_0 = 0\ 0$$

and $E = 1$,

So, $Y = 1$

Q.32 The output waveform of 8 bit ADC is shown in figure below.



If the refrence of ADC converter is 16 V then the actual input of the system will be can have uptil _____ decimal values.

32. (3)

$$\frac{16}{2^8}\left[0\times 2^7 + 1\times 2^6 + 0\times 2^5 + 1\times 2^4 + 0\times 2^3 + 1\times 2^2 + 1\times 2^1 + 0\times 2^\circ\right]$$

$$= \frac{16}{2^8}\times[86] = 5.375\ \text{V}$$

as : Analog voltage = resolution × binary equivalent

= 3 decimal value

Q.33 For implementation of a full adder using 2 : 1 multiplexers only, and available input A, B and C (complement of input not available) requires minimum _____ multiplexer.

33. (7)

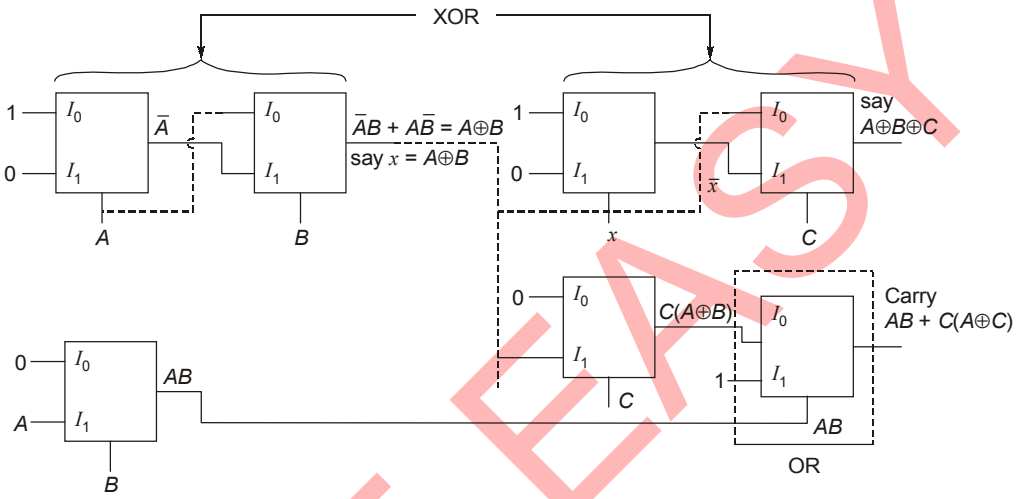
The relation required to be implemented for full adder.

$$S = (A \oplus B) \oplus C$$

$$C_{out} = AB + C(A \oplus B)$$

Multiplexer output relation $= \bar{S}_0 I_0 + S_0 I_1$

So,



Total multiplexer (2 : 1) required → 7

❍❍❍❍

