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EC : ELECTRONICS ENGINEERING

TEST No. - 12 | MICROPROCESSORS

Read the following instructions carefully

1. This question paper contains 33 MCQ's & NAQ's. Bifurcation of the questions are given below:

Subjectwise Test Pattern

Questions	Question Type	No. of Questions	Marks	Total Marks	Negative Marking
1 to 10	Multiple Choice Ques.	10	1	10	0.33
11 to 16	Numerical Answer Type Ques.	6	1	6	None
17 to 26	Multiple Choice Ques.	10	2	20	0.66
27 to 33	Numerical Answer Type Ques.	7	2	14	None
Total Questions : 33		**Total Marks : 50**		**Total Duration : 90 min**	

2. Choose the closest numerical answer among the choices given.

Multiple Choice Questions : Q.1 to Q.10 carry 1 mark each

Q.1 Which interrupt has highest priority in 8085 microprocessor?
(a) INTR (b) RST 4.5
(c) RST 6.5 (d) RST 7.5

1. (b)

Q.2 In 8085 microprocessor, the 16 bit register(s) is/are
(a) Stack pointer (b) Program counter
(c) Both (a) and (b) (d) Accumulator

2. (c)

Q.3 The contents of accumulator after execution of CMA instruction is A5 H. Its contents before execution is
(a) A5 H (b) 5A H
(c) 55 H (d) AA H

3. (b)
CMA instruction compliments the contents of accumulator

$\overline{A}$ = 10100101
A = 01011010 = 5 A H

Q.4 The serial input data of 8085 microprocessor can be loaded into MSB of the accumulator by
(a) executing RIM instruction (b) executing RST1
(c) using TRAP (d) none of these

4. (a)
RIM instruction i.e. Read Interrupt Mask can be used to load the serial input.

Q.5 The advantage(s) of memory mapped I/O over I/O mapped I/O is/are
(a) faster accessing
(b) more number of instructions supporting memory mapped I/O
(c) more number of I/O devices can be interfaced
(d) all of the above

5. (d)

Q.6 Which of the following mainly decides the speed of operation of a microprocessor?
(a) input clock frequency (b) data bus width
(c) Address bus width (d) all of the above

6. (a)

Q.7 Which of the following Assembly language instruction can be used to clear the lower four bits of the accumulator in 8085 microprocessor?
(a) XRI 0F H (b) ANI F0 H
(c) XRI F0 H (d) ANI 0F H

7. (b)

Q.8 The size of ROM used to store the table for multiplication of two 8 bit unsigned integers must be

(a) 256×16 (b) $64\text{ k} \times 8$

(c) $4\text{ k} \times 16$ (d) $64\text{ k} \times 16$

8. (d)

Total number of input lines = $16 = n$

Total number output lines = $16 = m$

ROM size = $2^n \times m = 2^{16} \times 16$

= $64\text{ k} \times 16$

Q.9 In 8085 microprocessor, if CMP B is executed and the status of carry flag and zero flag are set and reset respectively, then which of the following is true?

(a) Contents of Accumulator is equal to that of register B

(b) Contents of Accumulator is greater than that of register B

(c) Contents of Accumulator is less than that of register B

(d) Such status of carry and zero flags is not possible, when CMP B is executed

9. (c)

A < B

CY = 1

Z = 0

Q.10 Consider the following set of Assembly language instructions of 8085 microprocessor

```
STC
CMC
MOV A, B
RAL
MOV B, A
```

The above set of instructions

(a) doubles the contents of Register B

(b) divides the contents of Register B by 2

(c) multiplies the contents of B by A

(d) swaps the contents of Register A and B

10. (a)

The above instructions are used to multiply the contents of Register B by '2'.

Numerical Answer Type Questions : Q. 11 to Q. 16 carry 1 mark each

Q.11 In 8085 microprocessor, when RSTn instruction is executed, the contents of program counter is 0018 H. The value of n is _____.

11. (3)

$(n \times 8)_{10} = 0018\text{ H} = (24)_{10}$

$n = 3$

Q.12 Consider the following Assembly Language program.

```
MVI A, 30 H
ADI 30 H
XRA A
POP H
```

After execution of the above program, the contents of Accumulator will be $(\_\_\_\_\_)_{10}$.

12. **(0)**

A : 30 H - First step

A + 30 : 60 H - Second step

XRA A - A $\oplus$ A = 0

A : 00 H

$00\ H \xrightarrow{\text{decimal}} 0$

Q.13 Let a memory chip is represented as 8192 × 64. If there are A number of address lines and B number of data lines in the chip, then A + B is _____.

13. **(77)**

$$8192 \times 64 = 2^{13} \times 64$$

$\Rightarrow$ 13 address lines = A and 64 data lines = B

Hence $A + B = 64 + 13$

$= 77$

Q.14 The number of machine cycles required to execute the instruction PUSH B is _____.

14. **(3)**

PUSH B requires Opcode Fetch and 2 memory write operations. Thus 3 machine cycles are required to execute PUSH B instructions.

Q.15 The following set of instructions is executed by an 8085 microprocessor

1000 H LXI SP, 27 FF H

1003 H CALL 1006 H

1006 H POP H

The contents of HL register pair after execution of above set of instructions is _____ H.

15. **(1006)**

After execution

SP : 27FF H

HL : 1006 H

as after CALL instruction, the address of next instruction is stored in stack.

Q.16 The Addressable memory capability supported by 8085 microprocessor is _____ kB.

16. **(64)**

Address lines : 16

Data lines : 8

Size : $2^{16} \times 8 = 64$ kB

Multiple Choice Questions : Q.17 to Q.26 carry 2 marks each

Q.17 How many times, the LOOP will be executed in the following Assembly language program?

```
        LXI B, 0002 H
LOOP :  DCX B
        MOV A, C
        XRA B
        JNZ LOOP
        HLT
```

(a) once (b) twice
(c) zero (d) infinite

17. (b)

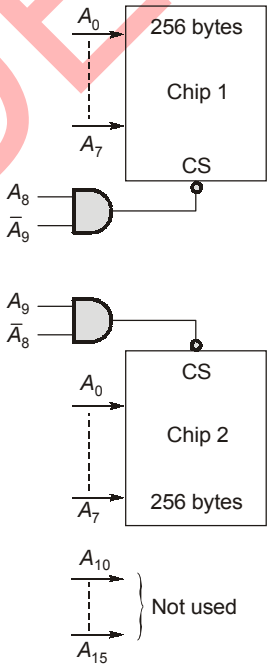
After LXI B, 0002 H
B : 00 H
C : 02 H
A = C

After two times executing DCX B, contents of C will be 00 H and B ⊕ A will be 00 H.

Q.18 The 'DMA' transfer implies
(a) direct transfer of data between memory and accumulator.
(b) direct transfer of data between memory and I/O devices without the interference of microprocessor.
(c) transfer of data exclusively within microprocessor registers.
(d) A fast transfer of data between microprocessor and I/O devices.

18. (b)

Q.19 Consider the following memory interfacing diagram with 8085 microprocessor.



What memory address range in the given options is NOT represented by combination of chip 1 and chip 2?
(A_0 to A_{15} are address lines and CS means chip select)
(a) 0100 H - 02FF H (b) F900 H - FAFF H
(c) 1500 H - 16FF H (d) F800 H - F9FF H

19. **(d)**

	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
(a)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1
(b)	1	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0
	1	1	1	1	1	0	1	0	1	1	1	1	1	1	1	1
(c)	0	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0
	0	0	0	1	0	1	1	0	1	1	1	1	1	1	1	1
(d)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1	1

For the address range to be represented by chip 1 and chip 2, A_9 A_8 should be either 01 or 10, here in option (d) A_9 A_8 is 00. So, this circuit can't address the range F800 H - F9FF H.

Q.20 Consider an 8085 microprocessor system. The following program starts at location 0700 H.
LXI SP, 00FF H
LXI H, 0701 H
MVI A, 20 H
SUB M
The contents of accumulator when the program counter reaches 0709 H is
(a) 00 H (b) 21 H
(c) 20 H (d) FF H

20. **(b)**
[PC]
0700 H LXI SP, 00FF H : contents of 0701 H = FF H, contents of 0702 H = 00 H
0703 H LXI H, 0701 H
0706 H MVI A, 20 H
0708 H SUB M
[PC] → 0709 H
When [PC] → 0709 H; contents of memory location 0701 H subtracted from accumulator.
i.e. 20 H – FF H = 21 H

Q.21 Consider the following set of instructions to be executed by an 8085 microprocessor. The input port having an address of 01 H has the data 05 H.
IN 01 H
ANI 80 H
After execution of the above two instructions, the contents of flag register will be

	D7	D6	D5	D4	D3	D2	D1	D0
(a)	1	0	×	1	×	1	×	0
(b)	0	1	×	0	×	1	×	0
(c)	0	1	×	1	×	1	×	0
(d)	0	1	×	1	×	0	×	0

21. **(c)**
05 H AND 80 H = 00 H
After ANI instruction, CY = reset, AC is set and S, Z, P are modified.
S = 0, Z = 1, AC = 1, P = 1, CY = 0

D7	D6	D5	D4	D3	D2	D1	D0
0	1	X	1	X	1	X	0
S	Z	X	AC	X	P	X	CY

Q.22 Consider the following statements

(i) DAD R_P doesn't affect any flag.

(ii) PCHL exchanges the content of program counter and HL pair.

(iii) PUSH R_P, INX R_P, PCHL, SPHL and XTHL, all these instructions have opcode fetch of 6-Tstates.

(iv) In INR R, all flags are affected except CY flag.

(R_P : Register pair and R : Register)

Which of the above statements are NOT correct?

(a) (i) and (iv) (b) (ii), (iii) and (iv)

(c) (i), (ii), (iii) and (iv) (d) (i), (ii) and (iii)

22. (d)

(i) DAD R_P doesn't affect any flag except CY

(ii) PCHL copies the content of HL pair to the program counter

(iii) All have fetch of 6 T-states except XTHL which has fetch of 4T states

(iv) In INR R, all flags are affected except CY flag

Q.23 When RET instruction at the end of subroutine is executed,

(a) the information where the stack is initialized is transferred to the stack pointer

(b) the memory address of RET instruction is transferred to the program counter

(c) the two data bytes stored in the top two locations of the stack are transferred to the program counter.

(d) the two data bytes stored in the top two locations of the stack are transferred to the stack pointer.

23. (c)

After the execution of RET instruction the top two bytes of stacks are transferred to program counter.

Q.24 Match **List-I** (Instruction) with **List-II** (Operation) for intel 8085 microprocessor and select the correct answer using the codes given below:

List-I	List-II
A. PCHL	**1.** Exchange the top of the stack with contents of HL pair
B. SPHL	**2.** Exchange the contents of HL pair with that of DE pair
C. XTHL	**3.** Transfer the contents of HL pair to the stack pointer
D. XCHG	**4.** Transfer the contents of HL pair to the program counter

Codes:

	A	B	C	D
(a)	3	4	1	2
(b)	3	4	2	1
(c)	4	3	2	1
(d)	4	3	1	2

24. (d)

Q.25 After execution of the following set of instructions of 8085 microprocessor, the contents of Accumulator will be

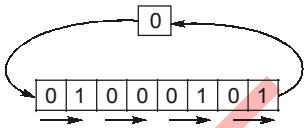
3000 H : MVI A, 45 H
3002 H : MOV B, A
3003 H : STC
3004 H : CMC
3005 H : RAR
3006 H : XRA B
3007 H : HLT

(a) 00 H (b) 45 H
(c) 67 H (d) E7 H

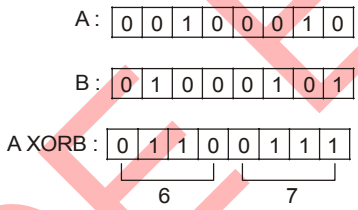
25. (c)

MVI A, 45 H $\Rightarrow$ A : 45 H
MOV B, A $\Rightarrow$ B : 45 H
STC $\Rightarrow$ CY = 1
CMC $\Rightarrow$ CY = 0

RAR =



(Rotate Accumulator Right with carry)



A : 67 H

Q.26 Consider the following set of instructions

MVI A, BYTE 1
RLC
MOV B, A
RLC
RLC
ADD B

If the contents of Accumulator, after the execution of the program is 46 H, then the contents of BYTE 1 initially will be

(a) 06 H (b) 07 H
(c) 08 H (d) 09 H

26. (b)

The above program is used to multiply the contents of Accumulator by $(10)_{10}$.

$10(A_{initial}) = 46\ H = (70)_{10}$
(BYTE 1) = $(A_{initial}) = 07\ H$

Numerical Answer Type Questions : Q.27 to Q.33 carry 2 marks each

Q.27 The following set of instructions is executed in an 8085 microprocessor based system. The frequency of clock of microprocessor is 5 MHz.

		T - states
	XRA A	4T
	LXI SP, 3A00 H	10T
	LXI H, 0000 H	10T
LOOP :	DAD SP	10T
	SHLD 4000 H	16 T
	JC LOOP	7T/10T
	NOP	4T

The total time required to execute the above set of instructions is _____ μsec.

27. 12.2 (11.9 to 12.5)

DAD SP : (HL) ← (HL) + (SP)

while executing DAD instruction, carry flag is set if the result is larger than 16 bits

3A00 H + 0000 H → 3A00 H → CY = 0

Hence LOOP will be executed once

$$\text{Total T-states} = 4T + 10T + 10T + 10T + 16T + 7T + 4T$$
$$= 61T$$
$$\text{Time required} = 61 \cdot \frac{1}{f}$$
$$= \frac{61}{5 \times 10^6} = 12.2\ \mu\text{sec}$$

Q.28 The minimum number of memory IC's of 4 k × 2 capacity required to construct a memory of 22 k × 8 capacity is _____.

28. (24)

To construct memory chip of 22 k × 8 from 4 k × 2 chips, we need to connect data lines of same address,

so for each address, number of chips needed = $\frac{8}{2} = 4$.

Also, to increase memory space from 4 k to 22 k, number of chips needed = $\frac{22\text{ k}}{4\text{ k}} = 5.5$

But, practically number of chips needed will be 6. So, total number of chips needed = 6 × 4 = 24.

Q.29 An INTEL 8085 microprocessor is interfaced with a memory chip of unknown size. The starting address by which memory can be addressed is 1001 H and the ending address is 2016 H. The size of the memory chip is _____ bytes.

29. (4118)

$$\text{starting address} = 1001\text{ H}$$
$$\text{ending address} = 2016\text{ H}$$
$$\text{size of memory} = (2016 - 1001)\text{ H} + 1\text{ H}$$
$$= 1016\text{ H} = 4118 \text{ bytes}$$

Q.30 If the time required to execute JMP 2017 H instruction is 2.5 microseconds, then the crystal frequency of 8085 microprocessor is _____ MHz.

30. (8)

Number of T-states required to execute JMP 2017 H = 10

Time required for execution = $10 \cdot T_{clk}$

$$= \frac{10}{f_{clock}} = 2.5 \times 10^{-6}$$

$$f_{clock} = \frac{10}{2.5} \times 10^{6}$$

clock frequency $f_{clock} = 4$ MHz

Crystal frequency $= f_{crystal} = 2f_{clk}$

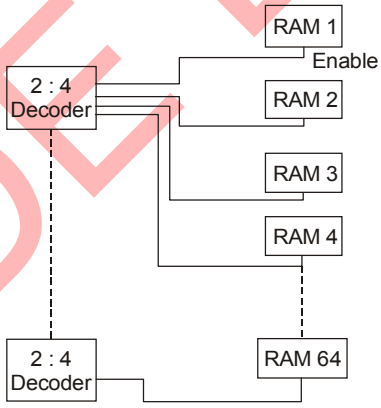
$= 2 \times 4 = 8$ MHz

Q.31 A memory system of 64 K bytes needed to be designed with RAM chips of 1K byte each and a decoder tree constructed with 2 : 4 decoder chips with "enable" input. The total number of decoder chips required is _____.

31. (21)

The number of RAM chips needed = $\frac{64\,k}{1\,k} = 64$

As 2 : 4 decoder chips are used to select the particular RAM chips



So, number of 2 : 4 decoders required = $\left(\frac{64}{4} = 16\right) + \left(\frac{16}{4} = 4\right) + \left(\frac{4}{4} = 1\right) = 16 + 4 + 1 = 21$

Q.32 The contents of some memory locations of an 8085 microprocessor based system are given as follows.

Address	Contents
3000 H	02 H
3001 H	30 H
3002 H	00 H
3003 H	30 H

Consider the assembly language program given below

```
LXI H, 3000 H
MOV E, M
INX H
MOV D, M
LDAX D
MOV L, A
INX D
LDAX D
MOV H, A
NOP
```

the contents of register H after execution of the above program will be (_____)$_{10}$.

32. (48)

LXI H, 3000 H	HL : 3000 H
MOV E, M	E : 02 H
INX H	HL : 3001 H
MOV D, M	D : 30 H
LDAX D	A : 00 H
MOV L, A	L : 00 H
INX D	DE : 3003 H
LDAX D	A : 30 H
MOV H, A	H : 30 H

After execution of the program contents of H =30 H = $(48)_D$

Q.33 Consider the assembly language program given below

```
XRA A
STA E008 H
DCR A
STA A008 H
HLT
```

The contents of memory location A008 H after execution of the above program in 8085 microprocessor is (____)$_{10}$.

33. (255)

XRA A		A : 00 H
STA E008 H		E008 : 00 H
DCR A		A : FF H
STA A008 H		A008 : FF H
$(FF)_H$	$\rightarrow$	$(255)_{10}$

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