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Open Practice Test Series
(Also useful for ESE & Other Exams)

EC : ELECTRONICS ENGINEERING
TEST No. - 10 | DIGITAL ELECTRONICS

Read the following instructions carefully

1. This question paper contains 33 MCQ's & NAQ's. Bifurcation of the questions are given below:

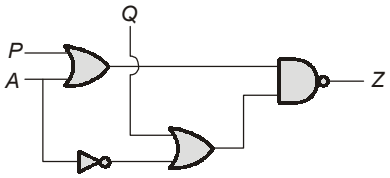
Subjectwise Test Pattern

Questions	Question Type	No. of Questions	Marks	Total Marks	Negative Marking
1 to 10	Multiple Choice Ques.	10	1	10	0.33
11 to 16	Numerical Answer Type Ques.	6	1	6	None
17 to 26	Multiple Choice Ques.	10	2	20	0.66
27 to 33	Numerical Answer Type Ques.	7	2	14	None
Total Questions : 33		**Total Marks : 50**		**Total Duration : 90 min**	

2. Choose the closest numerical answer among the choices given.

Multiple Choice Questions : Q.1 to Q.10 carry 1 mark each

Q.1 The circuit shown below is used to implement the function $z = f(A, B) = \bar{A} + B$. The values of P and Q are



(a) $P = A, \quad Q = B$ (b) $P = B, \quad Q = \bar{A}$

(c) $P = \bar{B}, \quad Q = 0$ (d) $P = 0, \quad Q = \bar{B}$

1. (d)

$$\bar{Z} = (P + A)(Q + \bar{A})$$

$$\bar{Z} = PQ + AQ + \bar{A}P$$

If $Z = \bar{A} + B$

$$\bar{Z} = \overline{\bar{A} + B} = A\bar{B}$$

$$Q = \bar{B}, \quad P = 0$$

Q.2 24 MHz clock frequency is applied to a cascaded counter of MOD-3, MOD-4 and MOD-5 counters. The lowest output frequency and the overall MOD value of the cascaded counter are

(a) 600 kHz, 60 (b) 400 kHz, 60

(c) 400 kHz, 120 (d) 600 kHz, 120

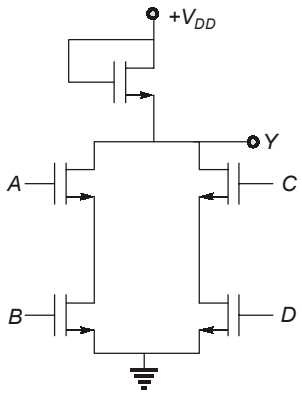
2. (b)

$$\text{Overall MOD} = 3 \times 4 \times 5 = 60$$

Lowest frequency is output frequency

$$f_{out} = \frac{24 \times 10^6}{60} = 400 \text{ kHz}$$

Q.3 For the NMOS logic circuit shown below, if the input $C = 0$ and $D = 0$, then for which combination of A and B the output Y will be 0?



(a) $A = 0, B = 1$ (b) $A = 0, B = 0$

(c) $A = 1, B = 1$ (d) $A = 1, B = 0$

3. (c)

$$Y = \overline{AB + CD}$$

for $C = D = 0$, $Y = \overline{AB}$

so, Y will be 0 when $A = B = 1$

Q.4 The irredundant minimised logic expression corresponding to the K-map shown below is

WX \ YZ	00	01	11	10
00			1	
01	1	1	1	
11		1	1	1
10		1		

(a) XZ

(b) $\bar{W}X\bar{Y} + \bar{W}YZ + W\bar{Y}Z + WXY$

(c) $\bar{W}X\bar{Y} + \bar{W}YZ + W\bar{Y}Z + WX\bar{Y}$

(d) $XZ + \bar{W}YZ + \bar{W}X\bar{Y} + WXY + W\bar{Y}Z$

4. (b)

WX \ YZ	00	01	11	10
00			1	
01	1	1	1	
11		1	1	1
10		1		

$$Z = \bar{W}X\bar{Y} + WXY + \bar{W}YZ + W\bar{Y}Z$$

Q.5 Consider the following statements.

1. A flip-flop can store 1-bit information
2. Race around condition occurs in a level triggered J-K flip-flop when both the inputs are 1
3. Master slave configuration is used in flip-flops to store 2 bits of data
4. A transparent latch consists of a D-type flip-flop

Which of these statements are correct?

(a) 1 and 2

(b) 1, 3 and 4

(c) 1, 2 and 4

(d) 2 and 3

5. (c)

Master slave configuration stores 1-bit of data.

Q.6 A certain 8-bit successive approximation type analog to digital converter has full scale voltage of 2.65 V. If the conversion time for V_A = 1.5 V is 75 μs, then the conversion time for V_A = 2 V is

(a) 75 μs

(b) 25 μs

(c) 225 μs

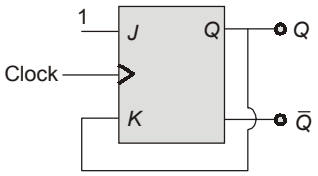
(d) 150 μs

6. (a)

For successive approximation type of converter, the conversion time is independent of V_A.

Hence, option (a) is correct.

Q.7 Assume that the initial value of Q is 0. After applying the clock signal to the given circuit, the subsequent states of Q will be



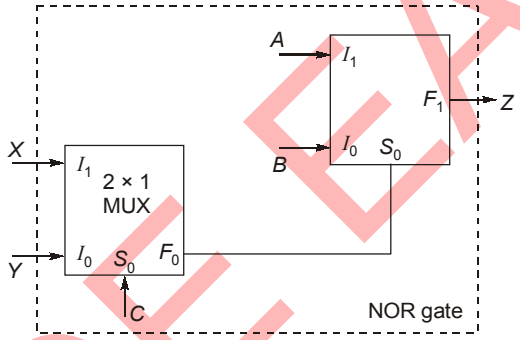
(a) 0, 1, 0, 1, 0
(b) 1, 0, 1, 0, 1
(c) 0, 0, 0, 0, 0
(d) 1, 1, 1, 1, 1

7. (b)

It is a toggle flip-flop, the values toggle

Q : 0 → 1 → 0 → 1 → 0 → 1
↑
initial state

Q.8 The circuit shown below implements a two input NOR gate by using two 2 × 1 multiplexers. The values of A, B, and C are respectively.



(a) 0, $\bar{X}$, 0
(b) 1, $\bar{X}$, 1
(c) 0, 0, $\bar{X}$
(d) 1, 1, X

8. (a)

$$F_0 = XC + Y\bar{C}$$

$$Z = F_1 = B\bar{F}_0 + AF_0$$

for NOR gate, $$Z = \overline{X+Y} = \bar{X}\bar{Y} = \bar{F}_0B + F_0A$$

for $A = 0$

$$\bar{F}_0B = \bar{X}\bar{Y}$$

Let us take $B = \bar{X}$ (as only X and $\bar{X}$ are used in the options)

then, $\bar{F}_0 = \bar{Y} \Rightarrow F_0 = Y$

$F_0 = \bar{C}Y + CX = Y$ ⇒ it is possible for $C = 0$

so correct combination is $A = 0$, $B = \bar{X}$, $C = 0$

Q.9 The initial value of output (Q_n) of a J-K flip flop is 0. If it changes to 1 after application of a clock pulse, then the inputs K_n and J_n before application of the clock pulse are respectively.

(a) 0, X (b) X, 0

(c) X, 1 (d) 1, X

9. (c)

Excitation table

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Q.10 The truth table of a combinational circuit is given below

A	B	C	Z
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

The Boolean expression for Z is

(a) $(AB\bar{C})+(\bar{A}\bar{B}\bar{C})$ (b) $(\bar{A}+\bar{B}+\bar{C})+(A+B+C)$

(c) $\bar{C}+(A\oplus B)$ (d) $\bar{C}+(A\odot B)$

10. (c)

Using POS form

$$\begin{aligned} Z &= (A+B+\bar{C})(\bar{A}+\bar{B}+\bar{C}) \\ &= (A+B)(\bar{A}+\bar{B})+\bar{C} \\ &= A\oplus B+\bar{C} \\ &= \bar{C}+(A\oplus B) \end{aligned}$$

Numerical Answer Type Questions : Q. 11 to Q. 16 carry 1 mark each

Q.11 If the number of comparators used in a k-bit flash type ADC is 15, then the value of k is _____.

11. (4)

$$\begin{aligned} \text{Number of comparators} &= 2^k-1 \\ 2^k-1 &= 15 \\ 2^k &= 16 \\ k &= 4 \end{aligned}$$

Q.12 The resolution of a 10-bit analog to digital convertor is _____ %.

12. 0.097 (0.07 to 0.12)

$$\% \text{ Resolution} = \frac{100}{2^n - 1} = \frac{100}{2^{10} - 1} = \frac{100}{1023}$$
$$= 0.097\%$$

Q.13 $(25.5)_8 + (75.4)_8 = (\_\_\_\_\_)_8$

13. 123.1 (123 to 123.20)

$$(25.5)_8 + (75.4)_8 = (123.1)_8$$
$$(9)_{10} = (11)_8$$
$$(11)_{10} = (13)_8$$
$$(10)_{10} = (12)_8$$

Q.14 Each cell of a static random memory contains n - number of MOS transistors. The value of n is _____.

14. (6)

Q.15 If $(211)_x = (152)_8$, then the value of x is _____.

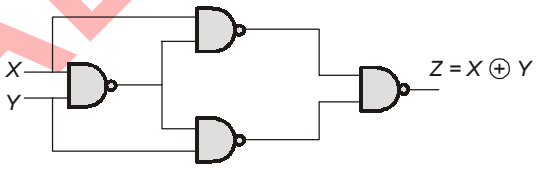
15. (7)

Converting to decimal equivalent

$$(211)_x = (2x^2 + x + 1)_{10}$$
$$(152)_8 = (64 + 40 + 2)_{10} = (106)_{10}$$
$$2x^2 + x + 1 = 106$$
$$2x^2 + x - 105 = 0$$
$$\Rightarrow \quad x = 7$$

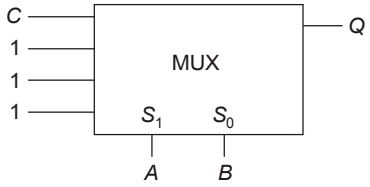
Q.16 If X and Y logic inputs are available and their respective complements $\overline{X}$ and $\overline{Y}$ are not available, then the minimum number of two input NAND gates required to implement $X \oplus Y$ is _____.

16. (4)



Multiple Choice Questions : Q.17 to Q.26 carry 2 marks each

Q.17 Consider the combinational logic circuit shown below.



The output Q can be expressed as

(a) $\Sigma m(0, 1, 2, 3, 4, 5, 6)$ (b) $\Pi M(0)$

(c) $\Pi M(0, 1)$ (d) $\Sigma m(1, 2, 3, 4, 5, 6)$

17. (b)

S_1	S_0	C	Q
$\bar{A}$	$\bar{B}$	C	$\bar{A}\bar{B}C$
$\bar{A}$	B	1	$\bar{A}B$
A	$\bar{B}$	1	$A\bar{B}$
A	B	1	AB

$$Q = \bar{A}\bar{B}C + \bar{A}BC + \bar{A}B\bar{C} + A\bar{B}C + A\bar{B}\bar{C} + ABC + AB\bar{C}$$
$$= \Sigma m(1, 2, 3, 4, 5, 6, 7)$$
$$= \Pi M(0)$$

Q.18 If the decimal number "4" is coded as "1000" in "4221" BCD system, then what will be the codeword for decimal number "5" in "4221" BCD system?

(a) 0111 (b) 1001

(c) 1101 (d) Not possible to say in an unique way

18. (a)

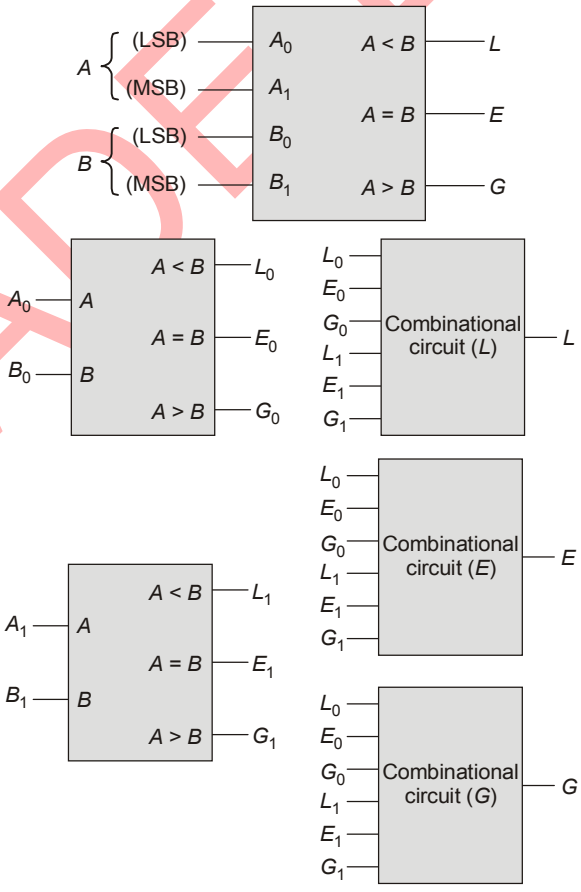
- 4221 code is a self complementing code. $\because 4 + 2 + 2 + 1 = 9$
- For a self complementing code system,

codeword of "5" = 1's complement of codeword of "4" $\because 5 = 9 - 4$ i.e, 9's complement of 4.

so, codeword of 5 = 1's complement of (1000)

= 0111

Q.19 A 2-bit magnitude comparator is designed using two 1-bit magnitude comparators as shown below:



Determine the boolean function for the combinational circuit G?

(a) $G = E_1G_0 + G_1L_0$ (b) $G = E_1G_0 + G_1E_0$

(c) $G = E_1G_0 + L_1G_0$ (d) $G = E_1G_0 + G_1$

19. (d)

$A \Rightarrow A_1\ A_0$ $\quad$ $B \Rightarrow B_1\ B_0$

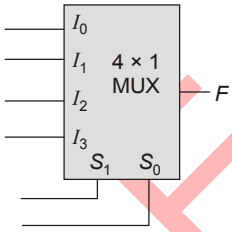
$A > B$ is possible when either of the following conditions is satisfied

1. When $A_1 > B_1 \Rightarrow$ i.e., when $G_1 = 1$
2. When $(A_1 = B_1)$ and $(A_0 > B_0) \Rightarrow$ i.e., when $E_1G_0 = 1$

So, the Boolean expression for G is

$$G = E_1G_0 + G_1$$

Q.20 The Boolean expression $F(X, Y, Z) = \Pi M(0, 2, 4, 7)$ is to be implemented by using a 4 × 1 multiplexer as shown in the figure below. Which one of the following choices of inputs to the multiplexer will realize the requried Boolean expression?



	I_0,	I_1,	I_2,	I_3,	S_1,	S_0
(a)	0,	1,	X,	$\bar{X}$,	Y,	Z
(b)	0,	1,	$\bar{X}$,	X,	Y,	Z
(c)	0,	1,	$\bar{X}$,	X,	$\bar{Y}$,	Z
(d)	1,	0,	X,	$\bar{X}$,	Y,	Z

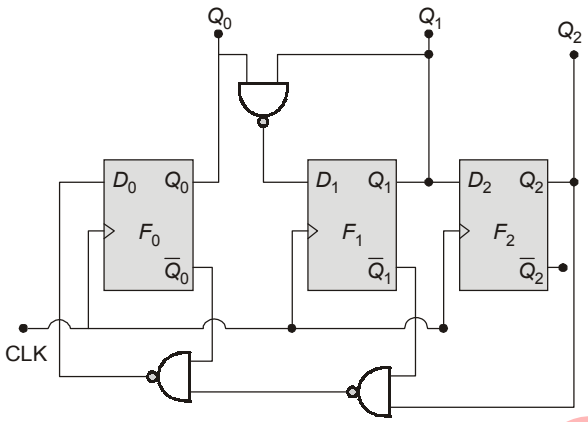
20. (a)

X	Y	Z	A
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

X \ YZ	I_0 00	I_1 01	I_2 10	I_3 11
0	0	1	0	1
1	0	1	1	0
	0	1	X	$\bar{X}$

Thus solution is option (a).

Q.21 Consider the counter circuit and propagation delay table shown below:



Device	Propagation delay
F_0	5 μsec
F_1	4 μsec
F_2	3 μsec
each two-input NAND gate	3 μsec

(Assume all the devices are ideal except for some propagation delay).
What is the maximum clock frequency that can be applied to the above counter?

(a) 125 kHz (b) 100 kHz
(c) 200 kHz (d) 142.85 kHz

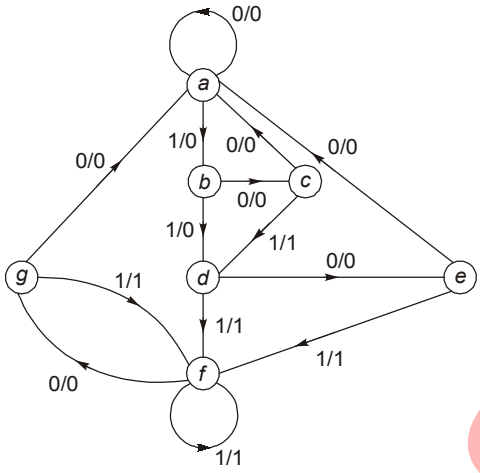
21. (b)

T_{min} = minimum clock period required
= time delay from the time of active clock edge to the point of time, where the latest change appears at the input of flip-flops before the application of next active clock edge.

Let us assume active clock edge is applied at $t = 0$,
then,
the latest change in Q_0 appears at $\Rightarrow t = 5\ \mu s$
the latest change in Q_1 appears at $\Rightarrow t = 4\ \mu s$
the latest change in Q_2 appears at $\Rightarrow t = 3\ \mu s$
the latest change in D_2 appears at $\Rightarrow t = 4\ \mu s$
the latest change in D_1 appears at $\Rightarrow t = 8\ \mu s$
the latest change in D_0 appears at $\Rightarrow t = 10\ \mu s$
so $T_{min} = 10\ \mu sec$

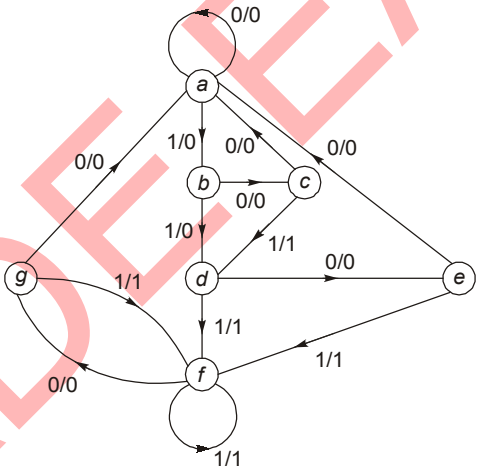
$$f_{c\,max} = \frac{1}{T_{min}} = \frac{1}{10\ \mu sec} = 100\ kHz$$

Q.22 Find the minimum number of flip-flops required to design a sequential circuit whose state diagram is given below?



(a) 2 (b) 3
(c) 4 (d) 5

22. (a)



the state table for given state diagram:

Present state	Next state		Output	
	for $X = 0$	for $X = 1$	for $X = 0$	for $X = 1$
a	*a*	*b*	0	0
b	*c*	*d*	0	0
c	*a*	*d*	0	1
d	*e*	*f*	0	1
e	*a*	*f*	0	1
f	*g*	*f*	0	1
g	*a*	*f*	0	1

X = input

state-*g* and state-*e* are equal, so we can replace state-*g* with state-*e* so, simplified state table will be,

Present state	Next state		Output	
	for $X = 0$	for $X = 1$	for $X = 0$	for $X = 1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	1
d	e	f	0	1
e	a	f	0	1
f	e	f	0	1

now, state-f and state-d are equal. So, we can replace state-f with state-d
so, simplified state table will be,

Present state	Next state		Output	
	for $X = 0$	for $X = 1$	for $X = 0$	for $X = 1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	1
d	e	d	0	1
e	a	d	0	1

now, state-e and state-c are equal. So, we can replace state-e with state-c
so, simplified state table will be,

Present state	Next state		Output	
	for $X = 0$	for $X = 1$	for $X = 0$	for $X = 1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	1
d	c	d	0	1

- it is not possible to reduce the state table further, as there are no more equal states.
- so, minimum number of states required to design the circuit = 4.
  and minimum number of flip-flops required = 2.

Q.23 An 8-bit digital ramp ADC with a 40 mV resolution uses a clock frequency of 2.5 MHz and a comparator with threshold voltage $V_T = 1$ mV. The digital output for $V_A = 6$ V is

(a) 10010111 (b) 10010110
(c) 10111110 (d) 10111111

23. (a)

$(\text{Digital Equivalent})_{10} \times \text{Resolution} > V_A + V_T$

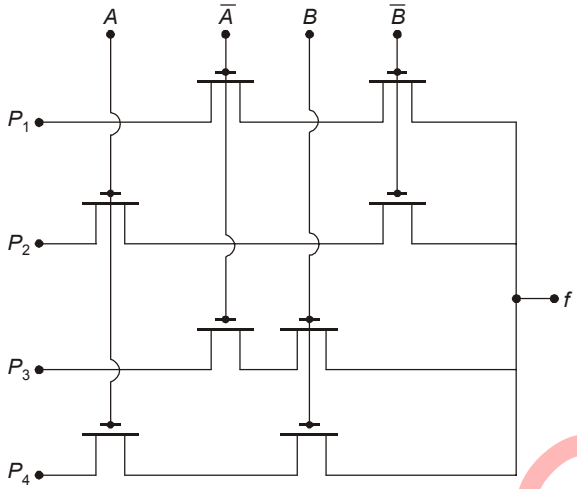
$> 6000 \text{ mV} + 1 \text{ mV}$

$(\text{Digital Equivalent})_{10} \times 40 \text{ mV} > 6001 \text{ mV}$

$$(\text{Digital Equivalent})_{10} > \frac{6001}{40} = 150.025 \Rightarrow 151 \text{ is the next quantization level}$$

so, digital output $= (10010111)_2 \Rightarrow (151)_{10}$

Q.24 Consider an NMOS pass logic network shown below:



if A, B are input variables and f is output variable, then for which combination of P_1, P_2, P_3 and P_4 the circuit will behave as EX-OR gate?

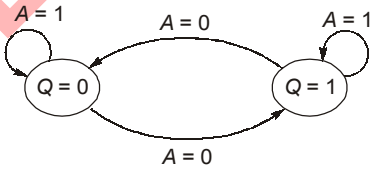
(a) $P_1 = P_4 = 1, P_2 = P_3 = 0$
(b) $P_1 = P_4 = 0, P_2 = P_3 = 1$
(c) $P_1 = P_3 = 1, P_2 = P_4 = 0$
(d) $P_1 = P_3 = 0, P_2 = P_4 = 1$

24. (b)

A	B	f
0	0	P_1
0	1	P_2
1	0	P_3
1	1	P_4

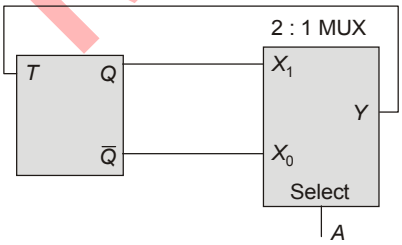
so, the given pass logic network acts as EX-OR gate when $P_1 = P_4 = 0$ and $P_2 = P_3 = 1$.

Q.25 The state transition diagram for the logic circuit is shown below

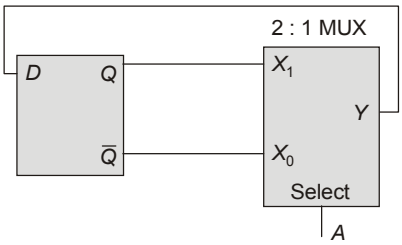


The logic circuit will be

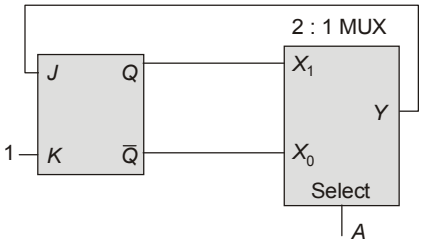
(a)



(b)



(c)



(d) None of these

25. (b)

from the state diagram,

When $A = 1 \Rightarrow Q_{n+1} = Q_n \Rightarrow$ next state is same as present state.

When $A = 0 \Rightarrow Q_{n+1} = \bar{Q}_n \Rightarrow$ next state is the toggle of present state.

In (a) and (c) case, when input $A = 1$ and $Q = 1$, they toggle,

Hence, correct representation in option (b).

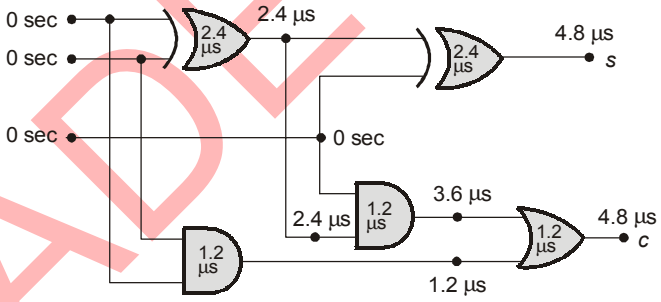
Q.26 A half adder is implement with XOR and AND gates. A full adder is implemented with two half adders and one OR gate. The propagation delay of an XOR gate is twice that of an AND/OR gate. The propagation delay of an AND/OR gate is 1.2 μsec. A 4-bit ripple carry binary adder is implemented by using full adders. The total propagation delay of this 4-bit binary adder is

(a) 19 μsec (b) 19.2 μsec

(c) 38 μsec (d) 38.4 μsec

26. (b)

For one full Adder :

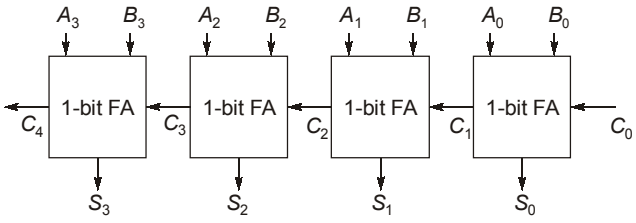


for one FA,

delay to produce sum $\Rightarrow t_{ds} = 4.8$ μs

delay to produce carry $\Rightarrow t_{dc} = 4.8$ μs

for 4-bit ripple carry adder :

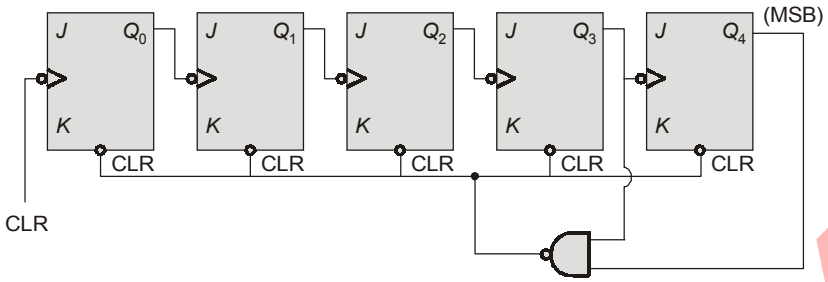


$t_d = 3t_{dc} + t_{ds} = 4(4.8)$ μs

$= 19.2$ μs

Numerical Answer Type Questions : Q.27 to Q.33 carry 2 marks each

Q.27 The MOD-number of the asynchronous counter shown in the figure below is



27. (24)

When Q_4Q_3 is 11, then CLR = 0, hence the count goes back to 00000.

$$Q_4\,Q_3\,Q_2\,Q_1\,Q_0 \quad 0\;0\;0\;0\;0 \longrightarrow 1\;0\;1\;1\;1 \longrightarrow 0\;0\;0\;0\;0$$

Thus, counter counts 0 - 23, and clears at 24. It's a MOD-24 counter.

Q.28 If the maximum frequency with which a 4-bit binary ripple counter can work is 25 MHz, then the propagation delay from CLK to Q of each flip-flop is _____ nsec.

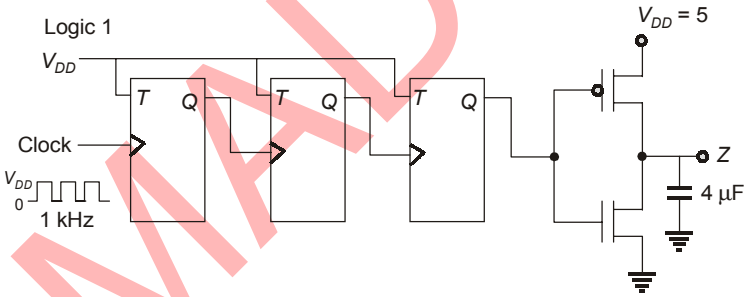
28. (10)

$$f_{max} = \frac{1}{nt_{pd}} \quad ; \quad t_{pd} = \text{propagation delay of each flip-flop and } n = \text{number of flip flops}$$

$$t_{pd} = \frac{1}{n \times 25 \times 10^6}\ \text{sec}$$

$$= \frac{1000}{4 \times 25} \times 10^{-9}\ \text{sec} = 10\ \text{nsec}$$

Q.29



Consider the circuit shown above. If the input clock frequency is 1 kHz, then the dynamic average power dissipated by the CMOS inverter circuit is _____ mW.

29. 12.5 (12.4 to 12.6)

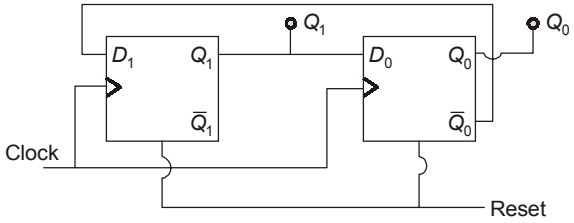
The input frequency of CMOS inverter = $f_{in} = \frac{f_{clk}}{8} = \frac{1 \times 10^3}{8}$ Hz

$$P_{dissipation} = CV_{DD}^2 f_{in}$$

$$= 4 \times 10^{-6} \times 25 \times \frac{1 \times 10^3}{8}\ \text{W}$$

$$= \frac{100}{8}\ \text{mW} = 12.5\ \text{mW}$$

Q.30 The initial state ($Q_1 Q_0$) of the counter shown below is (00). The minimum number of clock pulses required after which the state ($Q_1 Q_0$) goes to (00) again is _____.



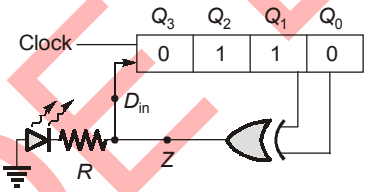
30. (4)

Clk No.	Q_1	Q_2	
0	0	0	→initial
1	1	0	
2	1	1	
3	0	1	
4	0	0	

It's a Johnson counter after 4 clock pulses the state ($Q_1 Q_0$) will be (00) again.

Q.31 The initial contents of a 4-bit serial-in-parallel out, right shift, shift register is shown in the given figure is 0110. By the end of 7th clock pulse from initial state, the number of times the LED will be in ON state is _____.

(Assume logic 1 as + 5 V and logic 0 as –5 V)



31. (3)

Clk No.	D_{in} before clk pulse	Q_3	Q_2	Q_1	Q_0	Z after clk pulse	LED state
0	-	0	1	1	0	1	OFF
1	1	1	0	1	1	0	ON
2	0	0	1	0	1	1	OFF
3	1	1	0	1	0	1	OFF
4	1	1	1	0	1	1	OFF
5	1	1	1	1	0	1	OFF
6	1	1	1	1	1	0	ON
7	0	0	1	1	1	0	ON

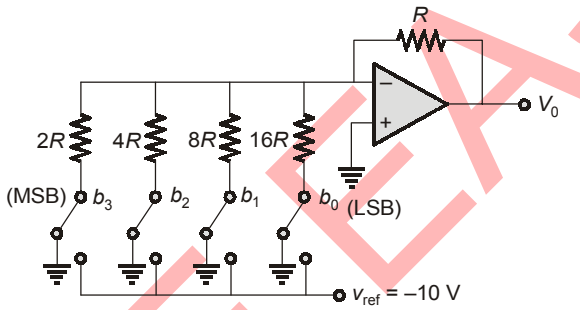
Q.32 An n-bit A/D convertor is required to convert an analog input in the range 0 - 5 V with a maximum error of 10 mV on each conversion. The minimum value of n is _____.

32. (9)

$$\text{maximum quantization error} = \Delta = \frac{5\text{ V}}{(2^n - 1)}$$

so,
$$\frac{5\text{ V}}{(2^n - 1)} \le 10\text{ mV}$$
$$(2^n - 1) \ge 500$$
$$2^n \ge 501$$
$$n \ge 9$$
$$n_{min} = 9$$

Q.33 Consider the 4-bit DAC shown in the following figure. The output voltage V_0 for an input data 0110 will be _____ V.



33. 3.75 (3.60 to 3.80)

$$V_0 = -RV_{ref}\left[\frac{b_3}{2R} + \frac{b_2}{4R} + \frac{b_1}{8R} + \frac{b_0}{16R}\right]$$
$$= -\frac{V_{ref}}{16}[8b_3 + 4b_2 + 2b_1 + b_0]$$
$$V_0 = -\frac{V_{ref}}{16}\text{ [decimal equivalent of input binary code]}$$

given input binary code $= (0110)_2 = (6)_{10}$

so,
$$V_0 = \frac{10}{16}(6) = 3.75\text{ V}$$

❍❍❍❍

