Digital Electronics & Microprocessors Laboratory (EC2P006)

EXPERIMENT-5

Shorya Sharma
19EE01017

PART 1

Aim:

Simulation and design of a 4 bit Multiplier

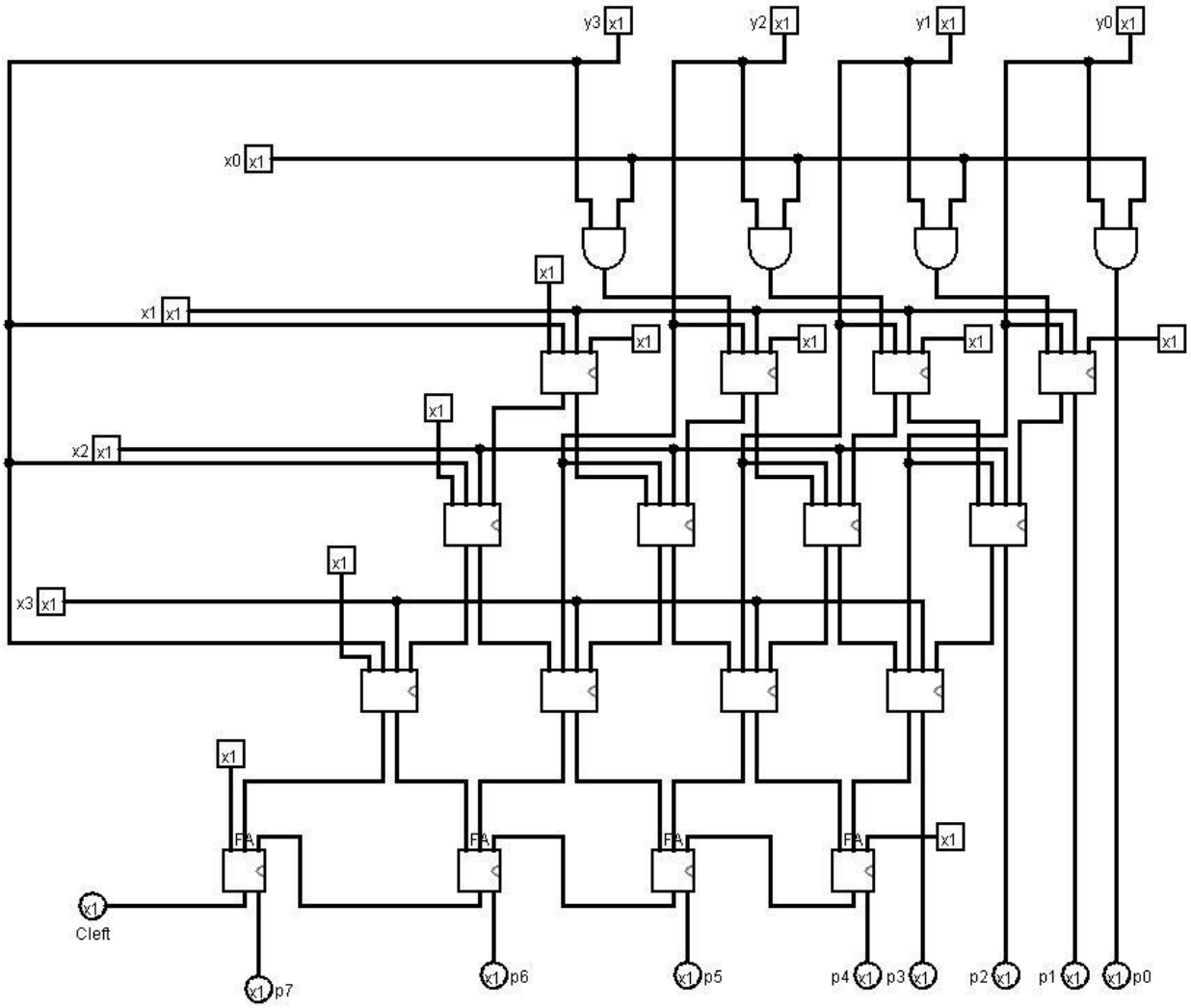
Theory:

A 4 × 4 unsigned binary multiplier takes two, four bit inputs and produces an output of 8 bits; the 8 bits together being the equivalent binary formof the product that is formed by multiplication of the decimal forms of the given numbers formed the bits of X(x0,x1,x2,x3) and Y(y0,y1,y2,y3) taken together in serial order.

Circuit Diagram:

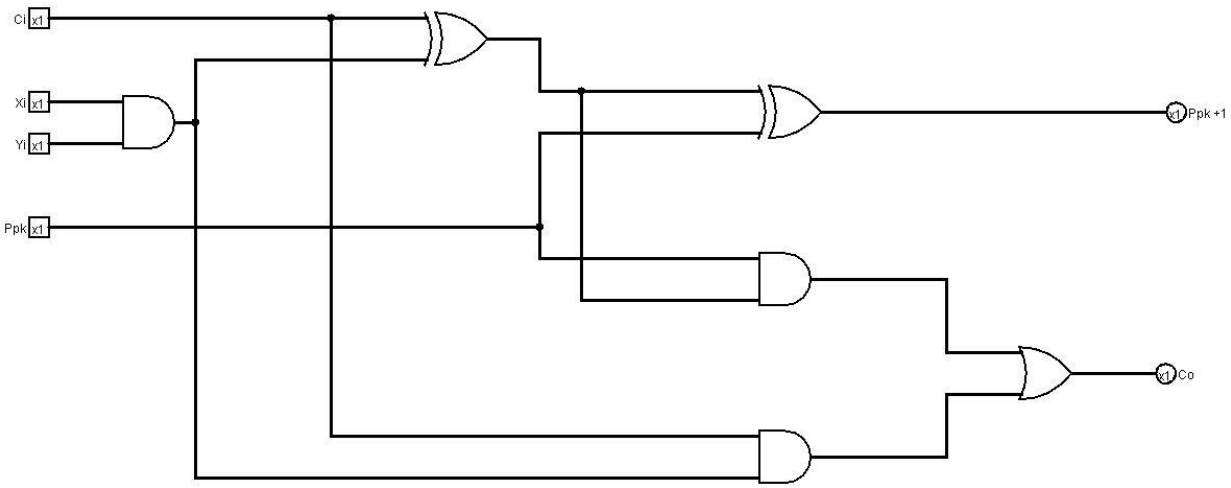
(Multiplication of 11(1011 in binary) and 10(1010 in binary)=110(01101110 in binary)

Overall Circuit:

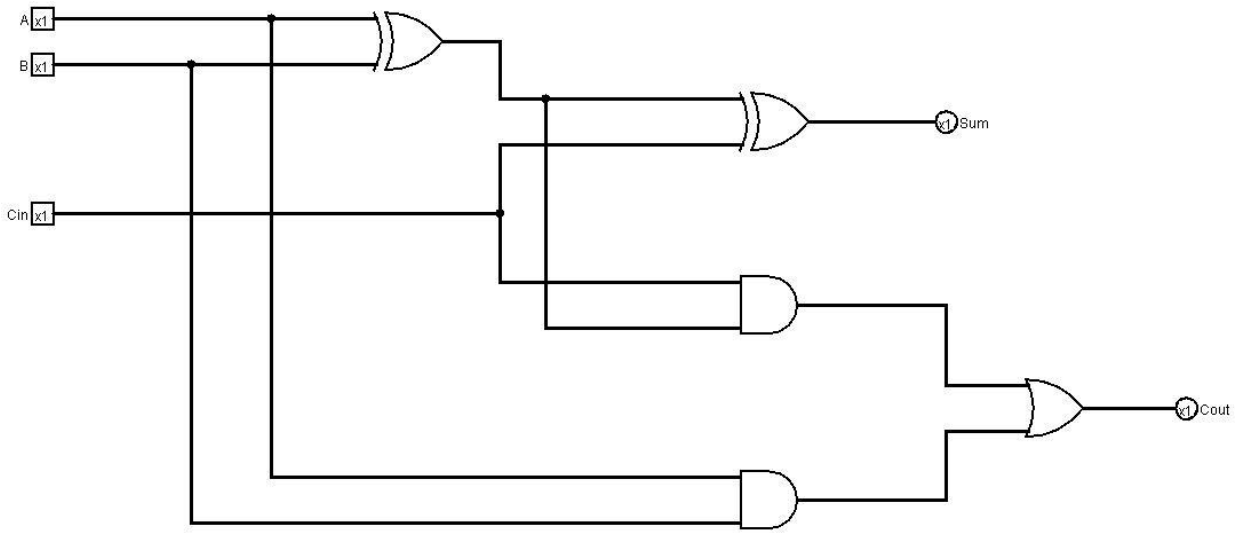


Observe the inputs in the sequence x3x2x1x0 and y3y2y1y0;and their product yields p7p6p5p4p3p2p1p0(11,10 and 110 respectively as vivid in the circuit above)

Basic building block:



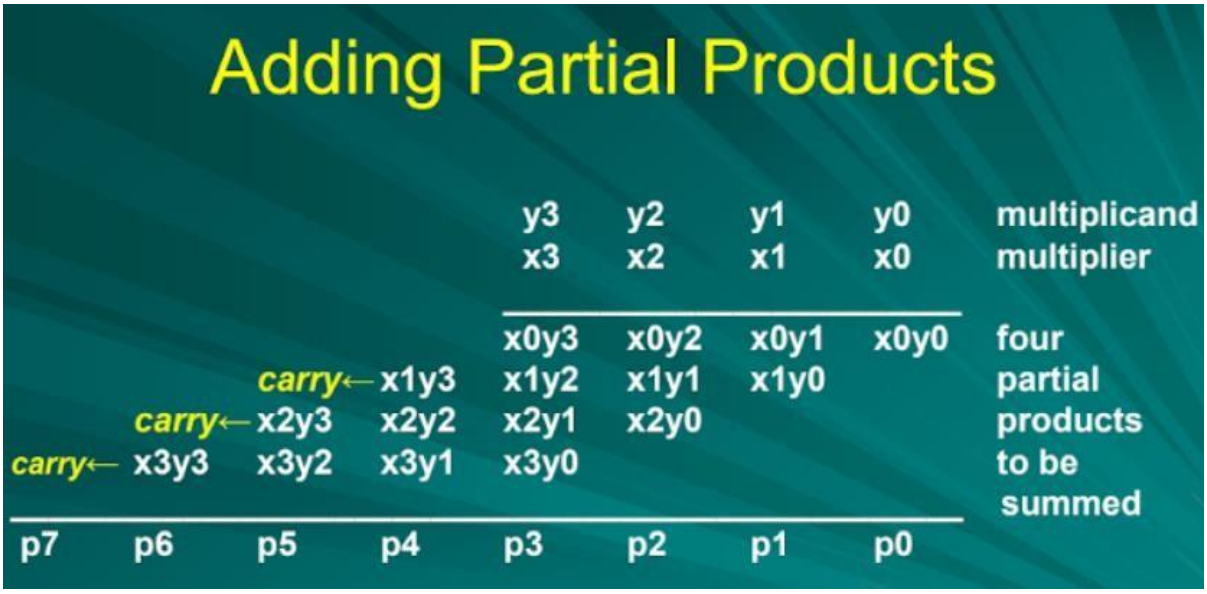
Full Adder:



Discussions

So what basically happens is in the basic building block(in the first step),a combined product of each bit combination of y(y3 y2 y1 y0) together with the last bit of x(x0) is combined together with the help of an and gate that is passed as one of the 3 inputs along with Ppk and Cin (0-for the first case) that leads to an output of Cout (that is passed on as Cin for successive basic building boxes) and a Ppk+1 that is passed on as a bit of the calculated output at the appropriately determined position of the resultant binary form of the output. In the last phase, we omit the And gate portions of the building block and use the

Full adder only that returns as an output bit and a carry that is passed in series to the neighboring full adders as a Cin.



If the multiplicand is 1011 (11) & multiplier is 1010 (10) as in the given case; then multiplication happens as follows:→

```
  1 0 1 0
  1 0 1 0
  0 0 0 0
1 0 1 1
0 0 0 0
1 0 1 1
1 1 0 1 1 1 0
```

→ Basic addition process where 0+1=0 with carry 0 & 1+1=0 with carry 1

This gives the desired output of 01101110 (110) with a Cout of 0.

PART 2

Aim:

To build a 8 bit comparator from 2 4 bit comparators using basic gates.

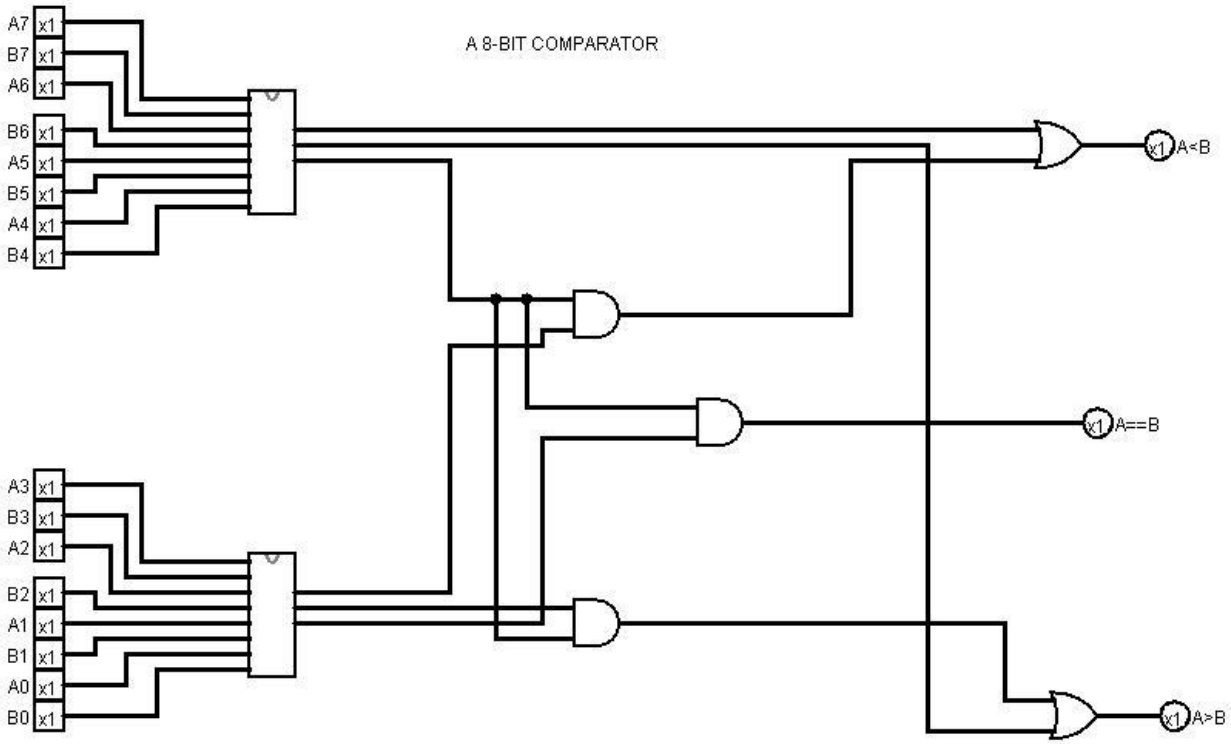
Theory:

An 8-bit comparator compares the two 8-bit numbers by cascading of two4-bit comparators. The circuit connection of this comparator is shown below in which the lower order comparator A<B, A=B and A>B outputs are connected to the respective cascade inputs of the higher order comparator.

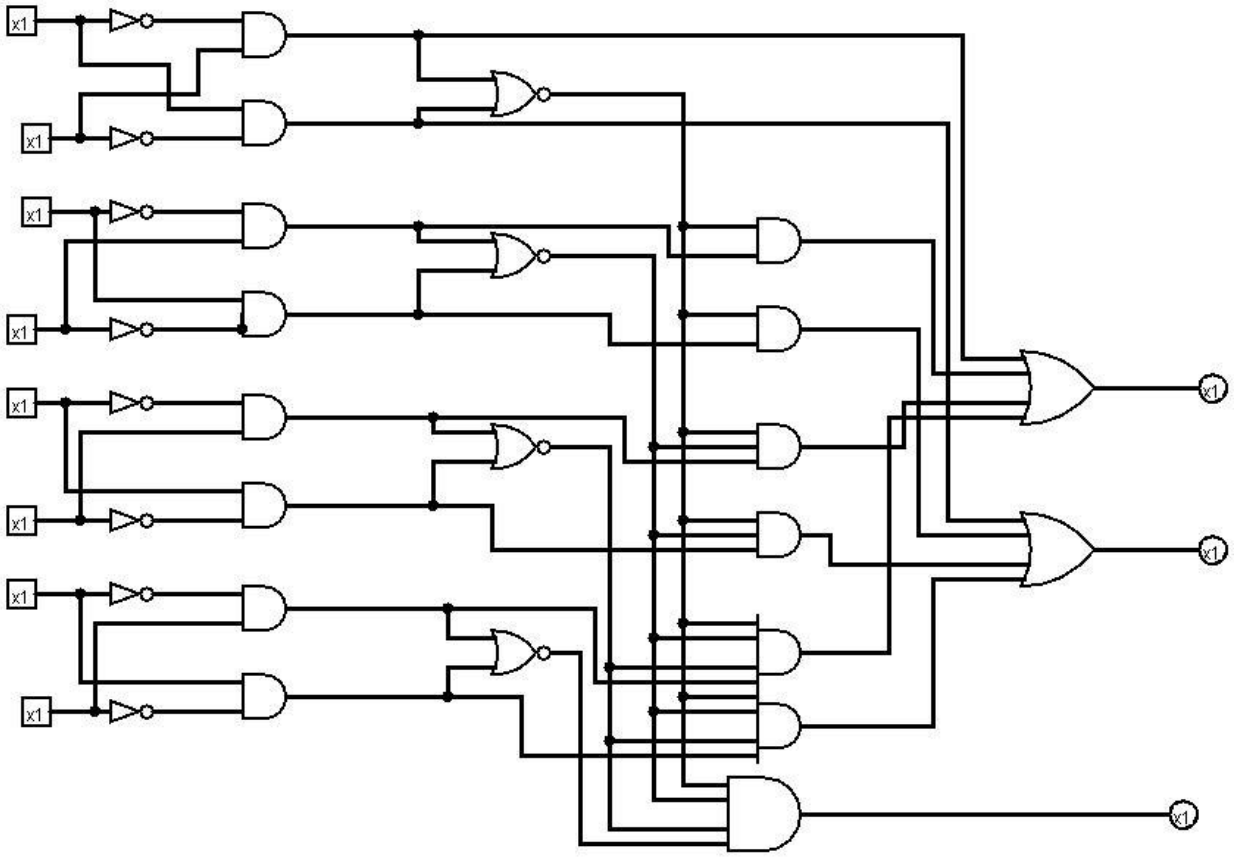
For the lower order comparator, the A=B cascade input must be connected High, while the other two cascading inputs A ,B must be connected to LOW. The outputs of the higher order comparator become the outputs of this eight-bit comparator.

Circuit Diagram:

4 bit Comparator:

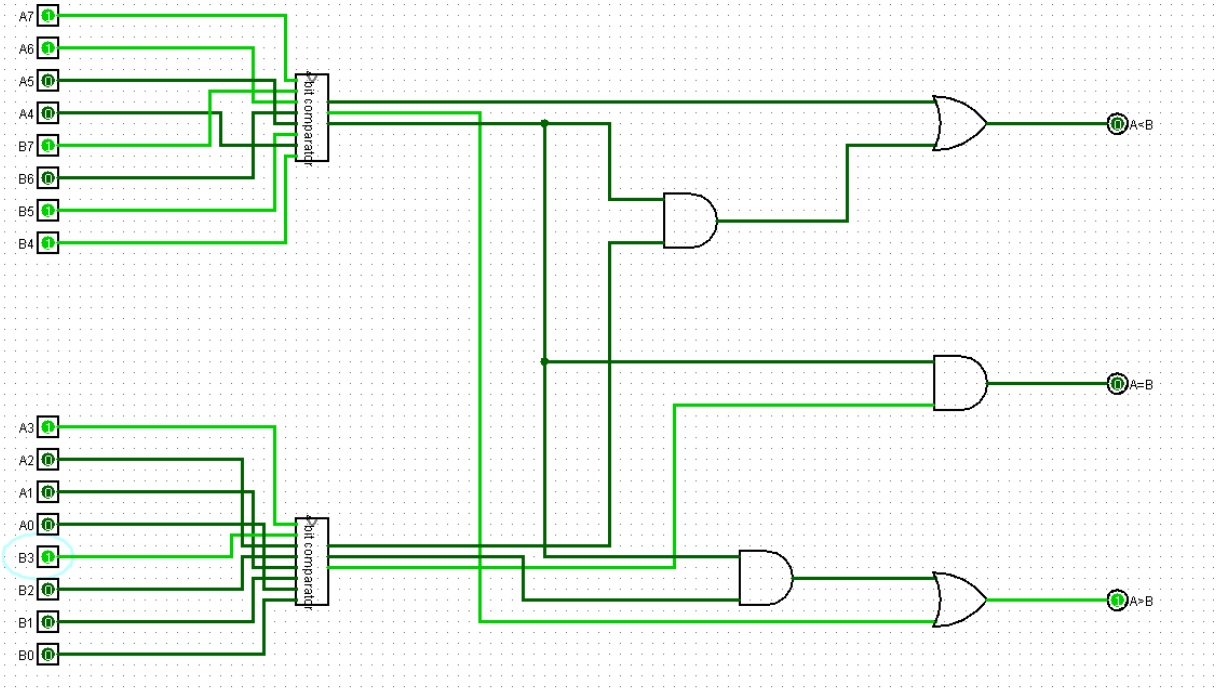


8-bit comparator(using 2 4 bit comparator):

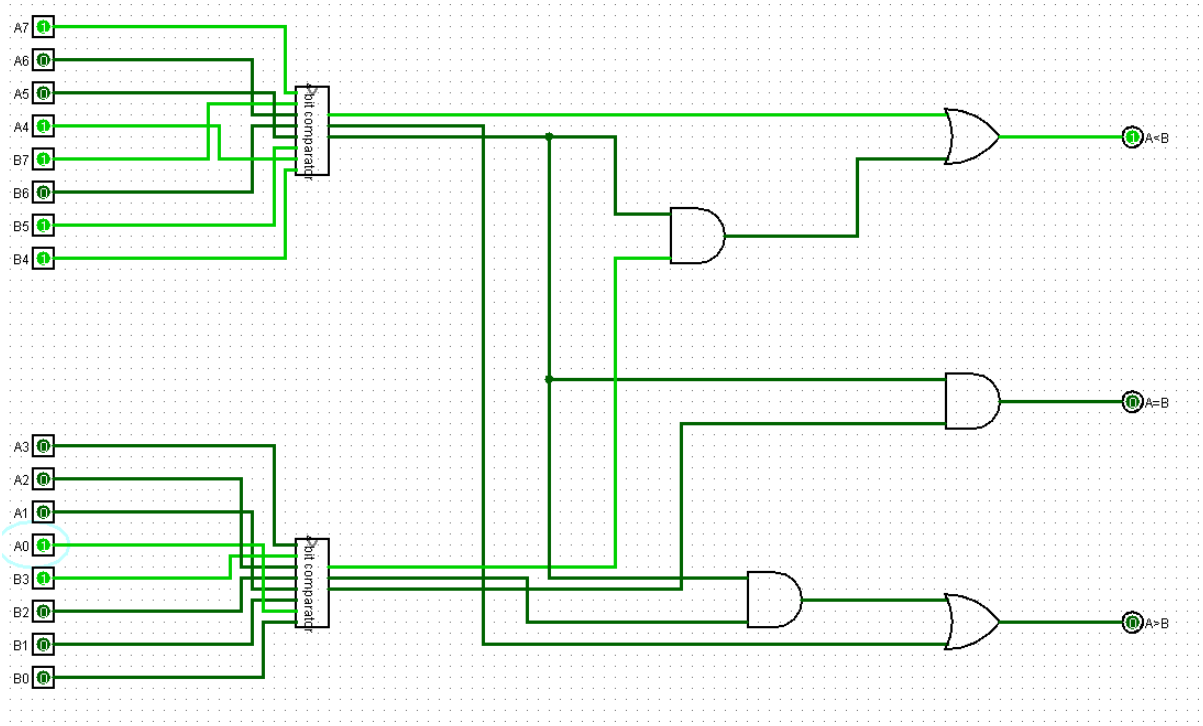


Simulations:

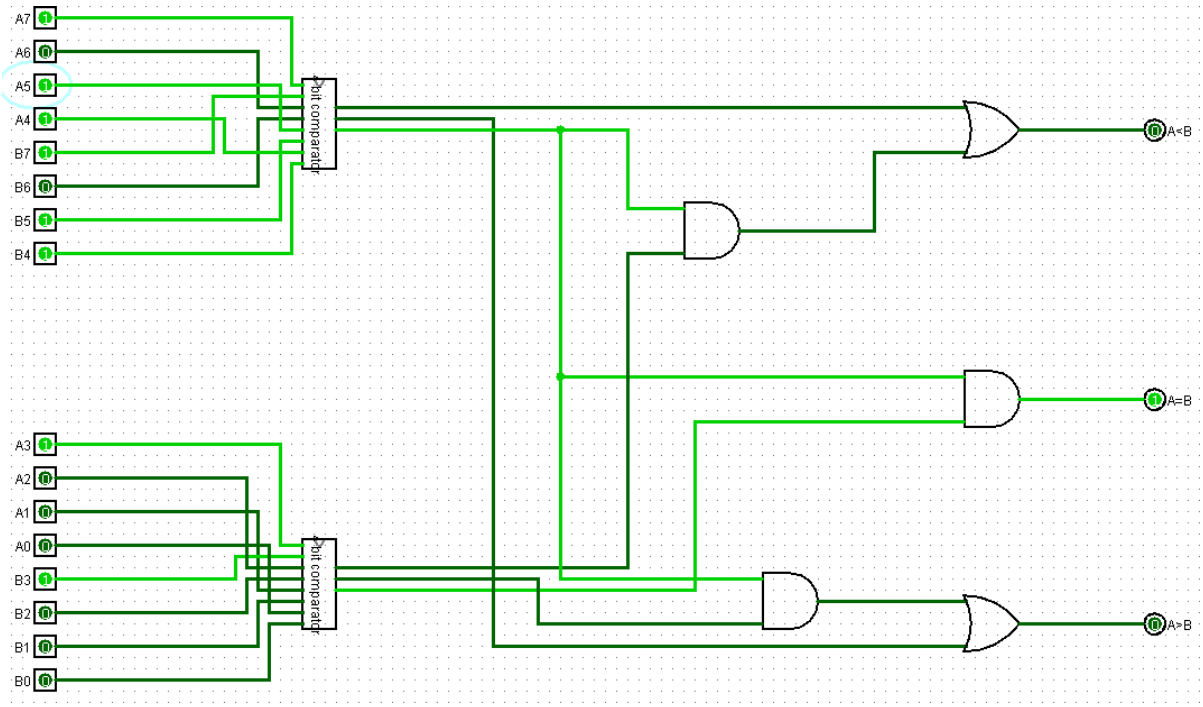
1) A=200(11001000 in binary) is greater than B=184(10111000 in binary)



2) A=145(10010001 in binary) is lesser than B=184(10111000 in binary)

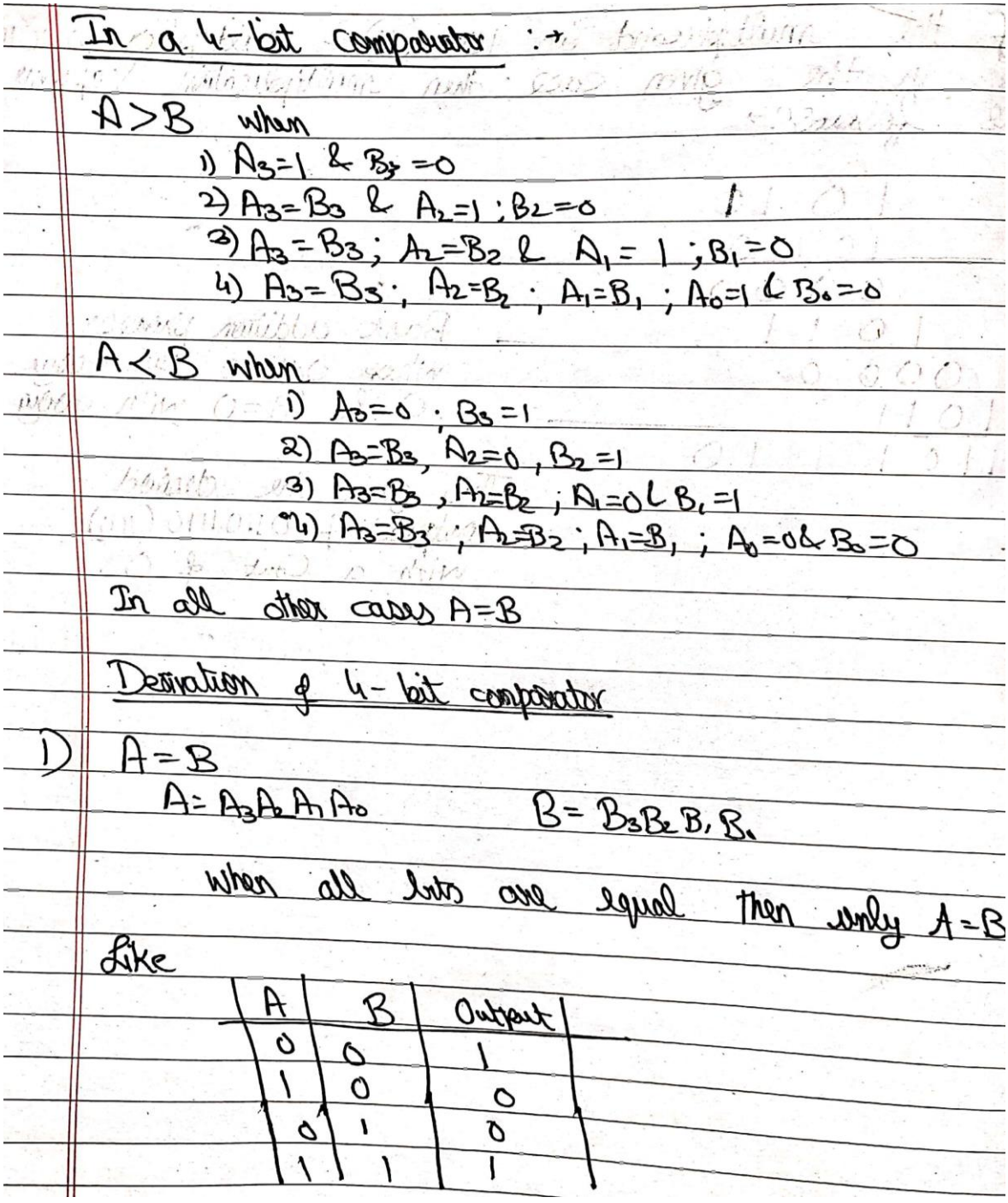


3)184(10111000 in binary) equals 184(10111000 in binary)



Discussions

So what we basically do here is design two 4 bit comparators, and then combinetwo 4 bit comparators by separating the binary forms of the two 8 bit numbers into first 4 and last 4 bits and then passing them as input values to the two 4 bit comparators and then combining the resultant outputs accordingly to obtain the 3 conditions: A<B; A=B and A>B. Like what we did here was obtained the greater case from one comparator and a lesser case from another one, combined them with AND gate and then combined the output with the greater output fromthe comparator (from which we earlier took the lesser output) and combined with OR gate that results in A<B.A similar case is performed for the A>B case. For equality case…all bits must be equal, therefore that's possible only when both the outputs of the comparators are A=B and combing them via AND Gate also give a true output(A=B).



In a 4-bit comparator :-

A>B when

1) $A_3=1$ & $B_3=0$
2) $A_3=B_3$ & $A_2=1$; $B_2=0$
3) $A_3=B_3$; $A_2=B_2$ & $A_1=1$; $B_1=0$
4) $A_3=B_3$; $A_2=B_2$; $A_1=B_1$; $A_0=1$ & $B_0=0$

A<B when

1) $A_3=0$; $B_3=1$
2) $A_3=B_3$, $A_2=0$, $B_2=1$
3) $A_3=B_3$, $A_2=B_2$; $A_1=0$ & $B_1=1$
4) $A_3=B_3$; $A_2=B_2$; $A_1=B_1$; $A_0=0$ & $B_0=0$

In all other cases A=B

Derivation of 4-bit comparator

1) A=B

$A=A_3A_2A_1A_0$ $\quad B=B_3B_2B_1B_0$

When all bits are equal then only A=B

Like

A	B	Output
0	0	1
1	0	0
0	1	0
1	1	1

Let's say if we take

$x_3 = \overline{A_3 B_3} + A_3 B_3$

$x_2 = \overline{A_2 B_2} + A_2 B_2$

$x_1 = \overline{A_1 B_1} + A_1 B_1$

$x_0 = \overline{A_0 B_0} + A_0 B_0$

$(A=B) = x_3 x_2 x_1 x_0$

$(A>B) = A_3 \bar{B}_3 + x_3 A_2 \bar{B}_2 + x_3 x_2 A_1 \bar{B}_1 + x_3 x_2 x_1 A_0 \bar{B}_0$

$(A<B) = \bar{A}_3 B_3 + x_3 \bar{A}_2 B_2 + x_3 x_2 \bar{A}_1 B_1 + x_3 x_2 x_1 \bar{A}_0 B_0$

These abv. expressions are sequentially bit dependent like say

if $A_3 > B_3$ is true ∴ the exp. in output is $A_3 \bar{B}_3$

Similarly other terms in $A>B$; $A<B$ & $A=B$

For finding 8-bit comparator from 24-bit comparator:

For $A=B$; all bits must be equal

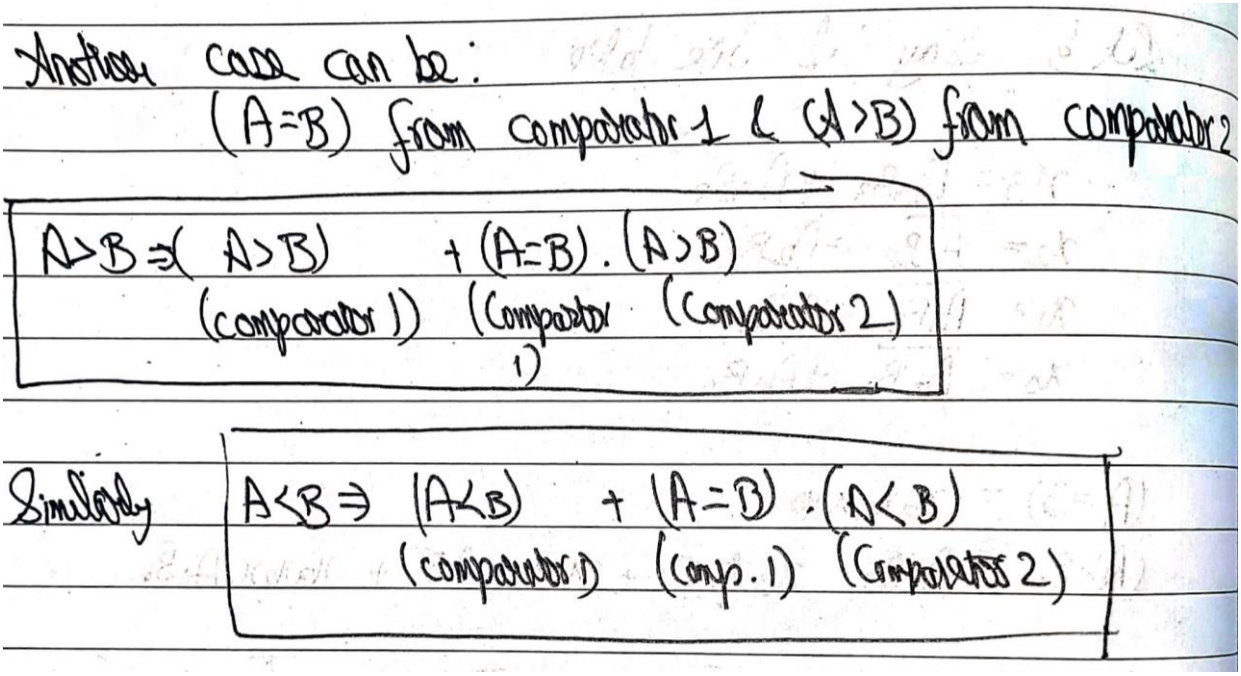
∴ $A=B \Rightarrow (A=B) \cdot (A=B)$

(from 1st comparator) (from 2nd comparator)

For $A>B$; if $(A>B)$ from comparator 1

MSP of $A >$ MSP of B

∴ Net $A>B$



Conclusion

Thus, I successfully simulated a 4 bit multiplier and also 4 bit and 8 bit comparators and verified their functioning simulating known theoretical results. It was a wonderful experience simulating and gaining insights into the actual working of these devices…that too from only Basic Gates.