Digital Electronics & Microprocessors Laboratory (EC2P006)

EXPERIMENT-4

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PART-1

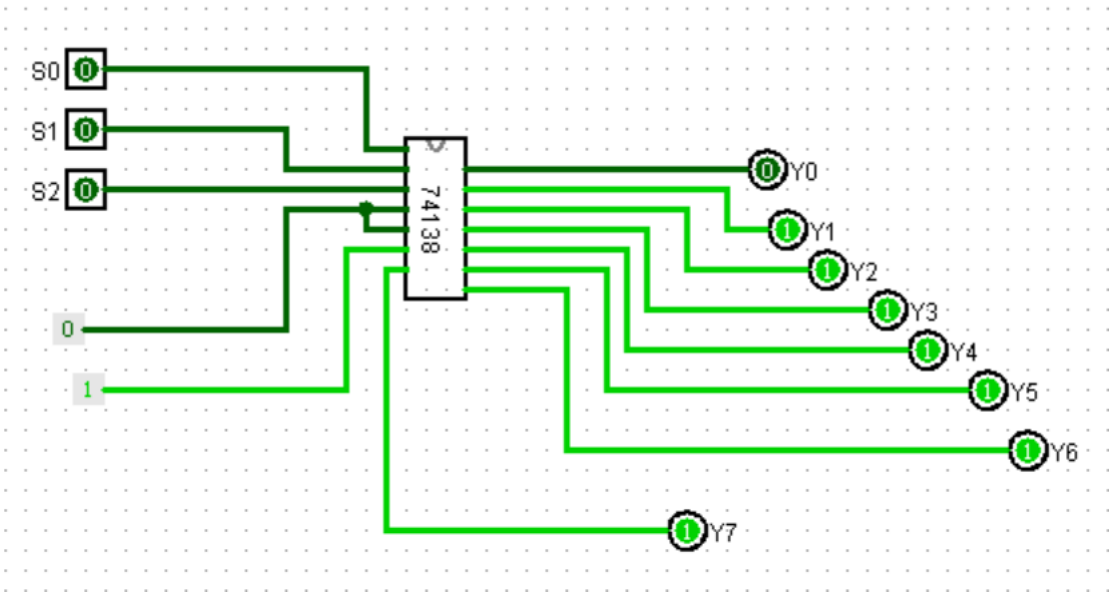
AIM:

Understanding how a 3:8 decoder works.

THEORY:

A 3:8 decoder circuit gives 8 logic outputs for 3 inputs and has a enable pin. The circuit is designed with AND and NOT gates. So, this will take 3 inputs and give 2^3 i.e. 8. The outputs of the decoder is the minterms of the 3- input variables. Its works just like an 1:8 DEMUX. These decoders can be active high decoder or an active low decoder. The enable pin helps to control the operation of the decoder. Based on the input at the enable pin the decoder can be classified as enable high decoder and enable low decoder.

RESULT:



TRUTH TABLE:

S0	S1	S2	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
0	0	0	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1
0	1	0	1	1	0	1	1	1	1	1
0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	0	1	1	1	1	1	1
1	0	1	1	1	1	1	1	0	1	1
1	1	0	1	1	1	0	1	1	1	1
1	1	1	1	1	1	1	1	1	1	0

DISCUSSION

The IC Model 74138 is a 3*8 Decoder. On comparing the output values in comparison to the inputs S0, S1 and S2 it can be seen that

Y0=S0'S1'S2' ,Y1=S0'S1'S2, Y2=S0'S1S2', Y3=S0'S1S2,Y4=S0S1'S2', Y5=S0S1'S2 ,Y6=S0S1S2' ,Y7=S0S1S2.

PART-2

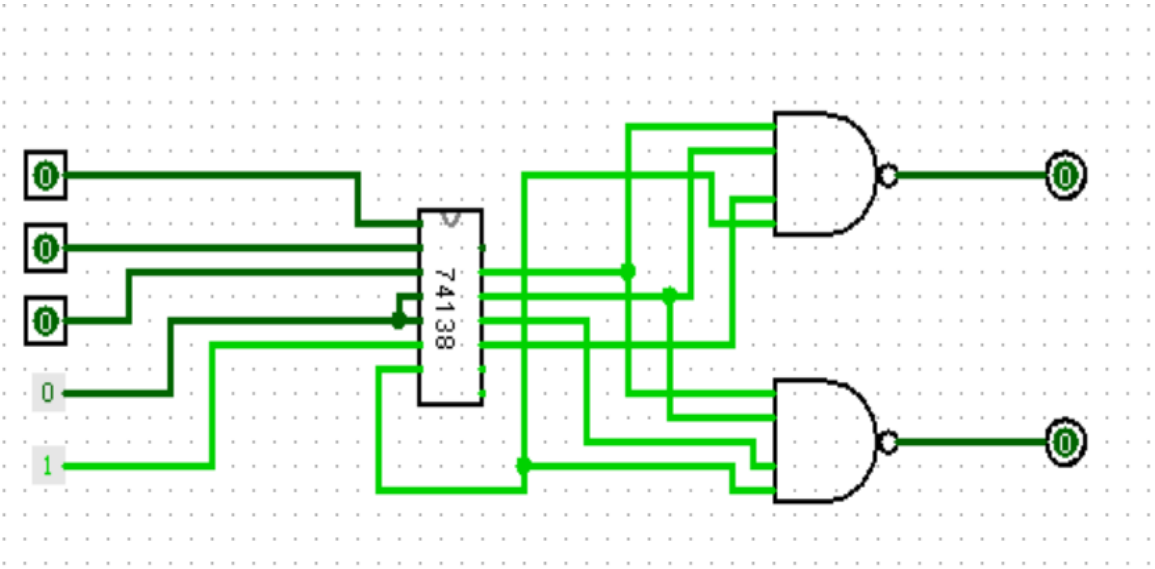
AIM:

To Design a full subtractor using a 3*8 DECODER.

THEORY:

A Full subtractor is a combinational circuit that accepts three inputs A
,B and Bin and gives two outputs-D(difference) and Bout (borrow).The operation its perform is A-B-Bin.

RESULT:



TRUTH TABLE:

A	B	Bin	D	Bout
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

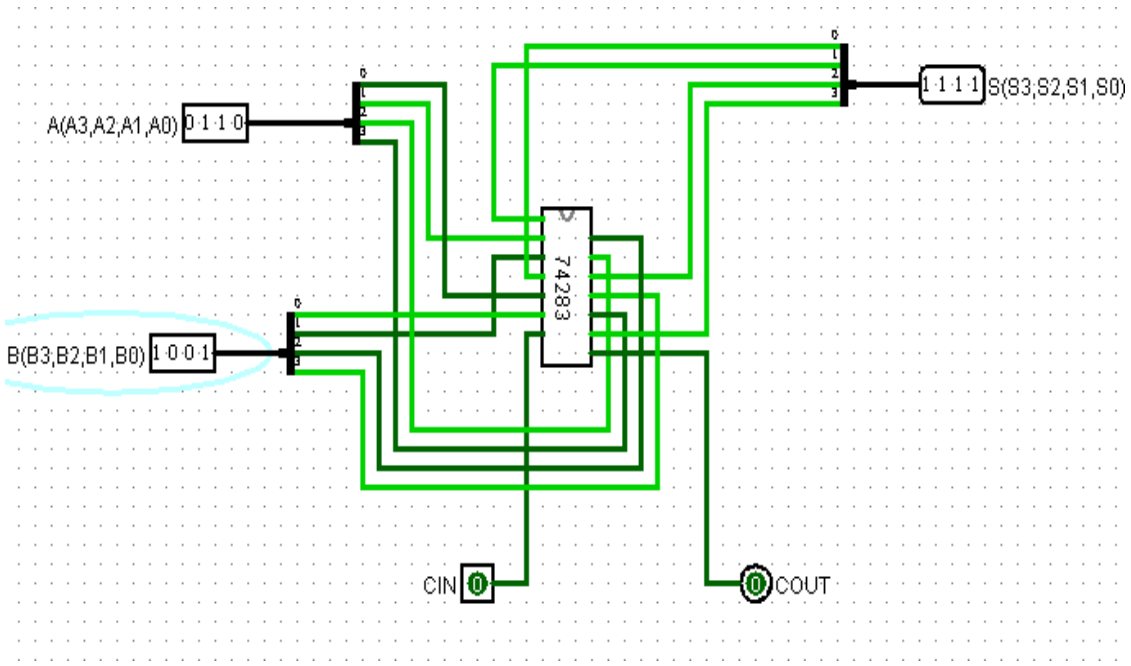
PART-3

AIM:

Understanding the working of a 4-bit binary adder through performingbasic4bitadditionlike6+9 withnocarryand8+14withcarry1.

RESULT:

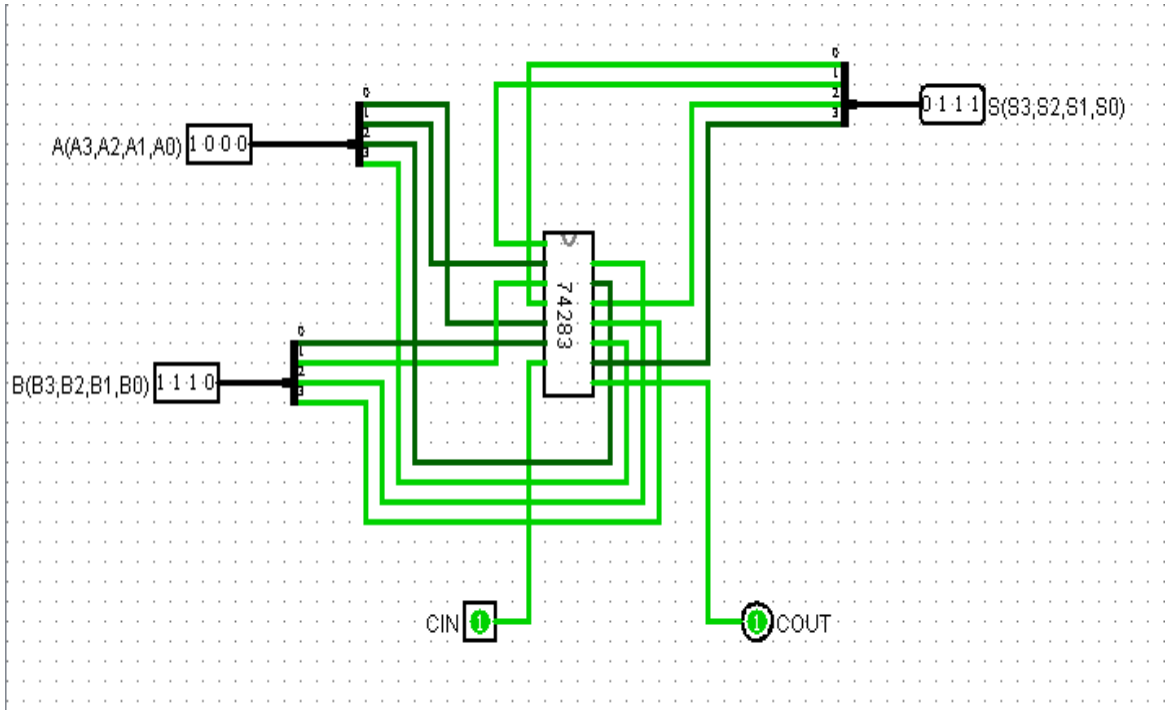
ADDITION OF 6+9 WITH CARRY 0



6 in base scale-10=0110 in base scale 2;A0=0,A1=1,A2=1,A3=0 9 in base scale-10=1001 in base scale 2;B0=1,B1=0,B2=0,B3=1 C-1(carry in)=0

6+9 =15 in base scale 10=01111 in base scale 2;C3(carry out)=0,S0=1,S1=1,S2=1,S3=1

ADDITION OF 8+14 WITH CARRY 1



8 in base scale-10=1000 in base scale 2;A0=0,A1=0,A2=0,A3=1 14 in base scale-10=1110 in base scale 2;B0=1,B1=1,B2=1,B3=0 C-1(carry in)=1

8+14=23 is in base scale 10=10111 in base scale 2; C3(carry out)=1,S0=0,S1=1,S2=1,S3=1

DISCUSSION

Here I performed addition of two 4 bits addition with carry and without carry. For performing this addition I used the IC 74283.

PART-4

AIM:

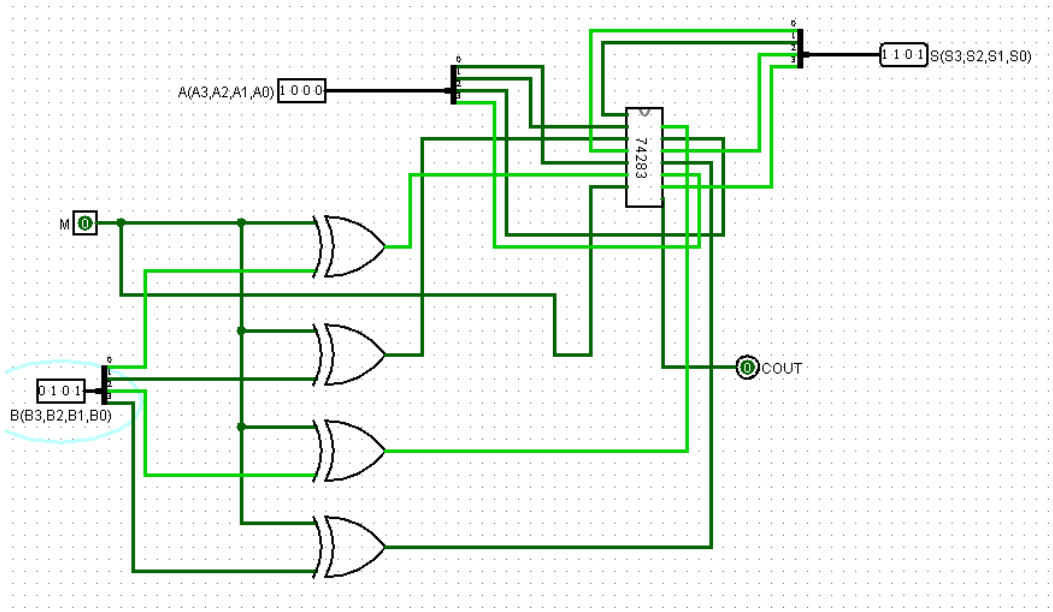
Designing the 4-bit parallel adder/Subtractor using the IC MODEL 74283.

THEORY:

A Binary Adder-Subtractor is one which is capable of both addition and subtraction of binary numbers in one circuit itself. The operation being performed depends upon the binary value the control signal holds. It is one of the components of the ALU (Arithmetic Logic Unit).

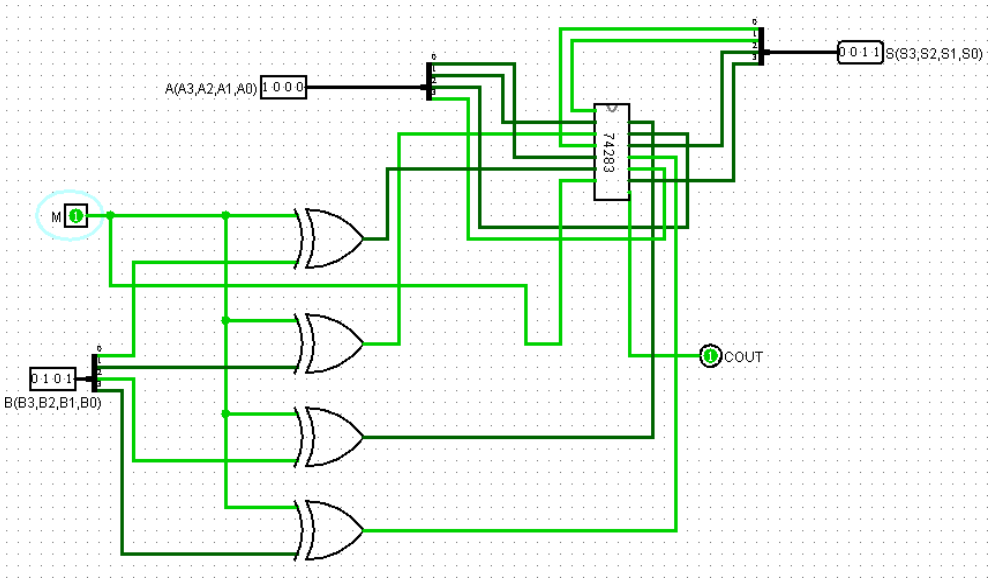
RESULT:

ADDITION OF (8+5)



8 in base scale-10=1000 in base scale 2;A0=0,A1=0,A2=0,A3=1 5 in base scale-10=0101 in base scale 2;B0=1,B1=0,B2=1,B3=0 C-1(carry in)=M=0 8+5=13 in basescale10=01101 in base scale 2;C3(carry out)=0,S0=1,S1=0,S2=1,S3=1

SUBTRACTION 8-5



8 in base scale-10=1000 in base scale 2;A0=0,A1=0,A2=0,A3=1 5 in base scale-10=0101 in base scale 2;B0=1,B1=0,B2=1,B3=0 CIN=M=0 8-5 =3 in base scale10=0011 in base scale 2;COUT=1,S0=1,S1=1,S2=0,S3=0

DISCUSSION

- So here the M is acting as a controller. Depending on the input of M the Digital circuit can be used as an adder or a subtractor. For M=1 its acts as a Subtractor and for M=0 its acts a Adder. Whenever M=0,0 XOR with any of B0, B1, B2,B3 gives the same B0,B1,B2,B3 because XOR with one input 0 acts as a buffer.
- So, the operation performed when M=0 is A+B+0=A+B.
- Whenever M=1;1 XOR with B gives B'. As XOR gate with one input 1 acts as an invertor.Now operation performed in the digital circuit is A+B'+1; Now B'+1 can be said as (1's complement of B)+1 which is equal to 2's complement of B which is –B So finally the operation that takes place in the circuit is A-B.

CONCLUSION

Through this experiment I designed the required circuits using decoders specifically 3*8 DECODER.I learnt the importance of carry in experiment4 which taught me how by just varying the carry a adder can be used as a subtractor and vice versa. I also implemented a full subtractor using a 3*8 DECODER and few NAND gates. So, the entire experiment was a great learning experience for me