Digital Electronics & Microprocessors Laboratory (EC2P006)

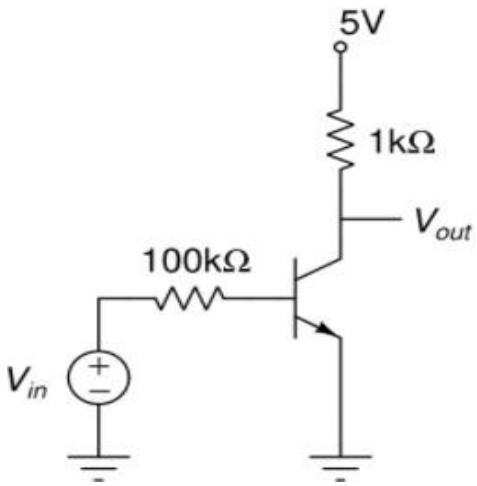
EXPERIMENT-1

Shorya Sharma
19EE01017

Part 1

Aim: Measuring the characteristics of a BJT based NOT gate.

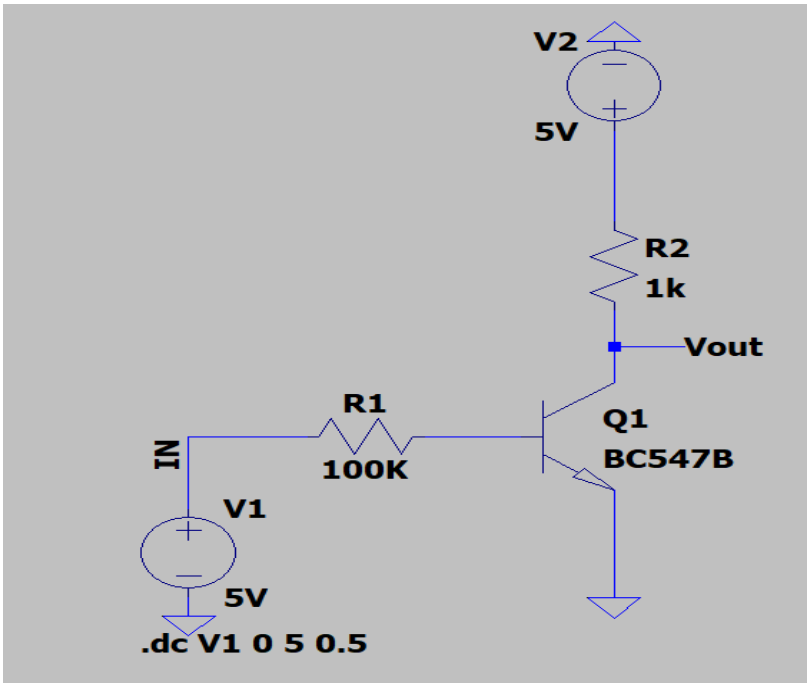
Circuit Diagram:



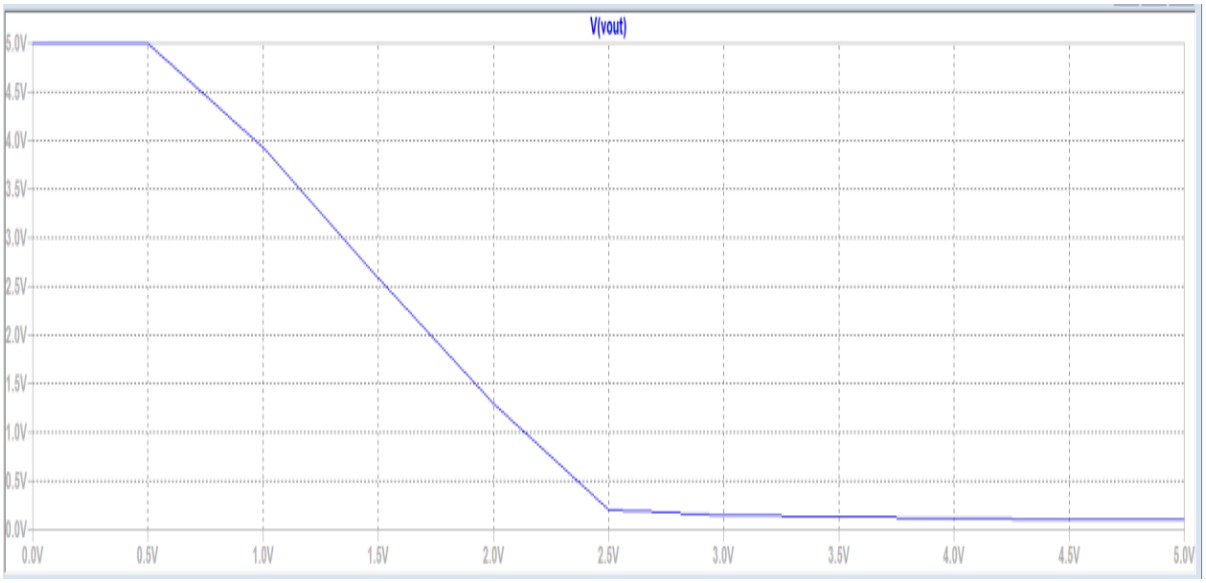
Theory:

A NOT gate simply inverts its input. If the input is HIGH, the output is LOW, and if the input is LOW, the output is HIGH. Such a circuit is easy to build, using a single transistor and a pair of resistors.

Circuit Diagram:



Graphs (Input/Output Characteristics):



Calculations:

From the graphs, we find that

- Voh(highest output gate can give)=5V,Vol=0.103V
- Vil(largest input voltage that is read as logic 0)=0.5V
- Vih(smallest input voltage that is read as logic 1)=2.5V
- DC Noise margins NM1=2.5V, NM0=0.397V

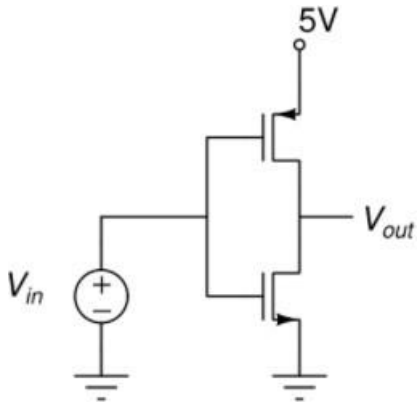
Discussion

DC Noise margins indicate the amount by which a signal exceeds the threshold for a proper '0' or '1';i.e in the given experiment the noise margin for '0' is the amount by which the signal is below 0.397V and the noise margin for '1' is the amount by which the signal is above 2.5V.

Part 2

Aim: Measuring the characteristics of a CMOS NOT gate.

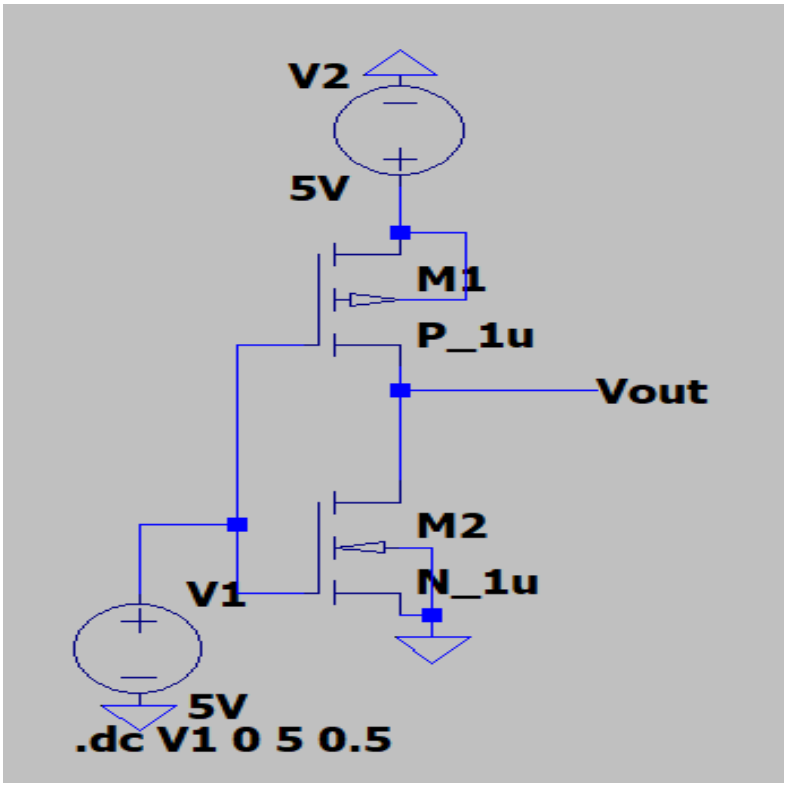
Circuit diagram:



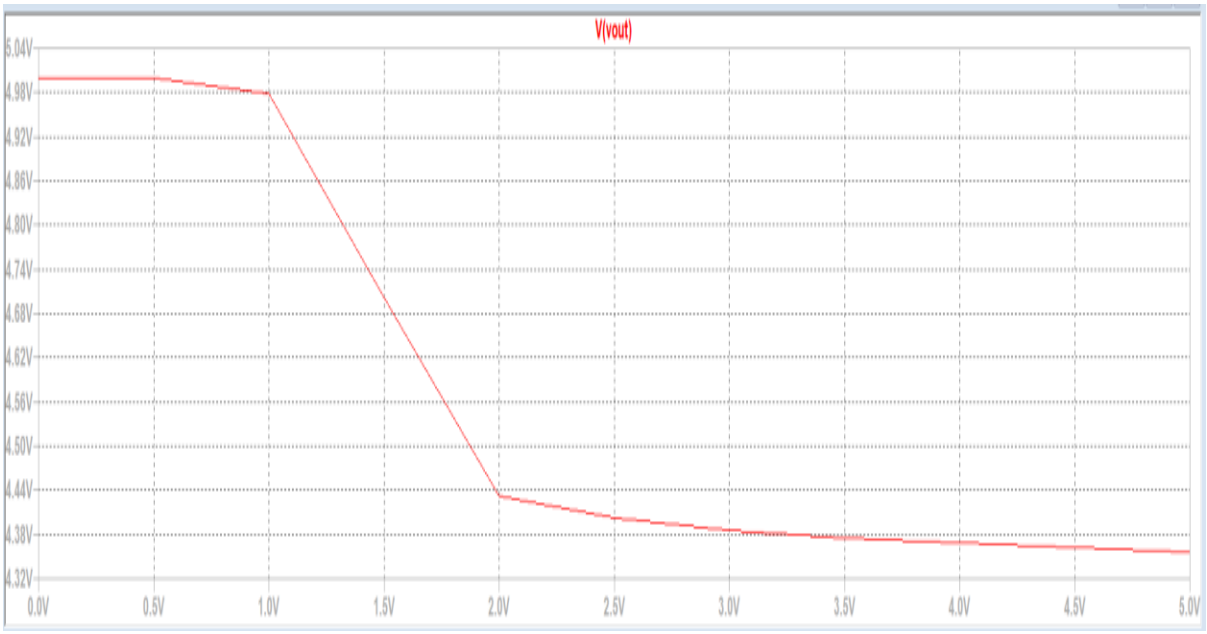
Theory:

The NOT gate is implemented by a pull-up circuit composed of only a pMOS transistor and its complementary pull-down circuit composed of only a nMOS transistor. If the input is HIGH, the output is LOW, and if the input is LOW, the output is HIGH.

Screenshot of Circuit:



Graphs(Input/Output characteristics):



Calculations:

From the graphs, We find that

- Voh(highest output gate can give)=5V,Vol=4.3560V
- Vil(largest input voltage that is read as logic 0)=1V
- Vih(smallest input voltage that is read as logic 1)=2V
- DC Noise margins NM1=3V, NM0=-3.3560V

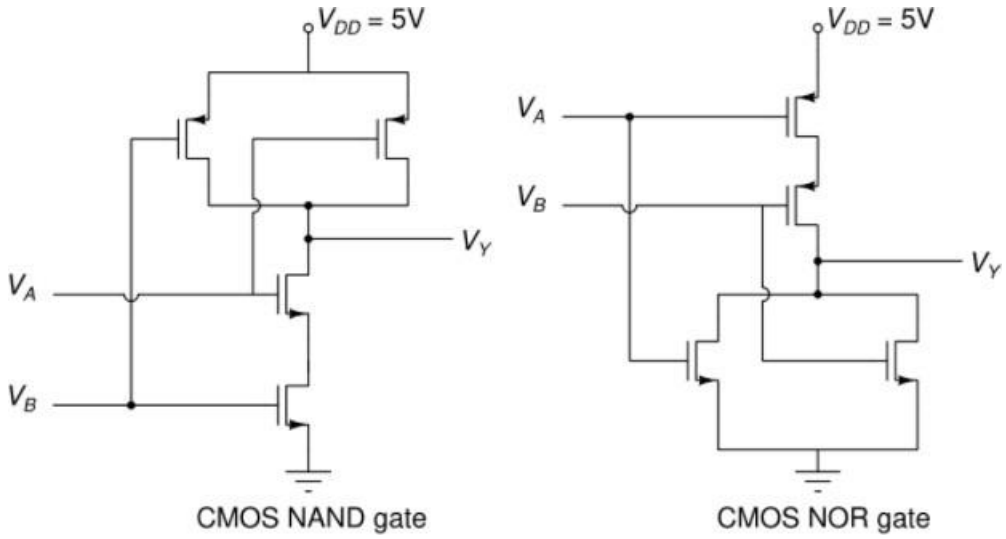
Discussion

DC Noise margins indicate the amount by which a signal exceeds the threshold for a proper '0' or '1';i.e in the given experiment the noise margin for '0' is the amount by which the signal is below -3.3560V and the noise margin for '1' is the amount by which the signal is above 3V.

Part 3

Aim: To wire up the following circuits for CMOS NAND and NOR gates and observe the characteristics.

Circuit diagram:



Theory:

For the design of any circuit with the CMOS technology; We need parallel or series connections of nMOS and pMOS with a nMOS source tied directly or indirectly to ground and a pMOS source tied directly or indirectly to V_{dd}.

The truth tables we desire are as follows:

Truth Table

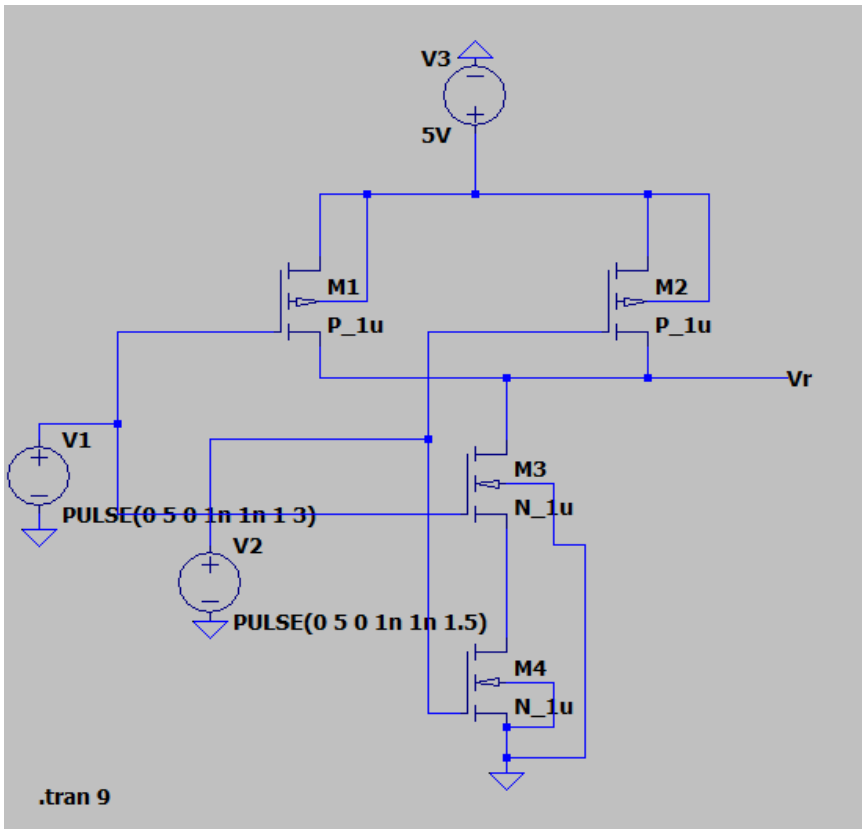
INPUT		OUTPUT
A	B	A NAND B
0	0	1
0	1	1
1	0	1
1	1	0

TRUTH TABLE

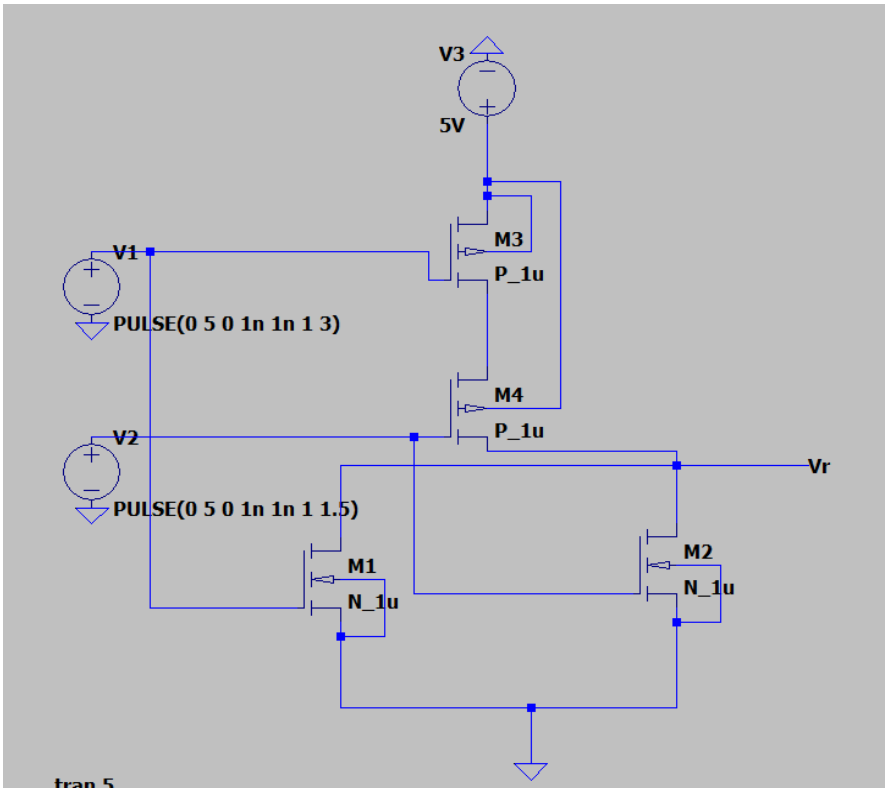
INPUT		OUTPUT
A	B	A NOR B
0	0	1
0	1	0
1	0	0
1	1	0

Screenshot of Circuit:

Nand Gate:

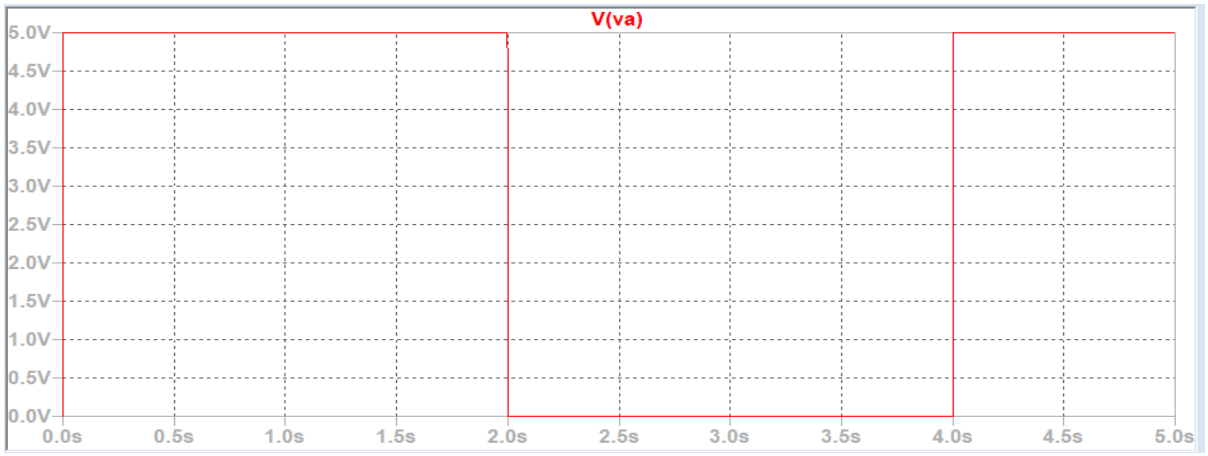


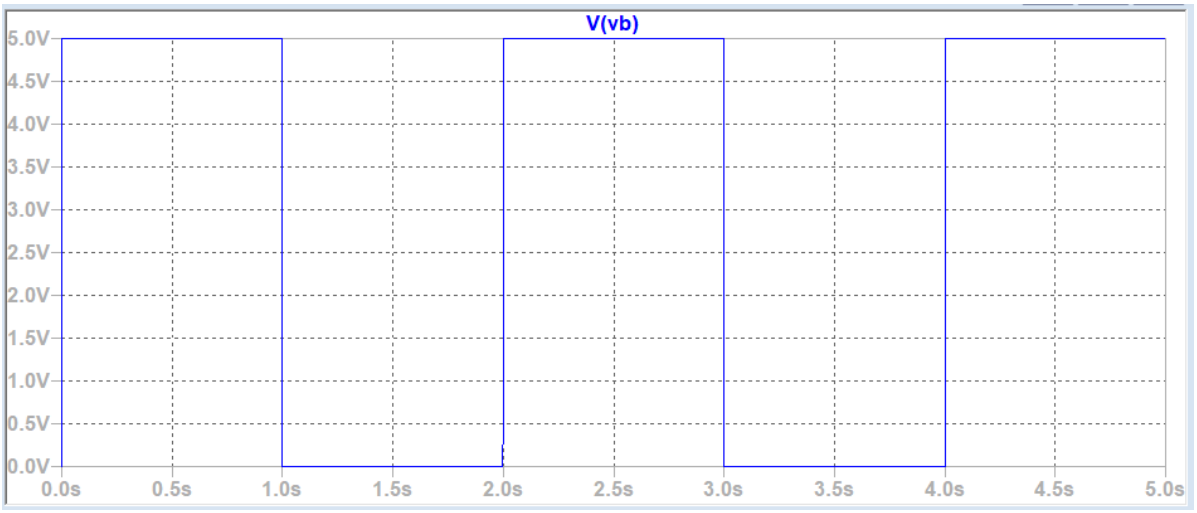
Nor Gate:

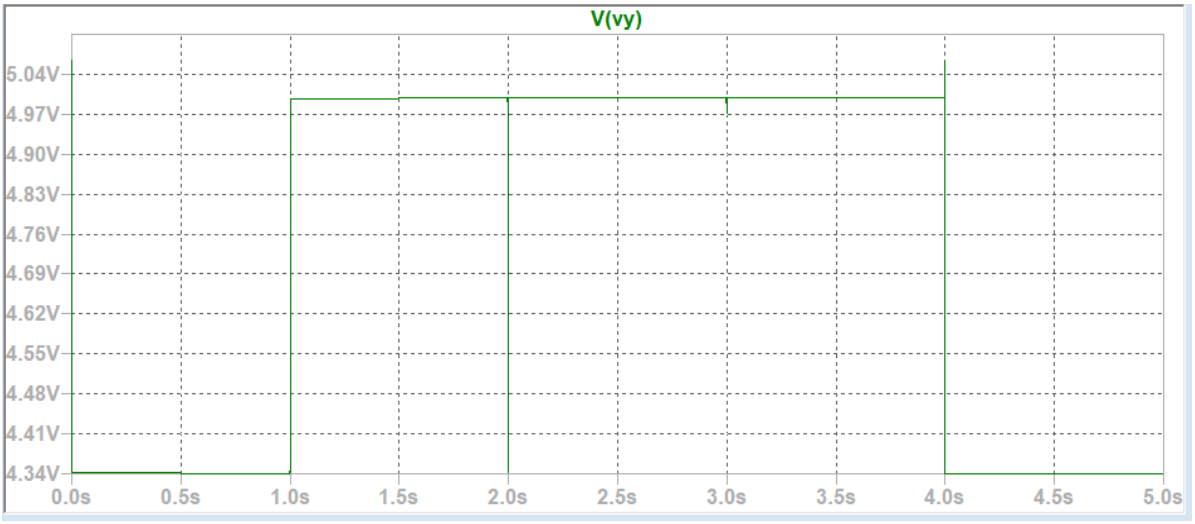


Graphs:

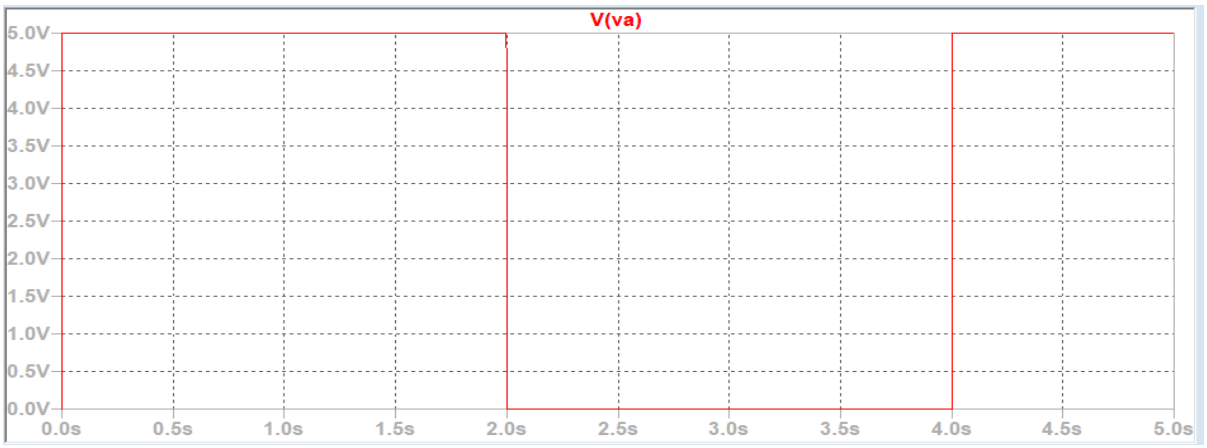
Nand Gate:

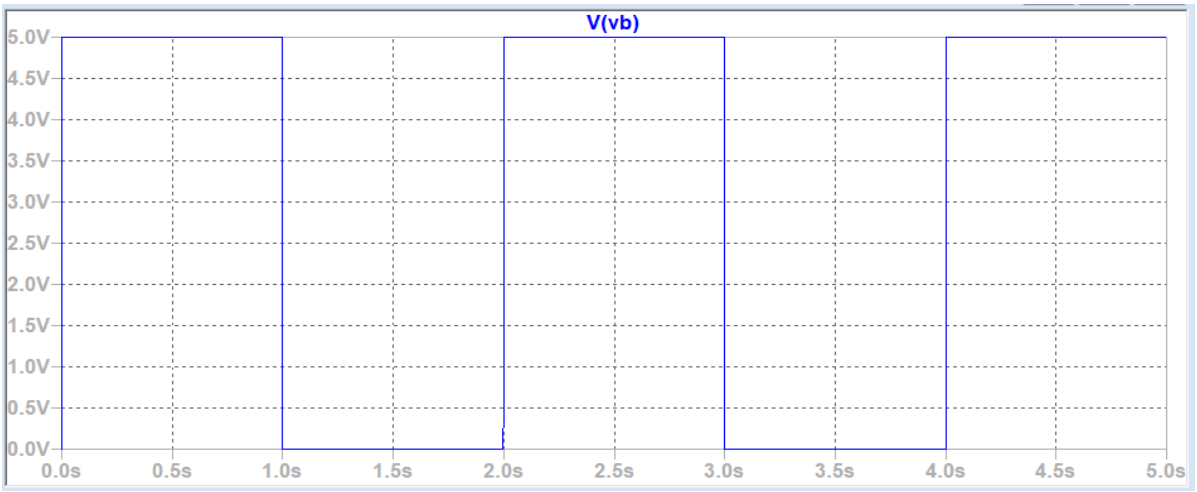


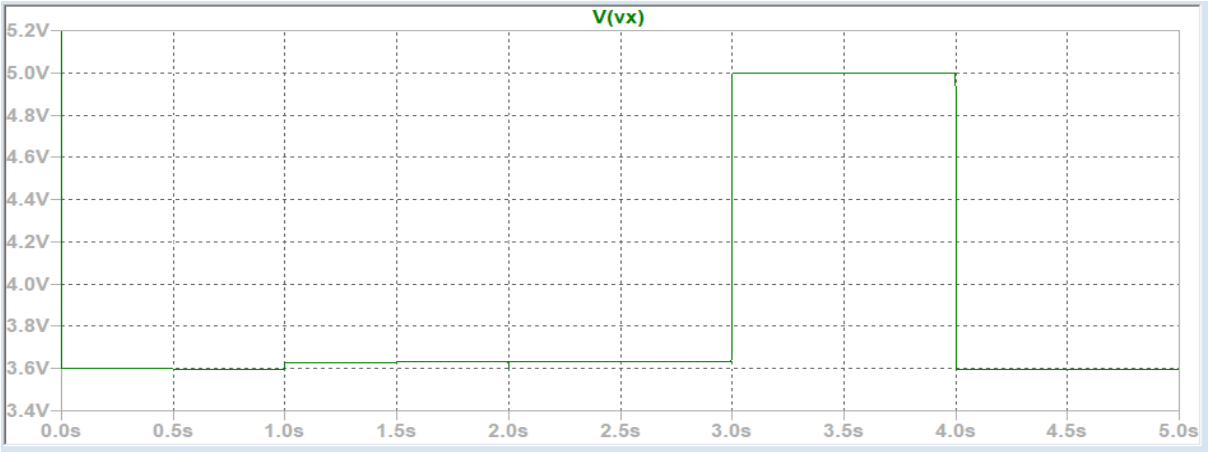




Nor Gate:


V(va)
5.0V
4.5V
4.0V
3.5V
3.0V
2.5V
2.0V
1.5V
1.0V
0.5V
0.0V
0.0s
0.5s
1.0s
1.5s
2.0s
2.5s
3.0s
3.5s
4.0s
4.5s
5.0s


V(vb)
5.0V
4.5V
4.0V
3.5V
3.0V
2.5V
2.0V
1.5V
1.0V
0.5V
0.0V
0.0s
0.5s
1.0s
1.5s
2.0s
2.5s
3.0s
3.5s
4.0s
4.5s
5.0s


V(vx)
5.2V
5.0V
4.8V
4.6V
4.4V
4.2V
4.0V
3.8V
3.6V
3.4V
0.0s
0.5s
1.0s
1.5s
2.0s
2.5s
3.0s
3.5s
4.0s
4.5s
5.0s

Discussion

In the first case of Nand Gate, considering a 5V signal to be ‘1’ and all other lower signals to be ‘0’,we find that when both Va and Vb are ON(5V or logic ‘1’),Vy is OFF(4.4 V or logic ‘0’);whereas in all other cases Vy is ON(5V or logic ‘1’);hence falling in confirmation with the desired TRUTH Table of NAND Gate.

In the second case of Nor Gate, considering a 5V signal to be ‘1’ and all other lower signals to be ‘0’, we find that when either Vc and Vd are ON (5V or logic ‘1’), Vx is OFF (3.7 V or logic ‘0’); whereas when both Vc and Vd are off, Vx is ON (5V or logic ‘1’); hence falling in confirmation with the desired TRUTH Table of NOR Gate.

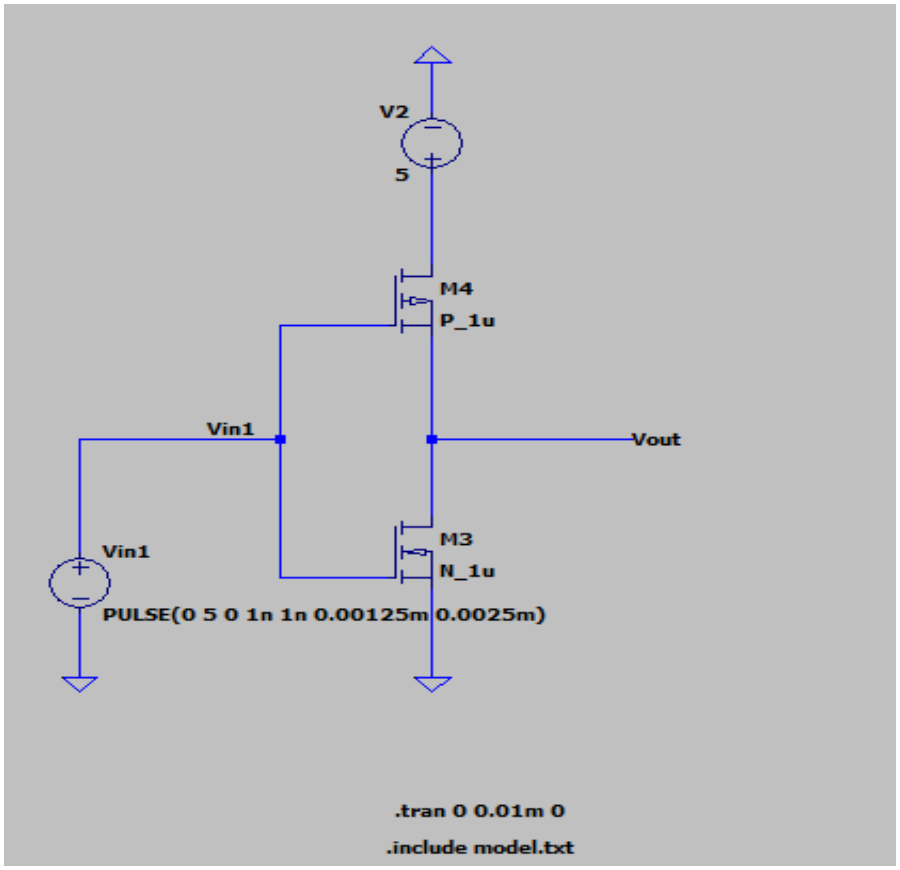
Part 4

Aim: Delay Measurement of a CMOS Not Gate.

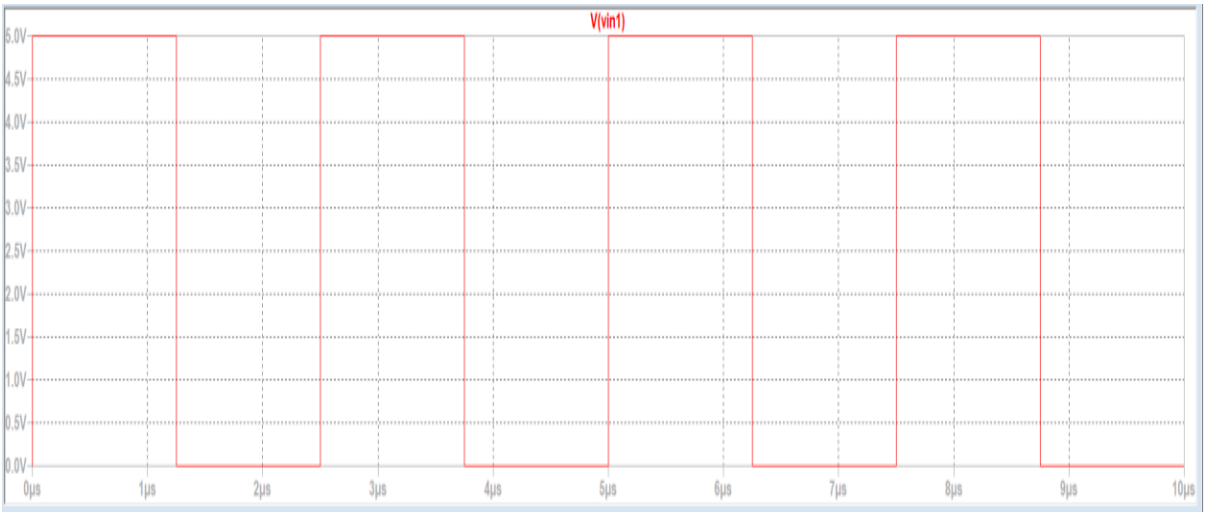
Theory:

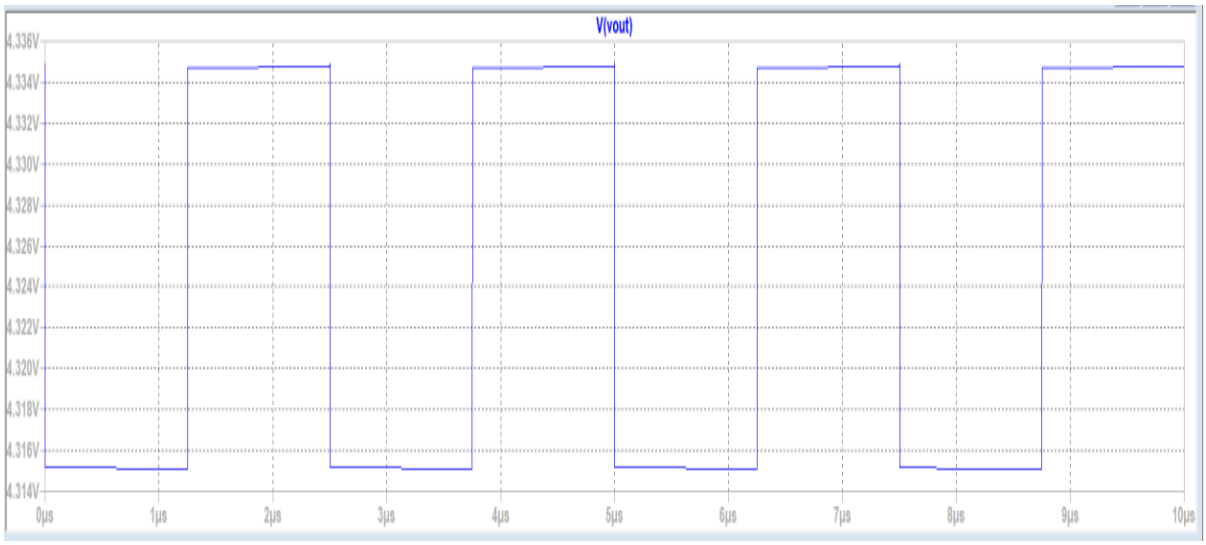
The NOT gate is implemented by a pull-up circuit composed of only a pMOS transistor and its complementary pull-down circuit composed of only a nMOS transistor. If the input is HIGH, the output is LOW, and if the input is LOW, the output is HIGH.

Screenshot of Circuit:



Graphs:





Discussion

Difference in time intervals between the ponts at which both Outputs and Inputs reach 50% of their maximum value (5.3455 V and 2.5V respectively) is approximately 1.25-0.02=1. 23µs.This 1.23 µs is the required Delay time.

Conclusion

Thus we formed all the desired logic gates using BJTs and CMOS devices, giving us the desired Truth tables thus giving different outputs under different conditions of input voltages.Such Logic gates form a crucial component of Digital Logic circuits and microprocessors along with playing a fundamental contribution in the study of binary systems.

Logic gates perform basic logical functions and are the fundamental building blocks of digital integrated circuits. Most logic gates take an input of two binary values, and output a single value of a 1 or 0. Some circuits may have only a few logic gates, while others, such as microprocessors, may have millions of them.

----------X----------