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Nano Electronics Project

A Report on

Design of PFD, CP, LPF for PLL at 83.33 MHz

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Abstract

A PLL consists of various significant components like Phase Frequency Detector, charge pump, filter, VCO, frequency divider. This report presents the design approach of a PFD, charge pump and an LPF for a PLL that operates at 833.33MHz for 10 Gbps connections over unshielded or shielded twisted pair cables, over a distance up to 100m. The PFD and Charge Pump are designed using CMOS logic. Circuit design is performed using SG25H3 kit from IHP.

ACKNOWLEDGEMENT

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1. Phase Locked Loop – Introduction

A Phase Locked Loop (PLL) is a feedback loop system which compares the phase and frequency of the output signal with the input signal. The oscillator generated frequency is constantly altered to match it with the input signal. They play a major role in stabilizing communication channel. Few of the essential components of a PLL include

- **Phase Frequency Detector (PFD)**
- **Charge Pump (CP)**
- **Low Pass Filter (LPF)**
- **Voltage Controlled Oscillator (VCO)**
- **Frequency Divider**

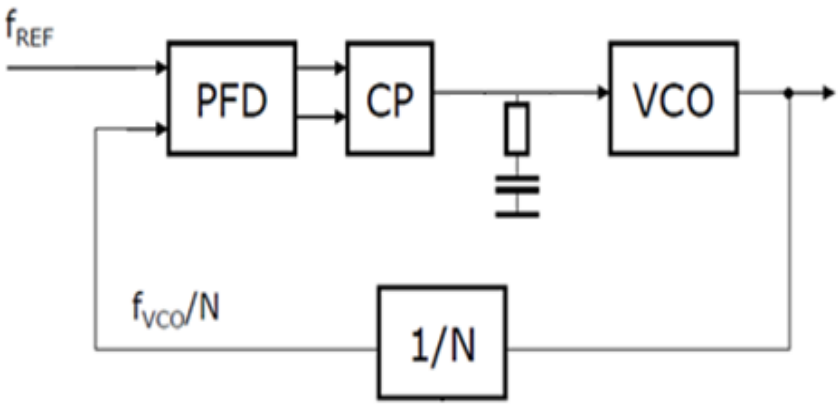

Figure 1: Block Diagram of PLL

2. Design Requirements and Specifications

2.1 Design Requirements

A PFD, CP and LPF is to be designed for a PLL which has a clock rate of 833.33MHz. The PLL is equipped with a static frequency divider with division ratio of 10, which implies that the input frequency for the PFD would be 83.33MHz. The charge pump should provide a current (I_{cpo}) of 35.93µA during switching. The first order LPF have their designated values of: R = 5KΩ, C = 55.6pF. Design of PFD and charge pump is done using RF MOSFET's from SG25H3 design kit from IHP. It is carried out in Cadence Virtuoso EDA tool.

2.2 Design Specifications

- Supply Voltage VDD = 2.5V
- Clock input is given as a voltage pulse varying between 0V and 2.5V with Time period of 12ns.
- The rise time and fall time of all the inputs are 600ps.
- The two clock inputs for both PFDs are separated by a delay of 5ns for test purposes.
- The transistor ‘rfpmos, ‘rfnmos’ for CMOS implementation of PFD and CP are used from SG25H3 kit.

3. Phase Frequency Detector Implementation

The phase difference between the input (reference) signal and the output (feedback) signal is measured using the phase frequency detector. It has two inputs which correspond to two different input signals, one of which is from an external reference source and the other from a Voltage Controlled Oscillator (VCO) as a feedback signal. The output of a PFD produces phase error as well as frequency error of the two input signals it receives and feeds it to the charge pump. The block diagram of a PFD looks as below:

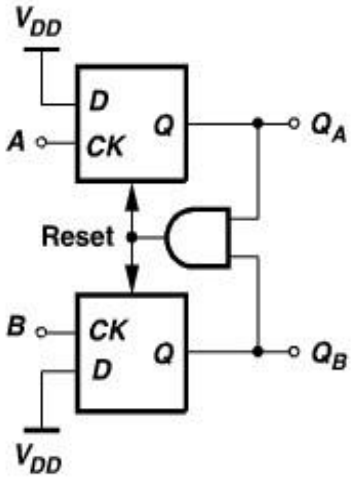

Figure 2: Block Diagram of PFD

It consists of two D- Flip-flops and to each of them, the reference signal and the feedback signal are given as inputs. The outputs of the flip-flops are given to a Charge pump in the next stage. To meet the input requirements of charge pump, only one of the outputs Q_A or Q_B can be at high state at a given time. As a result, the outputs are fed to an AND gate. The output of AND gate will act as a reset signal and will reset the D Flip-flops when high. The PFD- design requires a D flip-flop with reset.

3.1 D Flip-Flop

The basic D Flip-Flop which can be used for the construction of PFD is designed using interconnection if D latches made from NOR gates. This D Flip-Flop gives the desired output but there are huge number of transistors in this architecture. This increases the area consumed and as the number of transistors increases operating speed reduces. Each NOR gate consists of 4 MOSFET's and 1 D Flip-Flop has 16 MOSFET's. This is a huge number. Figure 3 shows the circuit diagram of D Flip-Flop using NOR gates.

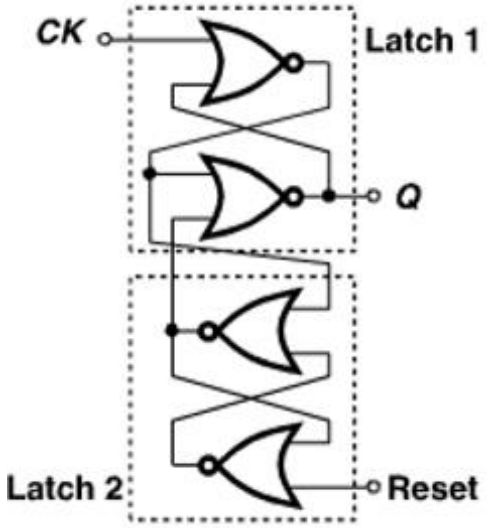

Figure 3: Circuit Diagram for D Flip Flop

So, to reduce the number of transistors used and to improve the response of circuit the best architecture suited is TSPC architecture. TSPC architecture is well known for its high-speed performance and low area consumption. Many of the available TSPC architectures are designed in such a way that few of the transistors in the design must have huge area to dominate other transistors to function efficiently. For example, to make the RESET signal over power the CLK signal else the reset functionality will not work in the PDF as desired. But the TSPC architecture used in this design has no such requirements of increasing the width or length which is an advantage when designed for low area consumption.

This D Flip-Flop has only 9 transistors in total which is very less when compared to previous architecture. One of the D Flip-Flops generates UP signal when reference signal leads feedback signal and the other D Flip-Flip controls Down signal when the reference signal lags the feedback signal. The D Flip-Flop has CLK and RESET as inputs and Q as the output. Circuit diagram for a D Flip Flop is shown in figure 4.

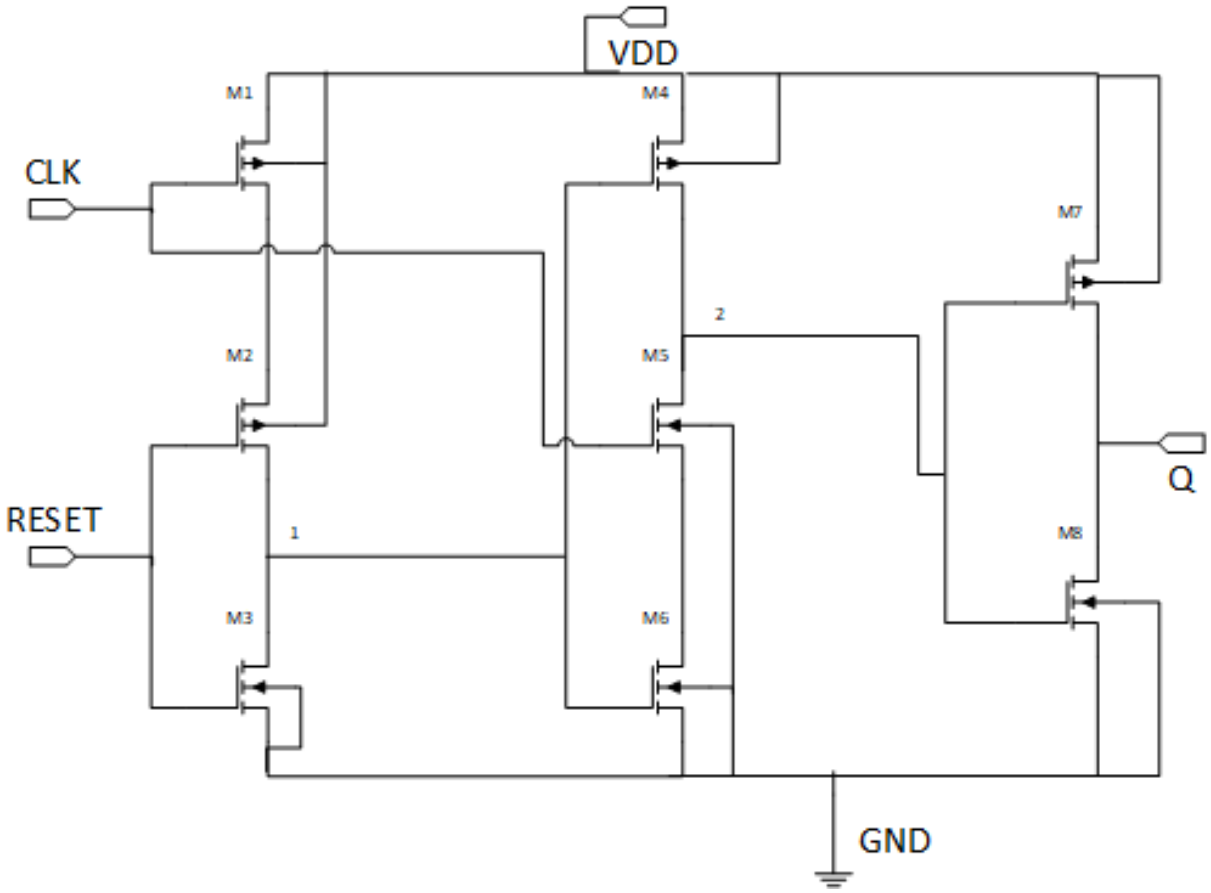

Figure 4: Circuit Diagram for D Flip Flop with Reset

The following explanation assumes that LOW relates to a digital 0 and HIGH relates to a digital. Let's divide the circuit in to three stages. Stage 1 consists of M1, M2 and M3. Stage 2 consists of M4, M5 and M6. Stage 3 consists of M7 and M8. When CLK and RESET are HIGH node 1 is connected to GND through M3. Node 2 is pulled to VDD as M4 switches ON. As stage 3 is an inverting stage Q is 0. When CLK goes LOW the node 1 is still connected to GND and node 2 is still charged to VDD. Hence, output Q is 0. Now when the RESET goes LOW node 1 and node 2 are pulled to VDD leading output Q to 0. When CLK starts charging up node 1 is charged to VDD and node 2 is pulled down to GND. Hence output Q is 1. So, when RESET is HIGH the output Q is low irrespective of the changes in CLK signal. When RESET is LOW the output Q follows CLK signal.

Hence, this circuit performs the function of a D latch along with Reset, if required. The same circuit is implemented in Cadence tool using the kit provided. This is depicted in figure 4. The output of the D Flip-Flop is given to AND gate. The output from the AND gate is fed back to the D Flip-Flop's as RESET input signal. The simulation of the above circuit yields a result as shown below in figure 5.

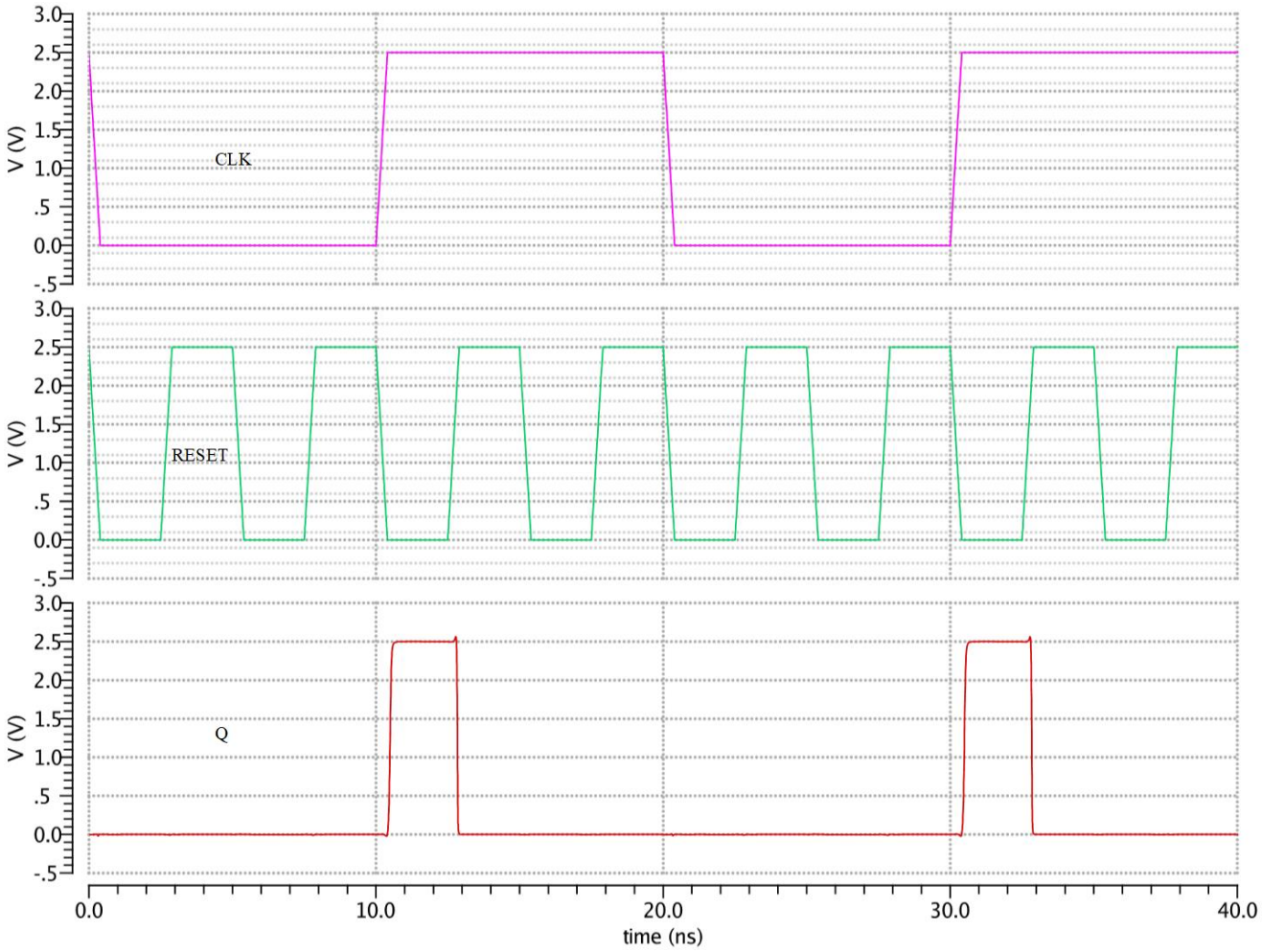

Figure 5: Simulation Results of DFF with Reset

We observe that, on every rising edge of clock, output follows the CLK input at that instant until the next rising edge of the clock (Positive Edge Triggered Flip-Flop). Also, when the RESET input to the Flip-Flop goes HIGH, the output stays LOW irrespective of the CLK inputs.

3.2 AND GATE

An AND gate is a universal gate, that has 2 inputs and 1 output. It is represented as shown in figure 6**.** The logic table relating the inputs A and B to the output Q is in table 1**.**

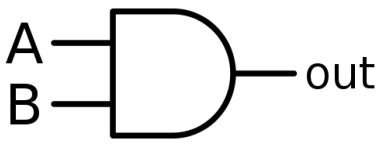

Figure 6: AND Gate

A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

Table 1: Truth Table for AND Gate

Implementation of AND Gate using NAND and Inverter is shown in Figure 7.

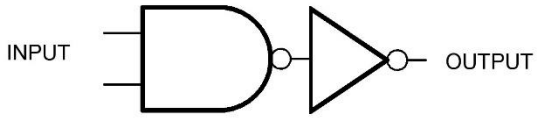

Figure 7: Symbol of AND gate using NAND gate and an Inverter.

The AND gate takes the outputs of both the D Flip-Flops and generates an output which is used to reset both the D Flip-Flops.

4. Charge Pump and Low Pass Filter

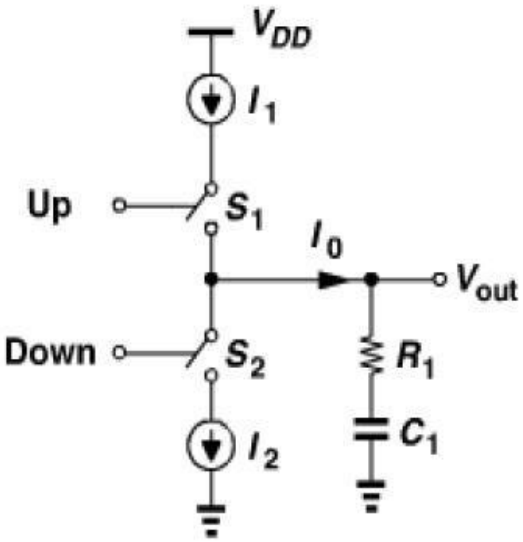

Figure 8: Charge Pump and LPF

A charge pump either sources or sinks current for a specific period which is decided by switching of the charge pump. The switching depends on signals 'Up' and 'Down' as in Figure 8. The current is sourced to LPF and capacitor charges when 'Up' is ON, giving a rise in V_{out}. The capacitor discharges when 'Down' is ON, thereby reducing the voltage V_{out}. CMOS implementation of the same is depicted in figure 9.

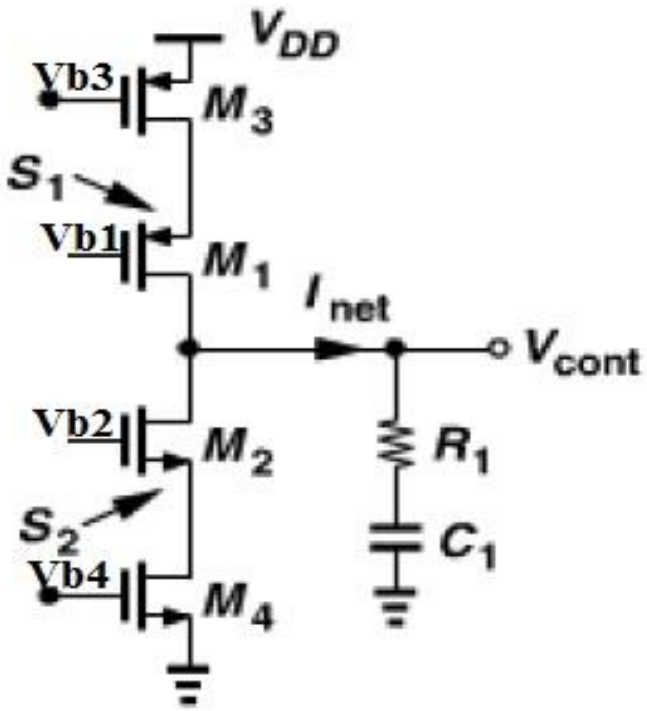

Figure 9: CMOS switch implementation for Charge Pump

In the design approach for the charge pump, we know that voltage Vb1 and Vb2 swing between 0 and 2.5V. The W/L scaling of each transistor is done to ensure that the required current of 35.93µA (I_{cpo}) is allowed through each of the transistor in their operation of saturation region. The biasing voltages are met by preceding it with current mirrors as shown in Figure 10, which includes the 1st order Low Pass Filter with R = 5KΩ, C = 55.6pF.

The simulation of the circuit when connected to PFD is shown in Figure 15 and 16. As seen in figures, the capacitor charges and increase the output voltage if the Up switch is ON. When Down switch turns ON, the Reset Pin on the PFD in the previous stages turns OFF and pulls down both the switches to OFF. Ideally, the output voltage should stay constant when both the switches are in OFF state as shown in Figure 13. Whereas, a steady reduction in output voltage is observed in this case.

The capacitor starts charging when the QA (UP) signal turns ON until QB (DOWN) signal turns ON and maintains this state until the next pulse of QA signal. In the next cycle when QA is ON the capacitor starts charging from the previous steady state and this process continues till it reaches VDD. The capacitor starts discharging when the QB signal turns ON until QA signal turns ON and maintains this state until the next pulse of QB signal. In the next cycle when QB is ON the capacitor starts discharging from the previous steady state and this process continues till it reaches GND.

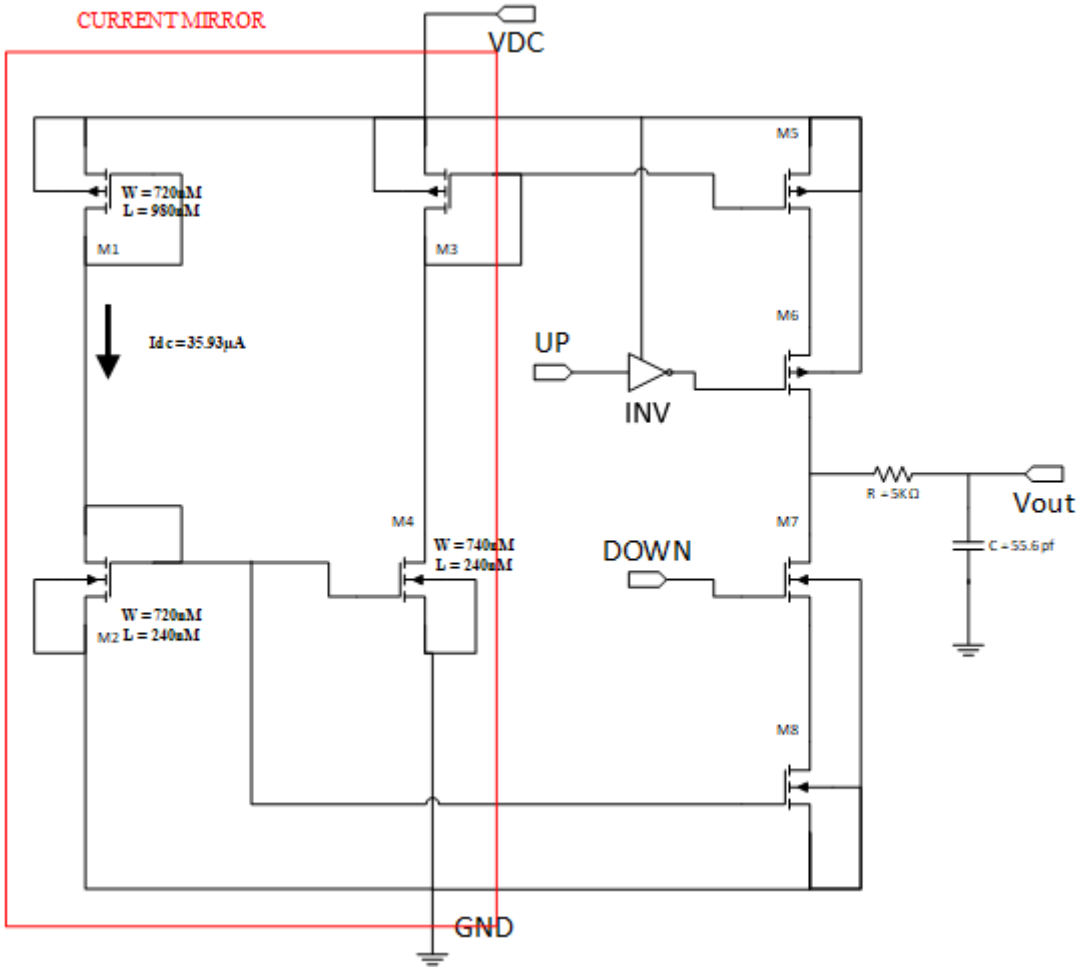

Figure 10: Charge Pump and LPF Implementation

To properly design the charge pump it is essential to match the current in all the three parallel paths. For this it is essential to calculate the width and length of M1, M2, M4 MOSFET's. A model of current mirror is given in figure 11. First, we keep the I_{cpo} as it is and calculate the W/L ratios of M2 and M4 transistors using current mirror formula.

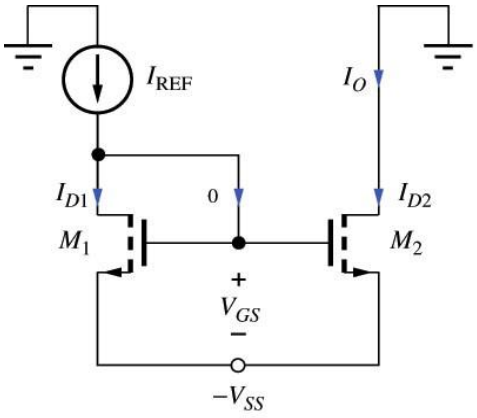

Figure 11: Model for current mirror

$$I_o = I_{REF}\frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1} \tag{1}$$

$$\left(\frac{W}{L}\right)_2 = \frac{I_o}{I_{REF}}\left(\frac{W}{L}\right)_1 \tag{2}$$

From the schematic simulation the value of I_o is calculated as 37µA. $(W/L)_1$ = 720nM/240nM and I_{REF} = 35.93µA. Substituting these values in equation 2 we get

$$\left(\frac{W}{L}\right)_2 = \frac{740nM}{240nM}$$

As a MOSFET can be configured act as a resistor we can replace a current source with a MOSFET of specific parameters. A model of this example is represented in figure 12. These parameters can be calculated using the following formula.

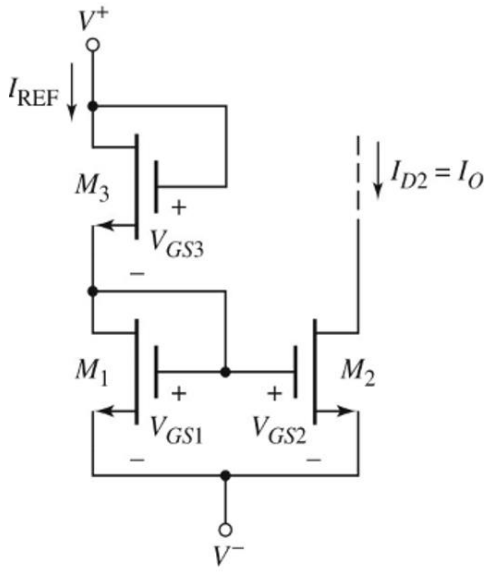

Figure 12: Model for replacing current source by a MOSFET

$$V_{GS1} = \sqrt{\frac{\left(\frac{W}{L}\right)_3}{\left(\frac{W}{L}\right)_1}}.V_{GS3} + \left(1 - \sqrt{\frac{\left(\frac{W}{L}\right)_3}{\left(\frac{W}{L}\right)_1}}\right).V_{TN} \tag{3}$$

Where $$V_{GS1} + V_{GS3} = V^+ - V^- \tag{4}$$

We have $V^+ = 2.5V$ and $V^- = 0V$ and $V_{GS1} = 1V$. So, we get $V_{GS3} = 1.5V$.

Solving for $(W/L)_3$ with $V_{TN} = 0.5V$, from equations 3 and 4 we get

$$\left(\frac{W}{L}\right)_3 = \frac{720nM}{980nM}$$

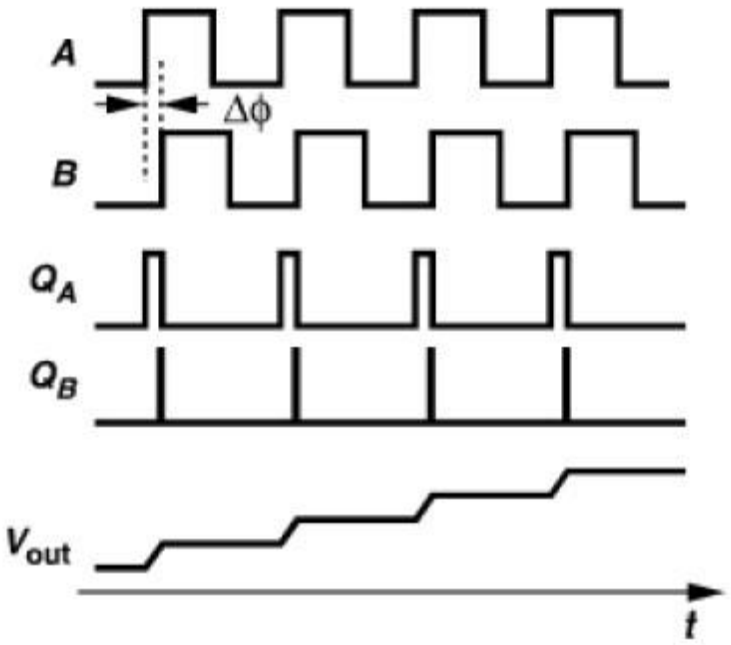

Figure 13: Ideal Response of LPF for UP state

The overall implementation of PFD, CP and LPF is as shown in figure 14 and its simulation results are shown in figure 15 and 16.

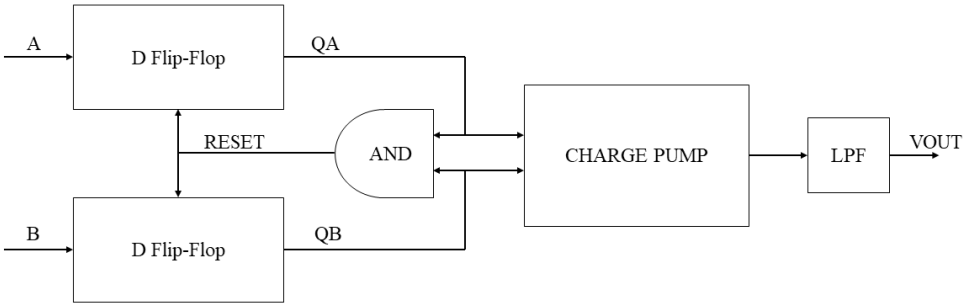

Figure 14: Implementation of PFD, CP and LPF

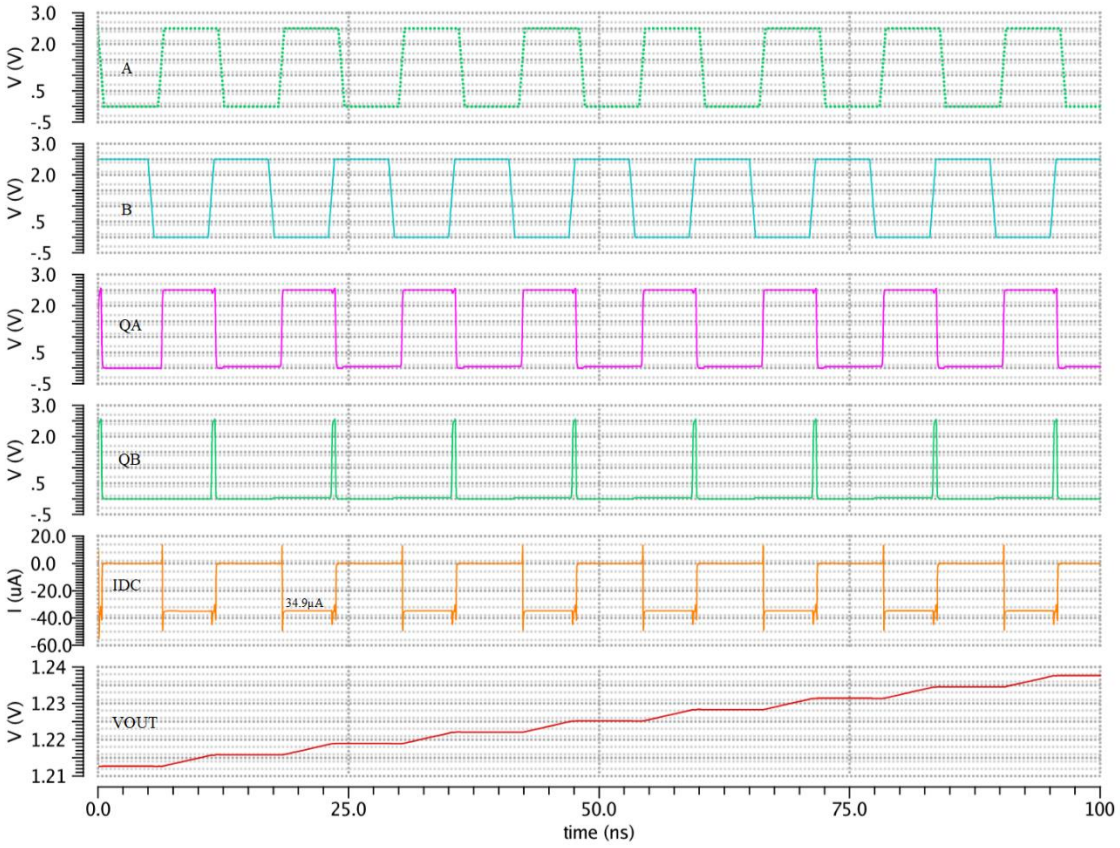

Figure 15: Simulation results for PFD, CP and LPF for UP state.

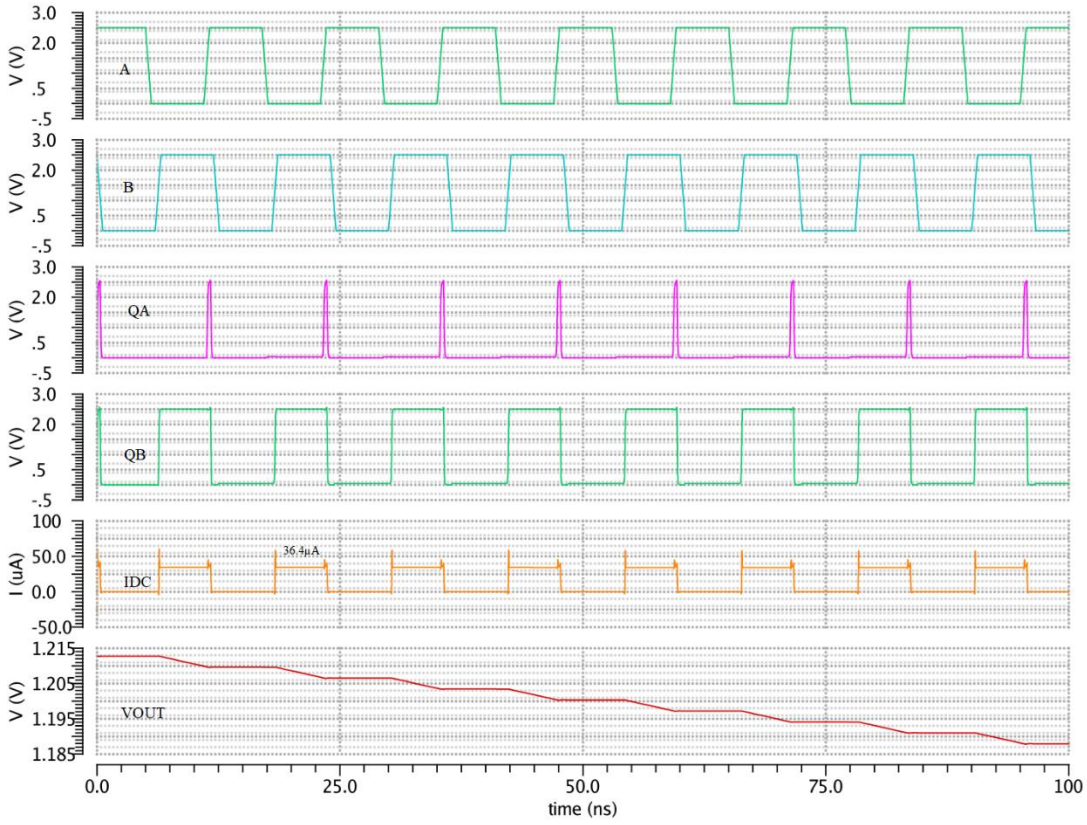

Figure 16: Simulation results for PFD, CP and LPF for DOWN state.

5. Layout Design

Layout is an essential part of circuit design. Layout for this task is carried out by 0.25µm technology and Cadence Virtuoso Layout editor.

As a part of layout design, few checks are performed to confirm proper placements of circuit components and to check if all proper connections are made. Design Rule Check (DRC) is performed to check for any design violations such as minimum spacing between 2 components, off grid errors, minimum metal width and area. Layout vs Schematic (LVS) check is performed to check for any faulty connections in the layout by comparing with schematic. QRC extraction is done to check for parasitic R and C for the overall circuit designed.

The circuit design uses Metal Layer 1 (M1), Metal Layer 2 (M2), Metal Layer 3 (M3), Top Metal layers 1 and 2 – TM1, TM2 are used. Voltage supply VDD runs on TM2 throughout the circuit. Ground connections run on TM1. Internal connections are made using M1, M2 and avoiding M3 until there is no other choice.

The overall layout design for the circuit PFD, CP and LPF is shown in figure 17. The capacitor 55.6pF in LPF is not included in the layout due to area concerns. This capacitor can be connected externally when used.

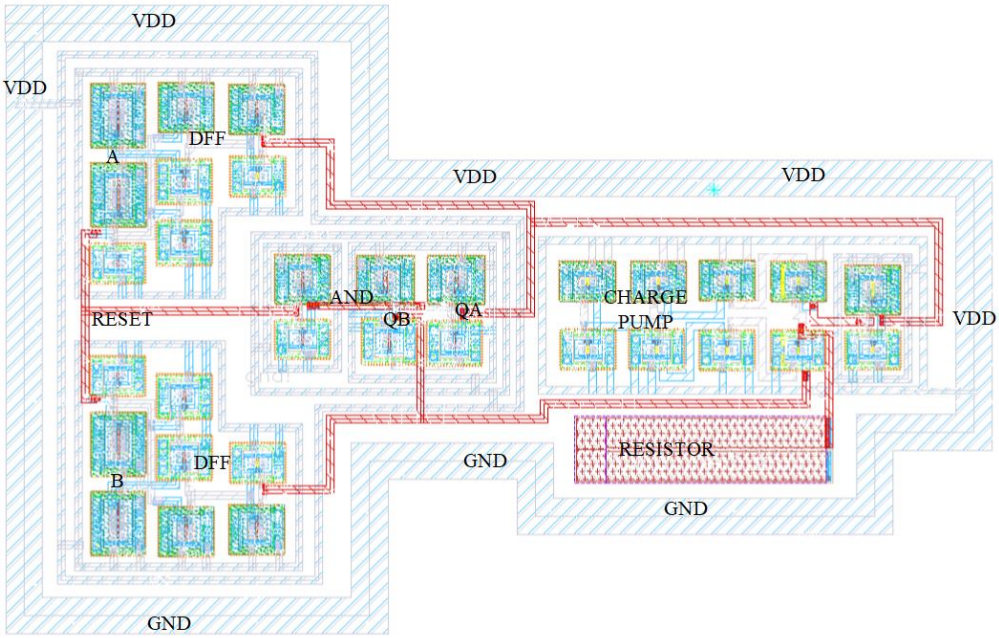

Figure 17: Layout for PFD, CP and LPF

6. Summary

The circuit for PFD, CP and LPF has been designed for a PLL that operates at 833.33Hz has been designed. RF MOSFETS are used in the design of PFD and charge pump which is then followed by a LPF. During the circuit design the challenges faced were, to choose an high speed and low area consuming D Flip-Flop and to properly configure the Charge Pump for current mirror which was calculated theoretically and also on schematic design. Challenges were also faced to configure the transistors connected to the input signals of Charge Pump as they must be in saturation region to operate as desired. These MOSFET's were configured by performing parametric analysis in cadence tool. A first order LPF is observed to meet the PLL requirements only to an extent. The layout for the same has been designed and checked.

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