8087 Numeric Data Processor

8087 numeric data processor is also known as **Math co-processor**, **Numeric processor extension** and **Floating point unit**. It was the first math coprocessor designed by Intel to pair with 8086/8088 resulting in easier and faster calculation.

Once the instructions are identified by the 8086/8088 processor, then it is allotted to the 8087 co-processor for further execution.

The most prominent features of 8087 numeric data processor are as follows −

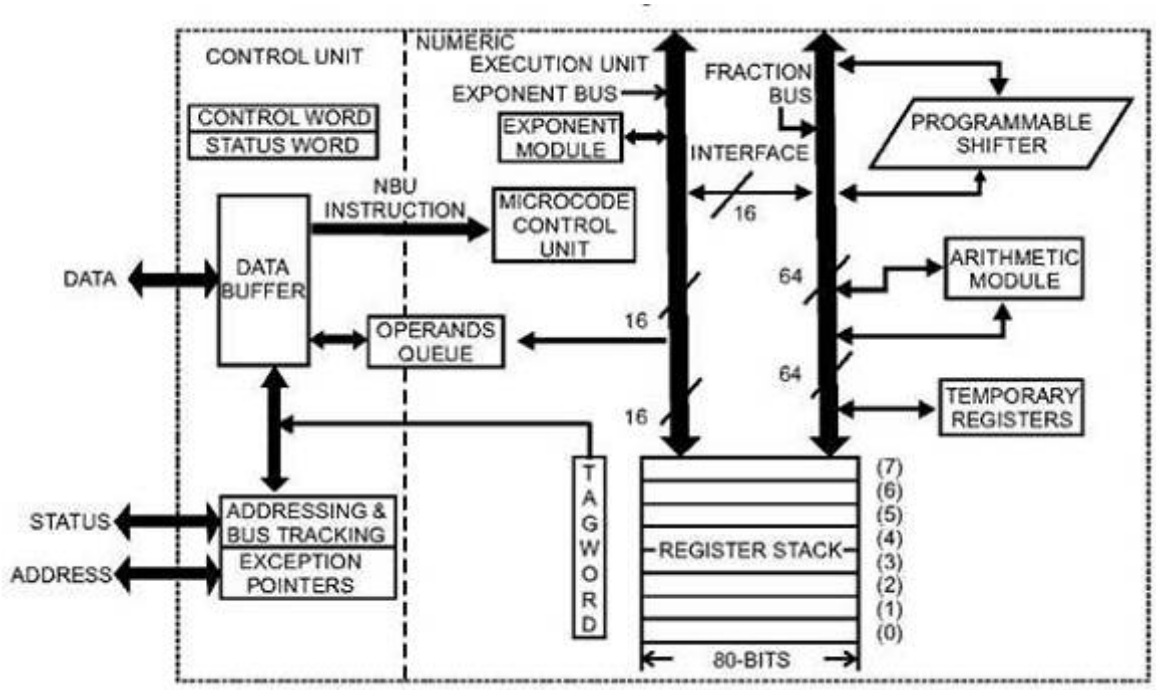
- It supports data of type integer, float, and real types ranging from 2-10 bytes.
- The processing speed is so high that it can calculate multiplication of two 64-bits real numbers in ~27 μs and can also calculate square-root in ~35 μs.
- It follows IEEE floating point standards.

8087 Architecture

8087 Architecture is divided into two groups, i.e., **Control Unit** (CU) and **Numeric Extension Unit** (NEU).

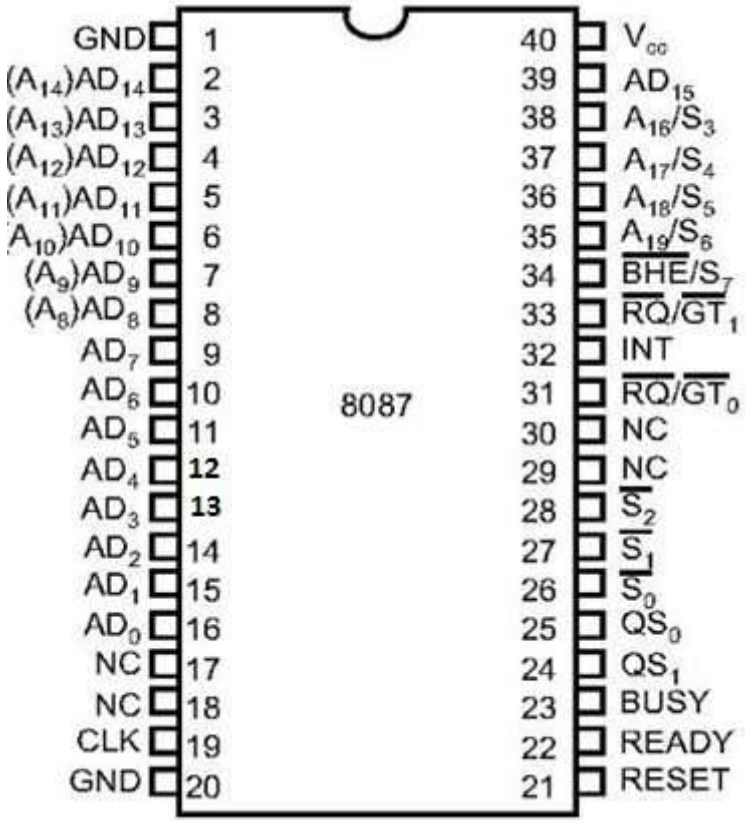
- The **control unit** handles all the communication between the processor and the memory such as it receives and decodes instructions, reads and writes memory operands, maintains parallel queue, etc. All the coprocessor instructions are ESC instructions, i.e., they start with 'F', the coprocessor only executes the ESC instructions while other instructions are executed by the microprocessor.
- The **numeric extension unit** handles all the numeric processor instructions like arithmetic, logical, transcendental, and data transfer instructions. It has 8 register stack, which holds the operands for instructions and their results.

The architecture of 8087 coprocessor is as follows −



8087 Pin Description

Let us first take a look at the pin diagram of 8087 −



The following list provides the Pin Description of 8087 −

- **$AD_0 – AD_{15}$ −** These are the time multiplexed address/data lines, which carry addresses during the first clock cycle and data from the second clock cycle onwards.
- **A_{19} / $S_6 – A_{16}$/S −** These lines are the time multiplexed address/status lines. It functions in a similar way to the corresponding pins of 8086. The S_6, S_4 and S3 are permanently high, while the S_5 is permanently low.
- **$\overline{BHE}$/S_7 −** During the first clock cycle, the $\overline{BHE}$/S_7 is used to enable data on to the higher byte of the 8086 data bus and after that works as status line S_7.
- **QS_1, QS_0 −** These are queue status input signals which provides the status of instruction queue, their conditions as shown in the following table −

QS_0	QS_1	Status
0	0	No operation
0	1	First byte of opcode from the queue
1	0	Empty the queue
1	1	Subsequent byte from the queue

- **INT −** It is an interrupt signal, which changes to high when an unmasked exception has been received during the execution.
- **BUSY −** It is an output signal, when it is high it indicates a busy state to the CPU.
- **READY −** It is an input signal used to inform the coprocessor whether the bus is ready to receive data or not.
- **RESET −** It is an input signal used to reject the internal activities of the coprocessor and prepare it for further execution whenever required by the CPU.
- **CLK −** The CLK input provides the basic timings for the processor operation.
- **VCC −** It is a power supply signal, which requires +5V supply for the operation of the circuit.
- **S_0, S_1, S_2 −** These are the status signals that provide the status of the operation which is used by the Bus Controller 8087 to generate memory and I/O control signals. These signals are active during the fourth clock cycle.

S_2	S_1	S_0	Queue Status
0	X	X	Unused
1	0	0	Unused
1	0	1	Memory read
1	1	0	Memory write
1	1	1	Passive

- **RQ/GT_1 & RQ/GT_0 −** These are the **Request/Grant** signals used by the 8087 processors to gain control of the bus from the host processor 8086/8088 for operand transfers.