

Lecture-1

8086/Microprocessor

8088

Chapter-1 of (Charles Manur 2nd)

Computer Organization and Assembly Language

No book 199, 097 part of study schedule + L (1)

Microcomputer Systems:

i) I/O devices are called peripherals.

Input devices - keyboard, mouse

Output devices - monitor

I/O device is microcomputer in relation to interfacing etc.

ii) Integrated Circuits, also known as chips. digital circuits
discrete voltage is either high or low.

IC circuits are known as digital circuits because it operates on discrete voltage signal levels typically a high voltage and a low voltage represented by 0's and 1's

iii) These symbols are called binary digits or bits.

iv) All information processed by the computer is represented by strings of 0's and 1's that is bit string.

Motherboard:

- I) The Motherboard is a printed circuit board that is the foundation of a computer, located at the bottom of the computer case.
- II) It allocates power to the CPU, RAM, and all other computer hardware components.
- III) Most importantly, the mother board allows hardware components to communicate one with one another.

Bytes and Words:

- I) Information processed by the computer is stored in its memory.
- II) The memory circuits are usually organized into groups that can store eight bits of data.
- III) A string of eight bits is called a byte.
A string of sixteen bits is called a word.
- IV) Each memory byte is identified by a number that is called address.

Address we use memory location to access data.

V) The data stored in a memory bytes are called its content.

VI) The address of a memory byte is fixed and is different from the address of any other memory byte in the computer.

VII) The contents of a memory byte are not unique and are subject to change, because they denote the data currently being stored.

Bit position:

- I) The positions are numbered from right to left, starting with 0.
- II) In a word, the bits 0 to 7 form the low byte and the bits 8 to 15 form the high byte.
- III) For a word stored in memory, its low byte comes from the memory byte with the lower address and its high byte is from from the memory byte with the higher address.

Buses

- i) A processor communicates with memory and I/O devices by using signals that travel along a set of wires or connections called buses.
- ii) There are three kinds of signals: address, data and control.
- iii) And there are three buses: address bus, data bus and control bus.
- iv) To read the contents of a memory location, the CPU places the address of the memory location on the address bus, and it receives the data, sent by memory circuits, on the data bus.
- v) A control signal is required to inform the memory to perform a read operation.
- vi) The CPU sends the control signal on the control bus.

Lecture-2

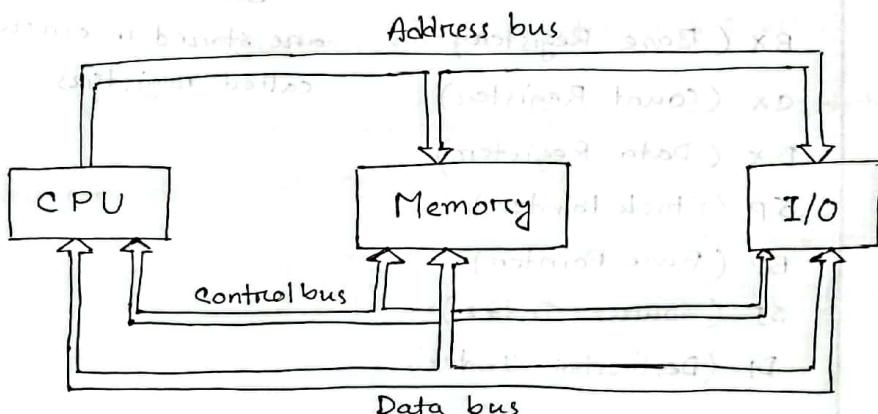
Address bus - CPU location (where data read or write)

→ location by CPU address CPU → Bus → CPU

Data bus - target specific location → (for data read or write)

→ (data bus by target device)

Control bus - target specific control bus. It controls signal to target, read operation or read signal. CPU signal control bus → through CPU send target.



#. Intel 8086 Microprocessor Organization

Two units:- i. Execution Unit : Executes any instruction

ii. Bus Interface Unit : Deals with the buses

Execution unit takes instruction execute तो रोड़े,
bus unit next कोडा instruction execute रोड़े रोड़े,
रोड़े info store तो रोड़े.

* General Purpose Registers : 8 registers

AX (Accumulator Register) data for the operations

BX (Base Register) one stored in circuits

CX (Count Register) called registers.

DX (Data Register)

SP (Stack Pointer)

BP (Base Pointer)

SI (Source Index)

DI (Destination Index)

* Internal Bus :

Execution unit and Bus Interface unit connect तो रोड़े,

* Temporary register: operand hold तो रोड़े,

* ALU: Arithmetic and Logic Unit

* Flag register: operation result reflect तो रोड़े,

* Registers

CS (Code Segment)

DS (Data Segment)

SS (Stack Segment)

ES (Extra Segment)

IP (Instruction Pointer)

* Bus Control logic

* Instruction queue : 6 byte तो रोड़े

next कोडा instruction execute रोड़े तो रोड़े bus interface
unit & instruction queue तो रोड़े रोड़े

BIU is responsible for transmitting addresses, data
and control signals on the buses.

The instruction pointer (IP) contains the address of
the next instruction to be executed by the FU.

Instruction prefetch:

While the EU is executing an instruction, the BIU fetches up to six bytes of the next instruction and places them in the instruction queue.

* Machine Instruction:

Opcode - The opcode specifies the type of operation

Operand - The operands are often given as memory addresses to the data to be operated on.

Fetch-Execute Cycle:

* Fetch -

- fetch an instruction from memory
- Decode the instruction to determine the operation.
- fetch data from memory if necessary

* Execute -

- Perform the operation on the data.
- Store the result in memory if needed.

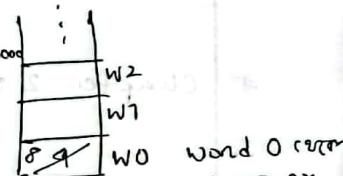
$$\begin{array}{c} C = a + b \\ \downarrow \quad \downarrow \quad \downarrow \\ AX = BX + CX \end{array}$$

Programming Language

* Machine language:

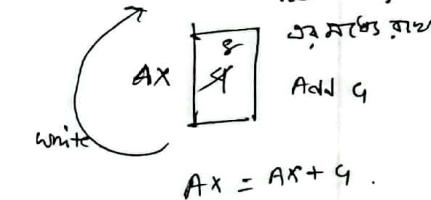
- CPU can only execute machine language instructions
- They are bit strings.

- Instruction - 101000010000000000000000
Fetch the contents of memory word 0 and put it in register AX.



- Add 4 to AX.

- AX in memory word 0.



$$w0 = AX$$

Assembly Language :

Assembly instruction -

MOV AX,A ; fetch the contents of location A and put it in register AX.

Add AX,4 ; Add 4 to AX .

MOV A\$,AX ; move the contents of Ax into location A .

Chapter-2 → Self Study

Lecture-3

Chapter-3

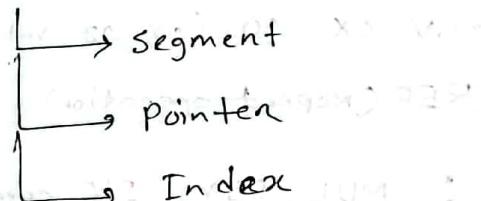
Registers →

Data Registers → instruction execute \rightarrow data \rightarrow store
 \rightarrow not store

Address Registers → data address store

Status Registers → operation \rightarrow data status /
information store

Address Register .



Status Register

FLAG Register

Data Register:

AX (Accumulator Register): Arithmetic operation, Logical operation (MUL, DIV, ADD, SUB, AND, OR) Input Output

BX (Base Register): XLAT → table look up
DX table in memory

CX (Counter Register): instruction > loop use

MOV CX 10 (CX \leftarrow value 10)

REP (Repeat operation)

DX (Data Register): MUL, DIV, I/O operation
Port output show করার জন্য

Address Register:

1. Segment Registers:

CS (Code Segment) → code লিপ্তার জন্য

DS (Data Segment) → data store

SS (Stack Segment) → stack operation মে জয়ো

ES (Extra Segment) → more than 16 bits জয়ো

Physical address - 20 bit

2^{20} , 1 MB \rightarrow 8086 জয়ো memory.

Registers 8bit or 16 bit জয়ো

Memory এর ছোট ভক্ট জয়ো নিয়ে access
বড় ভক্ট জয়ো নিয়ে access

00000000...00000000
00000000...00000000

00000000...00000000
00000000...00000000

00000000...00000000
00000000...00000000

00000000...00000000
00000000...00000000

Address range \rightarrow 00000H to FFFFFH.

Memory car ~~car~~ ~~size~~ (इन्हें) block = ग्राम तक यह बड़ी
size $2^{16} \rightarrow 64\text{kb}$

16 bit वाले memory (or segment) का इसका

एकाधिक segment का अंतर्गत specific location
का address (or offset) बला जाए।

Segment 0 → 000000

0000f

000001

00001

Segment 0 → 000000

0001f

00011

Segment 1 → 00010

offset

Last → ffffff

Logical Address
Segment : Offset

1256A

1240A

A4FB : 4872 h

Physical address = segment × 10 + offset.

∴ Physical address = A4FB0 + 4872
= A9822 h

4 bit carry left shift
Hex multiplication
Hex 10

Ex. 8.1

physical address : 1256A, h

Segment X : 1256h

Offset Y: 1240h
Segment

$$1256A = 1256 \times 10 + \text{Offset } X$$

$$X = A \text{ h.}$$

$$1256A = 1240 \times 10 + Y$$

$$Y = 16A \text{ h.}$$

logical address → 1256 : 000A .

1240 : 016A .

logical address →

Pointer Register:

Pointer { SP (Stack Pointer) → SS → stores current segment pointer location
BP (Base Pointer) → CS → stack → data access

Index { SI (Source Index) → DS
DI (Destination Index) → ES

SI

R U E T

TEUR .

LAB - 1

• MODEL SMALL

• STACK 100H

• DATA (not mandatory; variable initialize/zero define)

DB → byte

DW → word

A DW 2

B DW ?

SUM DW ? → value unknown

• CODE

MAIN PROC [int main()]

MOV AX, @DATA

MOV DS, AX

MOV AX, A ; AX = A

ADD AX, B ; AX = A + B

MOV SUM, AX

MOV AX, 4CH

INT 21H

MAIN ENDP

END MAIN

IOS - Basic I/O system

DOS - Disc Operating system

Windows

Mac OS

Linux

Android

iOS

Ubuntu

CentOS

Debian

Fedora

Arch Linux

Manjaro

Pop!_OS

Elementary OS

MX Linux

Ubuntu Server

CentOS Server

Debian Server

Arch Linux Server

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$$EXP = A + B - C$$

Input, Output &

Keyboard character print. • @, _, %

- MODEL SMALL

- STACK 100H

- CODE

MAIN PROC

MOV AH, 2 → output

MOV DL, '?'

INT 21H → mandatory

[Input]

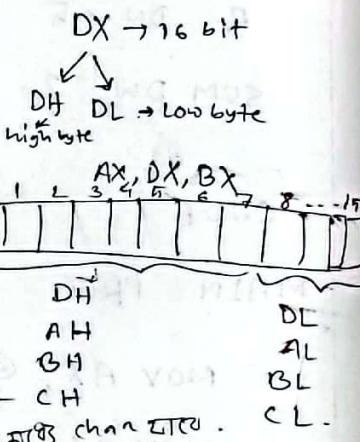
MOV AH, 1 / MOVAL, 1

INT 21H

MOV BL, AL.

variable name such as @, _, %

Output show to DL



INT 21H
MOV AH, 4CH
INT 21H
MAIN ENDP
END MAIN

Newline

MOV AH, 2

MOV DL, 0DH

INT 21H

MOV DL, 0AH

INT 21H

MOV AH, DL, BL

Lecture-4

IP (Instruction Pointer)

program u next instruction run to address car point वाले तरीके

FLAG Register

Parity
↓
PF = 1
Zf = 1 → result = 0

Startup Operation → स्टॉट ऑपरेशन
self-study

Chapter-4

a DB 'A'

a DB ?

Naming field

length [1-31] ↳ ?, ., @, \$, __, %

जावामध्य अनुदान

AB CD X

• ARROW

Operation field

NOP → No Operand

INC AX → Increment
↳ Operand

ADD AX, BX
↳ Operand

Binary, Decimal, Hexadecimal

10b/10B 10 10h/10H

DB → Define byte → 1 byte

DW → Define word → 2 byte

DD → Double word → 4W

DQ → Define Quad word → 8W

DT → Define Ten byte → 10B

Array

Symbol Address

B_ARRAY DB 10H, 20H, 30H

Symbol Address content

B_ARRAY 200h 10h

B_ARRAY+1 201h 20h

B_ARRAY+2 202h 30h

Character string

LETTER DB 'ABC'

LETTER DB 41H, 42H, 43H

EQU → equal

name EQU constant → value assign memory carriage return

LF EQU 0AH

newline → first space

new line
line fit

source \Rightarrow content unchanged
 dest, out dest. \Rightarrow move into

 $\text{MOV} \rightarrow \text{Move} \rightarrow \text{destination, source}$
 $\text{XCHG} \rightarrow \text{Exchange} \rightarrow \text{destination, source}$
~~both change~~ both change

$\text{MOV AX, Mem} \rightarrow$ memory location \Rightarrow
 content \rightarrow AX \rightarrow move
 $\text{MOV Mem, AX} \rightarrow$ AX \rightarrow mem loc. \rightarrow move
 $\text{Mov Mem, Mem} X$.
 memory register \Rightarrow through move \Rightarrow ZTS.

9.2 table

$\text{GR} \rightarrow \text{GR}$

$\text{GR} \rightarrow \text{ML}$

$\text{ML} \rightarrow \text{GR}$

$\text{ML} \rightarrow \text{ML} X$

$\text{GR} = \text{General Register}$
 $\text{ML} = \text{Memory Location}$

~~#~~ ADD
~~#~~ SUB
~~#~~ INC
~~#~~ DEC } only destination, no source

$\text{NEG} \rightarrow \text{Negation} \rightarrow 2^{\text{1's}} \text{ complement}$.

~~#~~ $A = B - 2A$ tiny

MOV AX, B

SUB AX, A

SUB AX, A

MOV A, AX

~~#~~ SMALL → { Code segment
~~#~~ MEDIUM → Data segment.
~~#~~ COMPACT →
~~#~~ LARGE → Memory models

~~*DATA~~ → global variable declaration \Rightarrow ZTS

WORDT DW 2

MSG DW 'Hello world'

• stack size.

100 H

•CODE

MAIN PROG

MAIN ENDP

Subfunction / user defined function

END MATN.

MOV AH,1 → single char input

INT 21H

INT Output

MOV AH, 2

Output \rightarrow DL .

INT 21H

Lecture - 5

Chapter-5

The Processor Status and FLAG Registers

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				OF	DF	IF	TF	SF	ZF		AF		PF		CF
Overflow flag				interrupt Flag	sign Flag	zero Flag				Auxiliary flag		Parity flag		Carry flag	
												(even or odd check)		(extra bit+)	

operation.result = 0 π zeroFlag = 1

$$\begin{array}{r}
 & \swarrow \\
 & 1 \\
 & | \\
 & 1 \\
 \hline
 1 & 0 & 0
 \end{array}
 \quad
 \begin{array}{l}
 \text{carry in} \\
 \text{carry out } \frac{1}{10}
 \end{array}$$

Addition 6

Parity flag →

$$\begin{array}{r} \text{FFFFE} \\ \underline{\text{LLL1 LLL1 LLL1 LLL0}} \\ \text{HB} \qquad \qquad \text{LB} \end{array} \quad PF = 0$$

Auxiliary carry flag (Af) :

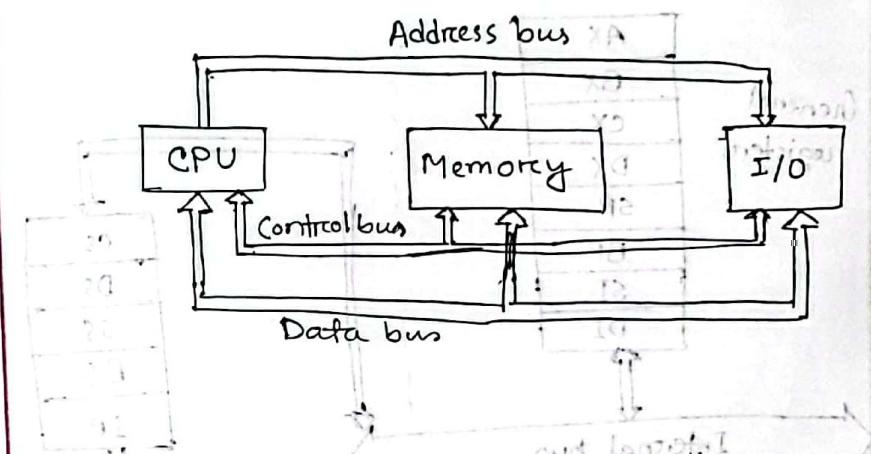
Sign flag

Overflow flag

$$\begin{array}{r} 1111 \ 1101 \\ + 1 \\ \hline - 2^8 = 1111 \ 1110 \end{array}$$

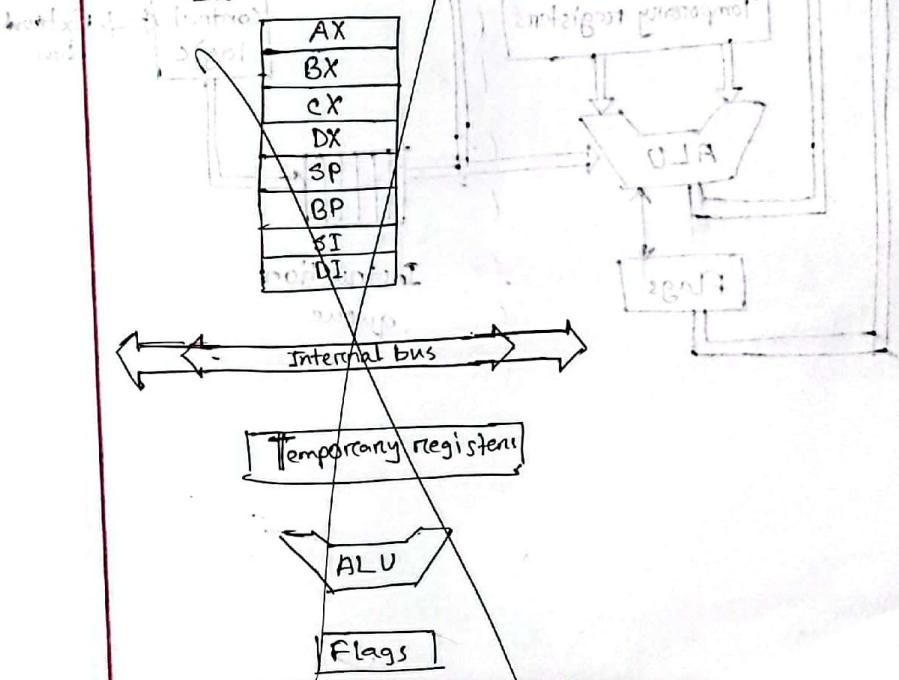
CT-1

Bus Connections of a Microcomputer:

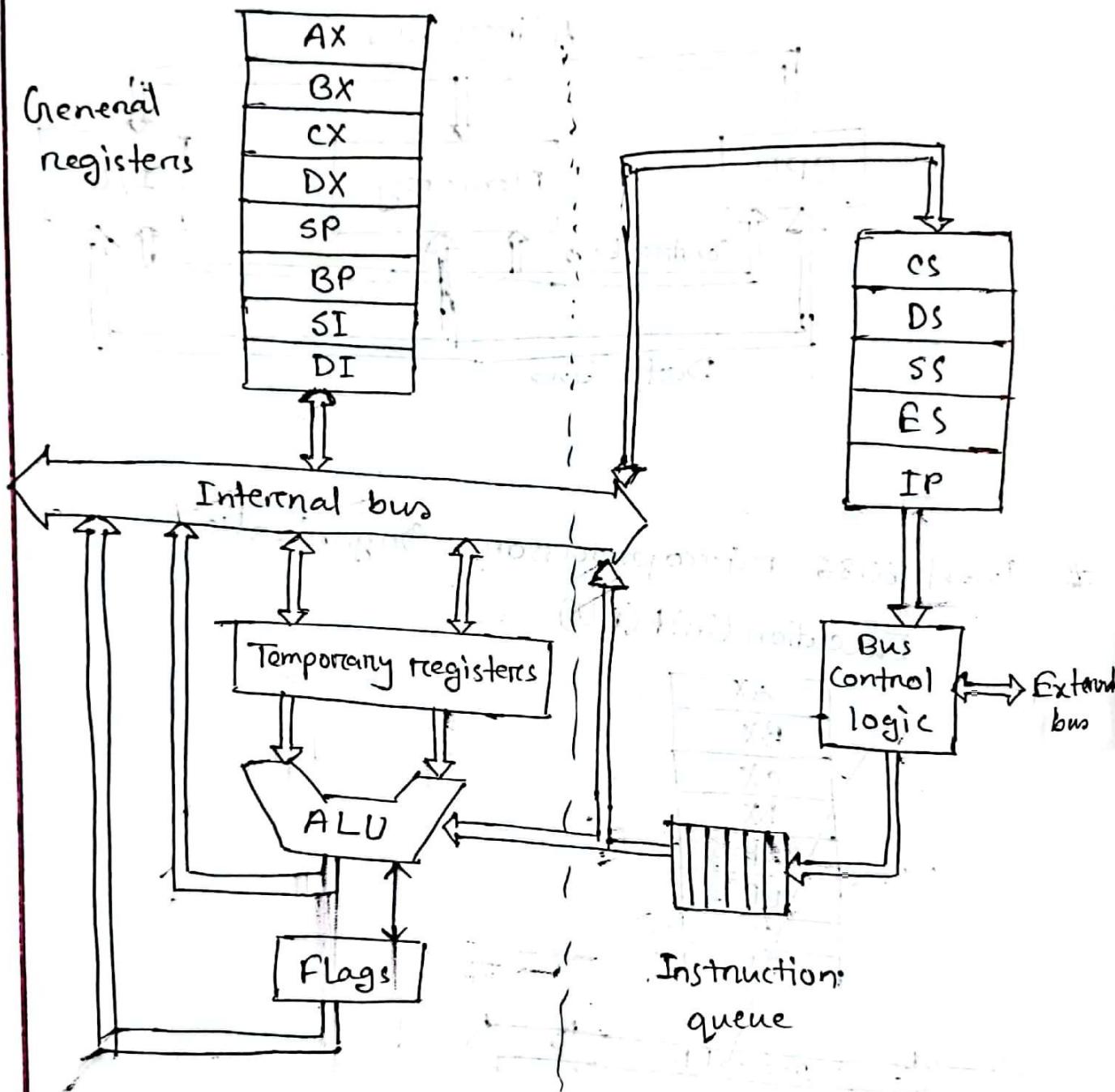


Intel 8086 Microprocessor Organization

Execution Unit (EU)



Execution Unit (EU)



Lecture-7

$35h = 00110101$

$0Fh = 00001111$

$\underline{-}$
 00000101

XOR - specific bit complement

NOT - 16 bit complement.

AND - destination change

Test - no change.

Assembly CT-2

Tuesday - 4 & 5

Lecture-8

Chapter-7

SHL AL, 1

AL 1011101

CF=1 0111010 , Leftside carry CF = 1
Right side 0 add 2⁰.

Multiply by 2 = Leftshift -

AL = 5 = 00000101_b

Leftshift = 00001010_b = 10

k times shift = 2^k multiply .

BL = 80h CL = 2

SHR

5

$$AL = 5 = 00000101$$

floor value
 $Z = 00000010 \quad CF=1$

Rotafe

ICF

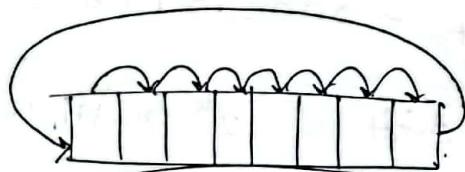
ROL

$$AL = 5$$

00000101

$$CF=0 \quad 00001010$$

ROR



AL

CX, 8

SHL

CF

RCR

AL → 1 0 1 0 1 0 0 0 0

CF

BL = 1 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 1

1 0

0 1 1 0 0 0 0

0 1 0 1 1 0 0 0

0 0 1 0 1 1 0 0

0 0 0 1 0 1 1 0

0 0 0 0 1 0 1 1

CT-2

Chapter-5

5.1 ADD AX, BX ; AX = fffffh
BX = fffffh.

$$\begin{array}{rcl} \text{fffff h} & = & 1111\ 1111\ 1111\ 1111 \\ \text{fffff h} & = & 1111\ 1111\ 1111\ 1111 \\ \hline & & 1111111111111110 \end{array}$$

SF = 1

ZF = 0

PF = 0

CF = 1.

OF = 0

AL = 80h , BL = 80h

$$80h = 1000\ 0000$$

$$80h = + 1000\ 0000$$

$$\hline 1000000000$$

SF = 0

PF = 1

ZF = 1.

CF = 1.

OF = 1.

5.3

SUB AX, BX . .

$$AX = 8000h = 1000\ 0000\ 0000\ 0000$$

$$BX = 0001h = 0000\ 0000\ 0000\ 0001$$

$$\begin{array}{r} 1000\ 0000\ 0000\ 0000 \\ - 0000\ 0000\ 0000\ 0001 \\ \hline 1111\ 1111\ 1111\ 1111 \\ + 1 \\ \hline 1111\ 1111\ 1111\ 1111 \\ \hline \neg 1 FFF h = 10111\ 1111\ 1111\ 1111 \end{array}$$

SF = 0

PF = 1

ZF = 0

CF = 0

OF = 1

-A-B = even

INC AL , AL = ffh = 1111 1111

$$\begin{array}{r} + 0000\ 0001 \\ \hline 1\ 0000\ 0000 \end{array}$$

SF = 0

PF = 1.

ZF = 1.

CF = 0 [unchanged]

OF = 0

-A+B = +ve

5.6 NEG AX .

$$AX = 8000h = 1000\ 0000\ 0000\ 0000$$

1's comp.

0111	1111	1111	1111
+ 0000	0000	0000	0001
<hr/>			
1000 0000 0000 0000			

$-8000h = \underline{\underline{1000\ 0000\ 0000\ 0000}}$

SF = 1 .

PF = 1

ZF = 0

CF = 1 (always unless result=0) .

OF = 1 .

Exercise

1. a) ADD AX , BX ; AX = 7FFFh , BX = 0001h .

7FFFh	= 0111	1111	1111	1111
0001h	= 0000	0000	0000	0001
<hr/>				
1000 0000 0000 0000				

SF = 1

ZF = 0

PF = 1

CF = 0

OF = 1 .

b) SUB AL,BL

$$01h = 0000\ 0001$$

$$FFh = 1111\ 1110$$

$$\underline{\underline{=100\ 0000\ 10}}$$

SF = 0

PF = 0

ZF = 0

CF = 1 .

OF = 0 .

c) DEC AL

$$AL = 00h = 0000\ 0000$$

$$- 0000\ 0001$$

$$\hline ffh = 1111\ 1111$$

$$SF = 1 \quad ZF = 0 \quad PF = 1 \quad CF = 0 \quad OF = 0$$

[unchanged]

[Same sign overflow set]

d) NEG AL

$$7Fh = 0111\ 1111$$

$$1's \text{ comp. } 1000\ 0000$$

$$+ 0000\ 10001$$

$$\hline 81h = 1000\ 0001$$

SF = 1.

ZF = 0

PF = 1

CF = 1. [always 1 unless result = 0]

OF = 0

$$- A + B =$$

e. XCHG AX, BX [does not affect]

f. ADD AL, BL

$$AL = 80h = 1000\ 0000$$

$$BL = ffh = 1111\ 1111$$

$$\hline 7Fh = 1011\ 1111$$

SF = 0

ZF = 0

PF = 0

CF = L

OF = 1.

g. SUB AX, BX

$$AX = 0000h = 0000\ 0000\ 0000\ 0000$$

$$BX = 8000h = 1000\ 0000\ 0000\ 0000$$

$$\hline 8000h = 1000\ 0000\ 0000\ 0000$$

SF = 1

ZF = 1

CF = 0

OF = 1.

$$A - B = A + B$$

= (-ve)

b) NEG AX

$$AX = 0001h = 0000\ 0000\ 0000\ 0001$$

1's comp $\begin{array}{r} 1111\ 1111\ 1111\ 1110 \\ + 0000\ 0000\ 0000\ 0001 \\ \hline fffffh = 1111\ 1111\ 1111\ 1111 \end{array}$

SF = 1

ZF = 0

PF = 1.

CF = 1

OF = 0

carry out = 0
carry in = 1.

2.a)

$$AX = 01** *000* *000* *000*$$

$$BX = 01** *000* *000* *000*$$

$\begin{array}{r} 10** *000* *000* *000* \\ + 01** *000* *000* *000* \\ \hline 10** *000* *000* *000* \end{array}$

Ex:

$$AX = 7FA0h = 0111\ 1111\ 1010\ 0000$$

$$BX = 600Dh = 0110\ 0000\ 0000\ 0101$$

$\begin{array}{r} 1101\ 1111\ 1010\ 1101 \\ + 0110\ 0000\ 0000\ 0101 \\ \hline DFADh = 1101\ 1111\ 1010\ 1101 \end{array}$

Cin XOR Cout = 1 XOR 0 = 1 = OF

b)

$c_{out} = 1$
 $c_{in} = 0$

$$AX = 10xx\ xxxx\ xxxx\ xxxx$$

$$\underline{BX = 10xx\ xxxx\ xxxx\ xxxx}$$

$$AX = 8DE4h = 1000\ 1101\ 1110\ 0100$$

$$BX = B216h = 1011\ 0010\ 0001\ 0110$$

$$3FFA h = \underline{\square}\ 0011\ 1111\ 1111\ 1010$$

$$c_{out} \text{ XOR } c_{in} = 1 \text{ XOR } 0 = 1 = OF$$

3.a)

$$512Ch = 0101\ 0001\ 0010\ 1100$$

$$+ 4185h = 0100\ 0001\ 1000\ 0101$$

$$\hline 92B1h = 1001\ 0010\ 1011\ 0001$$

SF = 1. signed OF = 1 unsigned CF = 0

ZF = 0

PF = 1

CF = 0

OF = 1.

b) $FE12h = 1111\ 1110\ 0001\ 0000$
 $+ 1AEBh = 0001\ 1010\ 1100\ 1011$
 $\hline - 18DDh = \boxed{1}0001\ 1000\ 1101\ 1101$
 $SF = 0, PF = 1, ZF = 0$

unsigned CF = 1 signed OF = 0

c) $E1E4h = 1110\ 0001\ 1110\ 0100$
 $+ DAB3h = 1101\ 1010\ 1011\ 0011$
 $\hline - BC97h = \boxed{1}011\ 1100\ 1001\ 0111$
 $SF = 1, PF = 0, ZF = 0$

unsigned CF = 1 signed OF = 0

d) $7132h = 0111\ 0001\ 0011\ 0010$
 $+ 7000h = 0111\ 0000\ 0000\ 0000$
 $\hline E132h = 1110\ 0001\ 0011\ 0010$
 $SF = 1, PF = 0, ZF = 0$
 $unsigned CF = 0, signed OF = 1.$

e) $6389h = 0110\ 0011\ 1000\ 1001$
 $1176h = 0001\ 0001\ 0111\ 0110$
 $\hline - 74FFh = 0111\ 0100\ 1111\ 1111$
 $SF = 0, PF = 1, ZF = 0$

unsigned CF = 0 signed OF = 0

4. a) $2143h = 0010\ 0001\ 0100\ 0011$
 $- 1986h = 0001\ 1001\ 1000\ 0110$
 $\hline - 07BDh = 0000\ \boxed{1011}\ 1101$
 $SF = 0, ZF = 0, PF = 1, CF = 0, OF = 0$

b) $81FFh = 1000\ 0001\ 1111\ 1110$
 $- 1986h = 0001\ 1001\ 1000\ 0110$
 $\hline - 6878h = 0110\ 1000\ 0111\ 1000$
 $SF = 0, ZF = 0, PF = 1$

unsigned CF = 0 signed OF = 1 [-A -B = +ve]

c) $198Ch = 0001\ 1001\ 1011\ 1100$
 $-81FFh = 1000\ 0001\ 1111\ 1110$
 $97BE = 1001\ 0111\ 1011\ 1110$

SF = 1, ZF = 0, PF = 1

unsigned CF = 1, signed OF = ∞ 1.

$$\begin{aligned} A - (-B) &= A + B \\ &= A + B \end{aligned}$$

d) $0002h = 0000\ 0000\ 0000\ 0010$
 $-FE0Fh = 1111\ 1110\ 0000\ 1111$
 $01F3h = 0000\ 0001\ 1111\ 0011$

SF = 0, ZF = 0, PF = 1.

unsigned CF = 1, signed OF = 0

$$\begin{aligned} A - (-B) &= A + B \\ &= A + B \end{aligned}$$

e) $8B0DH = 1000\ 1011\ 1100\ 1101$
 $-71ABh = 0111\ 0001\ 1010\ 1011$
 $7A22h = 0001\ 1010\ 0010\ 0010$

SF = 0, ZF = 0, PF = 1

unsigned CF = 0, signed OF = ∞ 1

Lecture

chapter-8

Stack

PUSH source \rightarrow source \Rightarrow value stack a push \Rightarrow $\times 0\ 909$

POP destination \rightarrow

Push \rightarrow
1. SP \rightarrow decrease $\stackrel{\text{2}}{\leftarrow}$ over

2. Push

POP \rightarrow

1. POP

2. SP \rightarrow increase $\stackrel{\text{2}}{\leftarrow}$ over

• STACK 100H Offset:

00F6

00F8

00FA

00FC

00FE

0100

0100 SP

1234 AX

5678 BX

Now 00FE SP

PUSH BX
00FC SP

PUSH AX .

High byte FD

Low byte FF.

00FC

SP

FFFF

CX

5678

CX

0001

DX

00FF

SP

POP DX

01234

DX

0100

SP

Procedure declaration

name PROC type

- - -

- - -

RET
mandatory

name ENDP.

A * B

product = 0

REPEAT.

If 1st bit of B = 1

then product = product + A.

END-If.

Lecture

Chapter 9

Multiplication & Division Instructions

unsigned

$$\begin{array}{r} 10000000 \\ \times 11111111 \\ \hline 128 \quad \times \quad 255 \quad = 32640 \end{array}$$

signed

$$\begin{array}{r} -128 \quad \times \quad -1 \\ \hline = 128 \\ = 0000000100000000 \end{array}$$

MUL - unsigned

IMUL - signed

Integer multiplication

MUL source

IMUL source

8 bit * 8 bit = 16 bit

16 bit * 16 bit = 32 bit

→ 2 word register

Byte form \rightarrow AL, Result \rightarrow AX → AH upper
AL lower.
Word form \rightarrow AX Result \rightarrow DX - upper half
AX - lower half

carry & overflow flag = 0, result ≥ 0
upper half ≥ 0 .

otherwise, CF/OF = 1.

IMUL \rightarrow CF
CF/OF $\begin{cases} 0 & \text{upper half, lower half sign extension } \geq 0, \\ & \text{lower half } \geq \text{sign bit} \\ & \text{upper half } \geq \text{sign bit} \\ 1 & \text{[Otherwise] Ex: Lower half } \geq \text{sign bit} \\ & 1 + 2^{32}, \text{ upper half } \geq \\ & \text{sign bit } 1 + 2^{32}, \end{cases}$

$AX = 1$

$BX = FFFF$

MUL BX ; $AX = 0000 FFFF$

DX AX

CF/OF=0 0000 FFFF

IMUL BX ; $AX = FFFF FFFF$

DX AX

CF/OF=0 FFFF FFFF

Ex: $5 \times 12 - 12 \times 5$

$A = 5 \times A - 12 \times B$

MOV AX, 5 ; $AX = 5$

IMUL A ; $AX = 5 \times A$

MOV AX, A ; $A = 5 \times A$

MOV AX, 12 ; $AX = 12$

IMUL B ; $AX = 12 \times B$

SUB A, AX ; $A = A - AX$
 $= 5 \times A - 12 \times B$

for Factorial .

g.7

DIV → unsigned

IDIV → signed

DIV divisor .

Byte form

dividend → 16 bit → AX

divisor → 8 bit

divisor) AX (AL

quotient → AL

remainder → AH

Word form

dividend → 32 bit → DX, AX

source/divisor → 16 bit → AX

quotient → AX

remainder → DX

source) DX; AX (AX

DX

Lecture

9.4

Sign Extension → self study.

Decimal I/O

Decimal Output.

$AX > 0$, print direct

$AX < 0$, print then $NEG AX$.

$AX = -1$.

$NEG AX$; $AX = 1$.

If $AX < 0$, Then print '-'

Replace $A \leftarrow 2^{\text{'s compliment}}$ (Neg)

End if.

Get digit in AX 's decimal representation
Convert digit → character & print.

9.8

$DX = 0000h$

$AX = 0005h$

$BX = 0002h$.

	decimal	decimal	
DIV	quotient	remainder	AX DX
	2	1	0002 0001

IDIV		2	1	0002 0001
------	--	---	---	-----------

$DX = 0000h$

$AX = 0005h$

$BX = FFFEh = 65534 = -2$

	decimal	decimal	
DIV	quotient	remainder	AX DX
DIV	0	5	0000 0005

IDIV	-2	1	FFFE 0001
------	----	---	-----------

Decimal representation

24618

10 द्वारा भाग करने का पथ

$$\begin{array}{l} 24618/10, Q=2461, R=8 \\ 2461/10, Q=246, R=1 \\ 246/10, Q=24, R=6 \\ 24/10, Q=2, R=4 \quad \text{Reverse} \\ 2/10, Q=0, R=2 \end{array}$$

Count count=0

Repeat

divide Q by 10.

push remainder into stack

count = count + 1; Pop stack करने का काम

until Q=0.

for count times do

pop digit from stack.

digit \rightarrow ch

output \rightarrow ch

End for.

9.1

Decimal Input

0101 - 51

1011 - 51

0111 - 71

1111 - 11

0100 - 4

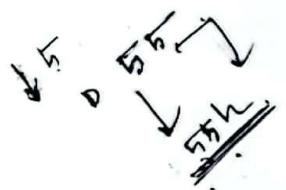
CT-3

$$\underline{01000001} = 41h \rightarrow A$$

$$\underline{00110111} = 37h$$

$$\underline{\boxed{00001010}} = A$$

$$\begin{array}{r} 00001001 \\ \times 00001111 \\ \hline 0001 \end{array}$$



A	- 10	- 1010
B	- 11	- 1011
C	- 12	- 1100
D	- 13	- 1101
E	- 14	- 1110
F	- 15	= 1111

$$42h = 1000010$$

Lecture

Chapter - 10

Arrays & Addressing Modes.

↳ Data structure to store data.

MSG DB 'ABCD'

W DW 20, 25, 35, 40

Offset	Address	Symbol	Decimal
	0200h	w	20
	0202h	w+2h	25
	0204h	w+4h	35
	0206h	w+6h	40

repeat duplicate operator \rightarrow DUP(value)

G	DW	100	DUP(0)
(array name)	(word size (2 byte))	(elements)	(initially 0)
Line	DB	5, 4, 3 DUP (2, 3 DUP(0), 1)	DUP(?)
	byte size (1 byte)	1st element 2nd element (constant duplicate) 3x (2, 0, 0, 1)	(no initialization)
Line	DB	n, 4, 2, 0, 0, 1, 2, 0, 0, 1, 2, 0, 0, 1	

<u>position</u>	<u>location</u>
1	A
2	$A = 1 \times S$
3	$A = 2 \times S$
.	
.	
N	$A = (N-1) \times S$

Byte
10th position element \leftrightarrow 25th position element

B+98 B+24

word

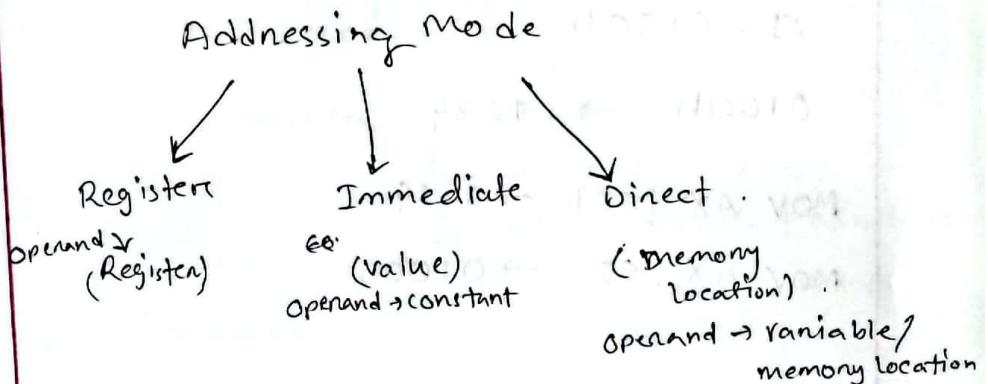
$w + 9 \times 2$

$w + 18$

MOV AX, w+18

XC₁₆ W+48, AX

MOV w+18, AX.



MOV AX, 0

↓

Registers

Immediate .

MOV VAR, AX

↓

Direct

Registers .

Addressing mode :

- I) Register Indirect \rightarrow Registers to point to [register] \rightarrow Address of content
- II) Based
- III) Indexed
- IV) Based Indexed .

BX, SI, DI, BP .
DS SS .

SI = 0100h

0100h → 1234

MOV AX, [SI] → 1234

MOV AX, SI → 0100h

W DW 10, 20, 30, ..., 100

XOR AX, AX

LEA SI, W

MOV CX, 10

REPEAT:

ADD AX, [SI]

ADD SI, 2

Loop REPEAT.

Ex: 10^4 → Reverse.

Lecture

Based & Indexed

displacement

variable : A

constant : -2

offset address ± constant;

A + 4

Representation

[reg + dis]

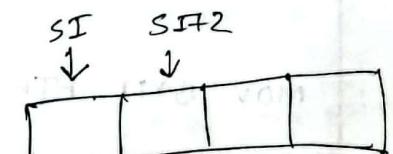
[dis + reg]

[reg] + displacement

displacement + [reg]

dis [reg]

BX, BP, SI, DI → Addressing mode
based indexed addressing



W, BX = 9

MOV AX, W[BX]

W + BX

W + 9

MOV AX, [SI+2] → end element
-W+2 . AX more etc.

W+L
W+4 → ^{3rd element} AX more etc.
^{more etc}

```

W DW 10, 20, 30, 40, 50, 60, 70, 80, 90, 100
    XOR AX, AX
    XOR BX, BX
    MOV CX, 10
    ADD AX, W[BX]
    ADD BX, 2

```

Loop ADD

PTR Operator

word instruction MOV AX, 5 ; 5 → 16 bit word
 byte instruction MOV AL, 5 ; 5 → 8 bit word

MOV [BX], 5X ; Byte/word both 20 bits
 so illegal.

MOV BYTE PTR [BX], 5 ; source, destination
 byte → word,
 Address indicate word.

MOV WORD PTR [BX], 5 ; word

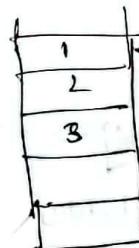
MSG1 DB 'this is a msg'
 $\frac{t}{5}$
 MOV [BX], MSG1 ; Byte → word - came MSG1
 जारी करा declare वर्त.
 source type वह एकआइ.
 one dimensional
 array
 MOV BYTE PTR [BX], MSG1

LEA SI, MSG1 ; ← SI first letter point वह जारी.

MOV MSG1[SI], 'T'

MOV MSG1[SI+3], 'S'

#



AX

BX

CX

MOV BP, SP

Stack top point
 जारी करा BP के

MOV AX, [BP]

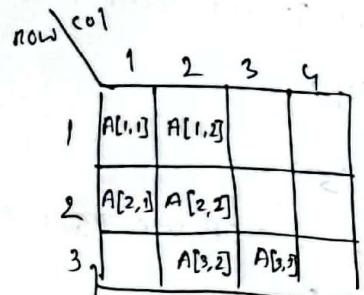
MOV BX, [BP+2]

MOV CX, [BP+4]

10.3 ex.

Array element cont

Two dimensional array to access data
Based Indexed addressing mode.



Row major order $\rightarrow A[\text{now}, \text{col}]$

Col major order $\rightarrow A[\text{col}, \text{now}]$.

Row major order

B DW 10, 20, 30, 40

DW 50, 60, 70, 80

DW 90, 100, 110, 120

[3x4] array

Column major order

B DW 10, 50, 90

DW 20, 60, 100

DW 30, 70, 110

DW 40, 80, 120

Array indexing

A DW ; M X N

Row i, $A[i, 1] \rightarrow A + (i-1) * N * 2$

col j, $A[1, j] \rightarrow A + (j-1) * 2$

Based-Indexed Addressing representation

$V[b_r] [i_r]$

~~$b_r + i_r + V + C$~~

$C[b_r + i_r + V]$

$V[b_r + i_r + C]$

107 A DW 5x7.

1) clear row 3.

2) clear col 4.

1) $A + (3-1) * 7 * 2 = A + 28$

~~2)~~ MOV CX, 7.

MOV BX, 28

XOR SI, SI

CLEAR_:

MOV A[BX][SI], 0

ADD SI, 2

loop CLEAR_



2) $A + (4-1) * 2 = A + 6$

~~MOV A[BX][SI], 0~~

~~MOV A[BX][SI], 0~~

ADD BX, 2

loop

average in test score

~~TESTSCORE~~

~~CLD~~

~~MOV CX, 10~~

~~MOV BX, 10~~

~~MOV SI, 0~~

~~MOV AX, 0~~

CT-3

chapter-6

1. a) `CMP AX, 0`
~~JNL/JGE END-IF~~
`MOV BX, -1`
~~END-IF:~~

b) `CMP AL < 0`
~~JNL/JGE ELSE-~~
`MOV AH, FFH`
~~JMP END-IF~~
~~ELSE-:~~
`MOV AH, 0`
~~END-IF:~~

c) `CMP DL, "A"`
~~JL THEN-IF~~
`CMP DL, "Z"`
~~JG THEN-IF~~
`MOV AH, 2`
`INT 21H`
~~END-IF:~~

d) `CMP AX, BX`
~~JLE THEN~~
~~JNL/JGE END-IF~~
`CMP BX, CX`
~~JNL/JGE ELSE-~~
`MOV AX, 0`
~~JMP END-IF~~
~~ELSE-:~~
`MOV BX, 0`
~~END-IF!~~

e) `CMP AX, BX`
~~JL THEN-~~
`CMP BX, CX`
~~JL THEN-~~
`MOV DX, 1`
~~JMP END-IF~~
~~THEN-!~~
`MOV DX, 0`
~~END-IF!~~

f) `CMP AX, BX`
~~JNL THEN ELSE-~~
`MOV AX, 0`
~~JMP END-IF~~
~~ELSE-:~~
`CMP BX, CX`
~~JNL ELSE2-~~
`MOV BX, 0`
~~JMP END-IF~~
~~ELSE2-:~~
`MOV CX, 0`
~~END-IF!~~

2.

`MOV AH, 1`
`INT 21H`
`CMP AL, 'A'`
`JF CAR_RET`
`CMP AL, 'B'`
`JF LINE_FEED`
`MOV AH, 4CH`
`INT 21H`
`JMP END_CASE`

CAR_RET:

`MOV AH, 2`
`MOV DL, ODH`
`INT 21H`
`JMP END_CASE`

LINE_FEED:

`MOV AH, 2`
`MOV DL, OAH`
`INT 21H`
~~RET~~
END_CASE:

3. a) $(148-1)/3 = 49$

```
MOV CX, 49
MOV AX, 1
MOV BX, 1
```

LOOP1:

```
ADD BX, 3
ADD AX, BX
LOOP LOOP1
```

b) $(100-5)/5 = 19$

```
MOV CX, 19
MOV AX, 100
MOV BX, 100
```

LOOP1:

```
SUB BX, 5
ADD AX, BX
LOOP LOOP1.
```

4. a) $(148-1)/3 = 49$

```
MOV CX, 50
MOV DX, 1
MOV AX, 1
```

```
L1: ADD AX, 4
      ADD DX, AX
```

LOOP L1

c) $100/5 = 20$
MOV CX, 5
MOV AH, 7

L1: INT 21H

LOOP L1

END: MOV DL, 'X'
MOV CX, 5
MOV AH, 2

L2: INT 21H
LOOP L2

b) $MOV AH, 1$
~~INT 21H~~

```
MOV AH, 2
MOV DL, 0AH
INT 21H
MOV DL, 0DH
INT 21H
MOV DL, AL
MOV CX, 80
```

DISPLAY:
INT 21H
LOOP DISPLAY;

d) $MOV CX, 0$

WHILE: INT 21H

CMP AX, BX ; AX = dividend
JL END- ; BX = divisor
INC BX ; CX = quotient
SUB AX, BX
JMP WHILE-
END:

6. MOV CX, 0

L1: ADD CX, AX , cx=product, AX=M, BX=N.

DEC BX

JNZ L1.

7. a) MOV AH, 1

INT21H

Mov CX, 80

b) MOV AH, 1

MOV CX, 80

L2: INT 21H .

CMP AL, 0DH

LOOPNE L2.

Chapter-7

1. a) 10001011b, b) 11111001b, c) 10100110b

d) 10100001b

2. a) AAAAh = 1010 1010 1010 1010b

Clearing even number of bits of AX .

AX = $\begin{smallmatrix} 1 & 0 & 1 & 1 & 1 & 0 & 0 & 1 \\ \text{IL} & \text{IL} \\ 0 & 1 & 1 & 0 & 1 & 0 & 1 & 0 \end{smallmatrix}$

AND AAAAh = $\begin{smallmatrix} 1 & 0 & 1 & 0 & 1 & 0 & 1 & 0 \\ \text{IL} & \text{IL} \\ 0 & 0 & 1 & 0 & 1 & 0 & 0 & 0 \end{smallmatrix}$

0010 1010 0000 1000

MOV AX, AAAAh .

b) 81h = 10000001b . set msb and ls6 of BL .

OR BL, 81h

c) Implement msb of DX

-8000h = 1000 0000 0000 0000 0000 1111

XOR DX, 8000h

d) NOT WORD1 → Complement word variable.

XOR WORD1, FFFFh .

3. a) TEST AX, 0FFFFh

b) TEST BX, 0001h

c) TEST DX, 8000h

d) TEST DX, 8000h

e) TEST BL, FFh

$$AL = 11001011_2 = CBh$$

4. a) 10010110₂ = 96h

b) 01100101₂ = 65h

c) 10010111₂

00101111₂ = 2Fh

d) 11100101₂

11110010₂

01111001₂ = 79h

e) 11100101₂

11110010₂ = F2h

f) 10010111₂ = 97h

g) 11100101₂, CF=1

11110010₂, CF=1

11111001₂, CF=0.

= F9h

5. a) Double the value of byte variable B9

MOV SHL B9, 1

b) Multiply AL by 8

MOV CL, 3
SHL AL, CL

c) Divide 32142 by 4 ; AX = quotient

MOV AX, 32142
SHR AX, 2

d) Divide -2145 by 16

MOV BX, -2145
SAR BX, 4

6. a) ~~MOV ADD AL, 30H // convert value to decimal~~
~~OR AL, 30H~~

b) ~~OR DL, 20H // Upper case to lower case~~

7. a) ~~MOV DL, BL~~ b) ~~MOV CL, 3~~
~~MOV CL, 3~~ ~~MOV AH, 0~~
~~SHL BL, CL~~ ~~ROR AX, CL~~
~~SHL DL, 1~~
~~ADD BL, DL~~

~~BL = 0011 1011~~ \Rightarrow ~~11011000~~
~~10d = 0000 1010~~ \Rightarrow ~~+ 00010100~~
~~0800 1010~~ \Rightarrow ~~11011100~~
~~01110110~~ \Rightarrow ~~1110~~

$$AX = \frac{0101}{5} \frac{1010}{A} \frac{0111}{27} \frac{0110}{6}$$

$$AH \rightarrow 0000 \ 0000 \ 0111 \ 0110$$

$$1 \rightarrow 0000 \ 0000 \ 0011 \ 1011$$

$$2 \rightarrow 01000 \ 0000 \ 0001 \ 1101$$

$$3 \rightarrow \frac{1100}{C} \ 0 \ 0000 \ 0000 \ 1110$$

Eq

$$BL = \underbrace{0101}_{10d} \ 0111_{=87d} \times 10d$$

$$DL = 0101 \ 0111$$

$$1 \rightarrow 10101110$$

$$2 \rightarrow 01011100$$

$$3 \rightarrow 10111000$$

$$\text{OR } \underline{10101110}$$

$$10111110$$

$$BL = 0000 \ 00111$$

$$DL = 0000 \ 0111$$

$$1 \rightarrow 00001110$$

$$2 \rightarrow 00011110$$

$$3 \rightarrow 00111000$$

$$\underline{00111110}$$

$AL = 8CH$

$= 1000\ 1100$

$ROR AL, 20$

$1 \rightarrow 01000110$

$2 \rightarrow 00100011$

$3 \rightarrow 10010001$

$4 \rightarrow 11001000$

$5 \rightarrow 001100100$

$6 \rightarrow 00110010$

$7 \rightarrow 00011001$

$8 \rightarrow 10001100$

$8 \times 2^4 + 4 = 20$

$AL = 11001000 = C8H$

ii) $SAR AL, CL, CL = 3$

$8CH = 1000\ 1100$

$1 \rightarrow 1100\ 0110$

$2 \rightarrow 1110\ 0011$

$3 \rightarrow 1111\ 0001$

$AL = F1H$

Lecture

* XLAT - chapter 10 → self study

Ex:

chapter-11

string operation

DF → flag register.

String operation transfer more data DF program
inc at dec ZR.

DF = 0 , → left to right , SI+1, DI+1

DF = 1 . ↪ right to left SI-1, DI-1

SI, DI

Offset address 0200H 0201H 0202H
0203H
STRING1 DB 'ABCDE'
0204H

CLD → DF = 0 clean DF

STD → DF = 1 set DF.

MVR SB → MVR string Byte.

↓
1 byte
ignore
Non operand instructions → CLD, STD

SI, DI → offset moving a string

segment DS: SI STR1 DB 'HELLO'
ES: DI STR2 DB " DUP(3)

MVR AX, @ DATA ↑ 5 st letter

MVR DS, AX

initialize -

MVR ES, AX

LEA SI, STR1 point memory

LEA DI, STR2

left to right

MOV CX, 5
REP: MOVSB
CLD
MOVSB

LOOP REP

MVR SW → word size string

SI+2, SI+4, SI+6

SI-2, SI-4, SI-6

CT-9 → chapter 8, chapter-9

decimal

Lecture

String store - character need

Dest. — string → FS:DI.

source — AL , AX

Byte Word

STR1 'HELLO'

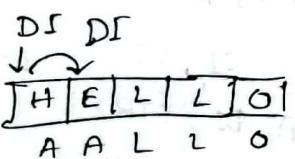
LEA DI, STR1

CLD

MOV AL, 'A'

STO SB

STOSB .



A directly DI finds
store into DI, Register
AL for store into DI

Load String

Source → string

Dest. → Register

DS:SI → AL

LODSB

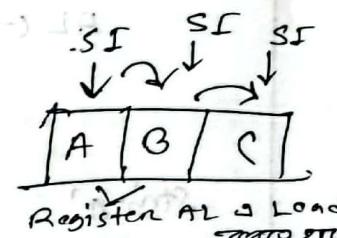
LODSW

→ AX

DF

STR1 DB 'ABC'

CLD



A

AL

B

AL

Read → DI is store into DI
Display → DI is load into DI

Display a character string.

FOR count-time DO

LOAD string ch into AL
MOV DL, AL .

Output ch .

Scan String

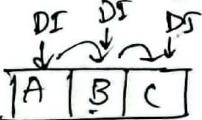
SCA SB → non operand.

SCA SW.

target byte → AL - register → character zero

AL (-) ES:DI → string (not scan zero).

ZF affected ??.



String1

target string → scan zero
character zero B zero

[B] → B address AL-ES:DI
ZF 0 यहाँ पाठी

SCASB → A-B → ZF=0

SCASB → B-B → ZF=1

string वा target
change हो ना,
असे flag affected
ZFA.

REP NZ → Repeat until not zero

REP NZ SCASB → यहाँ वास्तवically target zero
string वा control 0 जाए
counter scan ZD.

**
for counting vowels and consonants.

CT-4

Chapter-8

Initially SP → 0100h.



PUSH source → must be 16 bit register or memory word.

1. SP decreased by 2.

2. A copy of source content moved to SS:SP
Source unchanged.

PUSHF → no operands

→ pushes the contents of the FLAG register onto the stack
the stack

POP destination → must be 16 bit reg. or mem word
✓
except IP

1. The content of SS:SP moved to destination
(destination changed)
2. SP increased by 2.

Exercises

1. a) 0100h.

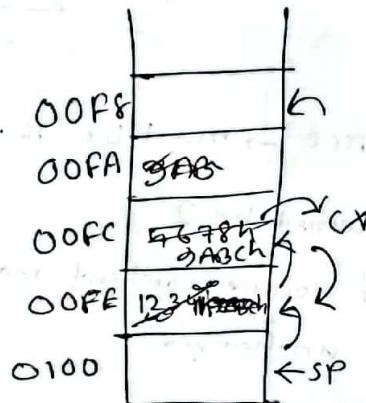
b) 100h byte for stack contains
 $100h/2 = 80h$ word.

2. AX = 1234h

BX = 5678h

CX = 9ABCCh. 00F8

SP = 100h.



XCHG AX, CX

POP CX = 5678h. AX = 9ABCCh

PUSH AX = 9ABCCh

BX = 9ABCCh.

SP = 00FE

4.

CALL PROC1

G8FD:0004 MOV AX, BX
08FD:0203h. FF H203
X8 H203

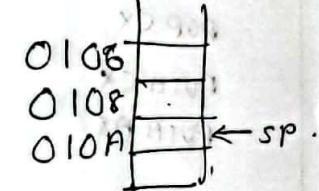
X8 H203

X8 H203

G8FD:0300h PROC1

SP = 0108h

IP = 0300h

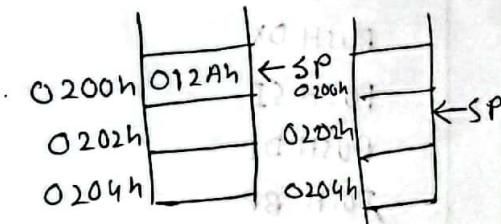


5. SP = 0200h

a) After RET

IP = 012Ah

SP = 0202h



b) RET 4

RET POP_VALUE

IP = 012Ah

SP = 0206h

SP = 0202h + 4 = 0206h

6. a) POP AX
PUSH AX

b) POP AX
POP CX
PUSH CX
PUSH AX

c) POP AX
POP BX
PUSH AX
PUSH BX

7. SAVE_REGS PROC

POP AX ; return address
PUSH BX
PUSH CX
PUSH DX
PUSH SI
PUSH DI
PUSH BP
PUSH DS
PUSH ES
PUSH AX ; return address at top.

RET

SAVE_REGS ENDP.

b) RESTORE_REGS PROC

POP AX ; save return address

POP ES

POP DS

POP BP

POP DI

POP SI

POP DX

POP CX

POP BX

PUSH AX ; top of stack is return address

RET

RESTORE_REGS ENDP.

Chapter-9

MUL source

SMUL source

Byte Form

One number → source → byte register or
memory byte.

other number → AL.

product → AX

Word Form

One number → source

other number → AX

product → DX! AX

MSB : LSB .

for positive numbers, MUL & IMUL are same.

After MUL,

0000 0000 1101 0110 → CF/OF = 0

1010 1011 0110 10 → CF/OF = 1

After IMUL,

1111 1111 1101 0110 → CF/OF = 0

$$\underline{9.1} \quad AX = 1, BX = FFFFh = 65535 \\ = -1$$

Inst.	Dec. Product	Hex product	DX	AX	CF/OF
MULBX	65535	FFFF	0000 FFFF	0000 FFFF	0
IMULBX	-1	ffff ffff	ffff ffff	ffff ffff	0

$$\underline{9.2} \quad AX = FFFFh, BX = FFFFh$$

Inst.	Dec Prod	Hex Prod	DX	AX	CF/OF
MULBX	429483625	FFFFE0001	FFFF E0001	0001	1
IMULBX	1	0000 0001	0000 0001	0000 0001	0

16	<u>9294836225</u>	1
16	<u>268427264</u>	0
16	<u>16776704</u>	0
16	<u>1048544</u>	0
16	<u>65534</u>	$14 \rightarrow F$
16	<u>4095</u>	$15 \rightarrow F$
16	<u>255</u>	$15 \rightarrow F$
16	<u>15</u>	$15 \rightarrow F$
		0

9.3 $AX = 0FFFh$

Inst.	Decimal Prod.	Hex Prod	DX	AX	CF/OF
MUL AX	16769025	00FFE001	00FF	E001	1
IMUL AX	16769025	00FFE001	00FF	E001	1

9.4 $AX = 0100h, CX = FFFFh$
 $= 256$
 $= -1$

Inst	Dec Prod	Hex Prod	DX	AX	CF/O
MUL CX	1C776960	00FFFF00	00FF	FF00	1
IMUL CX	-256	FFFF FF00	FFFF	FF00	0

9.5 $AL = 80h, BL = FFh$
 $= 128$
 $= 255$
 $1000\ 0000 = -128$
 $= -1.$

Inst	Dec Prod	Hex Prod	AH	AL	CF/OF
MUL BL	32640	7F80	7F	80	1
IMUL BL	128	0080	00	80	1

9.6

$A = 5 \times A - 12 \times B$

MOV AX, 5 ; $AX = 5$

MUL B ; $AX = 5 \times A$

MOV A, AX ; $A = 5 \times A$

Mov AX, 12 ; $AX = 12$

MUL B ; $AX = 12 \times B$

SUB A, AX ; $A = 5 \times A - 12 \times B$

9.7

FACTORIAL PROC

Mov AX, 1

TOP:

MUL BX

LOOP TOP

RET

FACTORIAL ENDP

#

DIV divisor

IDIV divisor

quotient & remainder same size as divisor

Byte form

divisor \rightarrow 8 bit reg or mem

dividend \rightarrow 16 bit \rightarrow AX

quotient \rightarrow 8 bit \rightarrow AL

remainder \rightarrow 8 bit \rightarrow AH

Word form

divisor \rightarrow 16 bit reg or mem

dividend \rightarrow 32 bit \rightarrow DX:AX

quotient \rightarrow 16 bit \rightarrow AX

remainder \rightarrow 16 bit \rightarrow DX

for signed \rightarrow remainder and dividend same sign

dividend & divisor \rightarrow positive then DIV & IDIV same

Flags undefined.

9.8

$$DX = 0000h, AX = 0005h.$$

$$Bx = 0002 \text{ h}.$$

<u>Inst</u>	<u>Dec. quo.</u>	<u>Dec. rem. Hex quo.</u>	<u>A1</u>	<u>Dx</u>
DIV BX	0002 2	1 0002	0007	
IDIV BX	2	1 0002	0001	

9.

$Dx = 0000h$, $Ax = 0005h$ misaligned

$$Bx = f \text{ for } h$$

$$\equiv -2$$

<u>Inst</u>	<u>Dec. quo.</u>	<u>Dec. rem.</u>	<u>A_X</u>	<u>D_X</u>
DIV BX	0	5	0000	0005
IDIV BX	-2	1	FFFF	0001

9.10

$$DX = ffffh \text{ (hex)} = 65535_{10}, AX = fff Bh \text{ (hex)} = -15_{10}$$

$$BX = 0002h \text{ (hex)} = 2_{10}$$

<u>Inst</u>	<u>Dec. quo.</u>	<u>Dec. rem.</u>	<u>AX</u>	<u>DX</u>
DIV BX	-2	-1	FFFF	FFFF

JDIV BX DIV DF
OVERFLOW

9.11

$$AX = 00FBh = 257$$

$$3L = ffn \approx 2\pi$$

<u>Inst</u>	<u>Dec. quo.</u>	<u>Dec. rem.</u>	<u>All</u>	<u>A/H</u>
DIV '82	0	277	0000 00	fB.

SDIV BL DIVIDE
OVERFLOW

SHOC SHOC (MAX 10) HR MM(3)
181

Exercise

1. a) $AX = 0008h, BX = 0003h$

b) $AX = 00FFh, BX = 1000h$

$$= 255, \quad 24096$$

c) $AX = 0005h, CX = FFFFh, DX = 65535$

$$= -1$$

d) $AX = 8000h, WORD1 = FFFFh$

$$= -32768$$

$$= -1$$

<u>Inst.</u>	<u>Dec prod</u>	<u>Hex prod</u>	<u>DX</u>	<u>AX</u>	<u>CF/OF</u>
--------------	-----------------	-----------------	-----------	-----------	--------------

a) MUL BX 24 00000018 0000 0018 0

b) MUL BX, 1044480 000FF000 000F F000 1.

c) MUL CX -5 FFFF FFFF FFFF FFFF 0

d) IMUL WORD1 32768 0000 8000 0000 8000 1

e) illegal

2. Inst.

		<u>AX</u>	<u>CF/OF</u>
a) MUL BL	2736	0AB0	01

b) IMUL B2

c) MUL AH (01 * A3) 00A3 00A3 0

d)

3.

a)

B

$DX = 00000h, AX = 0007h, BX = 0002h$

<u>Dec quo.</u>	<u>Dec rem.</u>	<u>AX</u>	<u>DX</u>
0003	00	0003	0001

b) $DX = 0000h, AX = FFFEH, BX = 0010h$

$$= 65534, \quad 2^{16}$$

<u>Dec quo</u>	<u>Dec rem</u>	<u>AX</u>	<u>DX</u>
4095	14	0FFF	000E

c) $DX = FFFFh, AX = FFFCh, BX = 0003h$

$$DX:AX = -4$$

<u>Dec quo</u>	<u>Dec rem</u>	<u>AX</u>	<u>DX</u>
-1	-1	000F FFFF	FFFF

d) DIVIDE OVERFLOW

$$\begin{array}{r} 3 \\ \overline{-3} \\ \hline -1 \end{array}$$

4. a) $AX = 0000h$, $BL = 03h$

Dec quo Dec rem AL AH AX
X 4 1 0001 01 0109

$AX = FFB8h$, $BL = FEh$

$= -65531$

$= -254$

Dec quo Dec rem AL AH AX
257 -253

$AX = 00FE$, $BL = 10$

AL AH
 $15 \rightarrow 0F$ $14 \rightarrow 0E$

5. a) 0000

b) FFFF

c) 0000

6. a) FFF0

b) 00FF

c) FF80

7. a) MOV AX, 5

IMUL AX

MOV A

SUB AX, 7

MOV A, AX

b) MOV AX, A

SUB AX, B

ADD B, 10

IMUL B

MOV B, AX

c) MOV AX, 9

IMUL A

MOV BX, 6

SUB BX, AX

MOV A, BX

d) MOV AX, A

IMUL AX

MOV A, AX

MOV AX, B

IMUL AX

ADD

MOV BX, AX

ADD BX, A

MOV AX, C

IMUL AX

CMPL BX, AX

JBE SET_CFL

CLC

CMPL END

SET_CFL: STC

END

$$1.(c) AX = 00005h, CX = fffffh.$$

$\Rightarrow -2$.

$$\begin{array}{r} \text{Dec op code} \\ -5 \end{array} \quad \begin{array}{r} DX \\ \text{FFFF} \end{array} \quad \begin{array}{r} AX \\ \text{FFFFB} \end{array}$$

$$2. b) AL = A3h \quad BL = 10h$$

$$= 171 \quad = 16$$

$$= 10101011$$

$$01010100$$

$$\underline{A + 1}$$

$$85 = 01010101$$

$$-85 \times 16 = \text{FFFF FAB0}$$

$$d) AL = 02h, B1 = FBh.$$

$$= 2$$

$$= 25$$

$$prod = -10$$

$$= 11111011$$

$$00000100$$

$$FF; F6$$

$$+ 1$$

$$-5 = 00000701$$

$$3.(c) DX = fffffh, AX = fffch$$

$$DX: AX = \text{FFFF EFFFFC}$$

$= -9$.

$$BX = 0003h$$

$\Rightarrow 3$.

$$\begin{array}{r} 3) -4 (-1 \\ -3 \\ \hline -1 \end{array}$$

$$\begin{array}{r} DX \\ \text{FFFF} \end{array} \quad \begin{array}{r} AX \\ \text{FFFF} \end{array}$$

$$9.b) AX = \text{FFFFB}$$

$$BL = \text{FEh}$$

$$1111\ 1111\ 1111\ 1011$$

$$0000\ 0000\ 0000\ 0100$$

$$+ 1$$

$$-5 = \overline{0000\ 0000\ 0000\ 0101}$$

$$\begin{array}{r} 1111\ 1111\ 1111\ 1010 \\ 0000\ 0000\ 0000\ 0001 \\ \hline + 1 \\ \hline -2 = 0000\ 0000\ 0000\ 0010 \end{array}$$

$$\begin{array}{r} 1111\ 1111\ 1111\ 1010 \\ 0000\ 0000\ 0000\ 0001 \\ \hline + 1 \\ \hline -2 = 0000\ 0000\ 0000\ 0010 \end{array}$$

$$\begin{array}{r} 1111\ 1111\ 1111\ 1010 \\ 0000\ 0000\ 0000\ 0001 \\ \hline + 1 \\ \hline -2 = 0000\ 0000\ 0000\ 0010 \end{array}$$

$$\begin{array}{r} AH \\ -1 \end{array} \quad \begin{array}{r} AL \\ 2 \\ \hline FF \end{array} \quad \begin{array}{r} AL \\ 02 \end{array}$$

$$\begin{array}{r} 1111\ 1111\ 1111\ 1010 \\ 0000\ 0000\ 0000\ 0001 \\ \hline + 1 \\ \hline -2 = 0000\ 0000\ 0000\ 0010 \end{array}$$

Lecture

Q) Compare string

CMPSB

CMPSW

DS:SI ~~0000~~

\hookrightarrow ES:DI

same ZF = 0

STR1 DB 'AED'
 SI
 SS
 ↓
 DI

STR2 DB 'ABC'
 DI
 ↑
 DI

CLD ; left to right

CMPSB

A - A = 0, ZF = 1.

CLD

CMPSB

C - B
 - 43H - 42H = 1

/ REPZ

condition REPZ

Compare string \rightarrow target string \Rightarrow substring
 base address.

SUB1 DB 'ABC'
 SI
 SS
 ↓
 DI

SUB2 DB 'CAB'

MAINST DB 'AB ABCA'

↑
 DI
 DI

ABC

AB ABCA

↑
 DI
 DI

ABC

AB ABCA

↑
 DI
 DI

AB ABCA

↑
 DI
 DI

STOP = MAINST + length_MAINST - length_subst

offset address

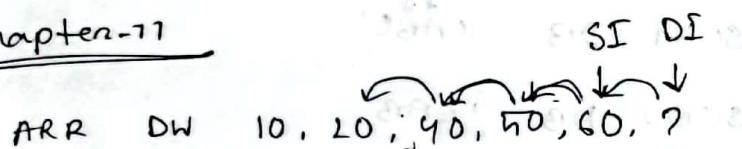
= MAINST + 6 - 3

\Rightarrow MAINST + 3

AB ABCA
 M MH MH MH MH MH

hardware / Architecture related

Chapter-71



STD

LEA SI, ARR+8h

LEA DI, ARR+Ah.

If DF = 0 , SI, DI increments
DF = 1 , SI, DI decrements.

MOVSB → Source → DS:SI
Destination → ES:DI

STOSB → Source → AL / AX
Destination → ES:DI

LODSB → Source → DS:SI
Destination → AL / AX

SCASB → Source → AL / AX
Destination → ES:DI

AL - DI

LODSB → loads byte in DS:SI
SCASB → scans byte in ES:DI

CMPSB → Source DS:SI → Destination ES:DI

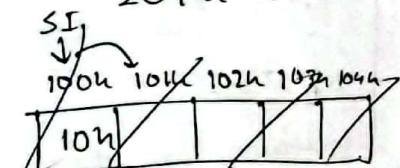
Exercise

1. SI contains 100h
DI contains 200h
AX contains 4142h

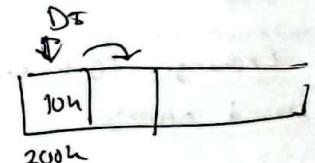
DF = 0

CLD

100h → 10h
101h → 15h
200h → 20h
201h → 25h



- a) MOVSB . → copy
SI → 101h → 15h
DI → 201h → 25h



- b) MOV SW

c) STOSB
Source = AL
DI = 42h → 290h

- d) STOSW

Source = AX
DI = 4142h

- e) LODSB

28

Chapter-10

LINE DB 5,4,3 DUP(2,3 DUP(0),1)

LINE DB 5,4,2,0,0,0,1,2,0,0,0,1,2,0,0,0,1

location of array elements

position

1

2

3

.

N

Location

A

$A = 1 \times S$

$A = 2 \times S$

,

:

$A = (N-1) \times S$

Ex10'1

Exchange 10th and 29th elements in a word array.

$$W + 9 \times 2 = W + 18$$

$$W + 29 \times 2 = W + 48$$

MOV AX, W+18

XCHG W+48, AX

MOV W+18, AX.

#

Addressing

i) register mode \rightarrow operand register

ii) immediate mode \rightarrow " constant

iii) direct mode \rightarrow " variable.

MOV AX, 0

$\begin{cases} \text{source. immediate mode} \\ \text{dest. register mode} \end{cases}$

MOV ALPHA, AX

$\begin{cases} \text{source register mode} \\ \text{dest. direct mode.} \end{cases}$

#

Register Indirect Mode \rightarrow acts as pointer to the mem loc.

BX, SI, DI \rightarrow operand's segment number in DS

BP \rightarrow " " " in SS

SI contains 0100h \rightarrow 1234h

MOV AX, [SI] \rightarrow 1234h

MOV AX, SI \rightarrow 0100h [register]

10.2

	<u>source offset</u>	<u>result</u>
a)	1000h	1BACH
b)	2000h	20FFh must be BX, SI, DI
c)	illegal	mem-mem add
d)	illegal	
e)	3000h	0316h

10.3

Based & Indexed Mode

offset address is obtained by adding a number called displacement

MOV AX, W[BX] → register
↳ displacement

MOV AX, [W+BX]

MOV AX, [BX+W]

MOV AX, W+[BX]

MOV AX, [BX]+W

MOV AX, 2[SI]

MOV AX, [SI+2]

BX or BP → Based

SI or DI → Indexed

10.4

	<u>Source offset</u>	<u>result</u>
i.	[ALPHA+2]	0456h
ii.	BX+2	2BACH
	2+2 = 4	
iii.	ALPHA+4	0789h
iv.	-2[SI] [SI-2] = 4-2=2	1084h
v.	[ALPHA+4]	0789h
vi.	illegal	
vii.	illegal	

PTR operator

MOV AH, 1 ✓

MOV AX, 1 ✓

MOV [BX], 1 X

MOV BYTE PTR [BX], 1

MOV WORD PTR [BX], 1

Using PTR to override a type

type PTR address_expression

LABEL Pseudop.

10.9

a) illegal

b) 7

c) 0BC9Ah

d) 5678h

e) 9Ah

f) 0BC9Ah

#

Segment override.

segment_register : [pointer_register]

MOV AX, ES:[SI]

MOV AX, DS:[DI]

#

Accessing stack

BP → SS

MOV BP, SP → BP points
to stack top

MOV AX, [BP]

MOV BX, [BP+2]

MOV CX, [BP+4]

Two dimensional Array

memory \rightarrow one dimensional

so, two dim. array elements must be stored sequentially.

i. Row major order $row_1 - row_2 - row_3$

ii. Col major order. $col_1 - col_2 - col_3$

Locating an element in an array

i. Row major order - MXN array

①

$Row_1 \rightarrow A$ $M = \text{row}$

$N = \text{col}$

$Row_2 \rightarrow A + N \times S$

$Row_3 \rightarrow A + 2 \times N \times S$ $S = 1 \rightarrow \text{byte}$

$Row_4 \rightarrow A + 3 \times N \times S$ $S = 2 \rightarrow \text{word}$

\vdots

$Row_i \rightarrow A + (i-1) \times N \times S$

②

1. Row major \rightarrow

$A[i,j] \rightarrow A + ((i-1) \times N + (j-1)) \times S$

2. Col major \rightarrow

$A[i,j] \rightarrow A + ((i-1) + (j-1) \times N) \times S$

1. $S = 2 \rightarrow \text{word}$

Row i begins, $A[i,j] = A[i,1]$

$A + (i-1) \times N \times 2$

2. col j begins, $A[1,j]$

$A + (j-1) \times 2$

3. N columns, $2 \times N$ bytes between elements.

Based Indexed Addressing Mode

variable [base-reg] + [index-reg]

[base-reg + index-reg + variable + constant]

variable [base-reg + index-reg + constant]

constant [base-reg + index-reg + variable]

MOV AX, W[BX][SI]

MOV AX, [W+BX+SI] \rightarrow MOV AX[W+6]

MOV AX, W[BX+SI]

$BX(4-1) + 4$

$(4-1) \times 4 + 4$

$BX(4-1) + 4$

MOV AX, W[2, constant] \rightarrow

10.13

$7 \times 7 \rightarrow \text{word}$
MXN.

now major order.

1) clear now 3.

$$A + (3-1) \times 7 \times 2$$

$$\rightarrow A + 28.$$

MOV BX, 28

MOV CX, 7

MOV A[BX][SI], 0

then SI + 2

2) clear col 4

$$A + (4-1) \times 2$$

$$= A + 6 \rightarrow \text{col } 4, \text{ Row } 1.$$

$$= A + 6 + 2 \times 7 \rightarrow \text{col } 4, \text{ Row } 2$$

$$= A + 20$$

$$= A + 20 + 2 \times 7 \rightarrow \text{col } 4, \text{ Row } 3$$

$$= A + 34$$

$$= A + 34 + 2 \times 7 \rightarrow \text{col } 4, \text{ Row } 4$$

$$= A + 34 + 2 \times 7 + 2 \times 7 \rightarrow \text{col } 4, \text{ Row } 4$$

$$= A + 65$$

	A	A+2	A+4	A+6	A+8	A+10
1						
2						
3						
4						
5						
6						
7						

~~XLAT~~ instructions

no operand instruction.

to convert byte value into
another value.

byte value \rightarrow AL

offset address of conversion table \rightarrow BX

Convert 0Ch to 'C'

MOV AL, 0Ch

LEA BX, TABLE

XLAT -



TABLE + Ch \rightarrow

TABLE + 12.

043h = C

Exercise

a) ~~legal~~; DI = 1500h

b) ~~legal~~; DI = 0200h

c) legal; AX = 0900h + 0150h
 $= 0650h$

d) legal; BX = 1000h - 0200h
 $= -1000h$
 $= 0600h$

e) legal; BX = BX + BE7A + BX
 $= 1000h + 1000h$
 $= 2000h$

f) illegal; mem-mem

g) illegal

h) illegal

i) $AX = [BX + DI + BE7A]$
 $= [1000 + 2000 + 1000]$
 $= [4000h]$
 $= 0300h$

2. a) legal, AH = 01h

b) AX = 0504h

c) AX = 'BA'

d) illegal

e) legal; AH = 'A'

3. a) MOV BP, SP

Mov [BP], 0

Mov [BP+2], 0.

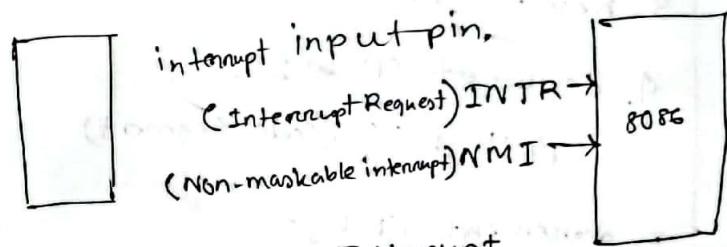
b)

Lecture

8086 Pin Diagram

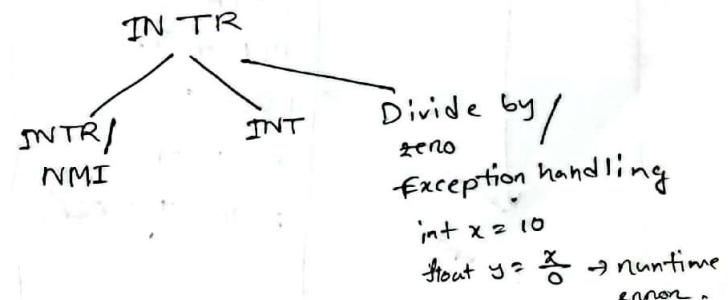
Hall - Chapter 8

8086 Interrupts & Interrupt Applications



INTR/NMI from External interrupt → Hardware interrupt

INT from program or software interrupt → Software interrupt



int x = 10
float y = $\frac{x}{0}$ → runtime error

1. decrement SP by 2 , PUSH → flag register

2. disable INTR input, IF clean
area PRB, IF = 0/Clear.

3. Reset → TF (Trap Flag)

4. decrement SP by 2 .

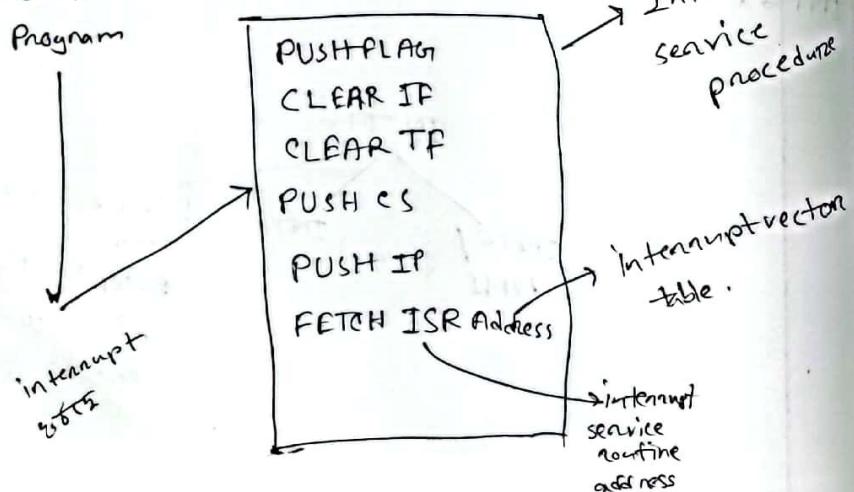
PUSH → CS (Code Segment)

5. decrement SP by 2 .

PUSH → IP

6. Jump → Start of procedure

Mainline
Program



Interrupt service
procedure
PUSH register .
POP register



interrupt → چه کاری ؟