PIN DIAGRAM OF 8086

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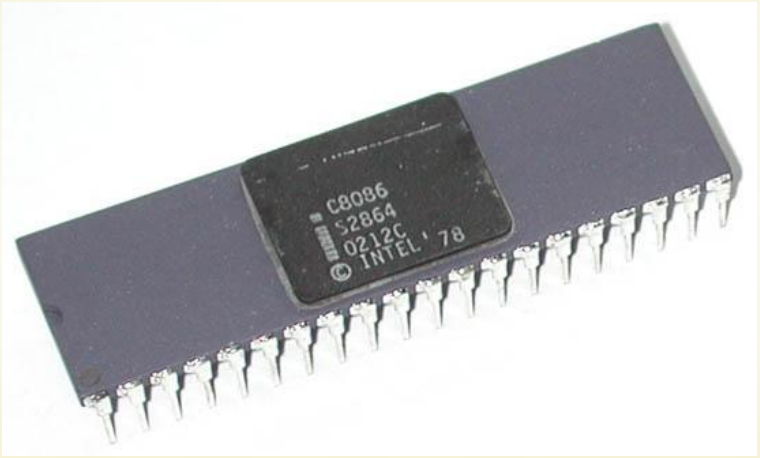
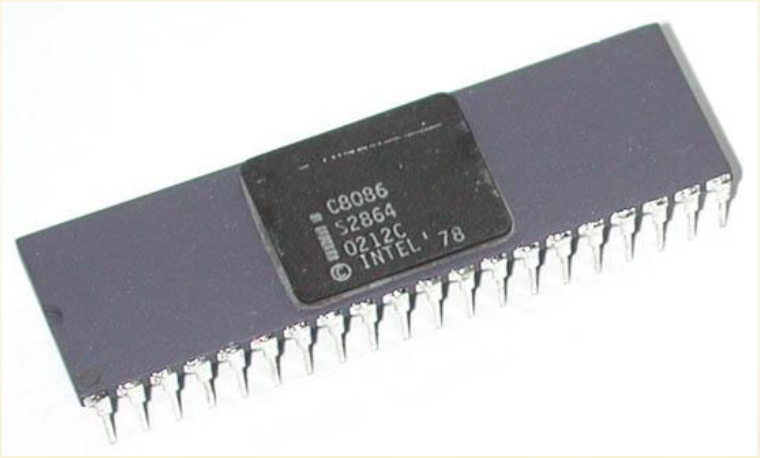
RUET

Intel 8086



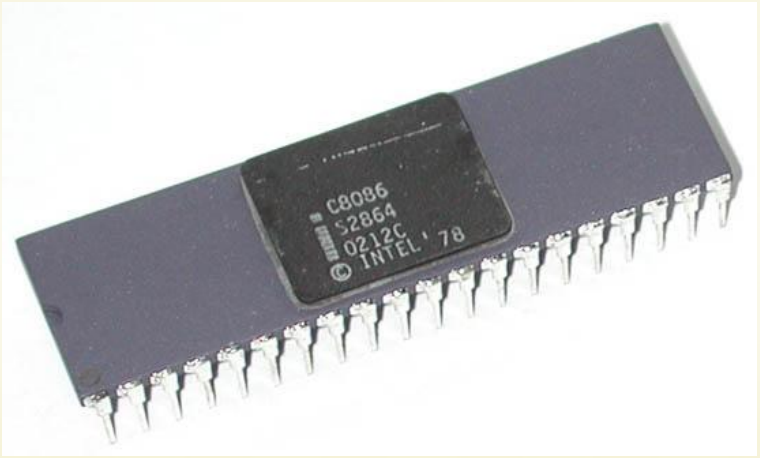
- Intel 8086 was launched in 1978.
- It was the first 16-bit microprocessor.
- This microprocessor had major improvement over the execution speed of 8085.
- It is available as 40-pin Dual-Inline-Package (DIP).

Intel 8086



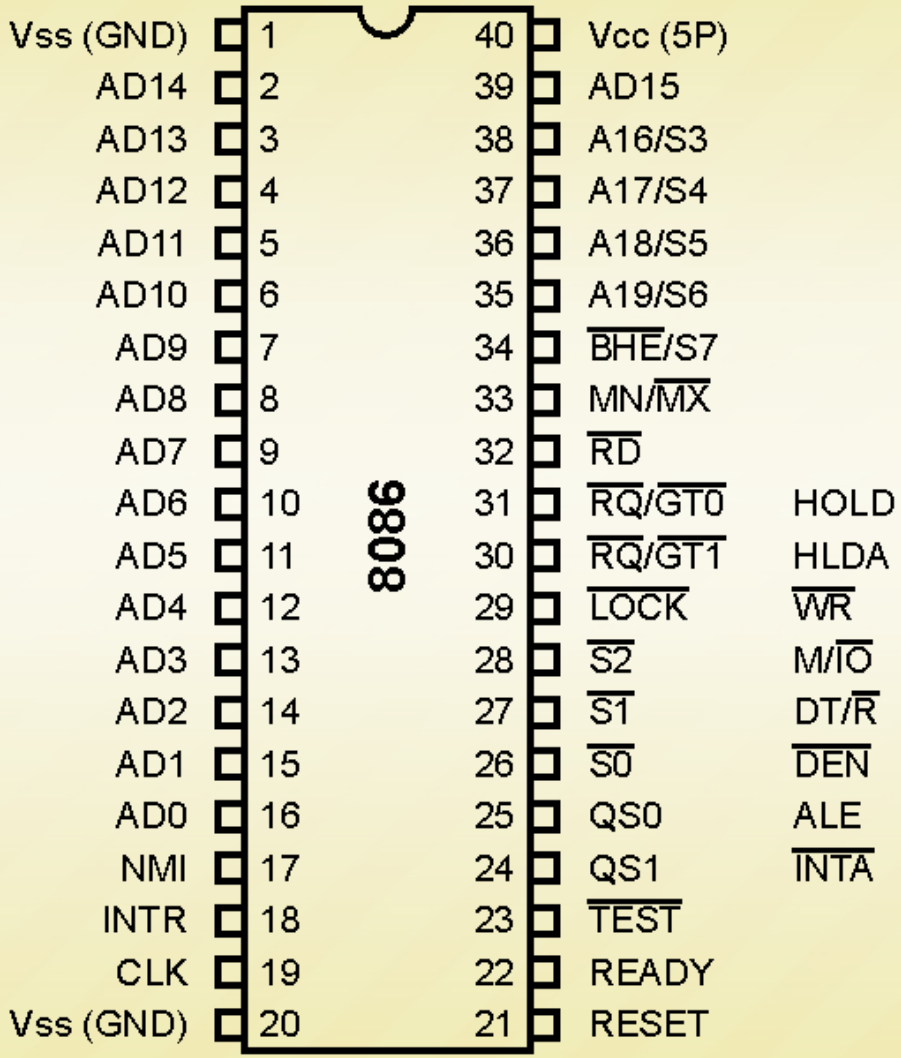
- It is available in three versions:
  - 8086 (5 MHz)
  - 8086-2 (8 MHz)
  - 8086-1 (10 MHz)
- It consists of 29,000 transistors.

Intel 8086



- It has a 16 line data bus.
- And 20 line address bus.
- It could address up to 1 MB of memory.
- It has more than 20,000 instructions.
- It supports multiplication and division.

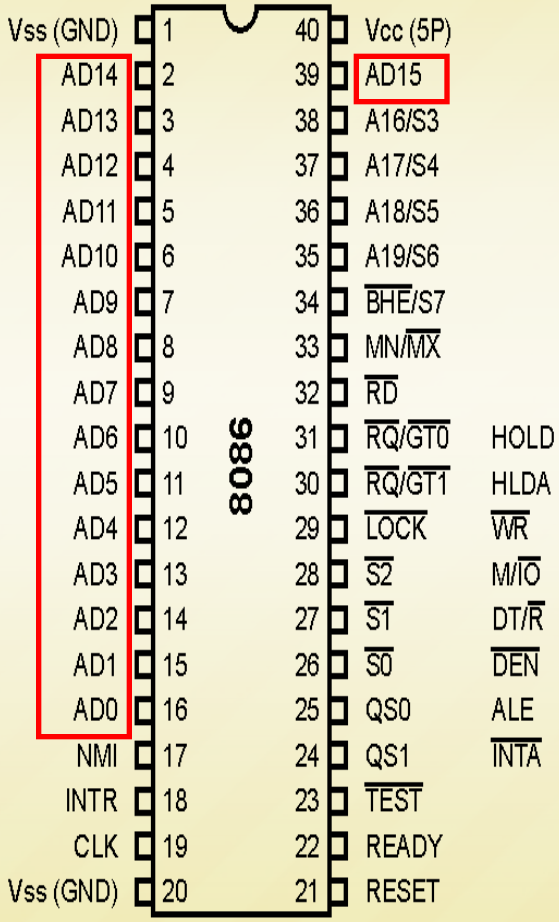
Pin Diagram of Intel 8086



$AD_0 - AD_{15}$

Pin 16-2, 39 (Bi-directional)

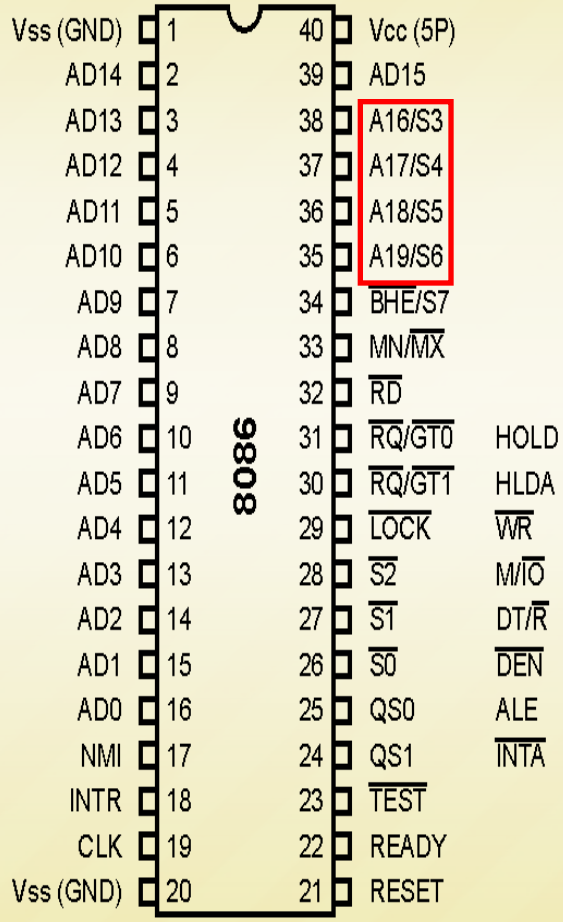
- These lines are multiplexed bi-directional address/data bus.
- During T_1, they carry lower order 16-bit address.
- In the remaining clock cycles, they carry 16-bit data.
- AD_0-AD_7 carry lower order byte of data.
- AD_8-AD_{15} carry higher order byte of data.



A_{19}/S_6, A_{18}/S_5, A_{17}/S_4, A_{16}/S_3

Pin 35-38 (Unidirectional)

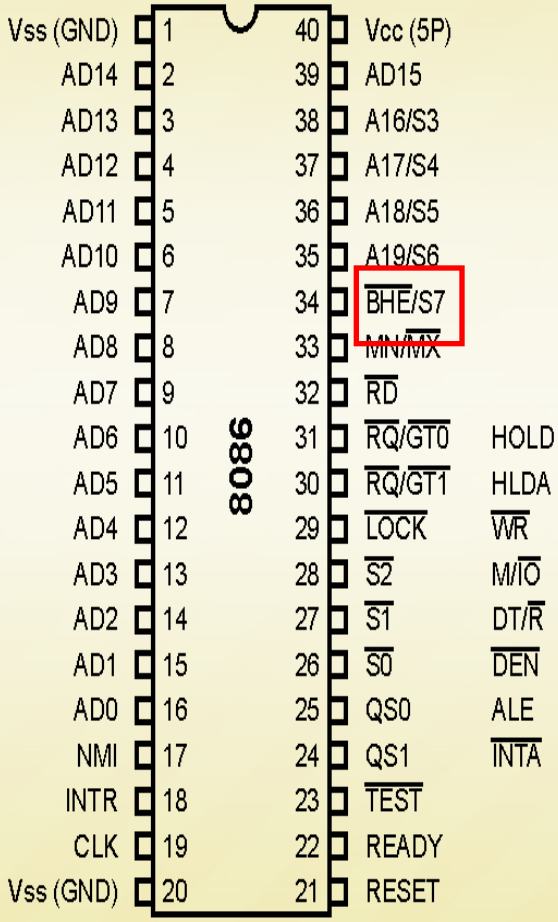
- These lines are multiplexed unidirectional address and status bus.
- During T_1, they carry higher order 4-bit address.
- In the remaining clock cycles, they carry status signals.



$\overline{BHE}$ / S_7

Pin 34 (Output)

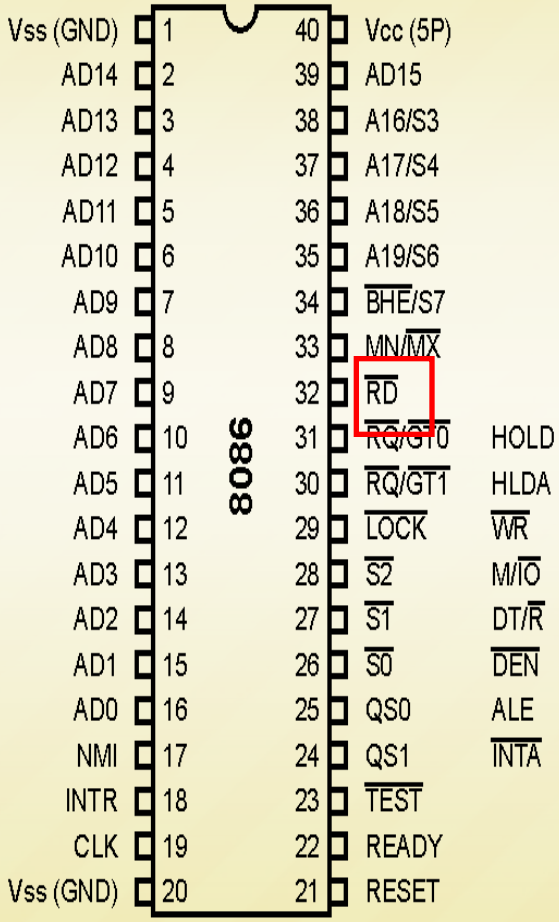
- BHE stands for Bus High Enable.
- BHE signal is used to indicate the transfer of data over higher order data bus (D_8 – D_{15}).
- 8-bit I/O devices use this signal.
- It is multiplexed with status pin S_7.



$\overline{RD}$ (Read)

Pin 32 (Output)

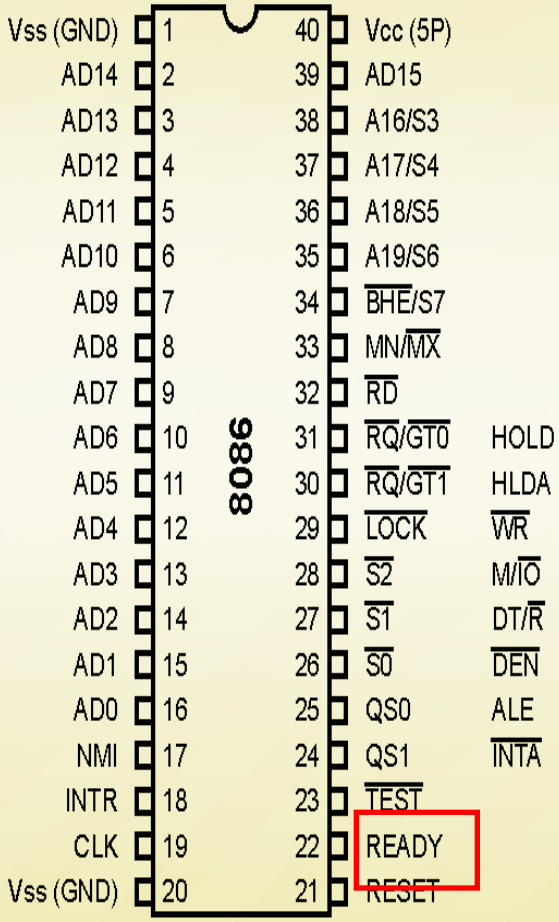
- It is a read signal used for read operation.
- It is an output signal.
- It is an active low signal.



READY

Pin 22 (Input)

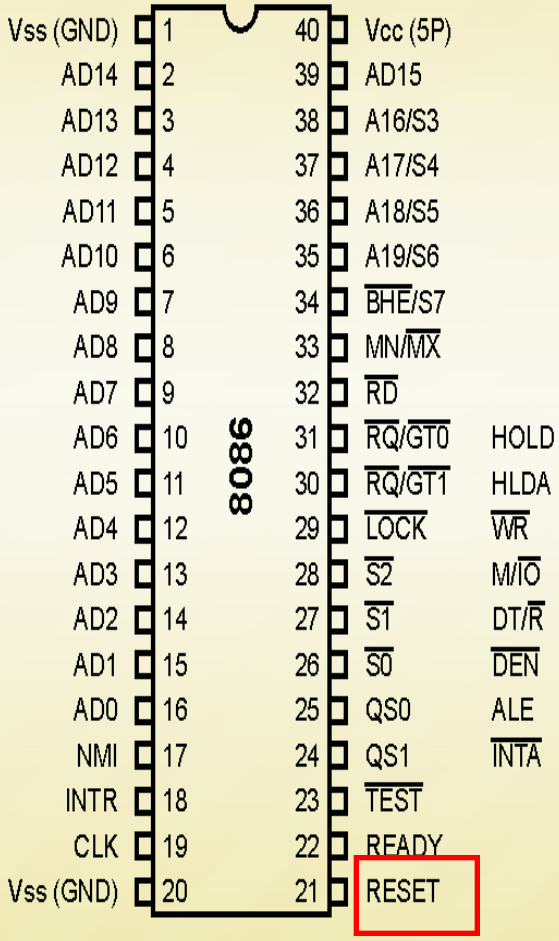
- This is an acknowledgement signal from slower I/O devices or memory.
- It is an active high signal.
- When high, it indicates that the device is ready to transfer data.
- When low, then microprocessor is in wait state.



RESET

Pin 21 (Input)

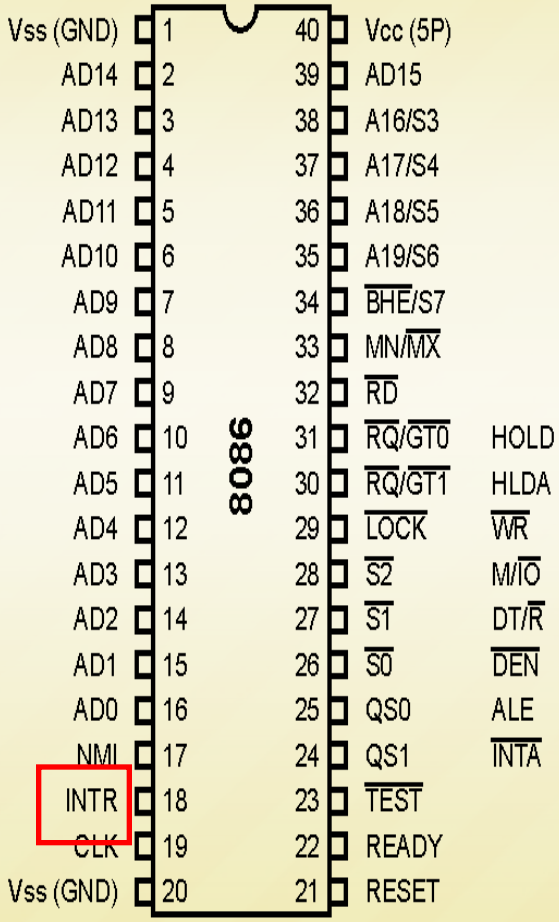
- It is a system reset.
- It is an active high signal.
- When high, microprocessor enters into reset state and terminates the current activity.
- It must be active for at least four clock cycles to reset the microprocessor.



INTR

Pin 18 (Input)

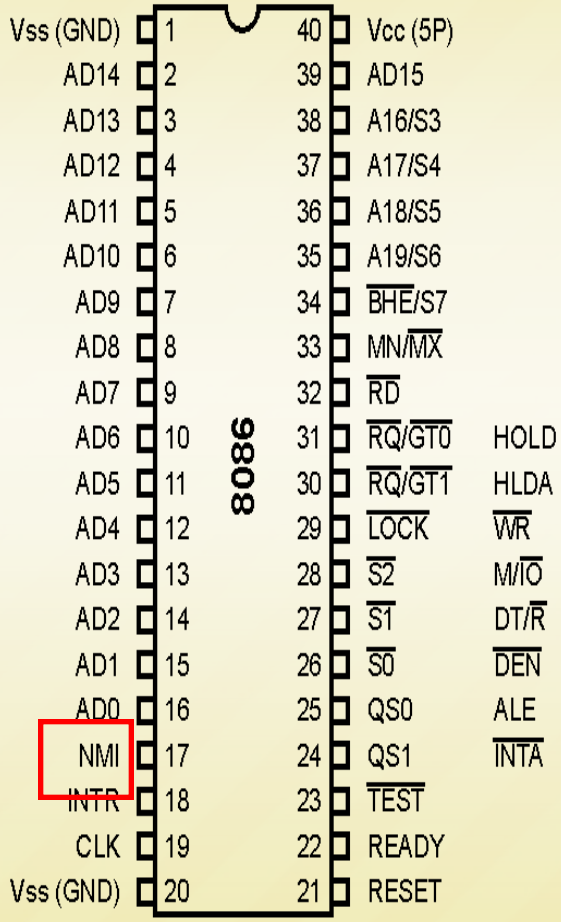
- It is an interrupt request signal.
- It is active high.
- It is level triggered.



NMI

Pin 17 (Input)

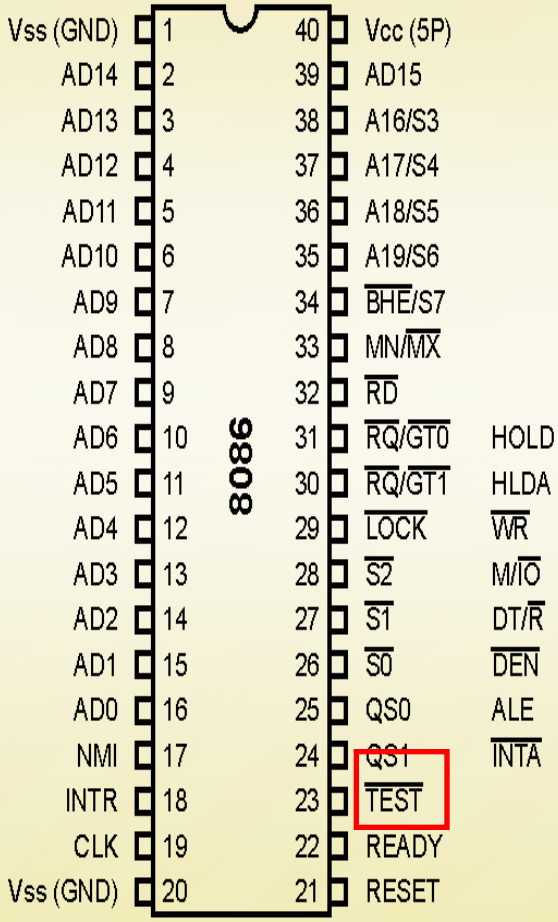
- It is a non-maskable interrupt signal.
- It is an active high.
- It is an edge triggered interrupt.



$\overline{\text{TEST}}$

Pin 23 (Input)

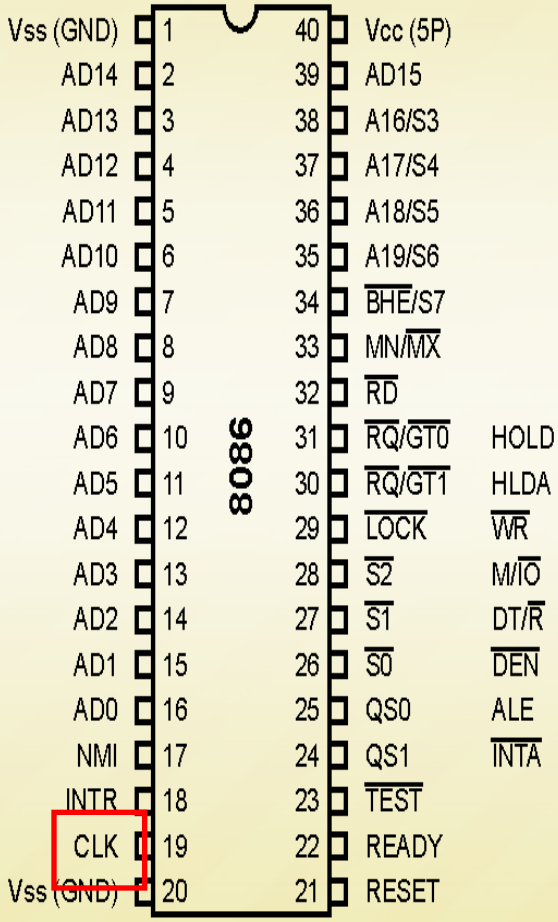
- It is used to test the status of math co-processor 8087.
- The $\overline{\text{BUSY}}$ pin of 8087 is connected to this pin of 8086.
- If low, execution continues else microprocessor is in wait state.



CLK

Pin 19 (Input)

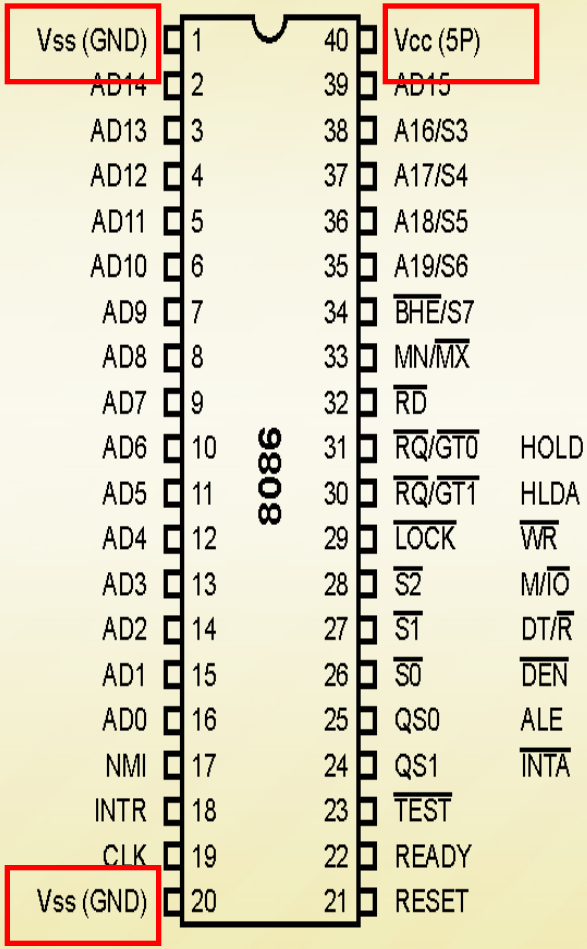
- This clock input provides the basic timing for processor operation.
- It is symmetric square wave with 33% duty cycle.
- The range of frequency of different versions is 5 MHz, 8 MHz and 10 MHz.



V_{CC} and V_{SS}

Pin 40 and Pin 20 (Input)

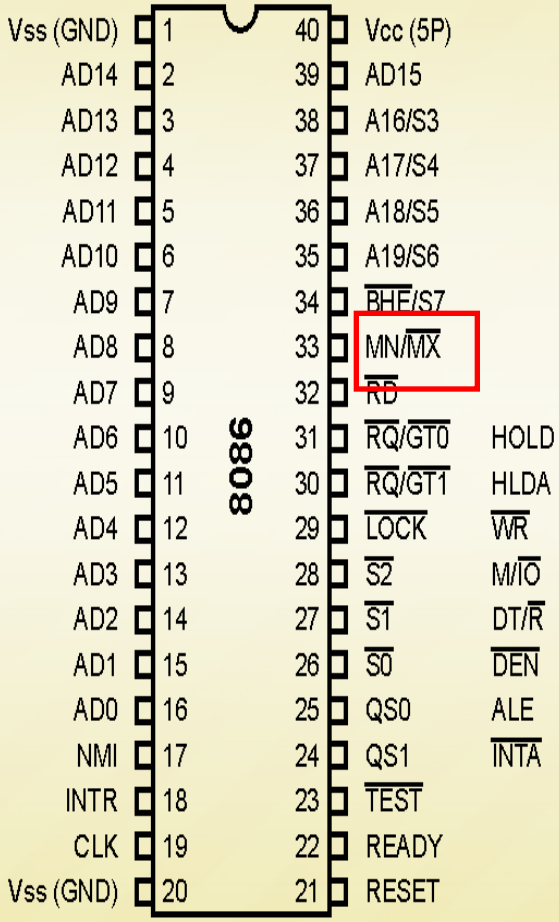
- V_{CC} is power supply signal.
- +5V DC is supplied through this pin.
- V_{SS} is ground signal.



MN / $\overline{MX}$

Pin 33 (Input)

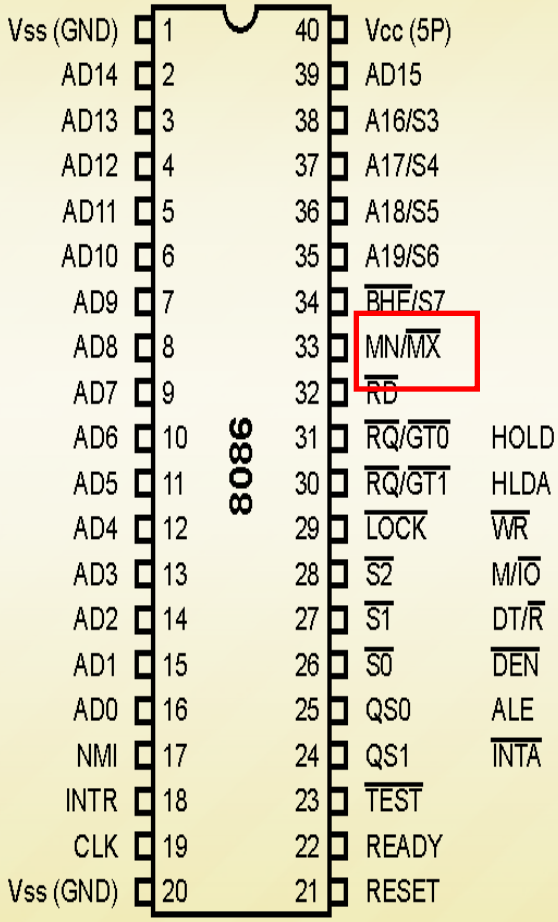
- 8086 works in two modes:
  - Minimum Mode
  - Maximum Mode
- If MN/$\overline{MX}$ is high, it works in minimum mode.
- If MN/$\overline{MX}$ is low, it works in maximum mode.



MN / $\overline{\text{MX}}$

Pin 33 (Input)

- Pins 24 to 31 issue two different sets of signals.
- One set of signals is issued when CPU operates in minimum mode.
- Other set of signals is issued when CPU operates in maximum mode.

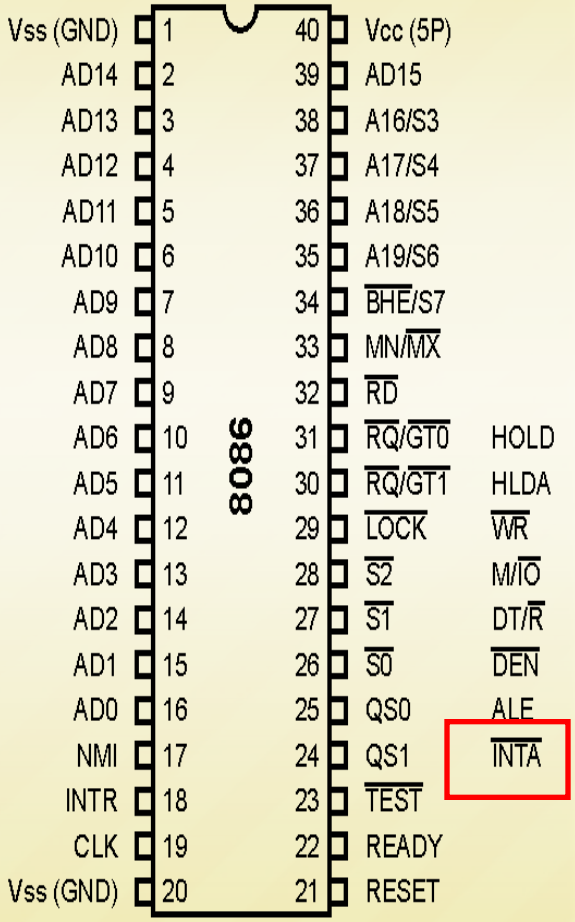


Pin Description for Minimum Mode

$\overline{\text{INTA}}$

Pin 24 (Output)

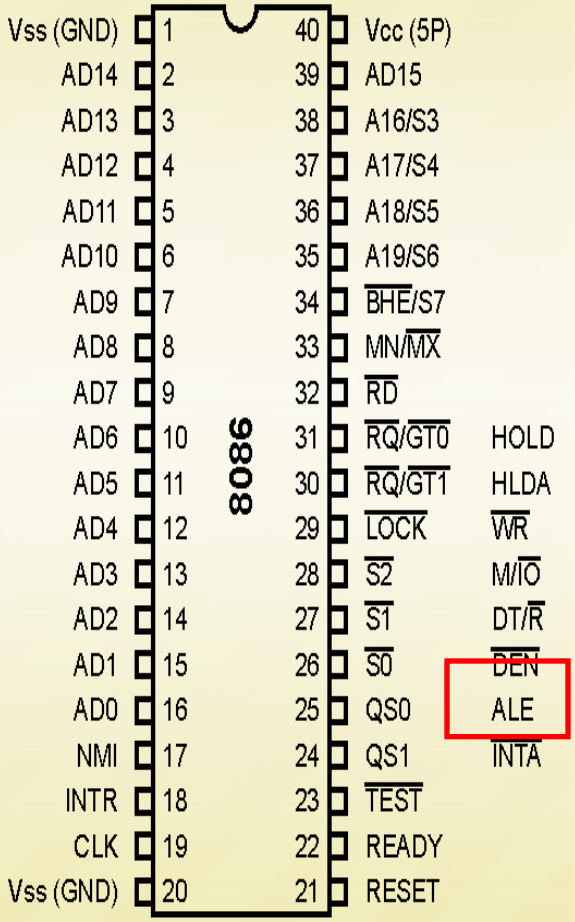
- This is an interrupt acknowledge signal.
- When microprocessor receives INTR signal, it acknowledges the interrupt by generating this signal.
- It is an active low signal.



ALE

Pin 25 (Output)

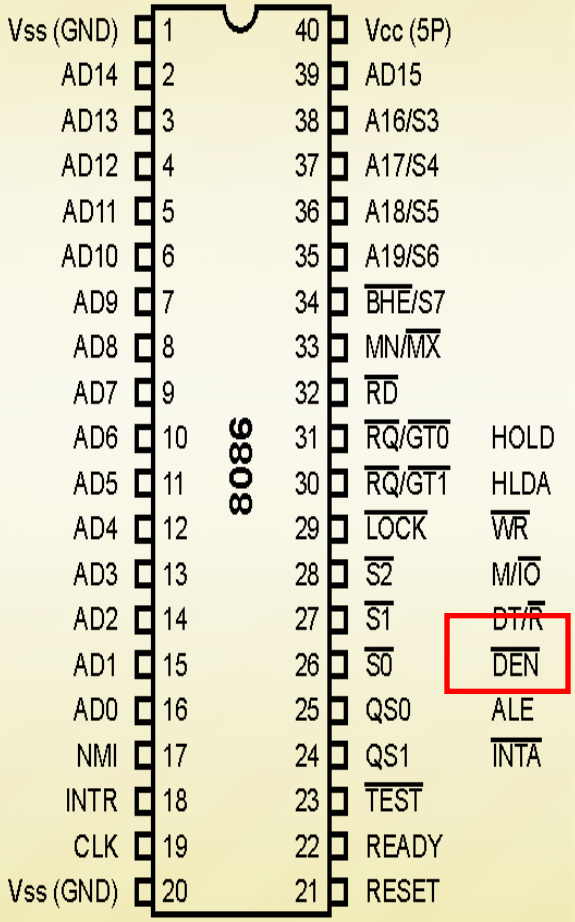
- This is an Address Latch Enable signal.
- It indicates that valid address is available on bus AD_0 – AD_{15}.
- It is an active high signal and remains high during T_1 state.
- It is connected to enable pin of latch 8282.



$\overline{\text{DEN}}$

Pin 26 (Output)

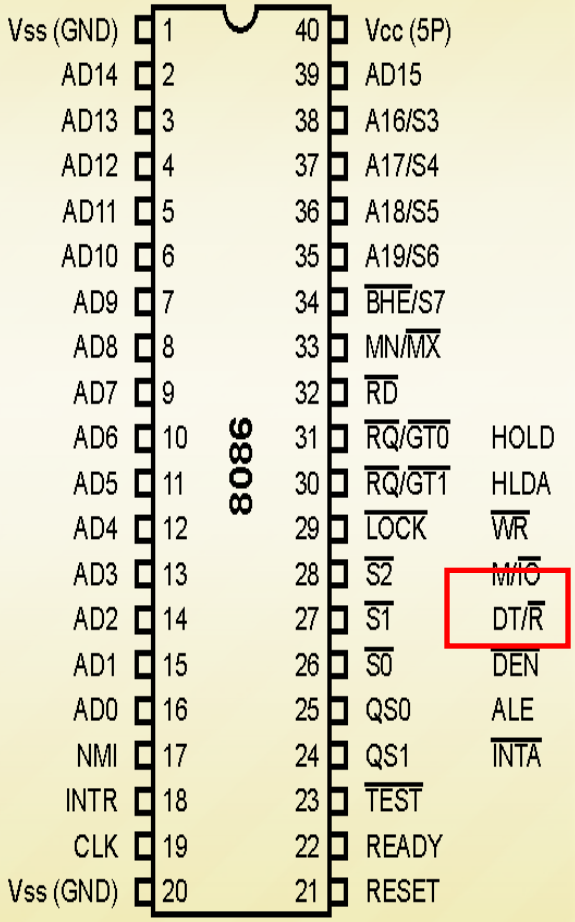
- This is a Data Enable signal.
- This signal is used to enable the transceiver 8286.
- Transceiver is used to separate the data from the address/data bus.
- It is an active low signal.



DT / $\overline{R}$

Pin 27 (Output)

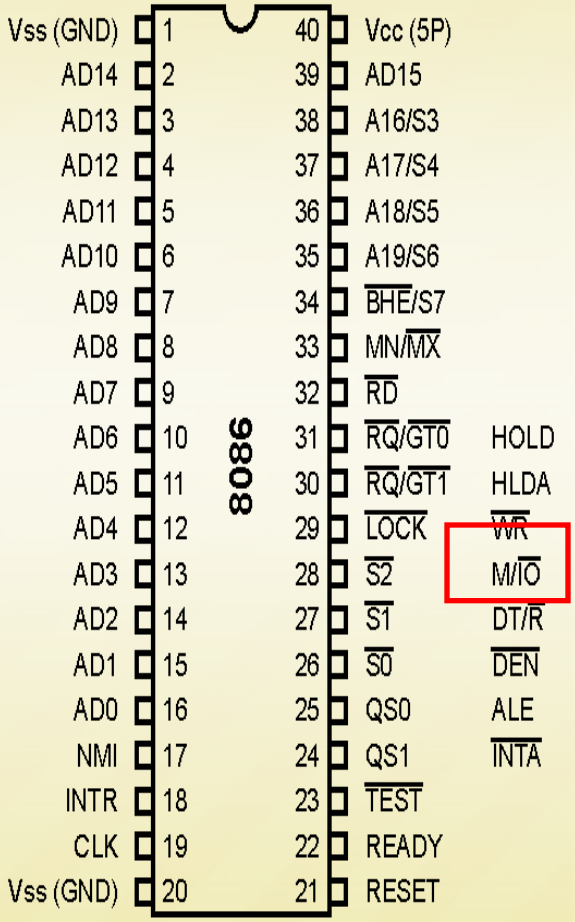
- This is a Data Transmit/Receive signal.
- It decides the direction of data flow through the transceiver.
- When it is high, data is transmitted out.
- When it is low, data is received in.



M / $\overline{IO}$

Pin 28 (Output)

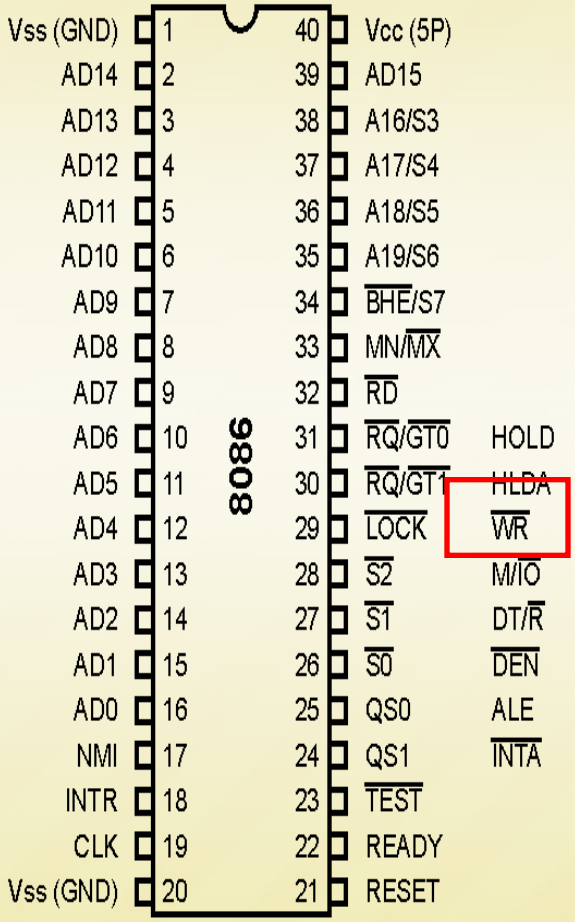
- This signal is issued by the microprocessor to distinguish memory access from I/O access.
- When it is high, memory is accessed.
- When it is low, I/O devices are accessed.



$\overline{WR}$

Pin 29 (Output)

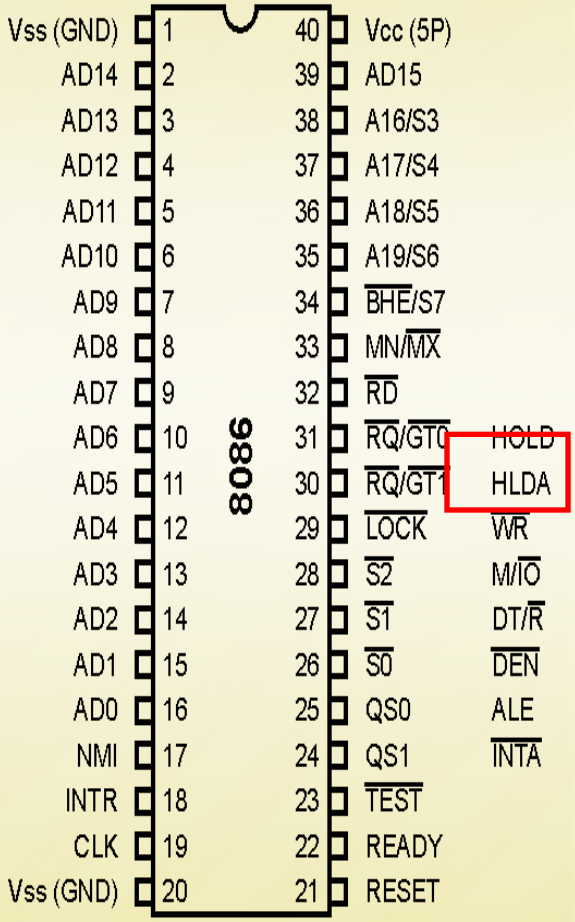
- It is a Write signal.
- It is used to write data in memory or output device depending on the status of $M/\overline{IO}$ signal.
- It is an active low signal.



HLDA

Pin 30 (Output)

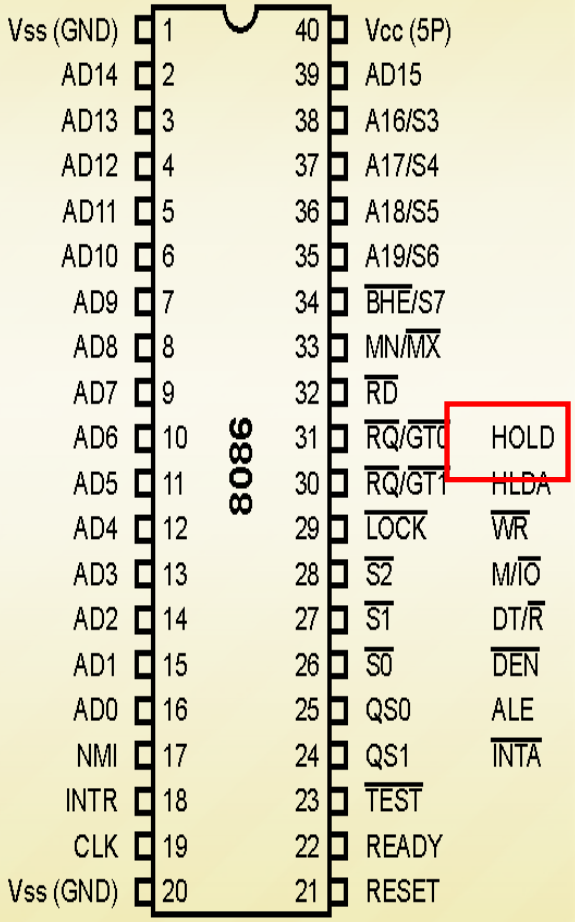
- It is a Hold Acknowledge signal.
- It is issued after receiving the HOLD signal.
- It is an active high signal.



HOLD

Pin 31 (Input)

- When DMA controller needs to use address/data bus, it sends a request to the CPU through this pin.
- It is an active high signal.
- When microprocessor receives HOLD signal, it issues HLDA signal to the DMA controller.



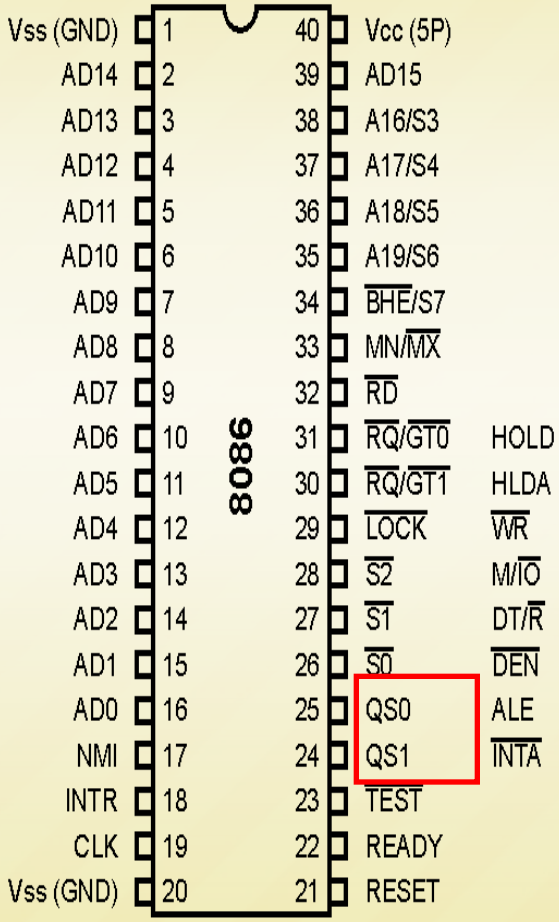
Pin Description for Maximum Mode

QS_1 and QS_0

Pin 24 and 25 (Output)

- These pins provide the status of instruction queue.

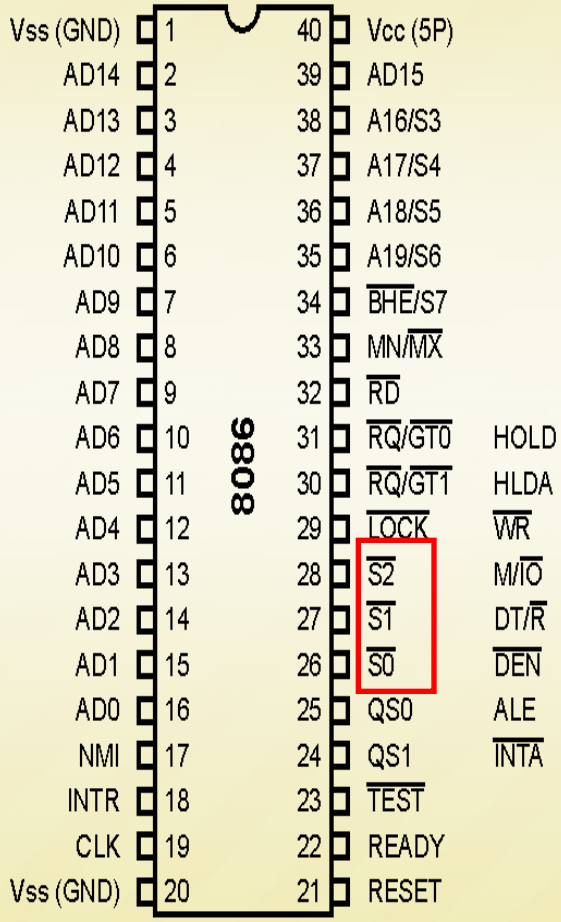
QS_1	QS_0	Status
0	0	No operation
0	1	1st byte of opcode from queue
1	0	Empty queue
1	1	Subsequent byte from queue



$\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$

Pin 26, 27, 28 (Output)

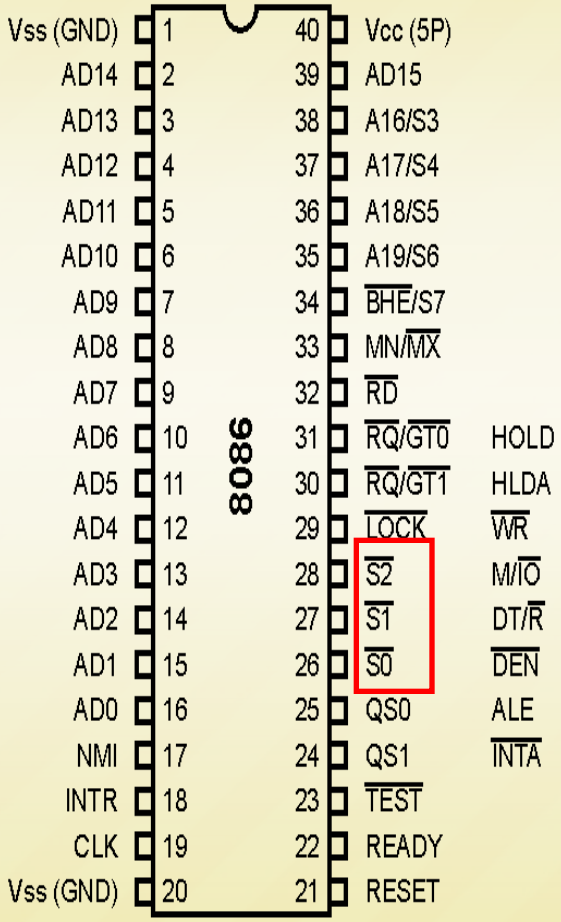
- These status signals indicate the operation being done by the microprocessor.
- This information is required by the Bus Controller 8288.
- Bus controller 8288 generates all memory and I/O control signals.



$\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$

Pin 26, 27, 28 (Output)

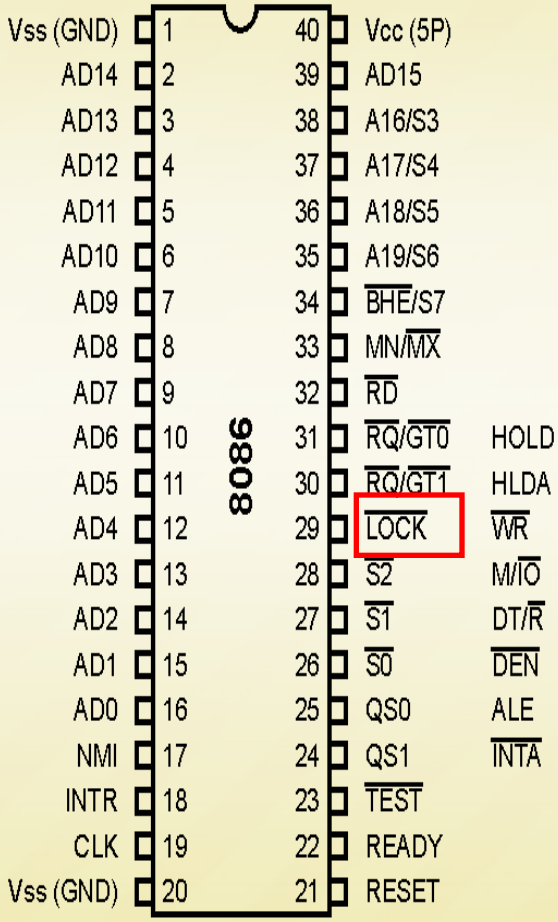
$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	Status
0	0	0	Interrupt Acknowledge
0	0	1	I/O Read
0	1	0	I/O Write
0	1	1	Halt
1	0	0	Opcode Fetch
1	0	1	Memory Read
1	1	0	Memory Write
1	1	1	Passive



LOCK

Pin 29 (Output)

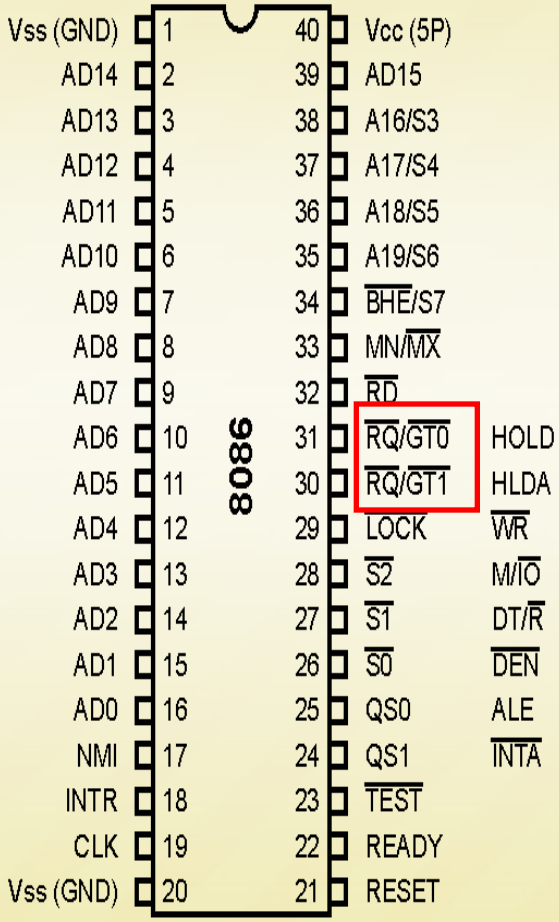
- This signal indicates that other processors should not ask CPU to relinquish the system bus.
- When it goes low, all interrupts are masked and HOLD request is not granted.
- This pin is activated by using LOCK prefix on any instruction.



$\overline{RQ/GT}_1$ and $\overline{RQ/GT}_0$

Pin 30 and 31 (Bi-directional)

- These are Request/Grant pins.
- Other processors request the CPU through these lines to release the system bus.
- After receiving the request, CPU sends acknowledge signal on the same lines.
- $\overline{RQ/GT}_0$ has higher priority than $\overline{RQ/GT}_1$.



Thank You 

Have a Nice Day