

1603020

\* How does the CPU implement a conditional jump?

Ans: To implement a conditional jump the CPU looks at the FLAGS register.

If the conditions for the jump are true, then the CPU adjusts the IP to point to the destination label so that the instruction in this level will be done next.

If the jump conditions is false, then IP is not altered, this means the next instruction in line will be done.

\* Explain the function of the following:

- (i) Debugger (ii) Linker (iii) Assembler

Ans:

(i) Debugger: Debugger is used to test and debug programs. The debugger allows a user to test a program step by step, so that the problem points or steps can be identified and rectified.

(ii) Linker: Linker takes one or more object files generated by a compiler and combines them into one.

(iii) Assembler: The assembler translates each assembly language statements into a single machine instruction.

In other words, the assembler ensures that the CPU can execute the program instructions.

\* What are the differences between NEAR and FAR procedure?

Ans:

NEAR procedure	FAR procedure
(1) A NEAR procedure can only be called by procedures residing in the same segment.	(1) A FAR procedure can be called by procedures residing in any segment.
(2) A NEAR procedure call replaces the old IP with new IP.	(2) A far procedure call replaces the old CS:IP with new CS:IP.
(3) It is also called intra-segment procedure	(3) It is also called inter-segment procedure call

intra

↑  
inter

\* What is the basic difference between AND and TEST instruction?

Ans:

AND	TEST
(1) The destination content changes at the end of AND operation according to the calculated result from the operation.	(1) The destination content never changes at the end of a TEST operation though TEST is a kind of AND operation.
(2) AND operation is used to clear or preserve particular individual bits of a bit string.	(2) TEST operation is used to clear & examine particular bits of a byte

\* Translate the following high-level language assignment statement into assembly language. A, B and C are word variables.

$$B = 3 \times B + 7 - A$$

Ans:

```
MOV AX, 3 ; AX gets 3  
IMUL B ; AX gets 3B  
ADD AX, 7 ; AX gets 3B+7  
SUB AX, A ; AX gets 3B+7-A  
MOV B, AX ; B gets 3B+7-A
```

\* How many cores are available in the following processor family

- (i) Core i3 (ii) Core i5 (iii) Core i7

Ans: (i) two

(ii) four

(iii) four (six or eight in some)

\* Explain the purpose of the following pin of 8086 (i) NMI (ii) M/I/O (iii) TEST (iv) A/D

Ans: (i) NMI: NMI stands for non-maskable interrupt which is a hardware interrupt pin. It is an edge triggered input, which causes an interrupt request to the microprocessor.

(ii) M/I/O: This is used to distinguish between memory and I/O operations. When it is high, it indicates I/O operation and when it is low it indicates memory operation.

(iii) TEST: The TEST pin is an input tested by the WAIT instruction. If TEST is at logic 0, the WAIT for instruction functions as a NOP. If TEST is at logic 1, the WAIT instruction causes 8086 to be idle, until the input becomes a logic 0.

\* What are the actions that take place when NMI is activated?

Ans:

- (1) The current instruction in progress is completed.
- (2) Flag register values are pushed onto the stack.
- (3) The CS and IP values of the return address are pushed onto the stack.
- (4) IP is loaded from the contents of the word location 00008H
- (5) CS is loaded from the contents of the next word location 0000AH
- (6) Interrupt flag and trap flag are reset to 0.

\* What is INTO?

Ans: INTO refers to interrupt on overflow instruction.

It is a conditional interrupt instruction. It is active only when the overflow flag is set to 1 and branches to the interrupt handler whose interrupt type number is 4.

If the overflow flag is reset then, the execution continues to the next instruction.

\* What is the purpose of TF in the FLAGS register?

Ans: TF or trap flag is a control flag.

Trap flag plays an important role in the interrupt process.

When TF is set, the 8086 generates a processor interrupt exception, interrupt type 1. This interrupt is used by DEBUG in the execution of trace command.

To trace an instruction, DEBUG first sets the TF and then transfers control to the instruction to be traced. After the instruction is executed, the processor generates an interrupt type 1 because TF is set.