# Cadence Palladium & Protium Introduction

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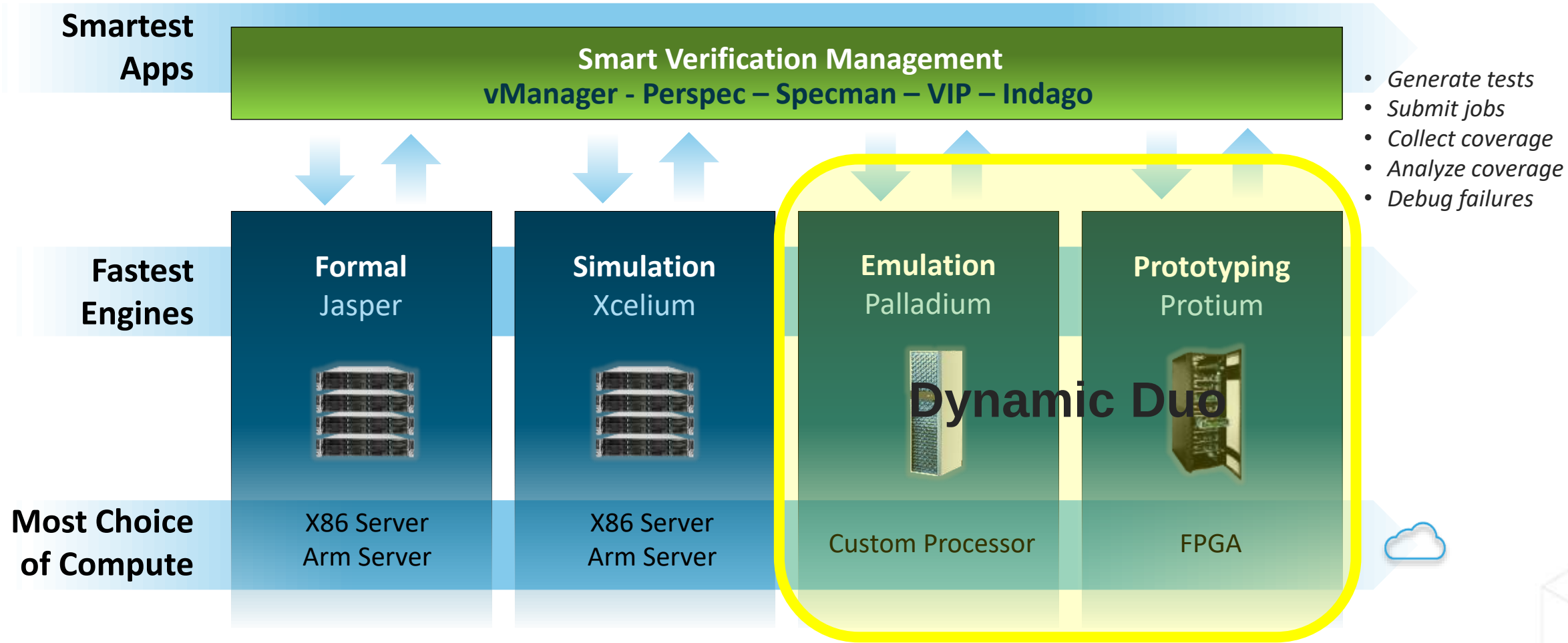
cadence®

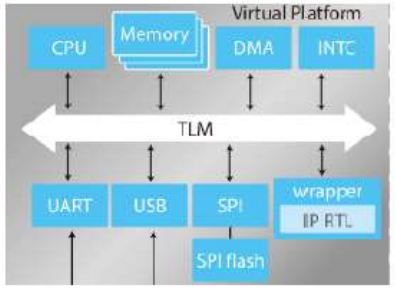
# Leadership in Verification Throughput

*Find and fix the most bugs per $ invested in bare metal compute*




- *Generate tests*
- *Submit jobs*
- *Collect coverage*
- *Analyze coverage*
- *Debug failures*

# SoC HW/SW validation requires high performance Platforms – Attributes





## Virtual Platform

- Almost at speed
- Less accurate (or slower)
- Reference model
- Before RTL
- Great to debug but less details
- Easy replication

## RTL Simulation

- KHz Range
- Accurate
- Excellent HW debug
- Design RTL
- Little SW execution

## Emulation

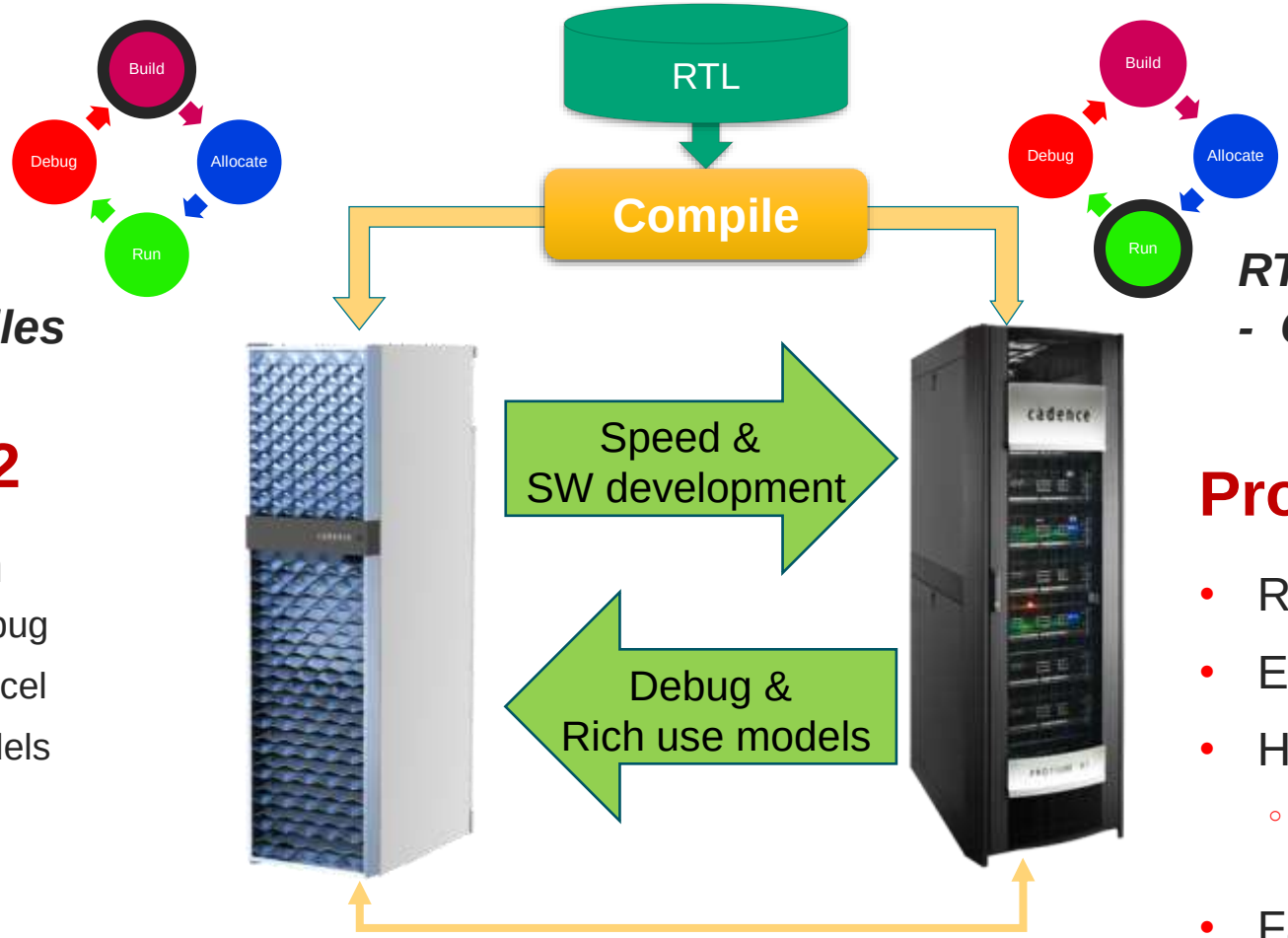
- MHz Range
- Cycle accurate
- Early RTL
- Fast compile
- Good visibility for fast and complete debug
- Datacenter form factor
- State of the art

## Prototyping

- 5-10MHz
- Cycle accurate
- Stable RTL
- Debug Software
- Limited visibility and debug at signal level
- Datacenter form factor
- State of the art

# Dynamic Duo: Palladium Z1/Z2 + Protium X2

*Right Application on the Best Platform*




***RTL < 85% Solid***
***- Multiple/daily compiles***

## Palladium® Z1/Z2

- Hardware Validation
  - Fastest/Deepest Debug
  - SoC integration & accel
  - Rich application models
- ~ 1 MHz
- Fast/Predictable deterministic compile
- 18+ BG monolithically

***RTL >85% Solid***
***- Compiles once a week or less***

## Protium™ X2

- Regressions Testing
- Early SW Validation/Debug
- Highest performance
  - ~5 to 10MHz ~ 500MG to BG
    ~10s of MHz for smaller designs
- Fast system Bring-up
- Scalable Capacity

**Congruency and common environment**

# Dynamic Duo: Z2 and X2 Use Model Distribution

## Palladium® Z1/Z2

- Architectural Exploration
- Performance / Coverage Analysis
- Simulation Acceleration
- Debug with Full Vision/Infinitrace
- SW Driven HW Verification
- Subsystem SOC
- Low Power Verification
- Power Analysis
- Post Silicon Debug
- Gate Level Sim
- Fault Test

Use models in emulation

RTL

Compile

- System Integration Level Test
- HW/SW Co-verification
- Early Firmware Development
- Continuous Regression

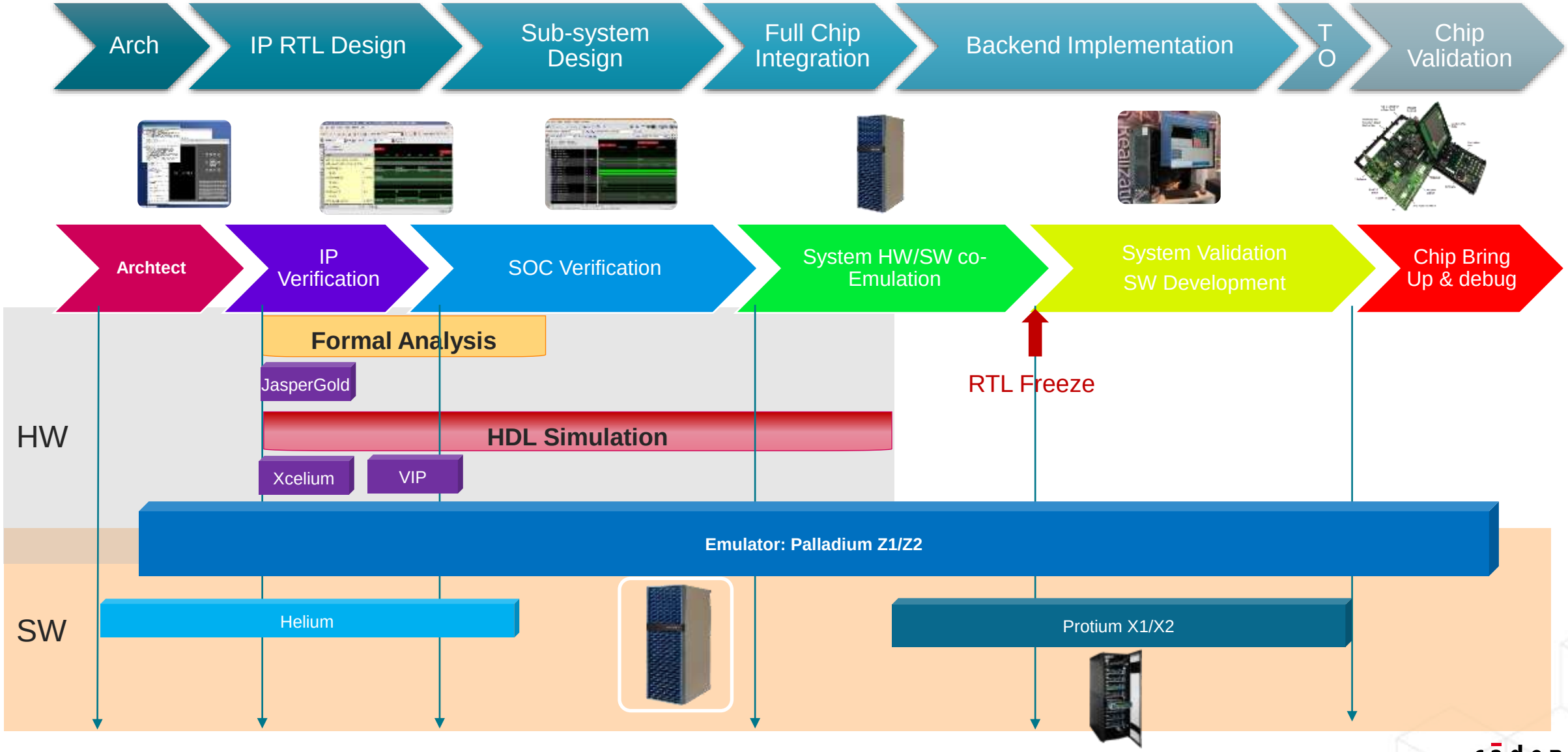
Use models in both

## Protium™ X1/X2

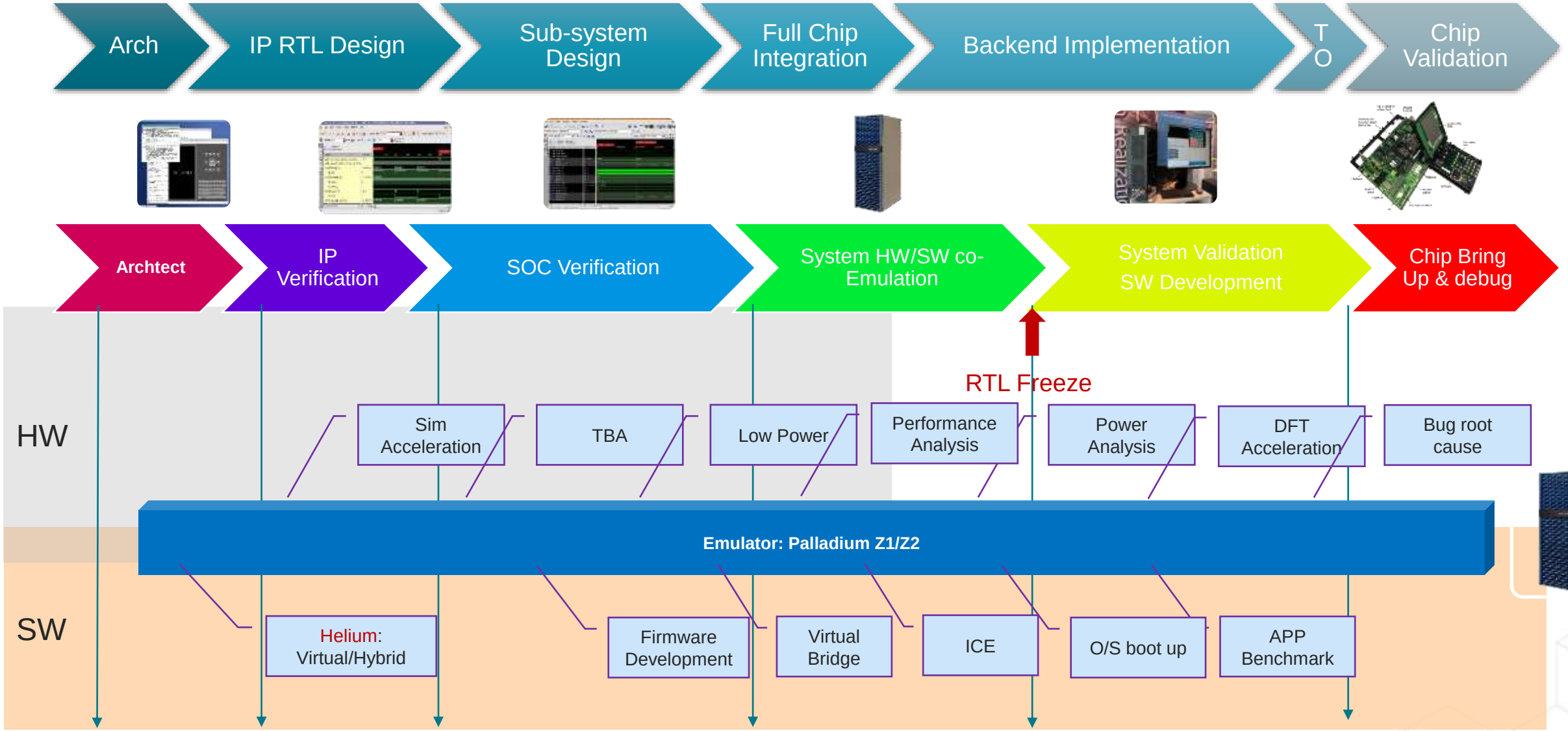
- Fast Test Iterations
- Exhaustive Regressions
- Firmware Development/ SW Debug
- Pre-Silicon Software/OS Development
- Product Validation Readiness

Use models in prototyping

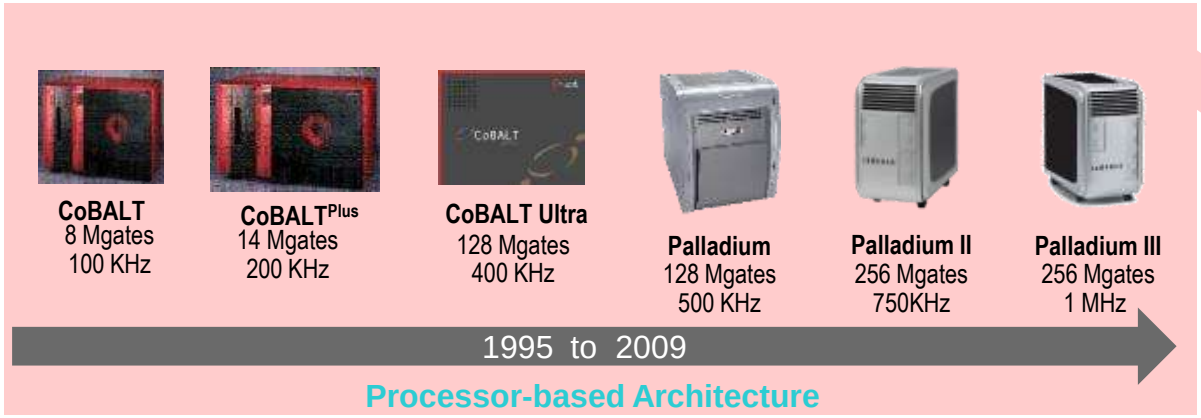
# SOC Verification Phases

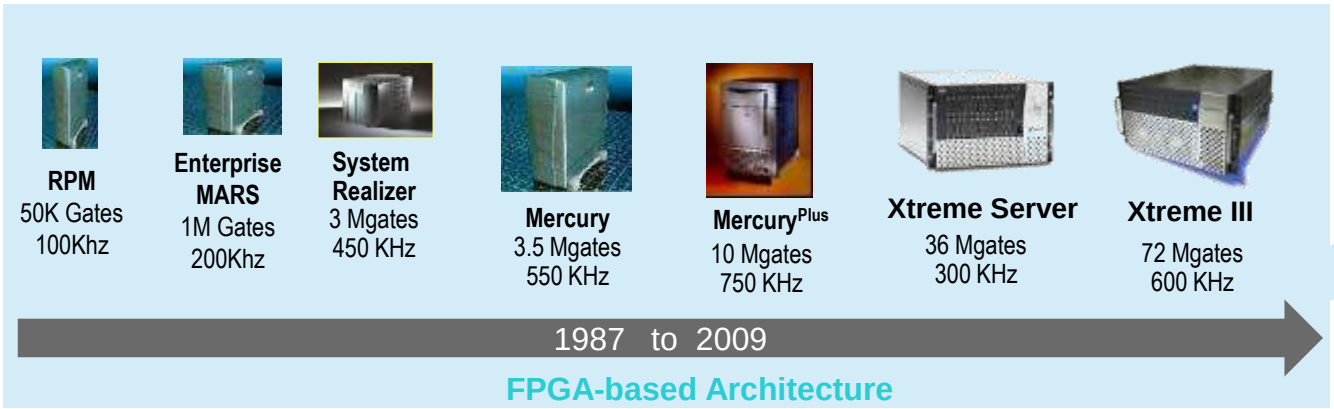


# SOC Verification Phases



# Innovation and leadership in acceleration & emulation



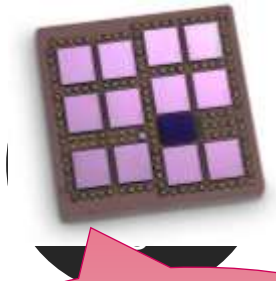



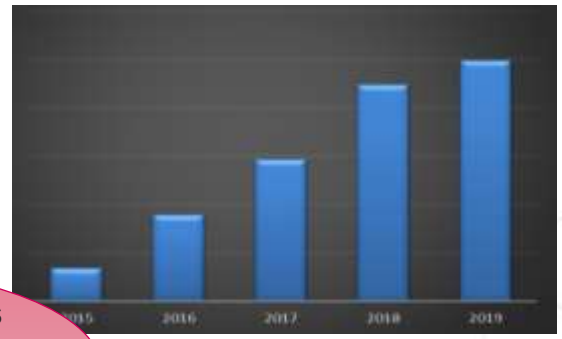

2000
Quickturn

2005
Verisity/Axis

## Verification Computing Platforms

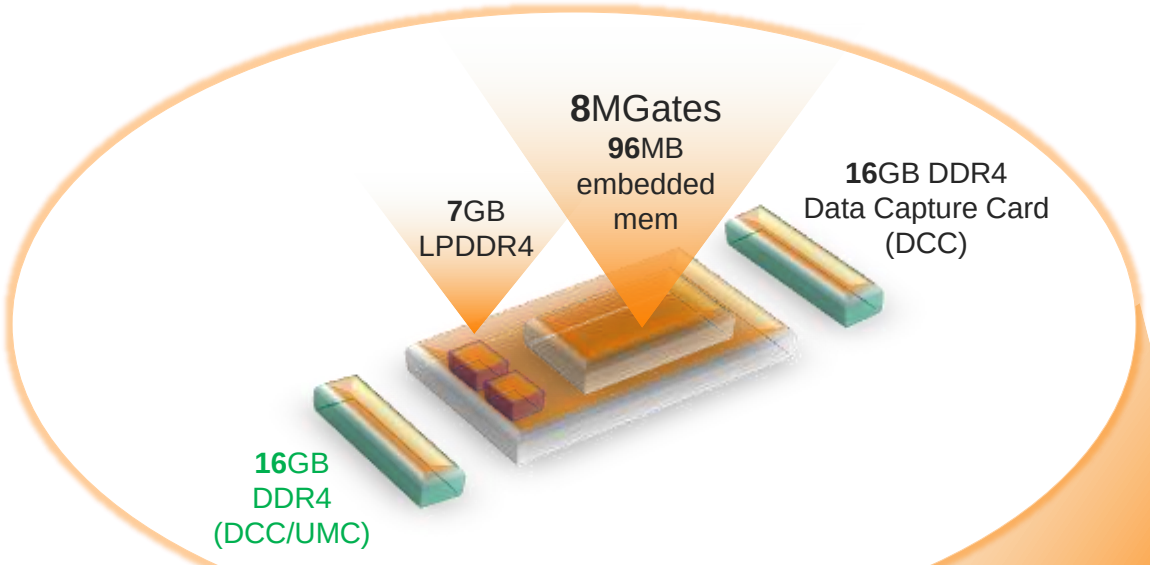

## Enterprise-class VCP

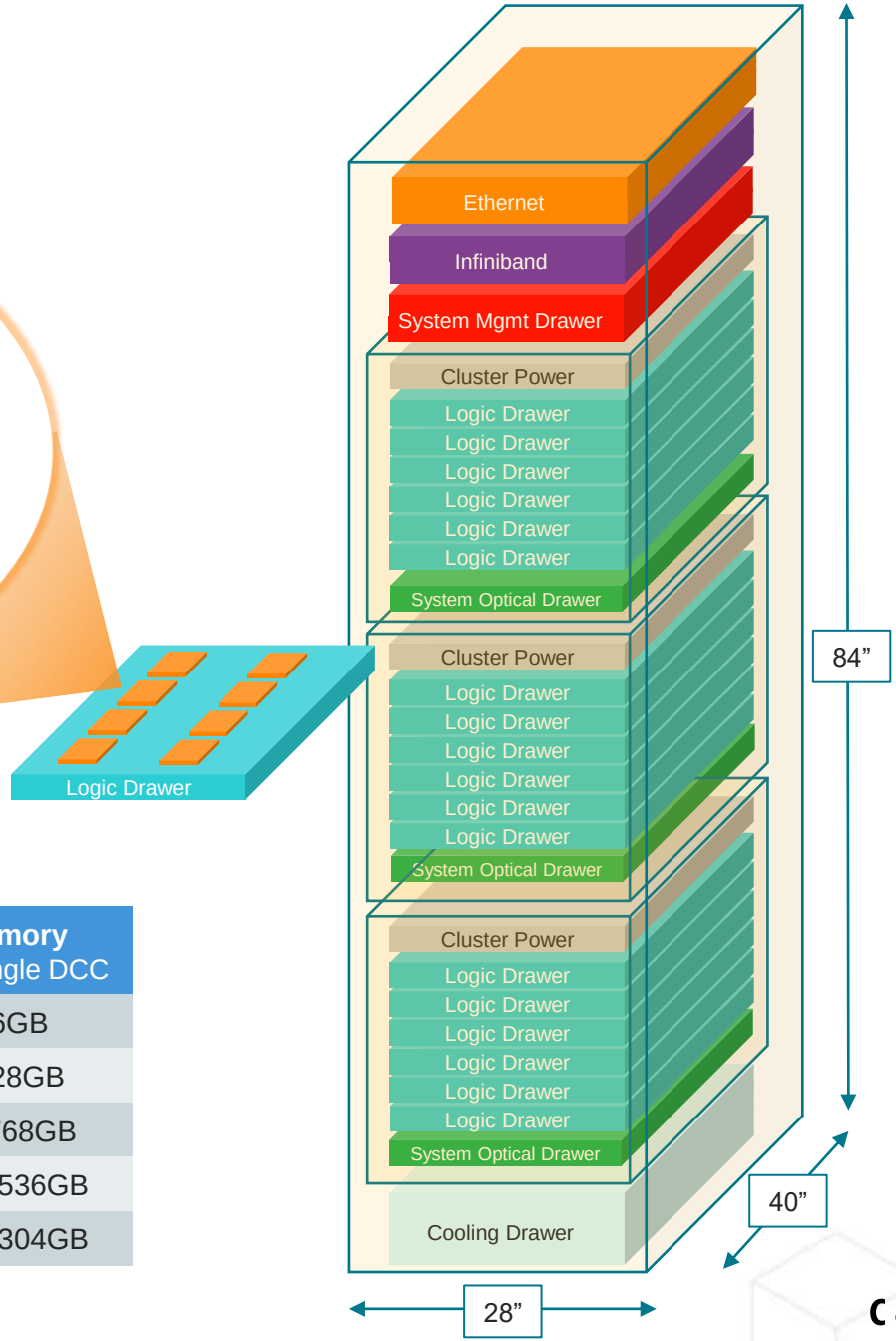


**4 M emulation gates**
3072 processors
72MB EDRAM
Cluster speed 2.0Ghz

# Palladium Z2: 3-cluster rack, GXL




**What's New**
- 2x capacity (2x logic content, 2x memory)
- 7GB of LPDDR4 (user memory)
- Flexible usage of 16 GB DDR4 as DCC or UMC




| Component | Logic | User Memory<br>Dual DCC / Single DCC | Debug Memory<br>Dual DCC / Single DCC |
|---|---|---|---|
| Domain | 8MG | 7GB / 23GB | 32GB / 16GB |
| Logic Drawer (8-domains) | 64MG | 56GB / 184GB | 256GB / 128GB |
| Cluster (6-boards) | 384MG | 336GB / 1,104GB | 1,536GB / 768GB |
| Rack (2-clusters) | 768MG | 672GB / 2,208GB | 3,072GB / 1,536GB |
| Rack (3-clusters) | 1,152MG | 1,008GB / 3,312GB | 4,608GB / 2,304GB |

# Palladium Z2 Migration

## From Palladium Z1

Palladium Z1

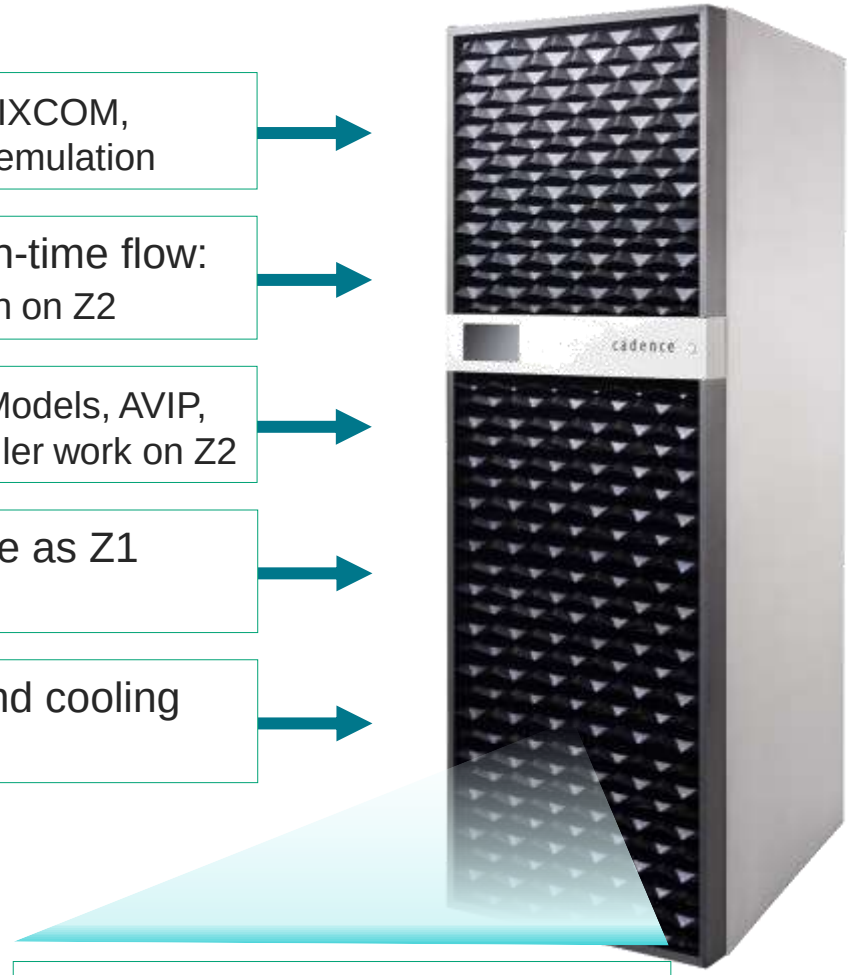
**Use mode match**: Classic ICE, IXCOM, UVM simulation acceleration, virtual emulation

**Easy transition**: Same compile/run-time flow: Z1 designs will quickly compile/run on Z2

**Ecosystem match**: Same Memory Models, AVIP, SpeedBridge, VirtualBridge & Job Scheduler work on Z2

**Compute infrastructure**: Same as Z1 on a per gate basis

**Installation**: Same rack power and cooling as Z1



- **3-state**: With native UPF X-propagation
- **High-speed** compressed waveform dump

Palladium Z2

**1.15BG** Per rack

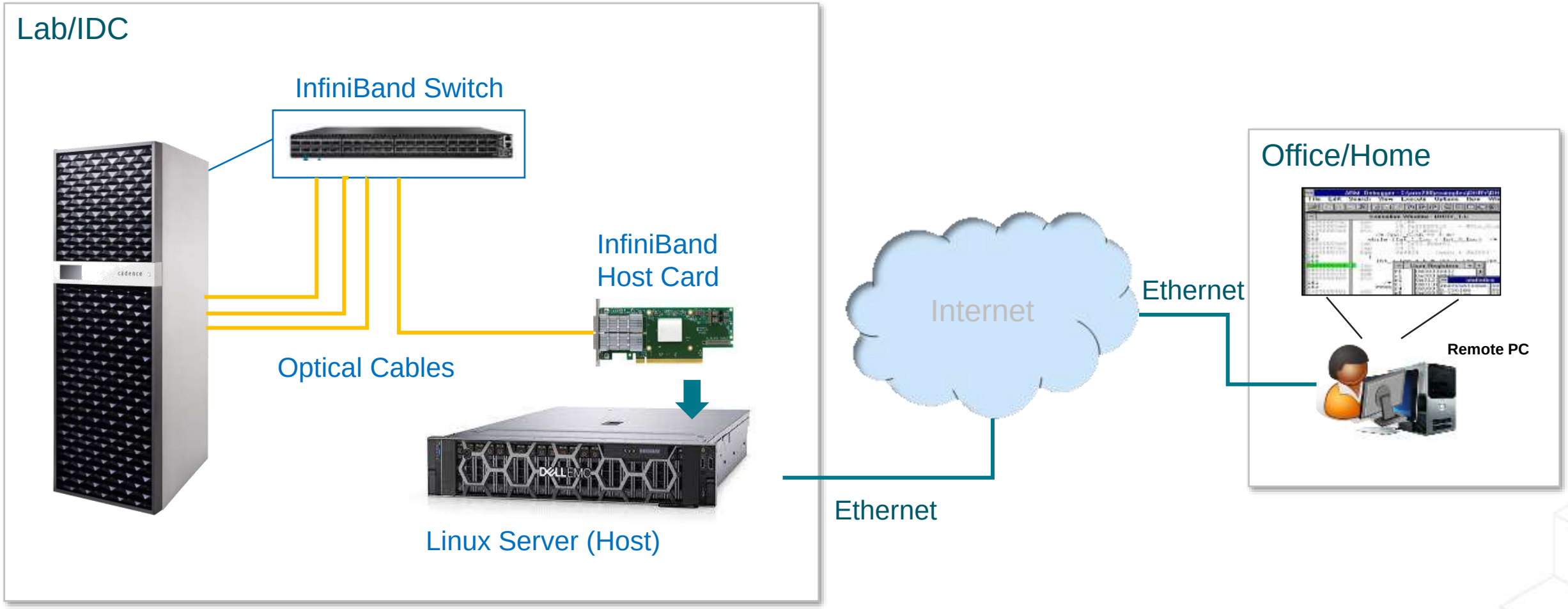
**2X** Capacity density

Up to **1.5x** Higher FCLK

**50%** Power per gate

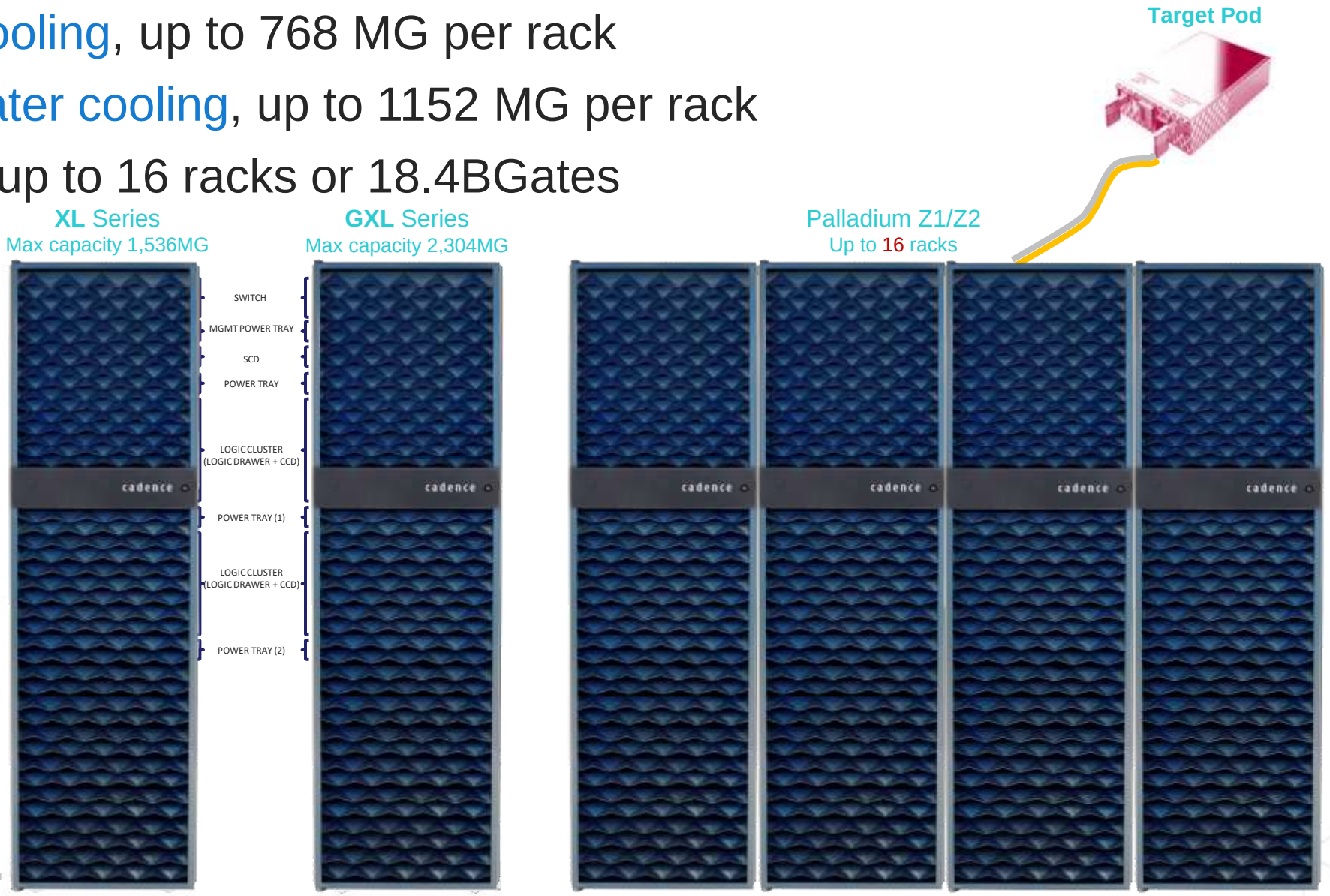
**2x** Debug capture option

# Palladium Z2 Installation Example



# Palladium Z2 configurations (examples)

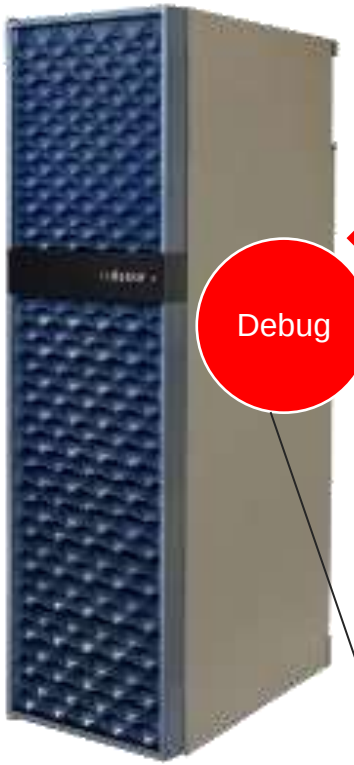
- XL –Air cooling, up to 768 MG per rack
- GXL – Water cooling, up to 1152 MG per rack
- Supports up to 16 racks or 18.4BGates

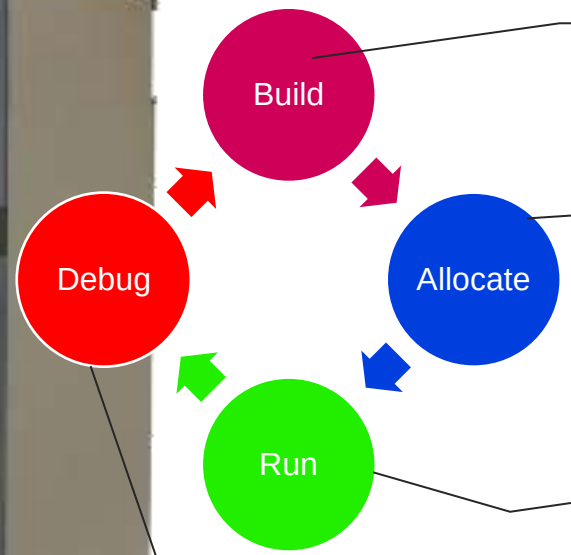


# Palladium Z1/Z2 installation examples

# Palladium Z1/Z2 platform: fastest time to fully verified design

## *Improves Every Aspect of Emulation Flow*






Compile databases for different workloads
**Fast and predicable compile**

Allocate workloads as efficiently as possible
**Best utilization efficiency, advanced job reshaping technology**

Use model versatility and flexibility
**22+ use models with RTL and GL support**

Best debug for both pre & post silicon bugs
**Best controllability and visibility**

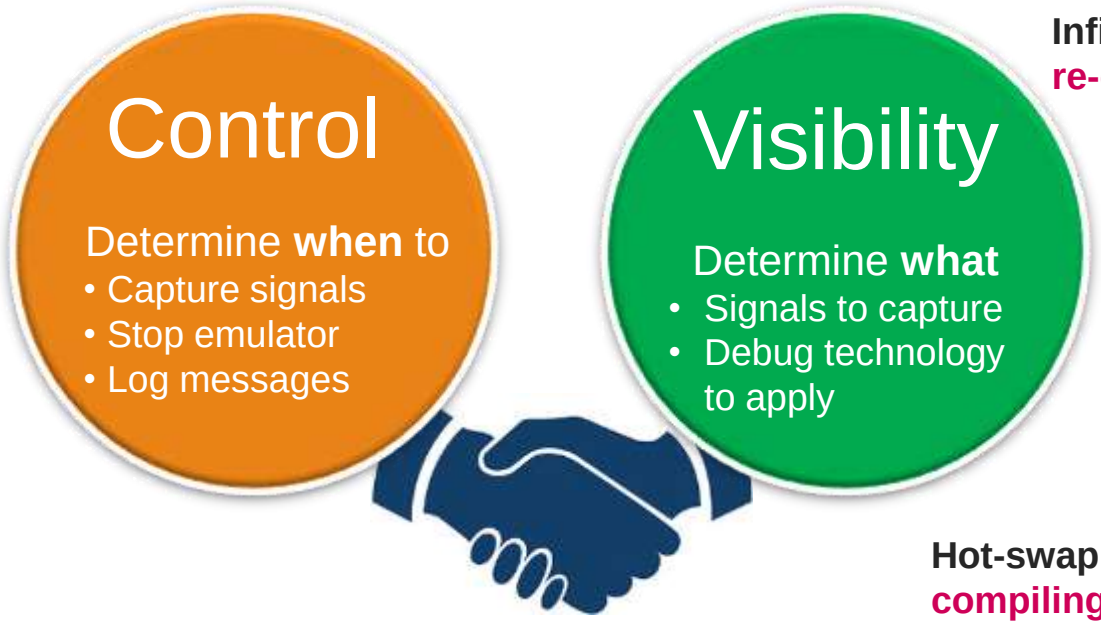
Model Turns Per Day: up to 5x better than competition

# Palladium Debug

## Unparalleled levels of productivity, without re-compiling, at speed

**FullVision** View any design signal at full speed. Debug design **without re-compilation**

**Dynamic Probe** Capture select signals with large traces (up to 80M samples) **without re-compiling**.




**InfiniTrace** Capture extremely long trace depth for post-analysis replay, **without re-compiling**. Move forward & backward to debug any time window of interest

**Offline Debug** Offline concurrent debugging on workstation. Free up Palladium resource for other jobs, jump to any time window using a specific trigger

**Waveform streaming** Continuously view small number of signals at full rate **without re-compiling**

**Save/Restore** Re-start emulation run from a previous state **without re-compiling**. Save time by restoring, avoid repetitive initializations or sequences

**Hot-swap** Swap state of design back to simulator for interactive debugging **without re-compiling** to free up Palladium resources for non-interactive jobs

**Force** Change design function during runtime **without recompile**. Set system conditions to analyze design behavior under un-modeled corner cases

**SDL/DRTL** Specify multi-level complex trigger conditions. Use design events to detect scenarios, **without re-compile**

**Combine control & visibility**

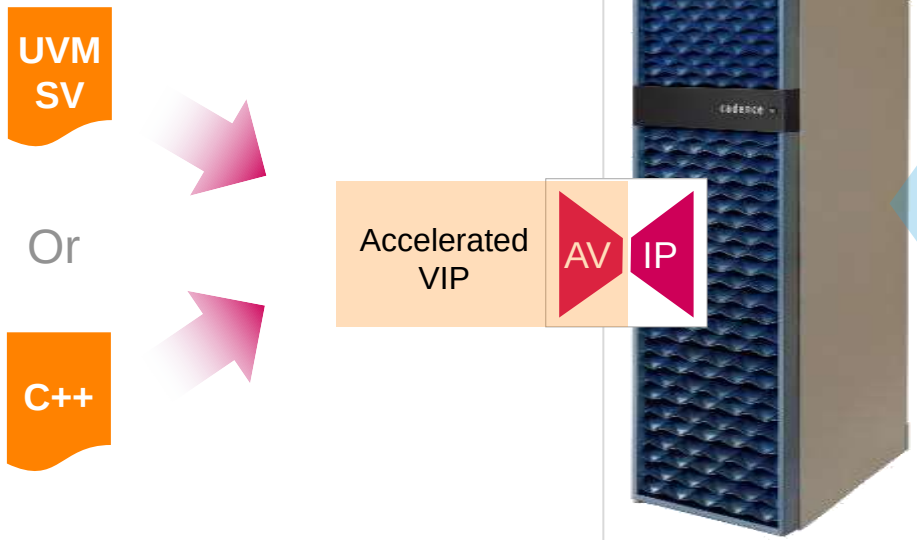
- Triggering waveform capture
- Full Vision & Waveform streaming
- Compiled Monitors with dynamic technologies (DRTL and SDL)

# Protocol solutions with Palladium

## Flexible options for full validation

### Virtualization

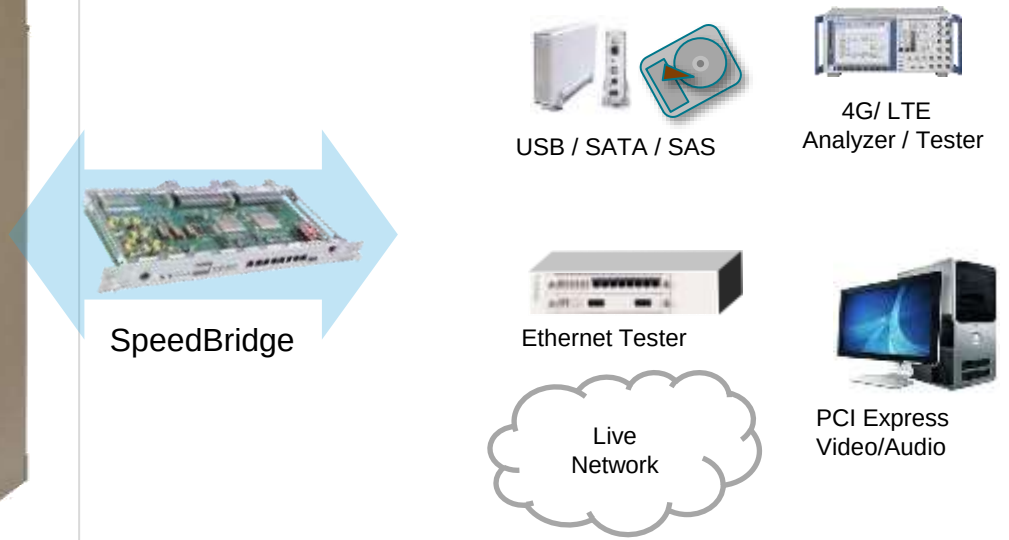
Acceleration & HW/SW verification with Accelerated VIPs




- Accelerate sub-system simulations that use UVM SystemVerilog testbenches
- Integrate sub-systems and validate HW/SW interaction early in the development cycle by driving traffic with C++ interface

### In-Circuit Emulation

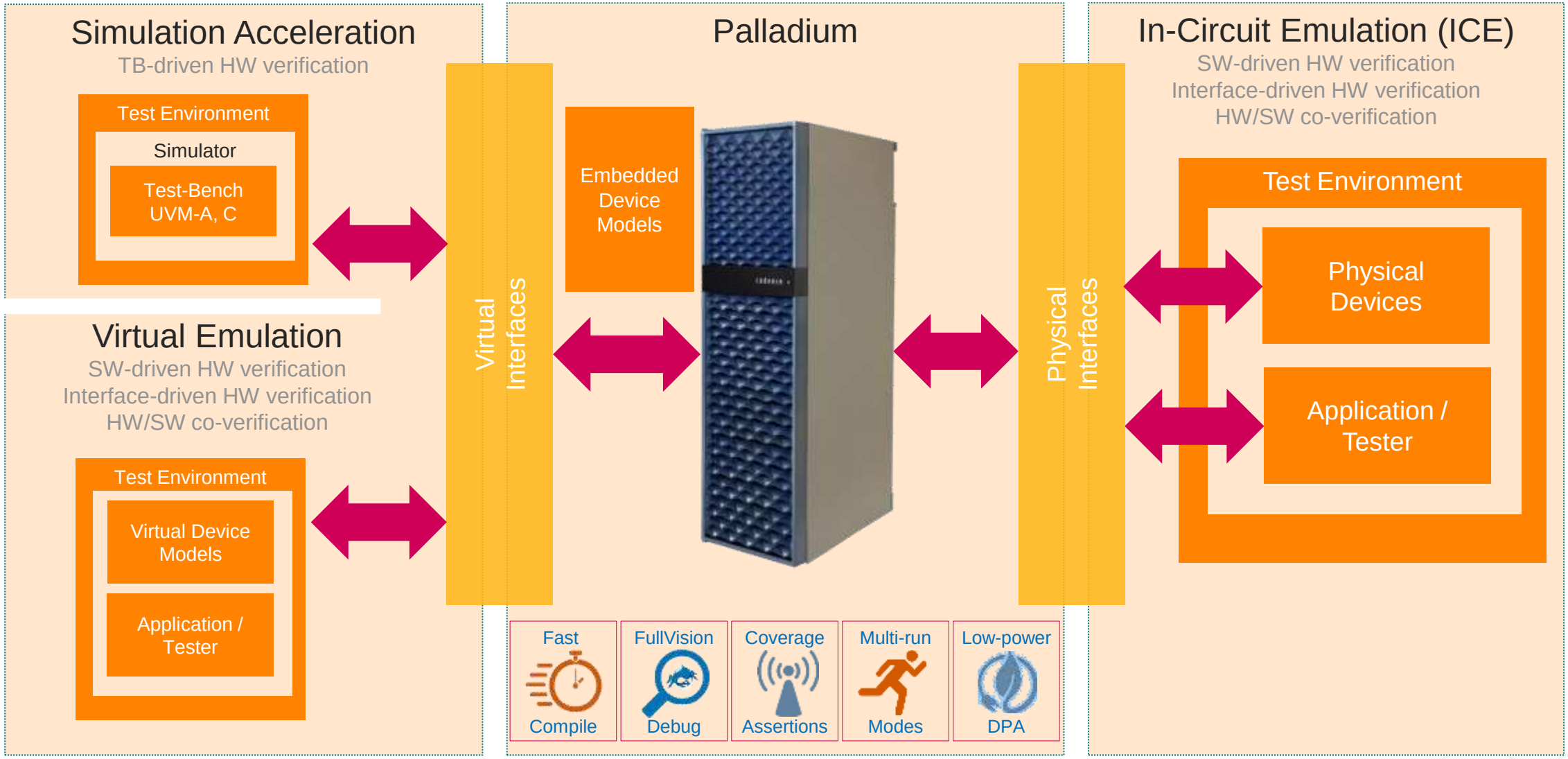
Real-world interfaces, real-time speed with SpeedBridge




- Perform full validation scaling to high performance per port
- Validate with industry standard 3rd party testers that generate complex traffic at high performance (e.g. Layer 4-7 traffic)
  - Live networks can generate realistic traffic streams, integrate network apps

# Palladium Use Modes

## Simulation Acceleration, Virtual and In-Circuit Emulation

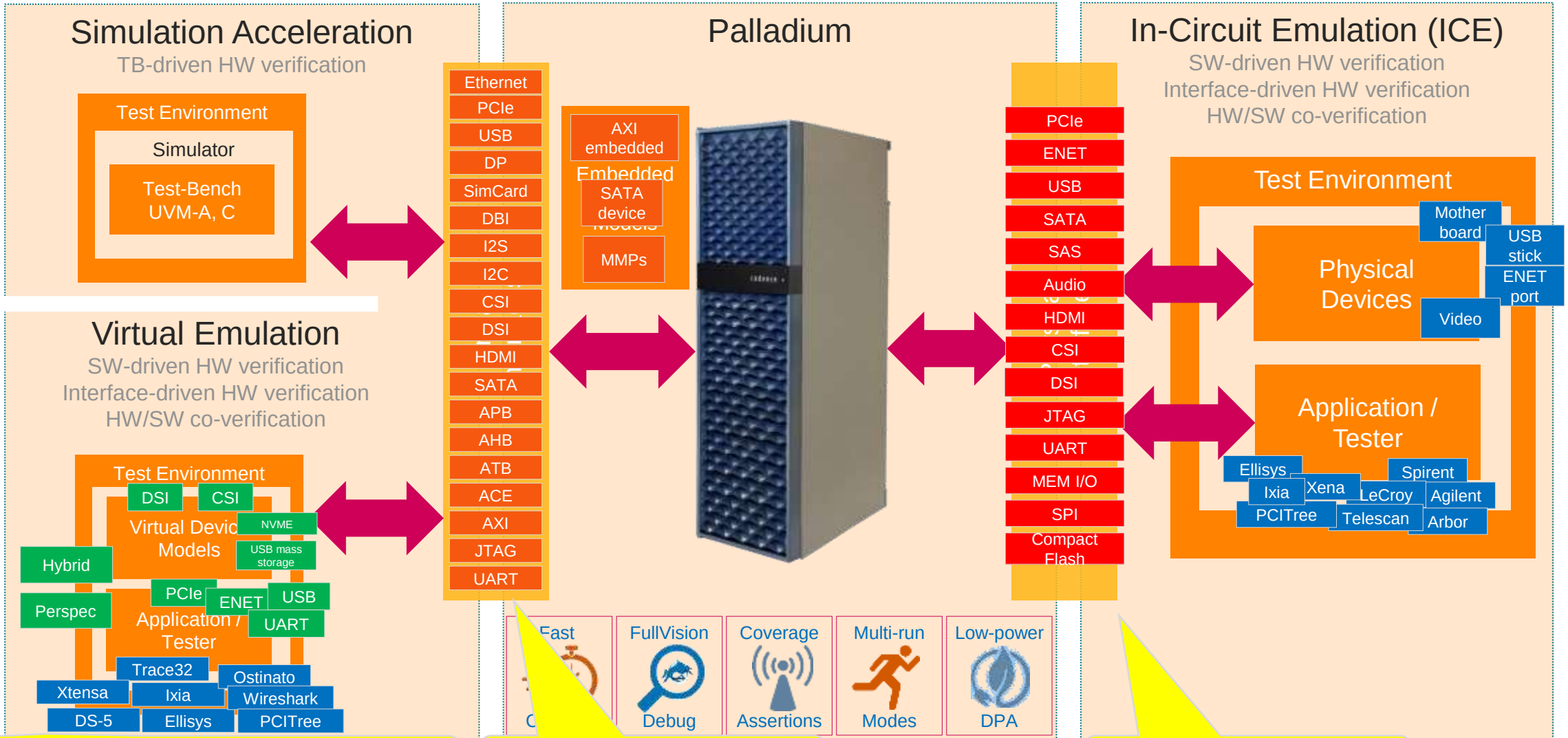



Examples shown

SpeedBridge / EDK
3rd party
Transactor

# Palladium Use Modes

## Simulation Acceleration, Virtual and In-Circuit Emulation



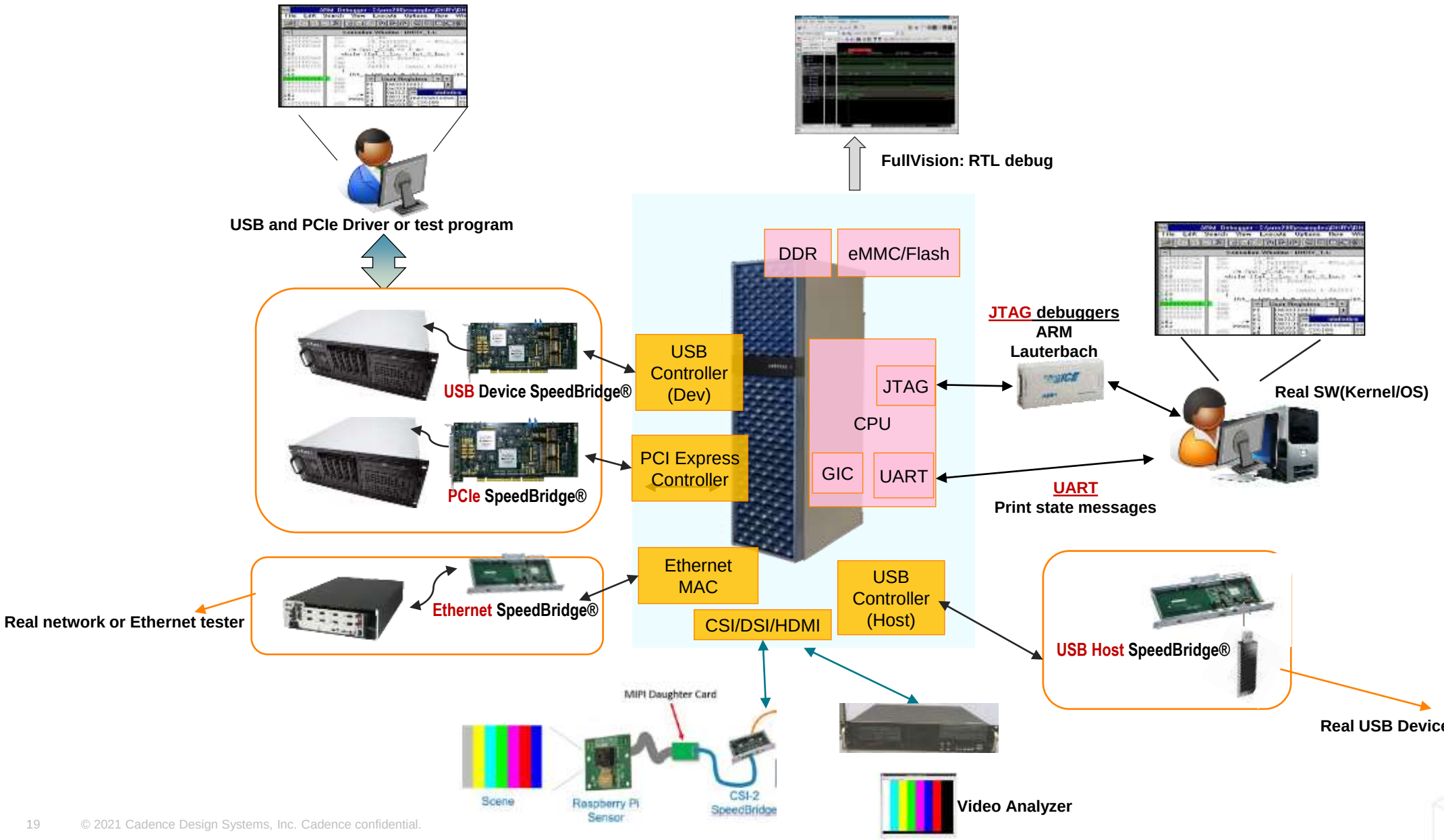

Use Palladium's virtual emulation products – VirtualBridge, Virtual Device, Hybrid and more

Use AVIP's C interface to create your own virtual extensions

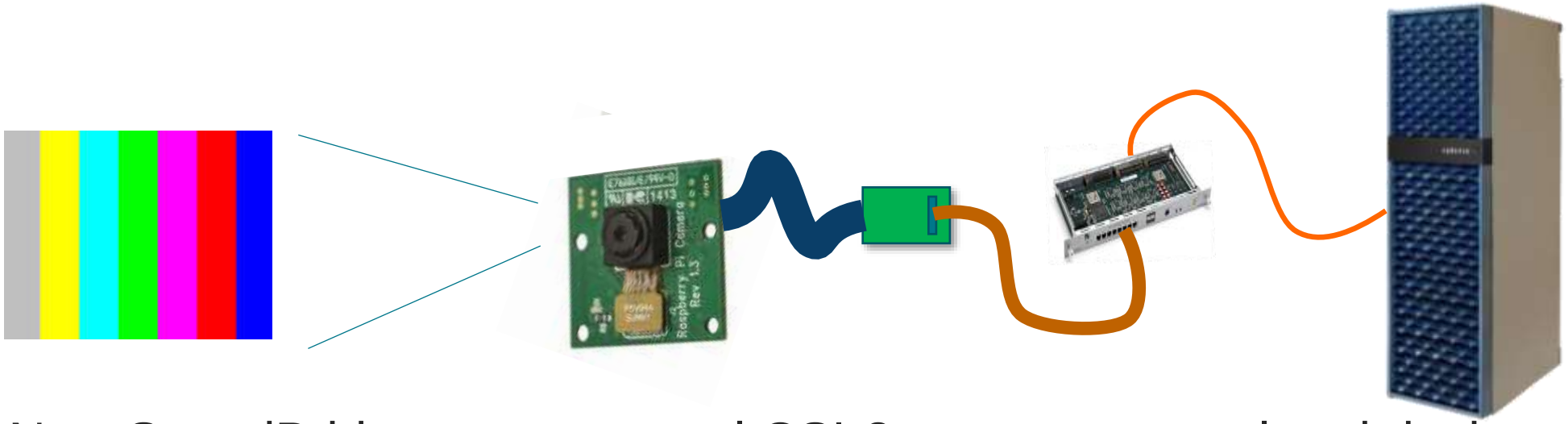
Use SpeedBridges to interface to live environments

cadence

# HW/SW Co-verification Environment (ICE mode) - Example



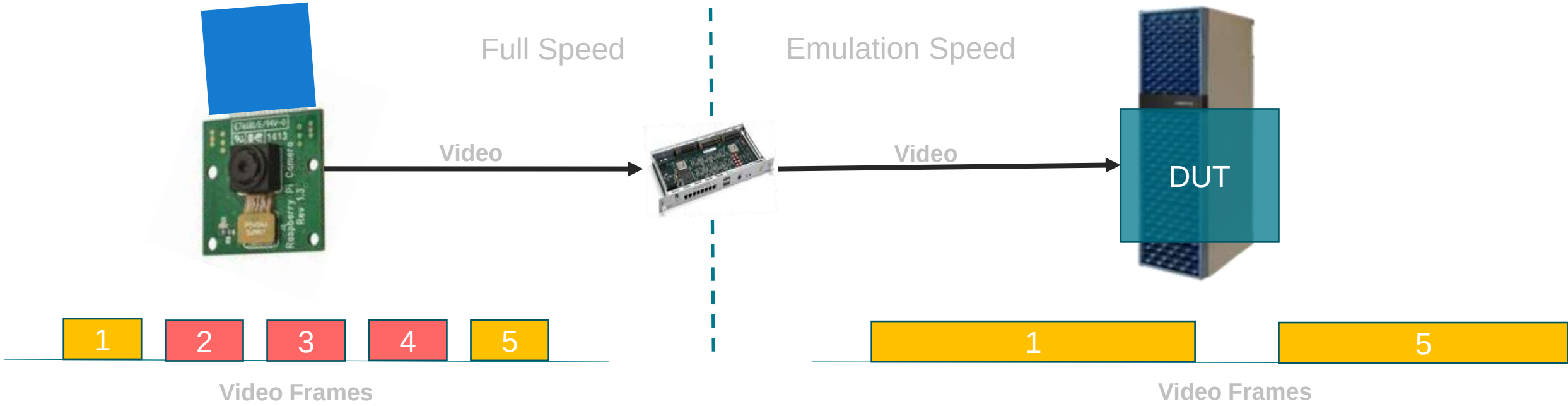
# MIPI CSI-2 SpeedBridge – Application




- New SpeedBridge connects real CSI-2 sensors to emulated designs (P15)
  - Support Palladium Z1, XP and Protium S1
- Sensor video is scaled to emulation speed
- Customers can verify their DUT with the actual sensor they are targeting for DUT
  - Vendor specific register spaces, image processing functions, etc
  - Real sensor behavior
  - Speedup s/w development and prototyping

# CSI-2 FPGA SpeedBridge (P25)

## Frame Filtering

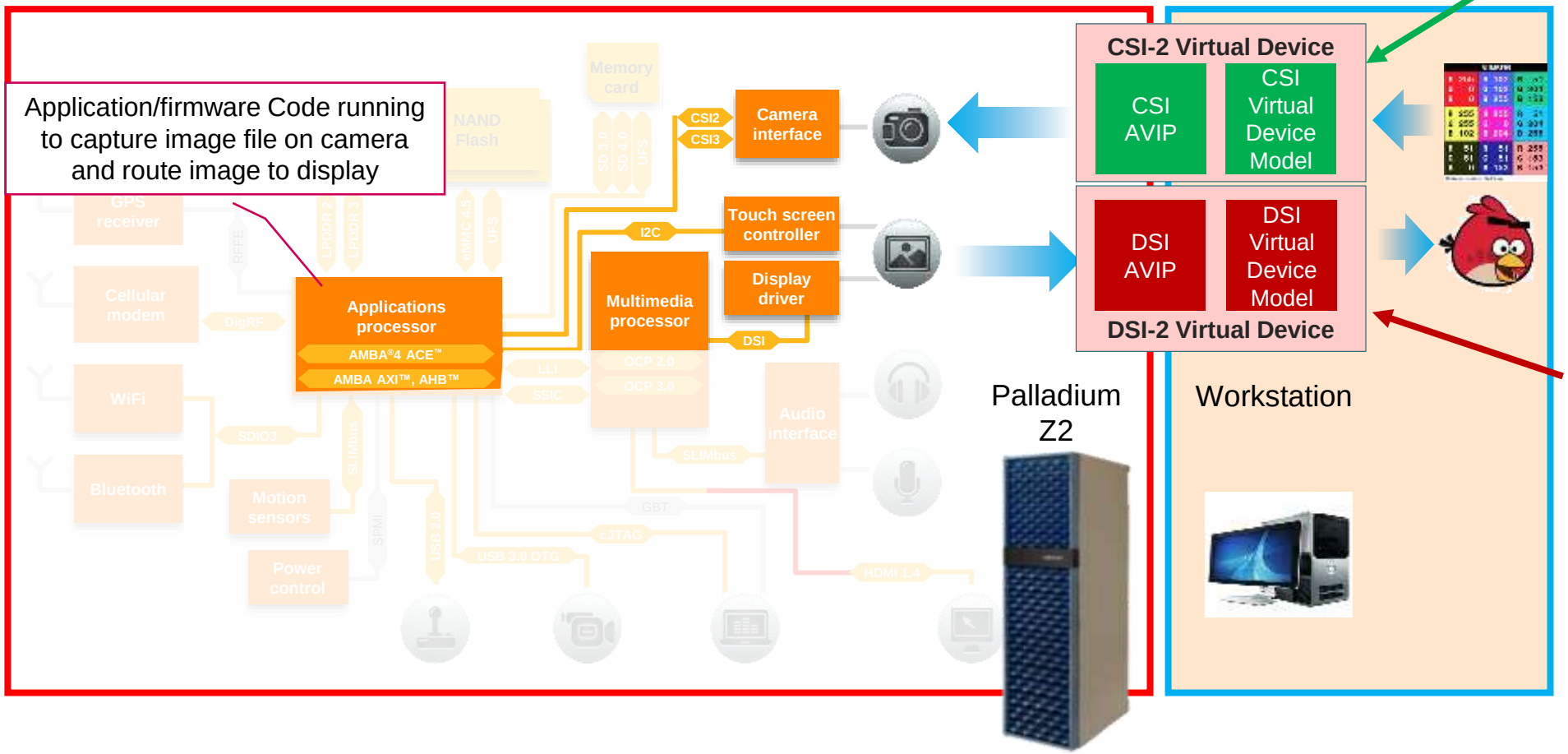



- CSI-2 video stream is slowed down to emulation speed
- SB forwards every Nth frame, depending on speed of emulated DUT
- Video can be streamed continuously to emulator

# Virtual Device (CSI-2, DSI-2)

## Visualize HW/SW operation of your video/image processing subsystem

Application/firmware Code running to capture image file on camera and route image to display




**CSI-2 Virtual Device**

Modeling a MIPI Camera Device

- Reads frame data from file, drives it to DUT with proper CSI2 packing
- APIs can be invoked from a test bench to initiate an image or video transfer

Supports

- RGB data: RGB444,RGB555,RGB565 & RGB888
- YUV data: 4:2:2 8bits,4:2:2 10 bits, 4:2:0 8bits and 4:2:0 10 bits
- RAW data: RAW6, RAW7, RAW8, RAW10, RAW12 and RAW14

**DSI2 Virtual Device**

Modeling MIPI Display Device

- Receives video DUT, displays on virtual display
- Automatically processes DSI commands from DUT and responds accordingly

Supports

- Command and video modes
- Read and write DCS commands modifying video buffer accordingly
- All RGB and YUV data formats in both command mode and video mode
- Blanking lines and HSync/VSync events
- BTA mode operation

# Samsung case study
## HW-SW verification using SpeedBridge

- Application
  - Memory
- Challenge
  - Verifying HW-SW in a single environment
  - Bug reproduction because of variability in multiple factors like HW, SW, drivers, etc.
  - Connecting DUT to live environment
- Solution
  - SpeedBridge® with Palladium
- Benefit
  - Post-Si test environment can be used in pre-Si validation
  - Found driver performance issues previously not detected


Source: CDNLIVE 2014

# SpeedBridge Portfolio

## Networking

SRIO HD

Ethernet HD

## Storage

SATA/SAS Host/Device

Fibre Channel HD

## Video

MIPI CSI/DSI HD

HDMI/DP/CSI/DSI


## USB

USB 3.2 Gen2 HD Host/Device + EDK

## Wireless

5G HD

WLAN HD

## PCIE

PCIE Gen5 HD + EDK

# Cadence SpeedBridge adapter solutions

## Protocol support overview

SATA

USB 3.2/2.0/1.1 Device

USB 3.2/2.0/1.1 Host

PCI-Express 5.0/4.0/3.0
1,4,8,16 lanes

SAS

Universal SpeedBridge Chassis

Palladium Z1/Z2 Protium X1/X2

Ethernet

1G, 10G, 40G, 100G, 400G

Ethernet Tester

MIPI CSI-2

5G speedbridge





5G Analyzer / Tester

Video (RGB,HDMI,MIPI)
Audio

Miscellaneous adapter boards:

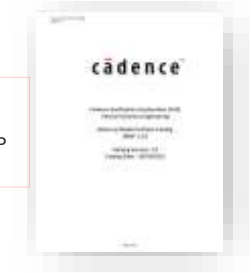
JTAG, Uart, SD card, Multi I/F, etc.

Fibre Channels

RapidIO

# Memory Model Portfolio (MMP) for Palladium

Memory Model catalog. Regularly updated under MMP release



## SDRAM

- SDRAM
- DDR2
- DDR3
- DDR4
- DDR4 LRDIMM
- DDR5
- LPDDR2
- LPDDR3
- LPDDR4
- LPDDR5
- GDDR5M
- GDDR5X
- GDDR6
- HBM2E
- WideIO
- WideIO2
- DDRx DIMM
- DDR4 DIMM
- DDR5 DIMM
- MRAM
- HyperRam

- JEDEC
- Micron
- Hynix
- Winbond
- Elpida
- Samsung

## Flash

- NAND
- ONFI 2.0
- ONFI 2.2
- ONFI 3.0
- ONFI 3.2
- ONFI 4.0
- ONFI 4.1
- ToggleDDR
- ToggleDDR2
- ToggleDDR3
- OneNAND
- LBANAND
- ClearNAND
- EZ-NAND
- NOR

- SPI
- Quad-SPI
- Octal-SPI
- SPI NAND
- Hyperflash

- Micron
- Samsung
- Toshiba
- Spansion
- Macronix
- Winbond

## SRAM

- Async
- Syncburst
- DDR
- DDR II
- DDR II+
- QDR
- QDR II
- QDR II+

- Cypress
- Samsung

## Cellular SRAM

- PSRAM
- ADMUX PSRAM
- OPIDDR PSRAM
- PSRAM x8
- OSPI PSRAM
- RLDRAM2
- RLDRAM3
- UTRAM
- UT2RAM

- Samsung
- Micron

## EEPROM

- I2C
- Microwire
- SPI

- Atmel

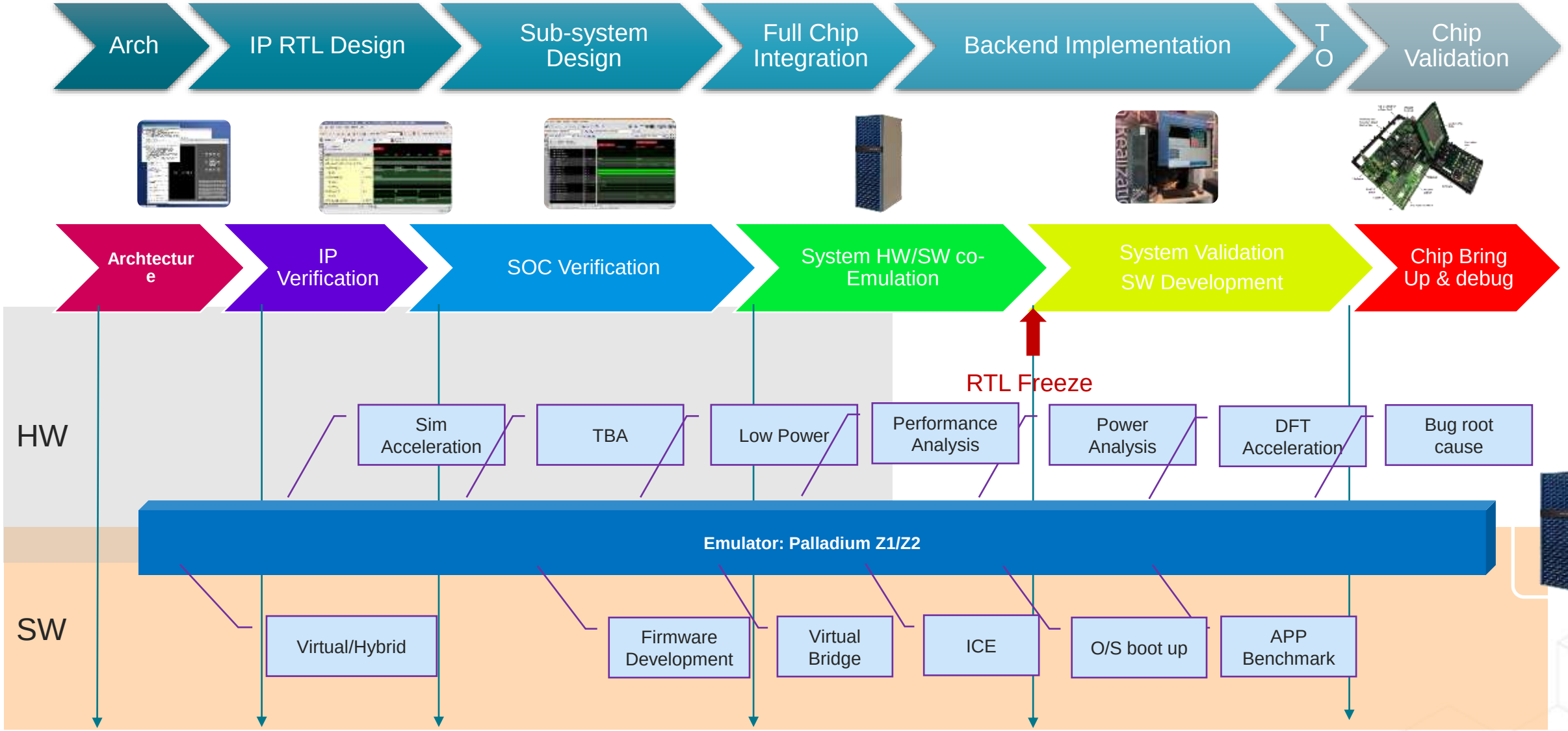
## System

- eMMC 4.5
- eMMC 5.0
- DFI PHY 4.0
- DFI PHY 5.0
- GDDR6 PHY
- HBM PHY
- Compact Flash
- SD Card
- UFS 2.1
- UFS 3.0
- UFS Card
- HMC 2.0

- Samsung
- Toshiba
- Sandisk

Note : Yellow highlighting indicates families with MMP_PLUS models either in whole or in part of family.

# SOC Verification Phases

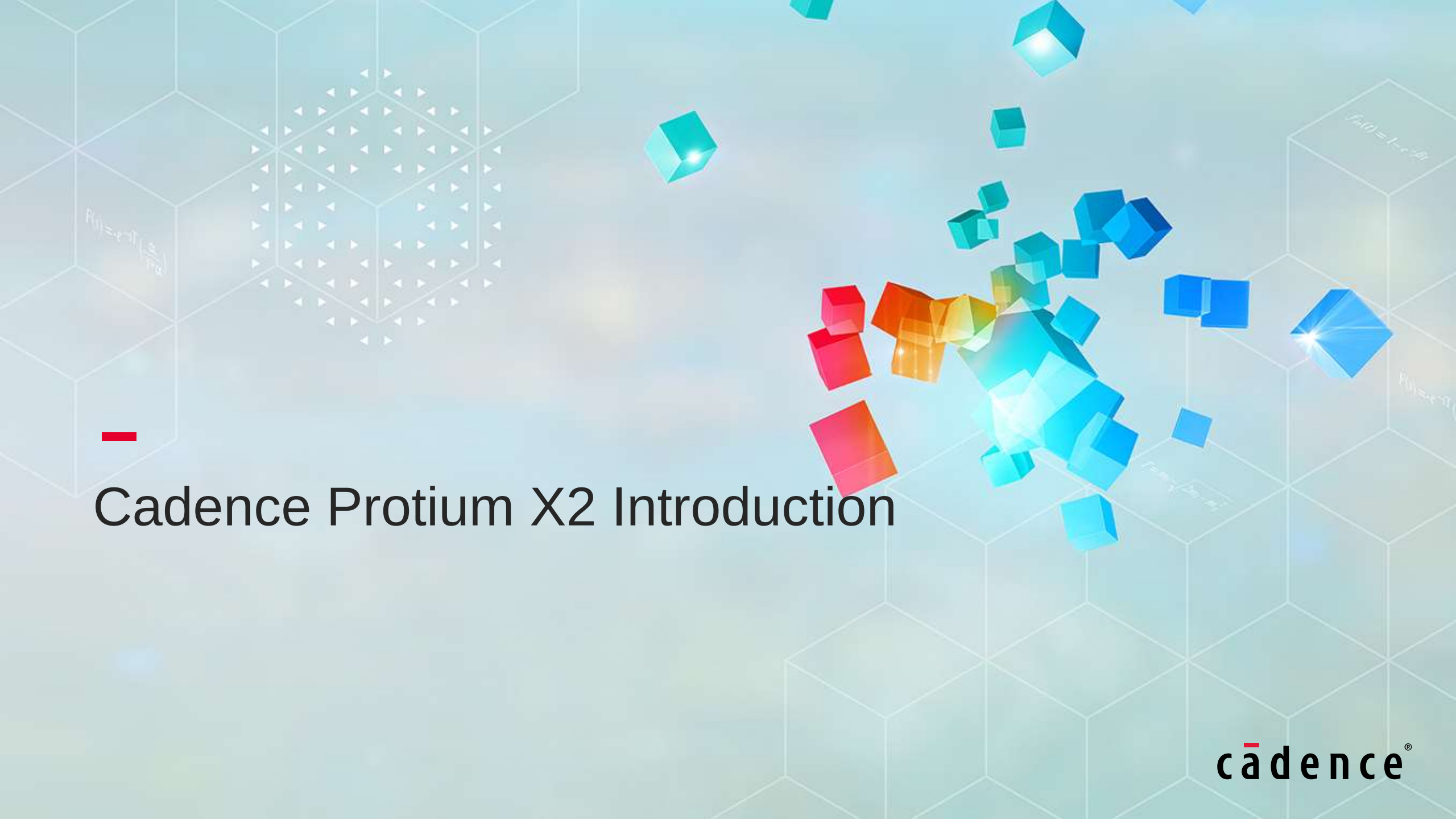


# Palladium Differentiation

| | Palladium | Competition | Notes |
|---|---|---|---|
| **Architecture** | Massively parallel(Processor) | Commercial FPGA | **Deterministic** |
| **Utilization** | 100% to 125% | 65% to 75% | **A gate is not gate!** |
| **Predictable Compile** | Compile time | tuned at runtime | **Unique to Palladium** |
| **Performance Trade Off** | 10% to 30% gain | Not possible | **Choice** |
| **Capacity optimization** | 10% to 30% (for performance) | Not possible | **Unique to Palladium** |
| **Granularity & Relocation** | Fine grain (device level)<br>4MG | Coarse grain at board-level<br>Increments of 60 or ~80MG | **4X to 15X better TCO** |
| **Gate-level** | Capacity: +10-15%<br>Runtime: <15% | Capacity:+50 to 200%<br>Runtime: N/A | **Unique to Palladium** |
| **User Memory** | Memory/Gate: 1X<br>Flexible Access | Memory/Gate: 0.06X to 0.2X<br>Access: direct, host memory | **Your design has memories, right?** |
| **Debug Methods** | Compile, Runtime, Post-runtime, Streaming, Monitors, Probes | Compile only, streaming, monitors, probes | **Key Differentiator** |
| **Trace Depths** | Streaming w/o perf impact<br>Full trace: 2 million samples | Monitors: limited with perf. Impact<br>Full trace: 300K samples; 100K typ. | **Root cause analysis** |
| **Triggers** | SDL, DRTL, SVA, F/F, Reg, Nets<br>small overhead | SVA, F/F, Reg: trigger resources, recompile | **Productivity w/o re-compile** |

# Palladium Z1/Z2 – Market-Leading Emulation Technology

| | | |
|---|---|---|
| **Only Emulator Scaling to**<br>**Billion Gate Designs** | 4MG to 9.2BG, 4.6BG installed | One emulator fits all:<br>Scalability addressing small and large payloads |
| **Industry-Leading**<br>**Debug Efficiency and Performance** | Debug at speed –<br>no slow down, largest buffers | 50% of time spent on debug:<br>Best ROI with Palladium Z1 platform |
| **2-Year Lead Optimizing**<br>**Transition Between Engines** | Congruency for DUT<br>HDL flow – Xcelium™/Palladium® HVL flow | No more cumbersome maintenance of multiple verification environments |
| **Up to 2X Better Throughput** | Unparalleled throughput<br>compile, allocation, run, debug | Fastest execution of long<br>queues of verification payloads |
| **Unique Run-Time Efficiency –**<br>**RTL and Gate** | Swap-in from Xcelium,<br>gate-level without capacity explosion | Reach verification states previously not reachable<br>(swap in for gate-level advance to point of interest) |
| **Largest Number of**<br>**Advanced Use Models for Best ROI** | 22 use models<br>adding DMS, Safety, etc. | Best ROI of hardware platforms |



# Cadence Protium X2 Introduction

cadence®

# Protium Platform Roadmap

**Large Capacity Prototype Platform**

- Protium S1
  - Xilinx Virtex7 FPGA
  - Max Capacity:
    - 24x FPGA
    - 600MGates

**1st Generation Enterprise Prototype Platform**

- Protium X1:
  - Xilinx VU440 FPGA
  - Max Capacity:2-rack
    - 120x FPGA
    - 2.4BGates

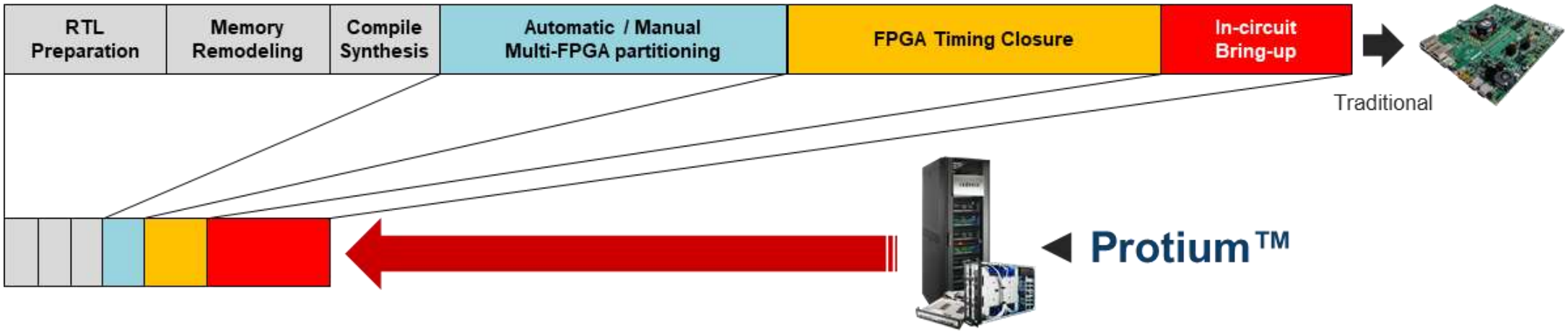
**2nd Generation Enterprise Prototyping Platform**

- Protium X2
  - Xilinx VU19P FPGA
  - Max Capacity: 4-rack
    - 240x FPGA
    - 9.6BGates

2016 → 2019 → 2021

# Cadence独特的Protium 企业级原型平台

## 全自动化，快速 Bring-Up




- 超大容量：可支持最大96亿门的设计规模
- 全自动化：全自动化的编译流程，数十亿门级别的原型系统可以在1-2周内迅速Bring-up
- 节省人力：一个工程师即可维护超大规模的FPGA原型系统
- 兼容加速器：重用Palladium编译脚本，通用外部硬件板卡，不修改客户设计

不需要修改用户设计

- 保持和ASIC一致的时钟
- 自动化的存储模型编译和映射

全自动化的多片FPGA设计分割

- 不需要人工分割设计

全自动化的FPGA 时序约束及收敛

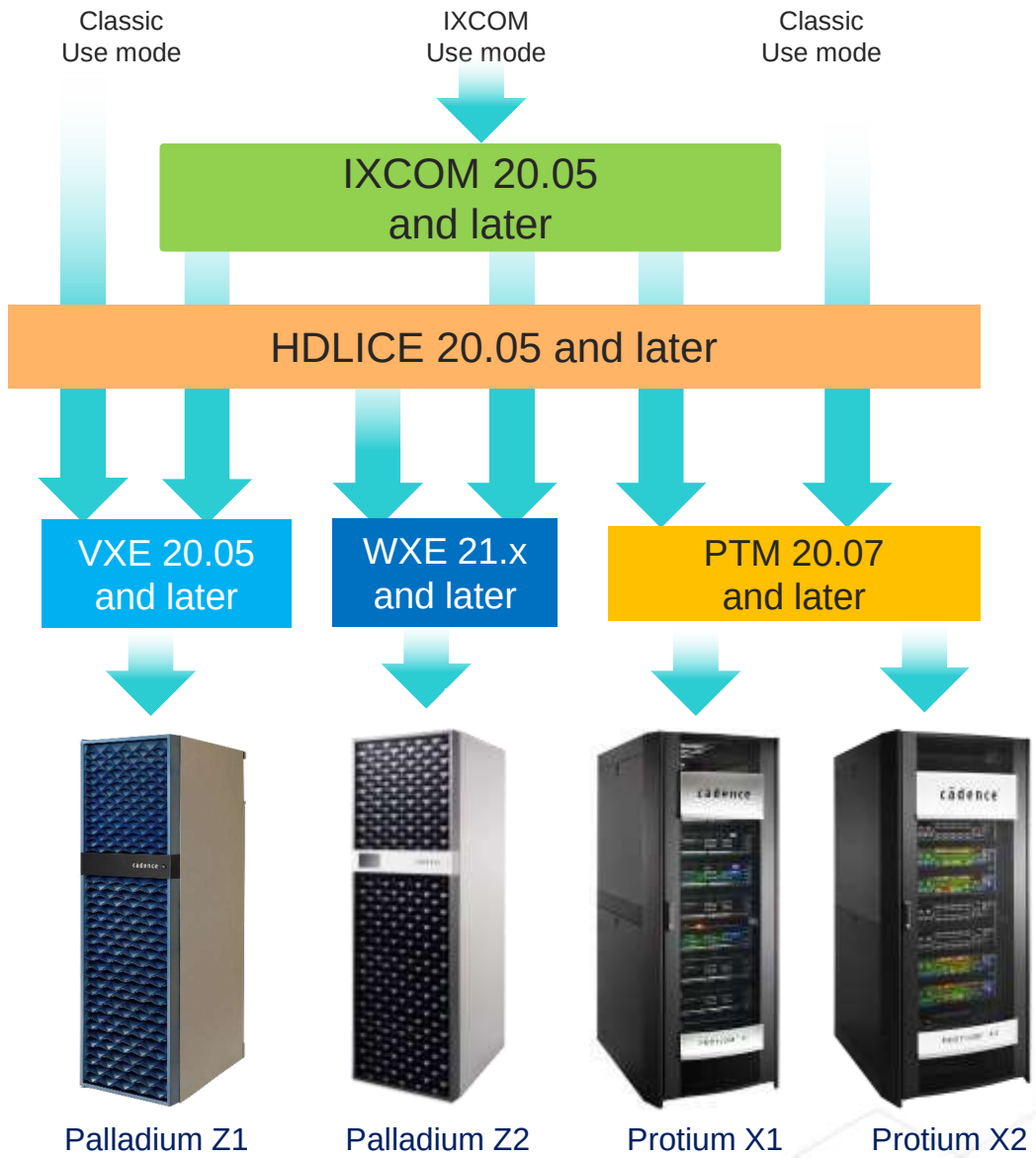
- 不需要人工手写任何时序约束脚本

全自动化集成的FPGA布局布线

- 所有脚本由工具自动生成

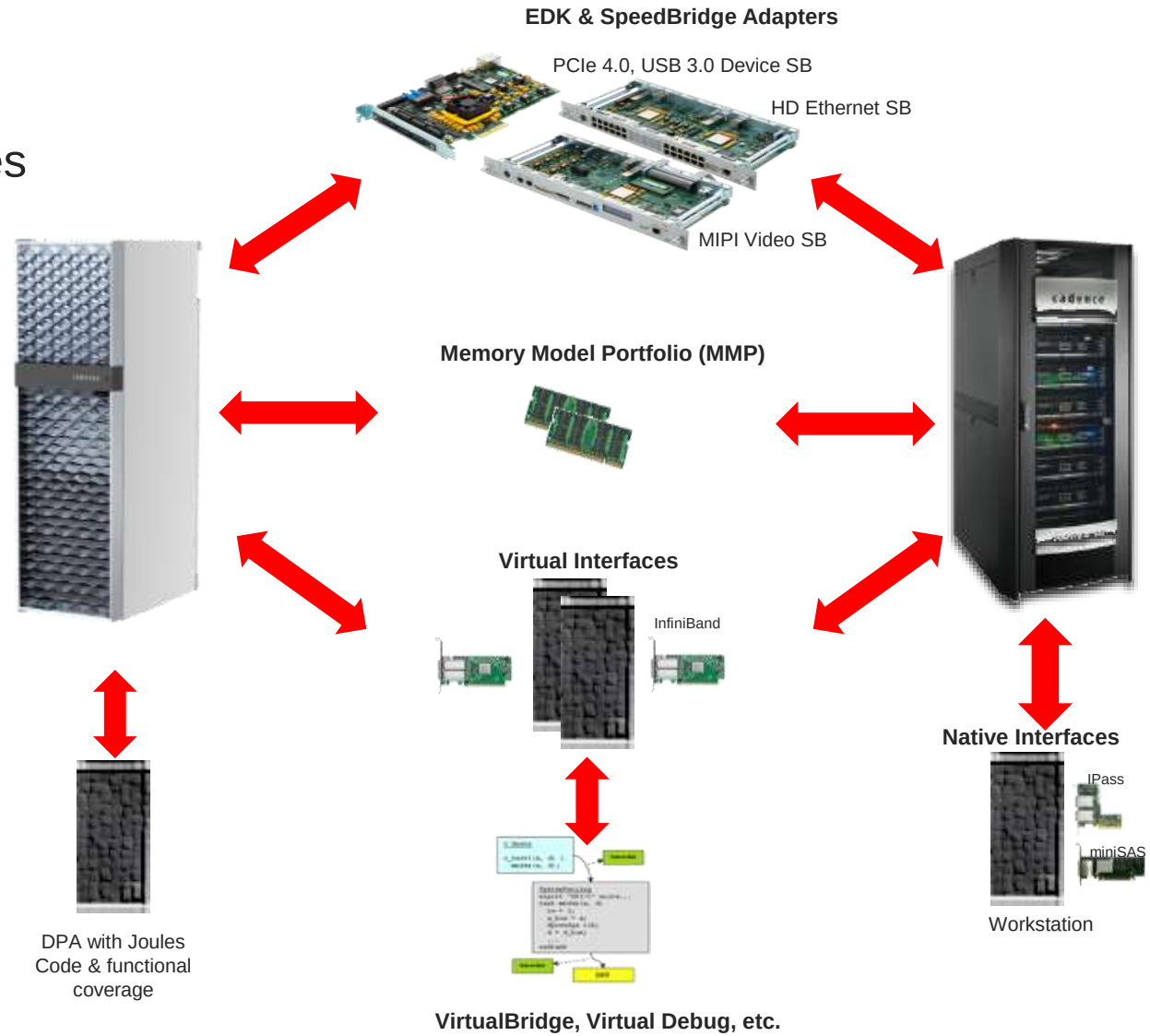
# Palladium and Protium: Common Front-end Compile

- No need to learn a new front-end compiler
  - Same front-end experience
  - Simply re-target different backend and engine
  -
- One version of IXCOM for
  - Z1, Z2, X1, X2
- One version of HDLICE for
  - Z1, Z2, X2, X2
- Mix and match releases
  - IXCOM, HDLICE, VXE, PTM



# Comprehensive Interface Solutions

- EDKs and SpeedBridge Adapters
  - Physical connection to real-world interfaces
- Memory Model Portfolio (MMP)
  - For all on-chip and off-chip memories
    - DDR, Flash, UFS, eMMC, SRAM, ROM etc.
  - Memory backdoor access
- Virtual Solutions
  - VirtualBridge, AVIP, Hybrid, Virtual Debug
  - InfiniBand-based link to virtual interfaces
- Palladium only
  - Dynamic Power Analysis with Joules
  - Code and functional coverage
- Protium only: native interfaces
  - Highest throughput
  - “breaks” congruency



# Introducing Protium X2

*Data-center class Prototyping System*

- FPGA-based prototyping platform
  - Fully customizable from single blade (desktop) to multi-rack
  - Mix and match with X1 hardware at the rack level
- Unmatched prototyping productivity
  - 1.5x performance and 2x capacity over X1
  - Fully integrated FPGA place & route
- Datacenter-class prototyping system
  - Up to 2,400MG per rack (480MG per blade)
  - Up to 60 concurrent users per rack (12 users per blade)
  - Multi-rack capable
- Virtualization and Eco-systems
  - Multi-host IXCOM flow with 2x the bandwidth over X1
  - Compatibility with SpeedBridge, VirtualBridge, AVIP and MMP
  - Native support for high-performance interface IP

# Protium X2 Blade Configurations

- 6U Blade
  - 12 Xilinx VU19P FPGAs
    - 2 boards with 6 FPGAs each
    - Up to 480MG
  - Supports up to 4 IO-cards (SB interfaces)
  - Available now

- 3U Blade
  - 6 Xilinx VU19P FPGAs
    - 1 boards with 6 FPGAs
    - Up to 240MG
  - Supports up to 2 IO-cards (SB interfaces)
  - Available in Q3’21 (see roadmap)

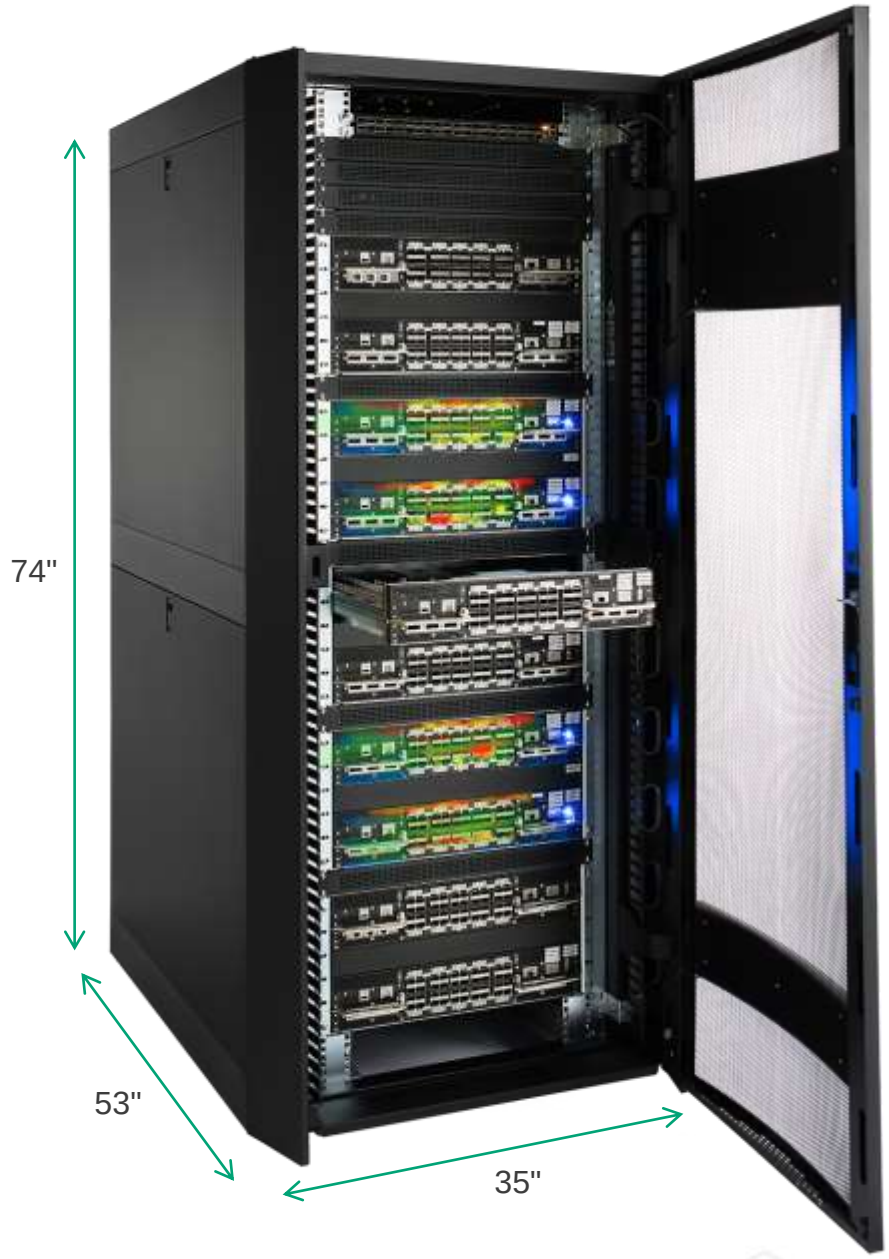
- Common Features
  - 10Gb & 40Gb Ethernet (control & management interface)
  - 200Gbps InfiniBand host interface (IXCOM, AVIP, VB, DPI, Hybrid)
  - 2 daughter-cards per FPGA
  - Can be used as stand-alone desktop system

6U

3U

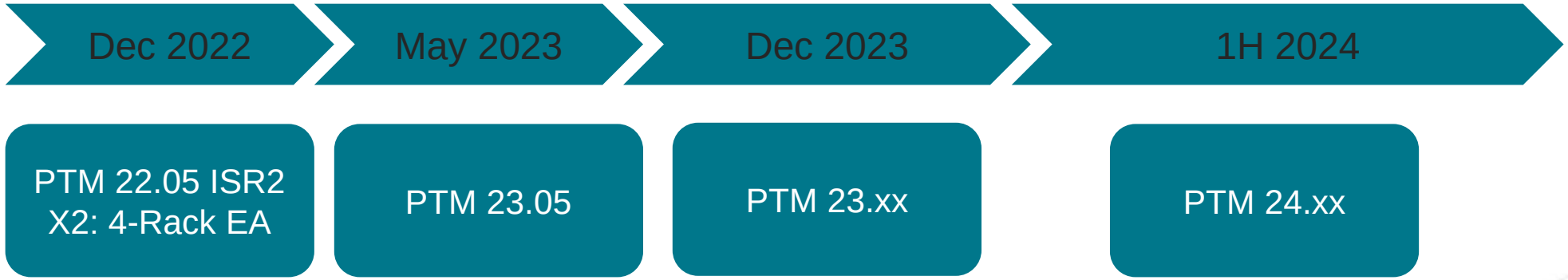
# Protium X2 Rack

- Standard rack size (w^x^d^x^h: 35in^x^53in^x^74in)
  - Wider and deeper than the X1 rack
- Requires two feet of floor space on each side for cabling and maintenance.
- Up to 5 6U-blades per rack
- Pre-installed PDUs
- Pre-installed 10G ethernet switch
- Has room for host on top
- Has room for InfiniBand Switch
- Removable covers on all sides
- Power requirements (typical):
  - 3U blade: 1,500W
  - 6U blade: 3,000W
  - Full rack: 15,300W
- Cooling: blade fans, front to back airflow



# Protium 2023 Updates

- PTM 23.05
  - Software FullVision performance and ALU support
  - Die-based Partitioning (SLR)
  - Record & Replay
  - Streaming DPI push
- Current and Future Projects:
  - Performance: Logic and memory synthesis QoR, critical path and multi-clock handling
  - Compile: Hierarchical Partition, Partition Replay, Distributed Compile
  - Debug: SDL, Deposit, Compiled Streaming Probe, SVA performance



# Deployment  - Advance Features

- swFullvision (have demoed basing ZEKU's database)
  - Dump the whole design signals
  - No compile-time probe
  - Support trigger
- DCC – Data Capture Card
  - Probe 16k – 32k signals per card
  - No runtime speed penalty
  - 16M cycles sample @16k signals
  - Support trigger position
- Save/Restore
  - Save the snapshot after OS bootup or other time to save run time
  - Save for another job with higher priority
  - Save for issue debug to reduce rerun time

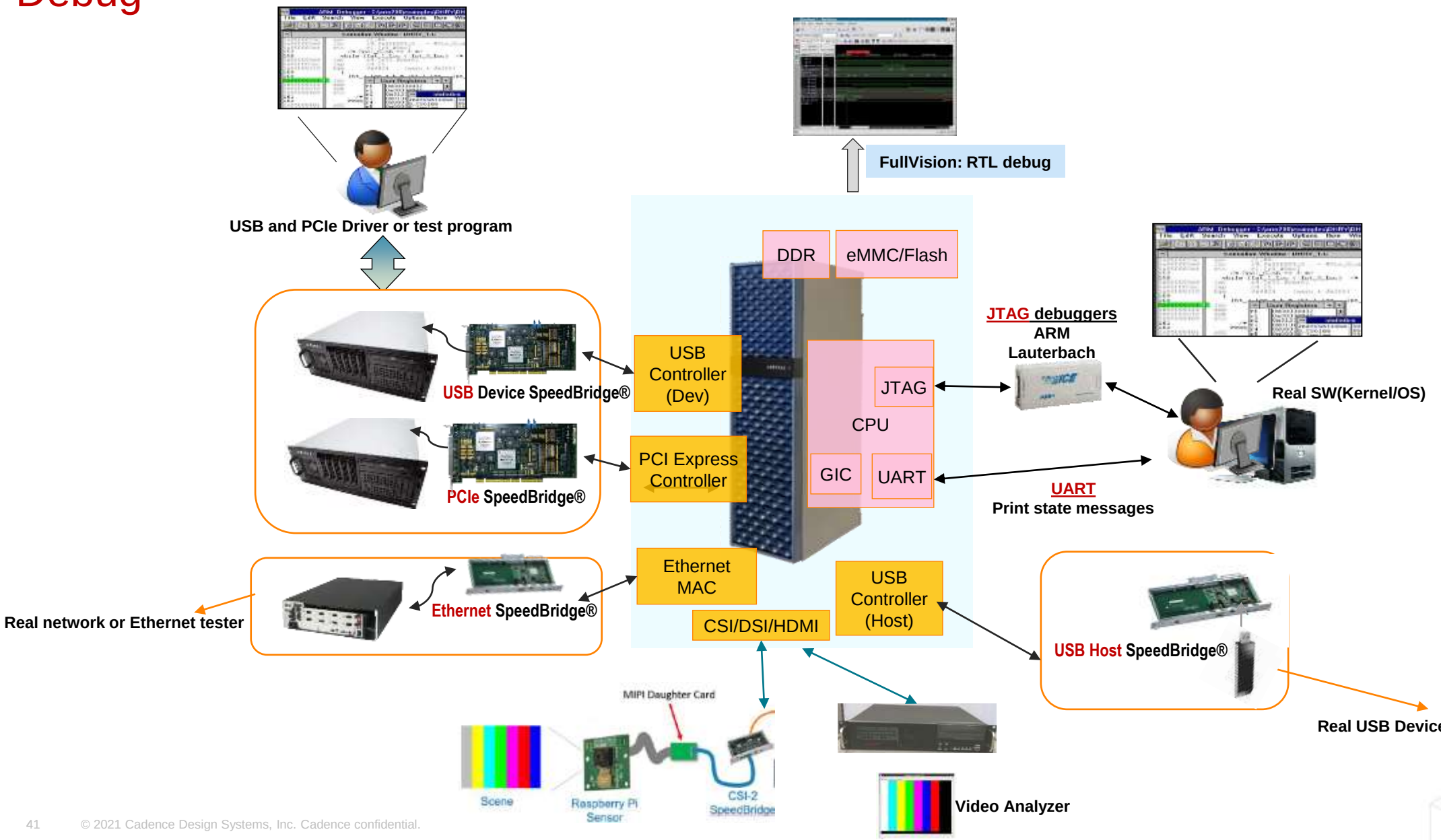
# Deployment - SpeedBridge

## Prototyping in the real physical environment

- PCIe Gen5
- Ethernet 1G-800G
- MIPI CSI/DSI
- Video HDMI/DP
- USB 3.2 host/device
- 5G
- WLAN
- SAS
- SATA
- SRIO
- JTAG/UART

# **Palladium**: HW/SW Co-verification Environment

## Debug



# **Protium**: SW Development on Prototyping

*Performance*

- 5-10Mhz on Billion Gate design
- Fast bring-up
- Maintain same env with Palladium

USB and PCIe Driver or test program

USB Device SpeedBridge®

PCIe SpeedBridge®

Ethernet SpeedBridge®

Real network or Ethernet tester

CSI/DSI/HDMI

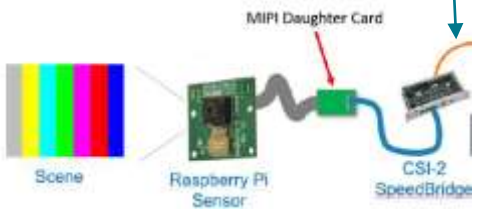
JTAG debuggers
ARM
Lauterbach

Real SW(Kernel/OS)

UART
Print state messages

USB Host SpeedBridge®

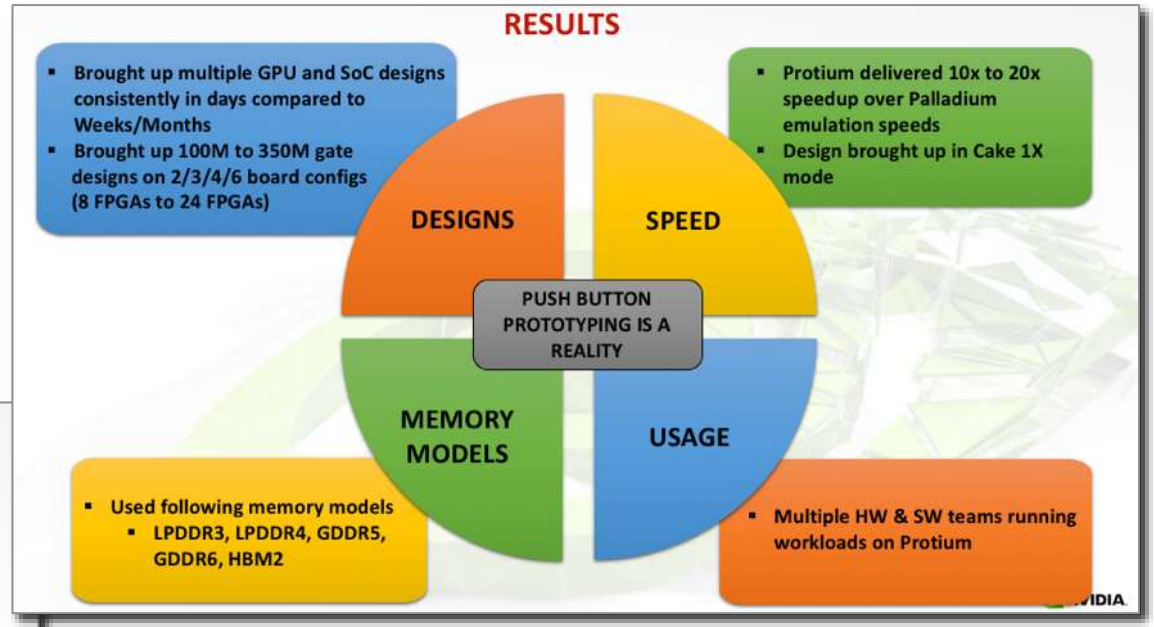
Real USB Device Connected

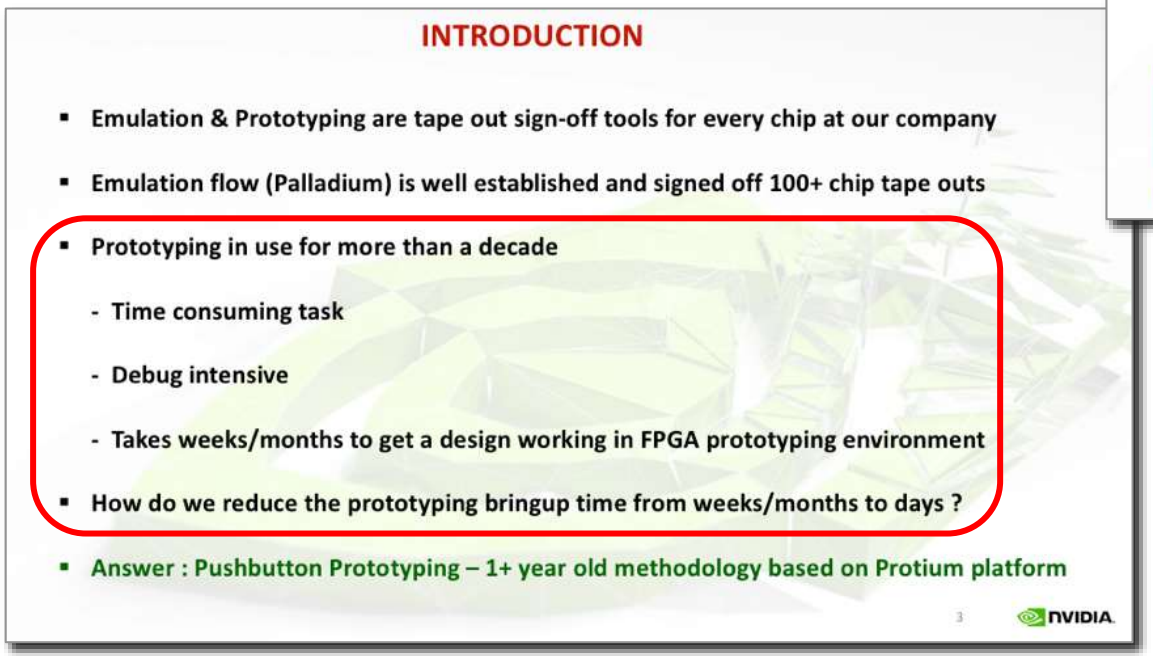



Video Analyzer

# Nvidia Pushbutton Prototyping

- Fast, 2-day, migration form emulation to prototyping
- 10x runtime speed-up
- Maintaining emulation congruency – common flow



# DeepChip – Protium Voted “Best of 2019”
# IBA: - Z2 & X2 “2021 Best Hardware in Semiconductor”

What the EDA users REALLY think
**DEEPCHIP**

cadence Spectre X Simulator

( DAC'19 Item 1a ) ---------- [12/19/19]

Subject: CDNS Protium crazy fast "Palladium-compiles" #1a for Best of 2019

**FAST COMPILES ROCK!**: My quick-and-dirty summary of the emulator/prototyper world. Say you have two designs to simulate. One design is 200 million gates, the other design is 1 Billion gates.

| | Initial Ramp Up Time / Incremental Compile Time | Operating Speed |
|---|---|---|
| **Palladium** | initial ramp 2-4 weeks | |
| 200 M gates | 1.0 hour | 1.2 Mhz |
| 1.0 B gates | 5.0 hours | 800 Khz |
| **Zebu Server 4** | initial ramp 4-6 weeks | |
| 200 M gates | 25.8 hours (1.1 days) | 2.0 Mhz |
| 1.0 B gates | 41.2 hours (1.7 days) | 750 Khz |
| **HAPS-80** | initial ramp 2-3 months | |
| 200 M gates | 93.6 hours (3.9 days) | 20.0 Mhz |
| 1.0 B gates | 146.4 hours (6.1 days) | 5.0 Mhz |
| **Veloce Strato** | initial ramp 3-5 weeks | |
| 200 M gates | 5.1 hours | 1.6 Mhz |
| 1.0 B gates | 12.5 hours | 750 Khz |
| | ramp 24 hours w/Palladium | |
| **Protium** | ramp 4-6 weeks w/o Palladium | |
| 200 M gates | 28.8 hours (1.2 days) | 8.3 Mhz |
| 1.0 B gates | 50.4 hours (2.1 days) | 4.5 Mhz |

- **Technical Innovation of the Year**
- **Best Hardware in Semiconductor**

## Palladium® Z2 and Protium™ X2


**Technical Innovation of the Year**
**Best Hardware in Semiconductor**

# Protium 平台横向对比

| Feature | Protium X1 | Protium X2 | Comments |
|---|---|---|---|
| **容量 & FPGA** | **VU440** | **VU19P** | |
| 刀片式电路板 | 1.5亿门/blade | 4.8亿门/blade | X2每个刀片集成了12片VU19P FPGA |
| 机柜容量 | 12亿门 | 24亿门 | 48 FPGA per X1 rack; 60 FPGAs per X2 rack |
| 最大可扩充容量 | 48亿门 | 96亿门 | X1和X2都支持4个机柜级联 |
| **典型性能** | 1x | 1.5x | X2相对于X1约有1.5倍提升 |
| **服务器主机接口** | | | |
| 控制和管理 | 10G以太网 | 40G以太网 | |
| 虚拟模型和测试环境 | 100Gbps InfiniBand | 200Gbps InfiniBand | |
| **板上系统架构** | PCIe gen3 (2x) | PCIe gen4 (4x) | PCIe gen4 大幅度提升了调试相关速率和流量， 如memory upload/download, probing 等) |
| **每片FPGA配备的PTMBC接口** | 24 | 26 - 31 | PTMBC接口数量越多越有利于性能优化 |
| **冗余供电模块** | 无 | 3+1 | |
| **多用户** | 每个电路板可支持一个用户 | 单FPGA可支持单用户 | |
| **增强的调试能力** | DPI | 2x DPI throughput<br>2x – 10x 调试吞吐量 | 2倍速的IB交换<br>4倍速的内部总线 |