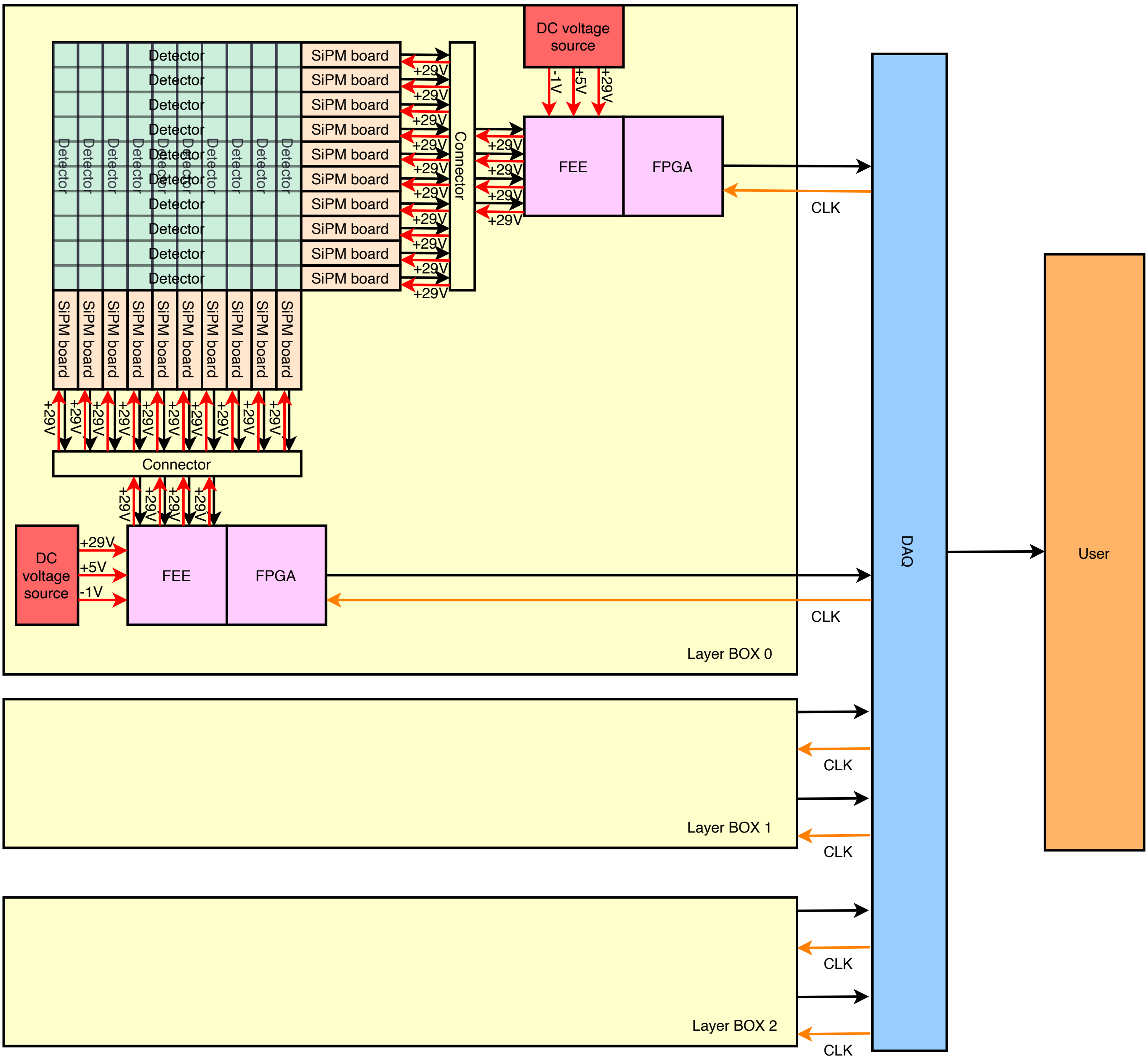
SiPM readout electronics

Detector

- there are 3 boxes
- each box have 2 layers scintillator, they are located in x,y direction.
- each layer have 10 modules, each module have 4 scintillator bars
- each scintillator bar have 1 SiPMs
- we have 3 * 2 * 10 * 4 = 240 Scintillator and SiPMs in total

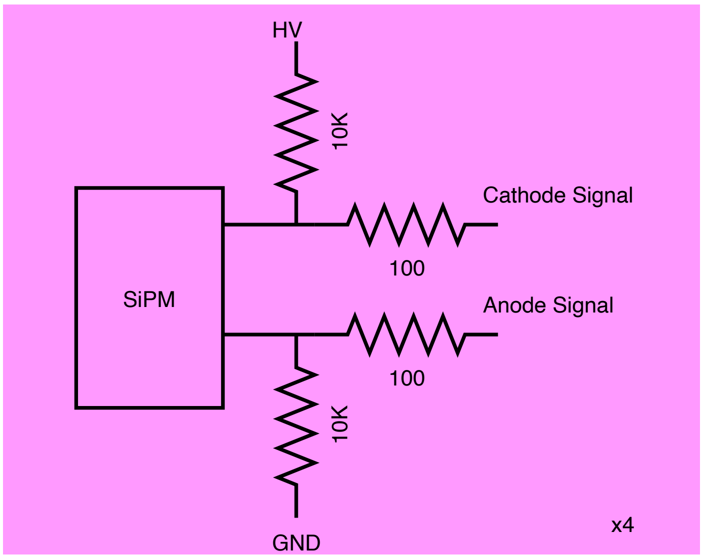
Basic connection

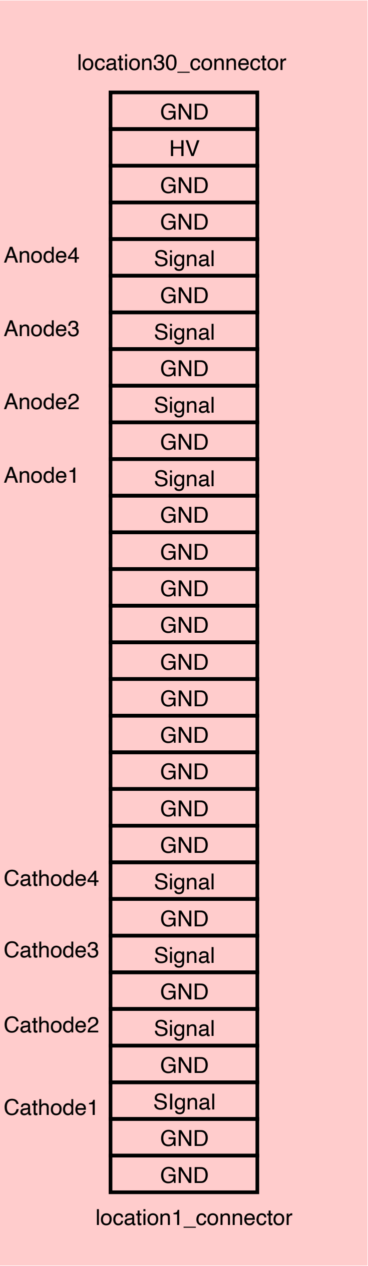
- each layer connect to one FEE and FPGA board
- each FEE and FPGA board have 64 channels,but we only use 40 channels
- each box have 2 FEE and FPGA board
- The FEE and FPGA board get CLK from DAQ and use LVDS send data to DAQ
- One DAQ get 3 boxes data and send to PC
- we can set the coincidence mode and coincidence window in DAQ by configure the switch on the board



SiPM board

- each SiPM board have 4 SiPMs
- each SiPM have 2 signal output, one is positive, one is negative
- SiPM board get HV from connector





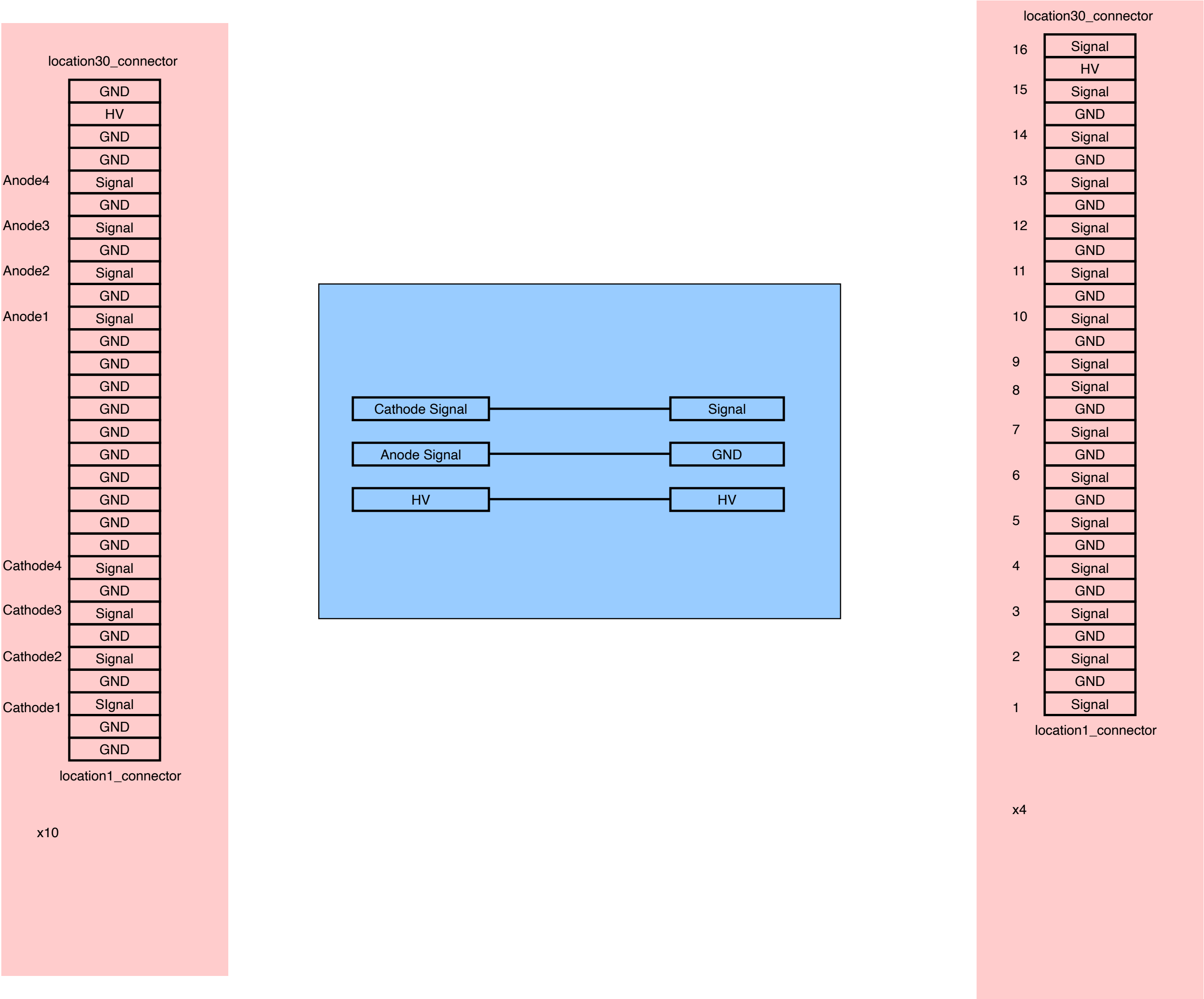
location30_connector

	GND
	HV
	GND
	GND
Anode4	Signal
	GND
Anode3	Signal
	GND
Anode2	Signal
	GND
Anode1	Signal
	GND
	GND
	GND
	GND
	GND
	GND
	GND
	GND
	GND
	GND
Cathode4	Signal
	GND
Cathode3	Signal
	GND
Cathode2	Signal
	GND
Cathode1	SIgnal
	GND
	GND

location1_connector

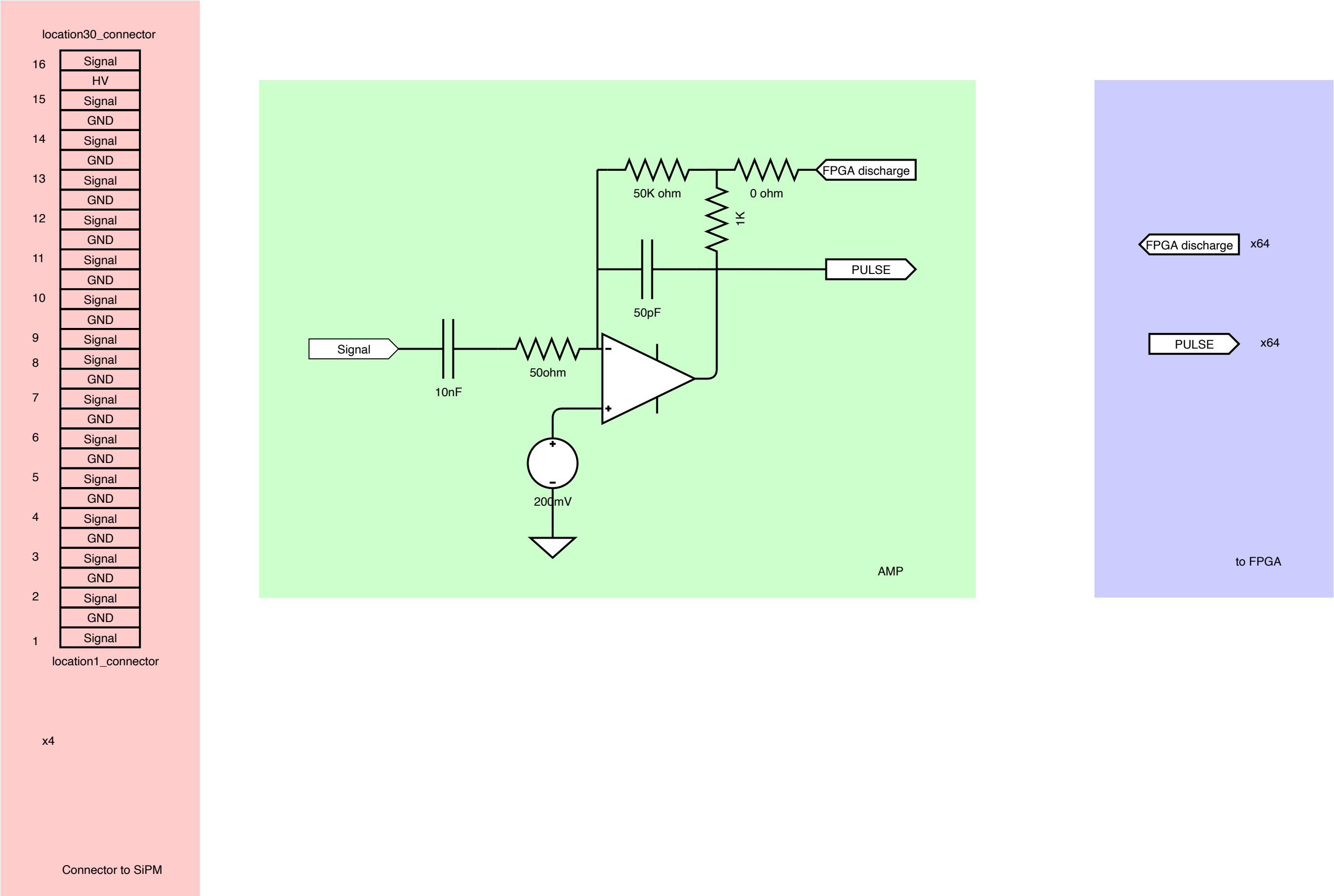
Connector board

- each connector board connect to 10 SiPM board
- connector get the cathode signal from SiPM board and send to FEE board
- connector get the anode signal from SiPM board but send it to GND
- connector get the HV from FEE board and send it to SiPM board



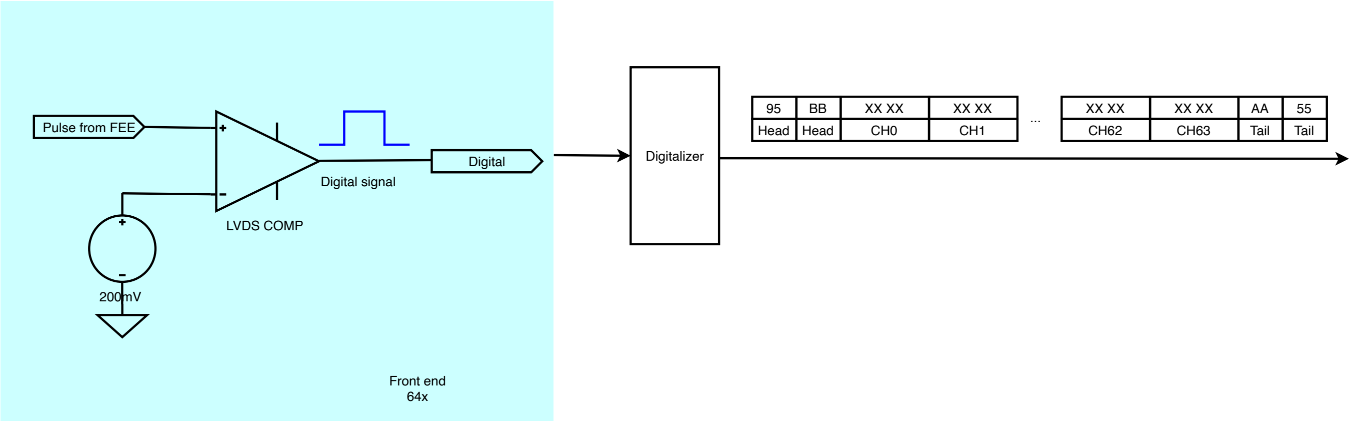
FEE (front end Electronics)

- each FEE board have 64 channels, we use 40 channels
- FEE get the cathode signal from connector board, get the HV from DC Voltage source.
- FEE get discharge signal from FPGA board and send the pulse to FPGA board



FPGA board

- each FPGA board have 64 channels, we use 40 channels
- FPGA get the pulse from FEE board and use inner LVDS comparator compare the pulse with threshold, and get the digital signal
- we can adjust the threshold by change the register of DC/DC circuit in FPGA board. usually we set the threshold to 0.2V
- FPGA get the CLK from DAQ board and send the data to DAQ board
- all parameters and feature can be find at "discharge_time_digitalize.v" file

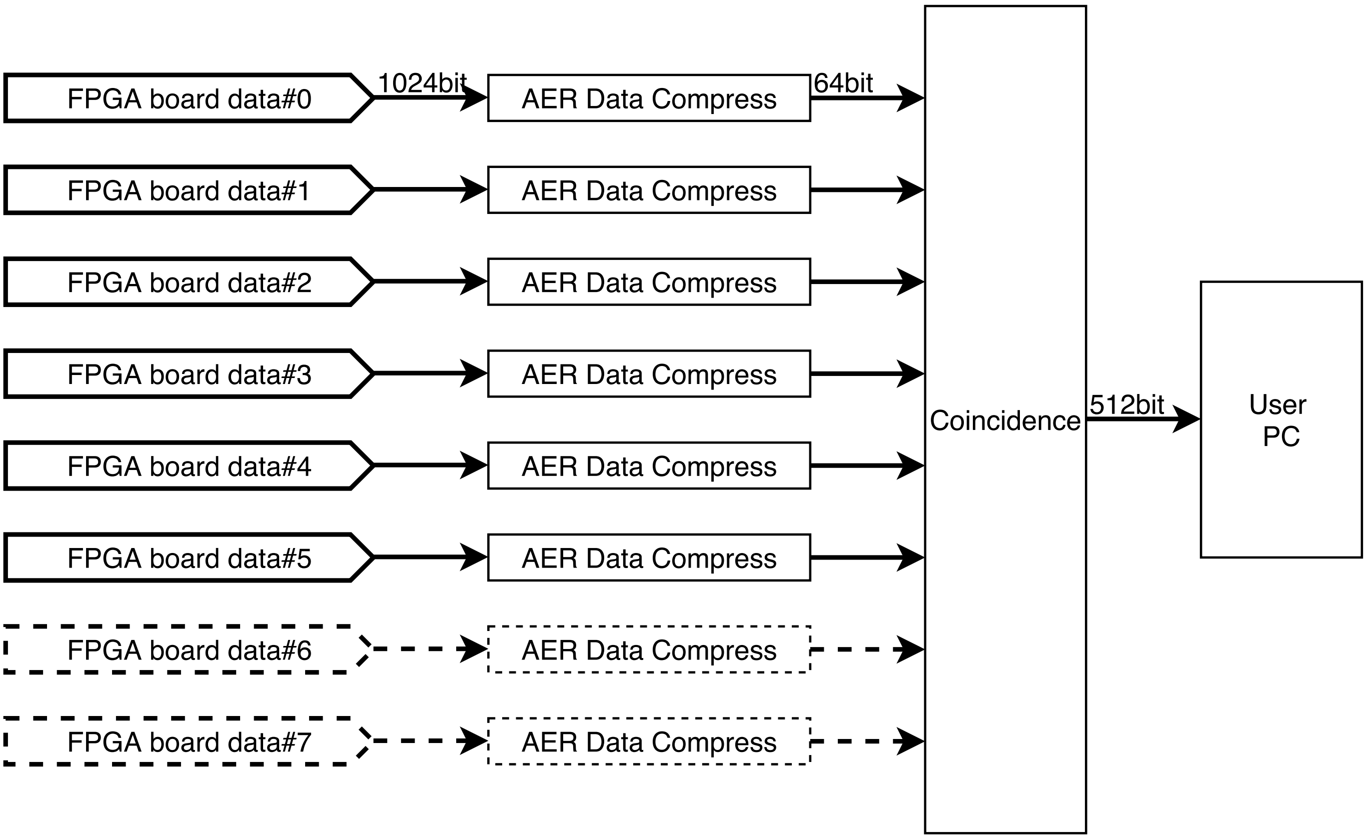


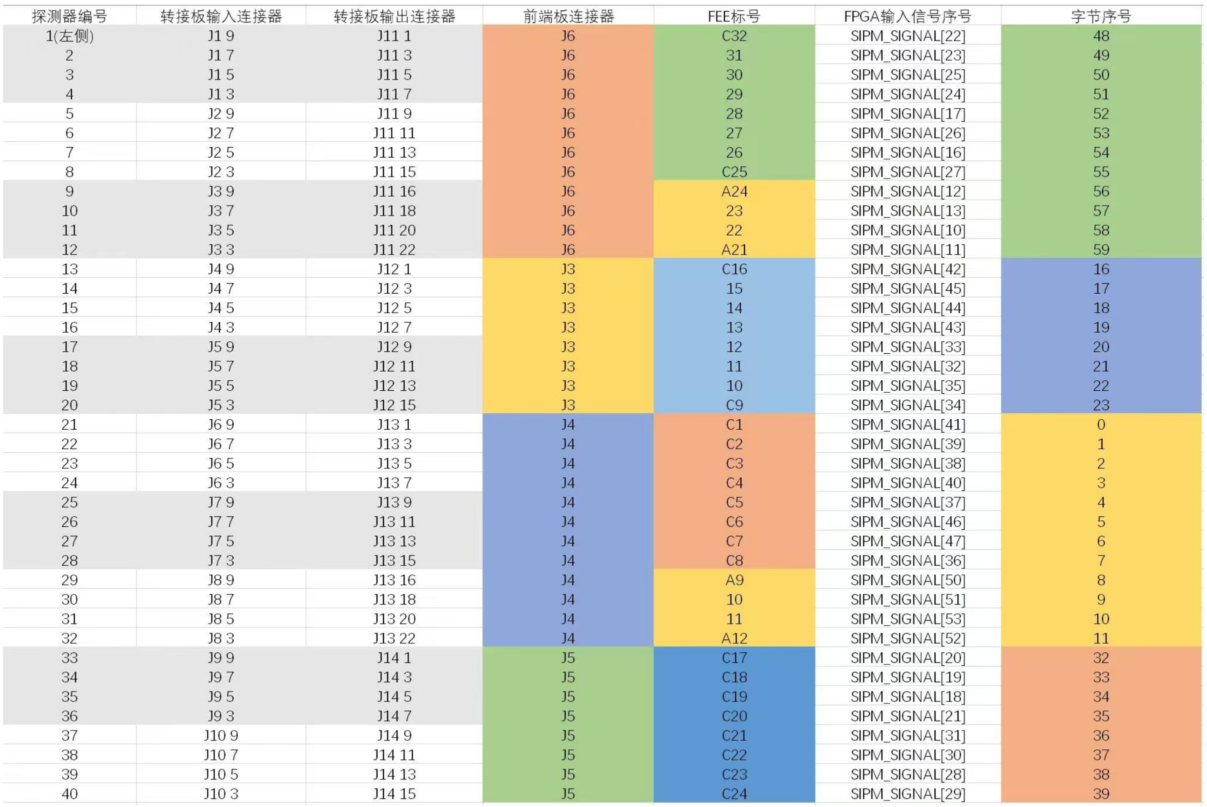
95	BB	XX XX	XX XX	XX XX	XX XX	AA	55
Head	Head	CH0	CH1	CH62	CH63	Tail	Tail

DAQ (Data Acquisition)

- each DAQ board can get data from 16 FPGA board but now we only use 6 FPGA board
- DAQ board get the data from FPGA board, send CLK to FPGA board, compress data and send to PC by UART

- we can set the coincidence mode and coincidence window in DAQ by configure the switch on the board



- DAQ data format
  - FPGA board data output [1024 bit]/[128 byte] per event
  - every 2 byte is one channel data
  - 

探测器编号	转接板输入连接器	转接板输出连接器	前端板连接器	FEE标号	FPGA输入信号序号	字节序号
1(左侧)	J1 9	J11 1	J6	C32	SIPM_SIGNAL[22]	48
2	J1 7	J11 3	J6	31	SIPM_SIGNAL[23]	49
3	J1 5	J11 5	J6	30	SIPM_SIGNAL[25]	50
4	J1 3	J11 7	J6	29	SIPM_SIGNAL[24]	51
5	J2 9	J11 9	J6	28	SIPM_SIGNAL[17]	52
6	J2 7	J11 11	J6	27	SIPM_SIGNAL[26]	53
7	J2 5	J11 13	J6	26	SIPM_SIGNAL[16]	54
8	J2 3	J11 15	J6	C25	SIPM_SIGNAL[27]	55
9	J3 9	J11 16	J6	A24	SIPM_SIGNAL[12]	56
10	J3 7	J11 18	J6	23	SIPM_SIGNAL[13]	57
11	J3 5	J11 20	J6	22	SIPM_SIGNAL[10]	58
12	J3 3	J11 22	J6	A21	SIPM_SIGNAL[11]	59
13	J4 9	J12 1	J3	C16	SIPM_SIGNAL[42]	16
14	J4 7	J12 3	J3	15	SIPM_SIGNAL[45]	17
15	J4 5	J12 5	J3	14	SIPM_SIGNAL[44]	18
16	J4 3	J12 7	J3	13	SIPM_SIGNAL[43]	19
17	J5 9	J12 9	J3	12	SIPM_SIGNAL[33]	20
18	J5 7	J12 11	J3	11	SIPM_SIGNAL[32]	21
19	J5 5	J12 13	J3	10	SIPM_SIGNAL[35]	22
20	J5 3	J12 15	J3	C9	SIPM_SIGNAL[34]	23
21	J6 9	J13 1	J4	C1	SIPM_SIGNAL[41]	0
22	J6 7	J13 3	J4	C2	SIPM_SIGNAL[39]	1
23	J6 5	J13 5	J4	C3	SIPM_SIGNAL[38]	2
24	J6 3	J13 7	J4	C4	SIPM_SIGNAL[40]	3
25	J7 9	J13 9	J4	C5	SIPM_SIGNAL[37]	4
26	J7 7	J13 11	J4	C6	SIPM_SIGNAL[46]	5
27	J7 5	J13 13	J4	C7	SIPM_SIGNAL[47]	6
28	J7 3	J13 15	J4	C8	SIPM_SIGNAL[36]	7
29	J8 9	J13 16	J4	A9	SIPM_SIGNAL[50]	8
30	J8 7	J13 18	J4	10	SIPM_SIGNAL[51]	9
31	J8 5	J13 20	J4	11	SIPM_SIGNAL[53]	10
32	J8 3	J13 22	J4	A12	SIPM_SIGNAL[52]	11
33	J9 9	J14 1	J5	C17	SIPM_SIGNAL[20]	32
34	J9 7	J14 3	J5	C18	SIPM_SIGNAL[19]	33
35	J9 5	J14 5	J5	C19	SIPM_SIGNAL[18]	34
36	J9 3	J14 7	J5	C20	SIPM_SIGNAL[21]	35
37	J10 9	J14 9	J5	C21	SIPM_SIGNAL[31]	36
38	J10 7	J14 11	J5	C22	SIPM_SIGNAL[30]	37
39	J10 5	J14 13	J5	C23	SIPM_SIGNAL[28]	38
40	J10 3	J14 15	J5	C24	SIPM_SIGNAL[29]	39

  - [channel63high,channel63low....channel0high,channel0low]

    - if you find byte100 is 0x22,byte101 is 0x11, it means “字节序号50”，“探测器编号3” channel data is 0x1122
- data compress
    - cosmic ray signal is rare, so we can compress the data by remove the 0 data
    - we can compress one FPGA board data to 8/16 byte
    - data format is
    - 8bit compress[byteaddr0,byte0,byteaddr1,byte1,byteaddr2,byte2,byteaddr3,byte3]
    - 16bit compress[byteaddr0,byte0,byteaddr1,byte1,byteaddr2,byte2,byteaddr3,byte3,byteaddr4,byte4,byteaddr5,byte5,byteaddr6,byte6,byteaddr7,byte7]
    - notice that is the byte address,if a signal adc value <256,it will only cost 1 byte to store the data,if the adc value >256,it will cost 2 byte to store the data.
    - so in the case of 8 byte compress, we can get 4 channel data at maximum, 2 channel data at minimum
    - in the case of 16 byte compress, we can get 8 channel data at maximum, 4 channel data at minimum
- data pack to User PC(uart)
    - [header(11111100),DAQ0(8/16byte),DAQ1(8/16byte),DAQ2(8/16byte),DAQ3(8/16byte),DAQ4(8/16byte),DAQ5(8/16byte),DAQ6(8/16byte)(0 now),DAQ7(8/16byte)(0 now),end(00000011)]
- user data reconstruct
    - we can use the header and end to get package
    - check package length to filter the data
    - reconstruct the data to get the channel data