**IE3-DI Digital Circuits LAB REPORT**

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| --- | --- |
| Lab session (please tick)  1 2 3 4× | Topic:  Design of traffic light controllers in VHDL |
| Lab group (please tick)  01 02 03  Team name / number | Team members Responsible Author   (please tick) |
| 1. Muhammad Adib Bin Ali × |
| 2 Ievgenii Nudga × |
| 3  |

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| --- | --- |
| correctness of **lab preparation** (hard copy) | / 5 pts. |
| **lab tasks** successfully completed (proven by protocol) | / 5 pts. |
| **lab report**  purpose and set-up of the lab tasks are properly introduced and supported by sketches, figures, flowcharts, etc. results are summarized at the end  correctness of information given in report  results are proven by e.g. measurements, simulations, calculations, source code etc. and have been discussed  correctness of formal aspects, e.g. figures with numbers and captions, citation of foreign sources, structure, spelling and style | / 3 pts.  / 2 pts.  / 2 pts.  / 3 pts. |
| **sum** |  |
|  | |

Task 1.1

The VHDL code was implemented on the CPLD and it was working according to specification

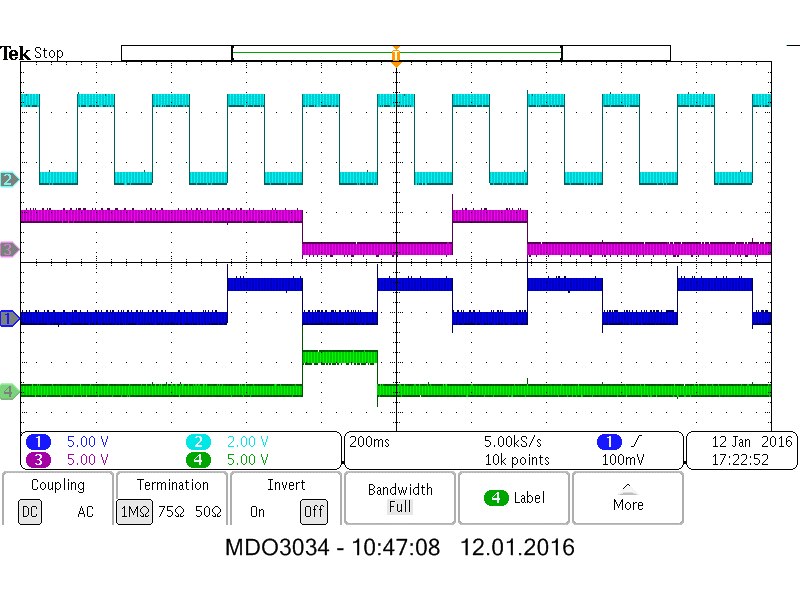


Figure 1: Transition from day to night

Task 2.1

The traffic light controller from Lab Task 1.1 was extended to model the durations of the traffic light phases. The counter developed in Prep Task 2.1 was added and instantiated to realise this.

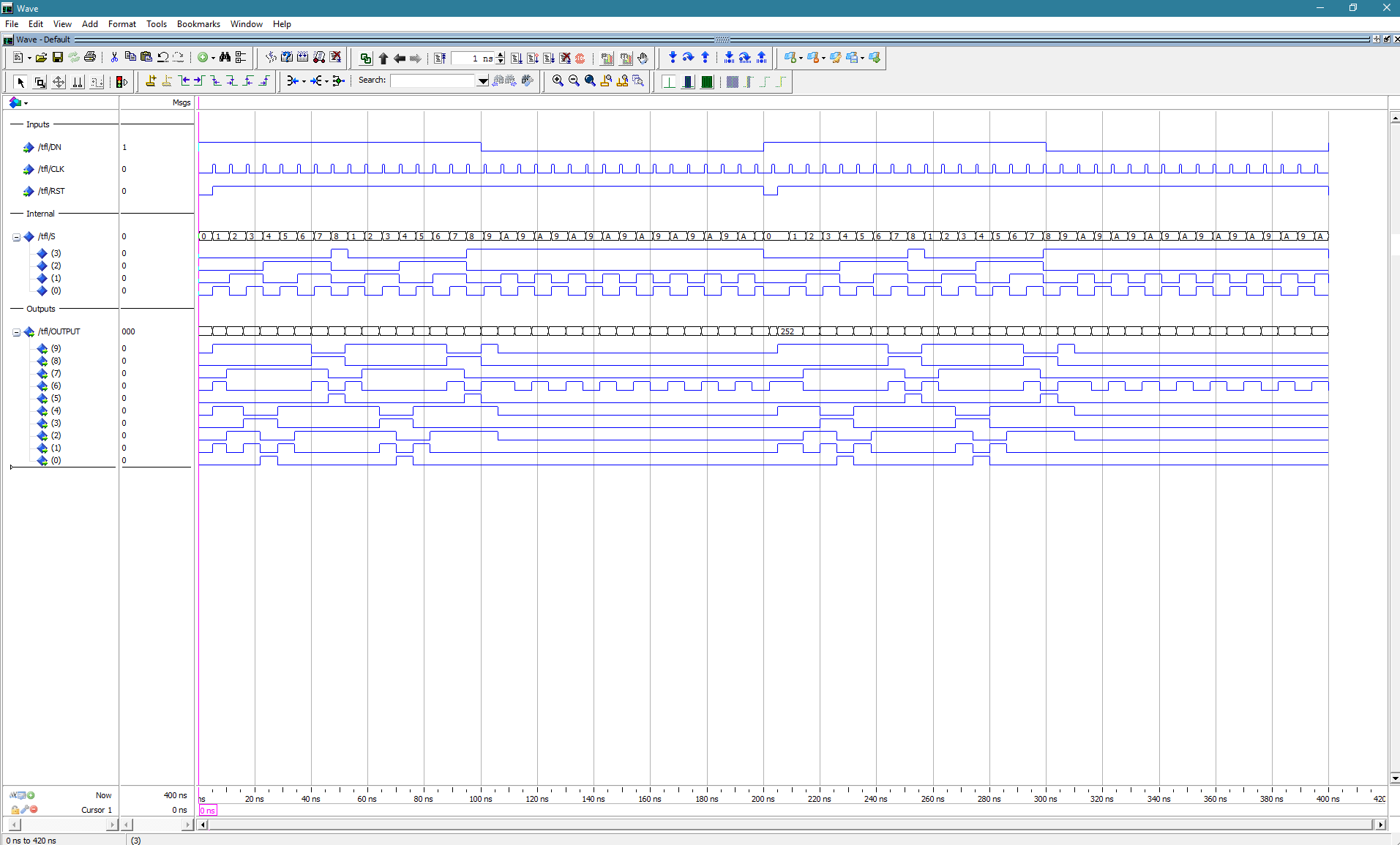


Figure 2: Two cycles of day and night

Output CLRN is Moore type because it only depends on current state and not current input.

Due to time restrictions, we were not able to implement the traffic light controller and get the measurements.