Khulna University of Engineering & Technology

Department of CSE

CSE 4224 : DIGITAL SYSTEM DESIGN LABORATORY

Lab Report

IMPLEMENTING SAP-1 USING LOGISIM

Submitted By:

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Year: 4th
Semester: 2nd
Date: 15.6.21

Objectives:

Objectives are given below:

- To gather knowledge about the architecture of SAP-1 (Simple-As-Possible).
- To implement SAP-1 circuit using logisim.
- To learn about the functionalities of Program counter, Memory address Register, flipflop RAM, IR, controller, accumulator & so on.

Introduction:

The Simple-As-Possible (SAP)-1 computer is a very basic model of a microprocessor explained by Albert Paul Malvino. The SAP-1 design contains the basic necessities for a functional Microprocessor. Its primary purpose is to develop a basic understanding of how a microprocessor works, interacts with memory & other parts of the system like input & output. The instruction set is very simple & limited. SAP can only perform addition & subtraction & no logical operation.

The architecture of SAP-1 is a bus-organized computer. All register outputs to the W-bus are three-state; this allows orderly transfer of data. All other register outputs are two-state; these outputs continuously drive the busses they are connected to.

Program Counter:

- It counts from 0000 to 1111
- It signals the memory address of next instruction to be fetched & executed.

Inputs & MAR:

- During a computer run, the address in Program counter is latched into Memory Address Register (MAR).

The RAM:

- The Program code to be executed & data for SAP-1 computer is stored here.
- During a computer run, the RAM receives 4-bit address from MAR & a read

operation is performed. Hence, the instruction or data would stored in RAM is placed on the M bus for use by some other part of the computer.

It is asynchronous RAM, which means that the output data is available as soon as valid address & control signal are applied.

IR (Instruction Register):

IR contains the instruction (composed of (OPCODE + ADDRESS) to be executed by SAP-1 computer.

Controller - Sequencer:

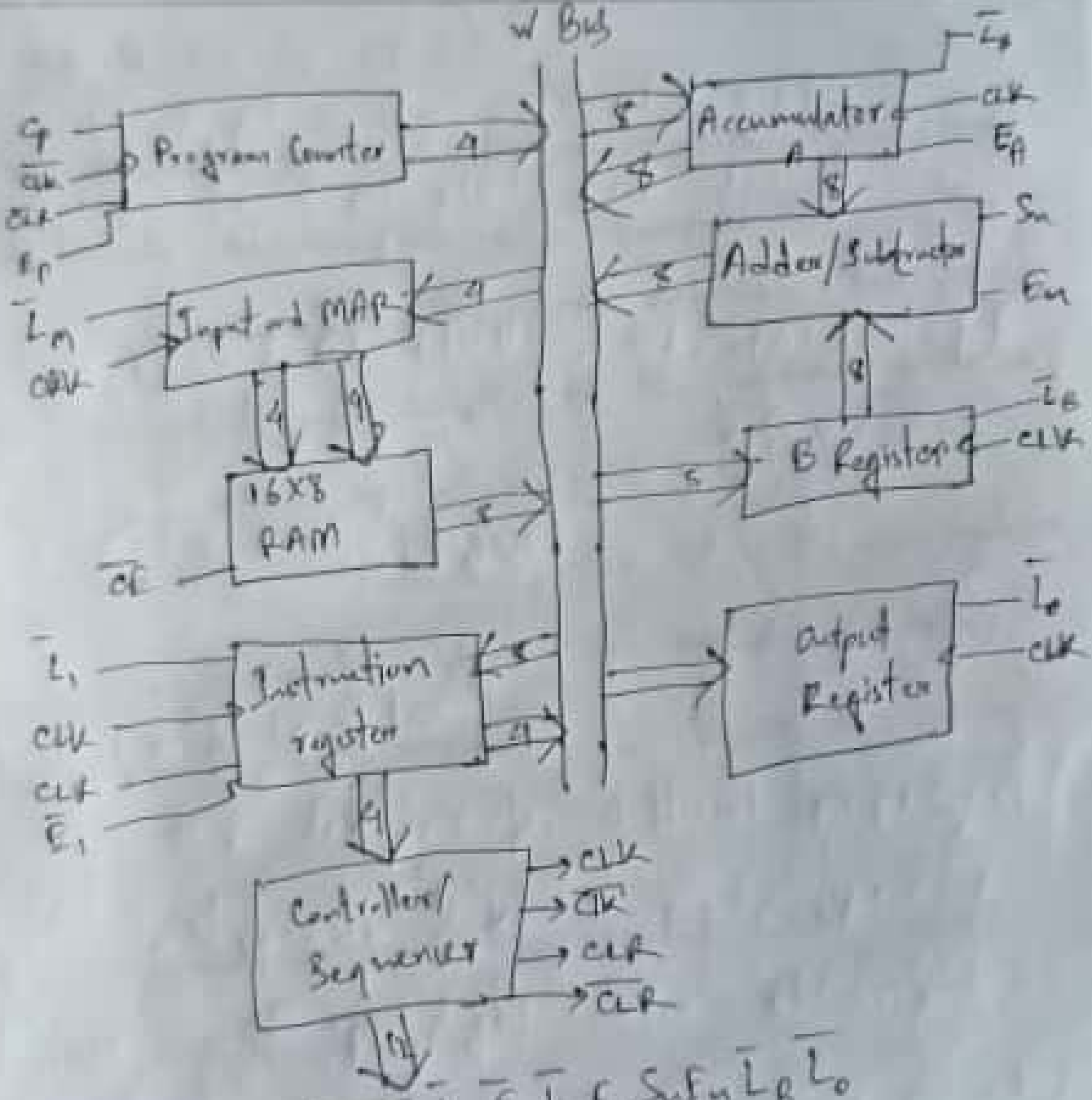
It generates the control signals for each block so that actions occur in desired sequence. CLK signal is used to synchronize the overall operation of the SAP-1 computer.

A 12-bit word comes out of the controller-sequencer block. This control word determines how the registers will react to the next positive clk edge.

Accumulator

The accumulator (A) is a buffer register that stores intermediate answers during a computer run. The Fig 5.1 accumulator has two outputs. The two state output goes directly to the adder-subtractor. The three state output goes directly to the W bus. Therefore, the 8 bit accumulator word continuously drives the adder-subtractor; the same word appears on the W bus when E_A is high.

The accumulator can be created with three buffer register.



$C_P E_P \bar{L}_M \overline{CE} \bar{L}_I \bar{E}_I \bar{L}_A E_A S_U E_M \bar{L}_B \bar{L}_O$

Fig 1.1: SAP-1 Architecture

B Register

The B register is another buffer register. It is used in arithmatic operations. A low $\overline{LB}$ and positive clock edge load the word on the w bus into B register. The two-state output A the adder. B register drives the adder subtractor, supplying the number to be added or subtracted from the contents of the accumulator.

Output Register:

At the end of a computer run, the accumulator contains the answer the problem being solved. At this point, these outputs would be given to binary display.

The Adder - Subtractor

SAP-1 uses a 2's-complement adder-subtractor. When S_u is low in Fig. 10-1, the sum out of the adder-subtractor is

$$S = A + B$$

When S_u is high, the difference appears:

$$A = A + B'$$

The adder-subtractor is asynchronous (unclocked); this means that its content can change as soon as the input words change. When E_u is high, these contents appear on the $\overline{w}$ bus.

Binary Display:

The output is shown in the display (LED).

Instructions:

Table 1.1 : SAP-1 OP CODE

Mnemonics	op code (Hex)
LDA	0000 (0)
ADD	0001 (1)
SUB	0010 (2)
OUT	1110 (E)
HLT	1111 (F)

Discussion:

Through this project, the construction of SAP 1 has been implemented using logisim. left part of SAP-1 such as PC, MAR, RAM, IR has been done by me & Right part of SAP1 (Accumulator, Adder/Substracter), B Register, Output Register, Binary display) has been done by my project partner. We implemented Controller sequence by diving this circuit equally. After loading file on RAM & enabling clock we sequencially get our desired output on Binary display.

Conclusion:

By performing this SAP-1 circuit, we gathered knowledge about PC, MAR, RAM, IR, Controller Sequencer, Accumulator, Adder/Substractor, Register, Binary display & their functionalities. We got clearification about ~~how~~ working principle of SAP-1 computer.