EXPERIMENT No.: - 12

Simulation of VHDL Models.

TITLE:

Implementation of JK flip-flop in VHDL using Behavioural Modelling.

OBJECTIVE:

To implement the Behavioural model of JK flip-flop in ISE Simulator.

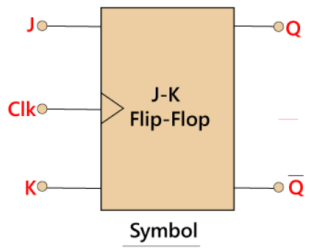
THEORY:

The JK flip flop is one of the most used flip flops in digital circuits. The JK flip flop is a universal flip flop having two inputs 'J' and 'K'. In SR flip flop, the 'S' and 'R' are the shortened abbreviated letters for Set and Reset, but J and K are not. The J and K are themselves autonomous letters which are chosen to distinguish the flip flop design from other types.

The JK flip flop work in the same way as the SR flip flop work. The JK flip flop has 'J' and 'K' flip flop instead of 'S' and 'R'. The only difference between JK flip flop and SR flip flop is that when both inputs of SR flip flop is set to 1, the circuit produces the invalid states as outputs, but in case of JK flip flop, there are no invalid states even if both 'J' and 'K' flip flops are set to 1.

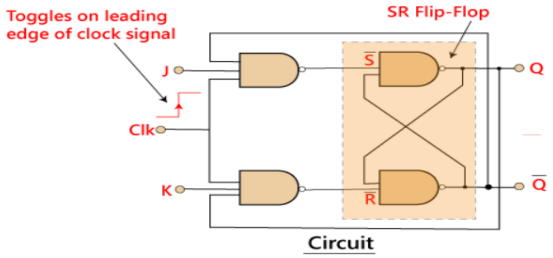
The JK Flip Flop is a gated SR flip-flop having the addition of a clock input circuitry. The invalid or illegal output condition occurs when both of the inputs are set to 1 and are prevented by the addition of a clock input circuit. So, the JK flip-flop has four possible input combinations, i.e., 1, 0, "no change" and "toggle". The symbol of JK flip flop is the same as **SR Bistable Latch** except for the addition of a clock input.

Block Diagram:



Symbol

Circuit Diagram:



Circuit

The truth table of JK flip-flop is given below: -

Clk	J	K	Q	Q'	State
1	0	0	Q	Q'	No change in state
1	0	1	0	1	Resets Q to 0
1	1	0	1	0	Sets Q to 1
1	1	1	-	-	Toggles

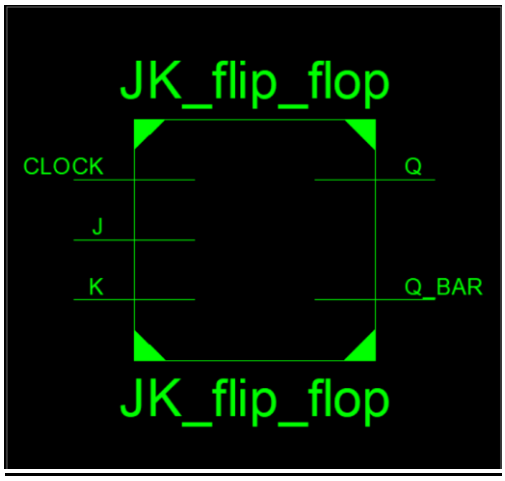
SOURCE CODE: -

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity JK_flip_flop is
    Port ( J : in  STD_LOGIC;
           K : in  STD_LOGIC;
           CLOCK : in  STD_LOGIC;
           Q : out  STD_LOGIC;
           Q_BAR : out  STD_LOGIC);
end JK_flip_flop;

architecture Behavioral of JK_flip_flop is

begin

                PROCESS(CLOCK)
                        variable TMP: std_logic;
                        begin
```

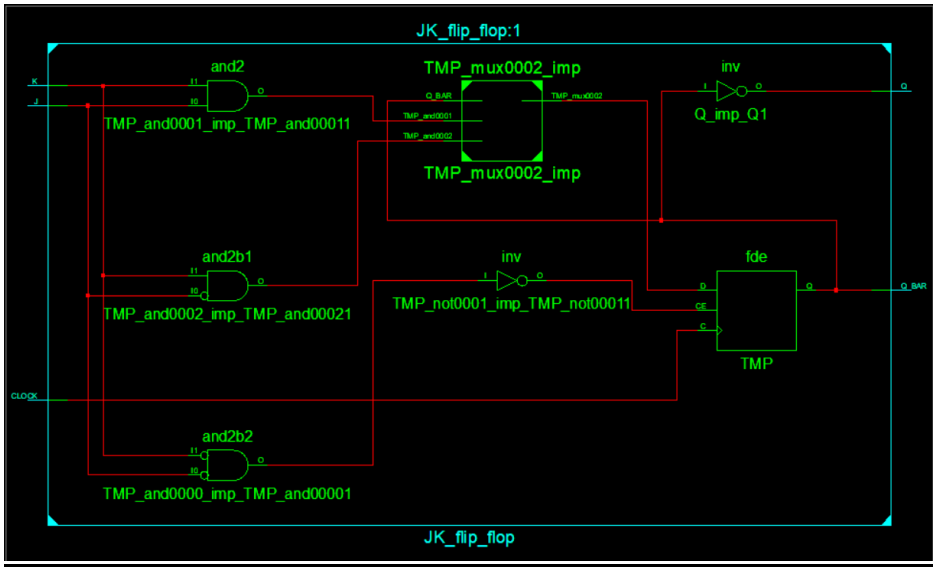
```
                    if(CLOCK='1' and CLOCK'EVENT) then
                        if(J='0' and K='0')then
                        TMP:=TMP;
                        elsif(J='1' and K='1')then
                        TMP:= not TMP;
                        elsif(J='0' and K='1')then
                        TMP:='0';
                        else
                        TMP:='1';
                        end if;
                    end if;
                Q_bar<=TMP;
                Q<=not TMP;
            end PROCESS;
end Behavioral;
```

OUTPUT: -

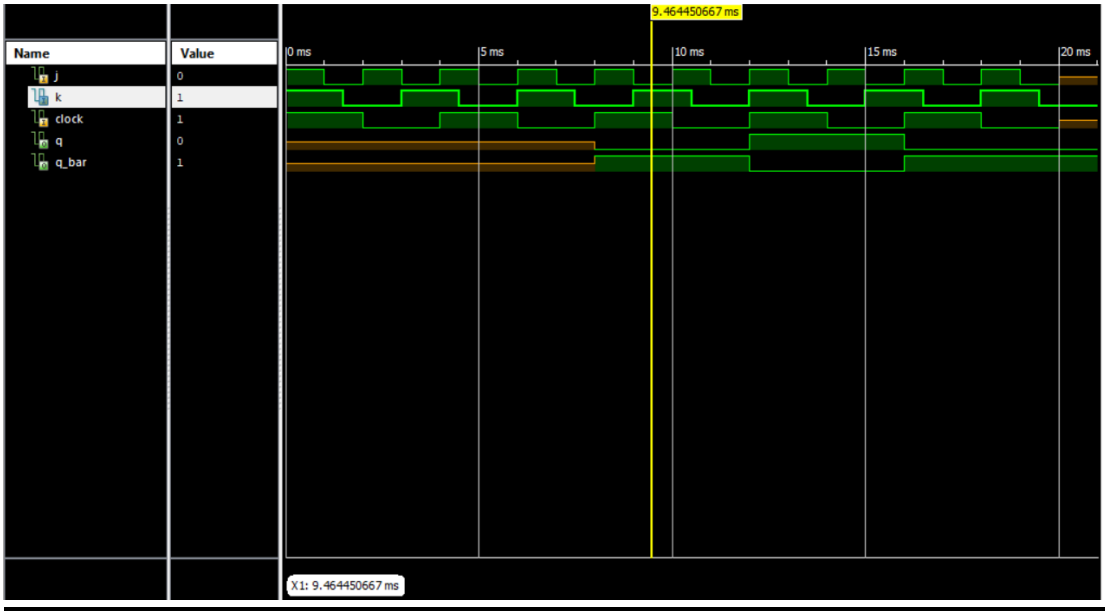
ENTITY DIAGRAM: -



DETAILED ENTITY DIAGRAM: -



SIMULATION: -



RESULT:

Thus, we have implemented the Behavioural Model of JK flip flop in VHDL, and the Entity Diagram and RTL are shown above. Also, the flip flop's truth table has been verified using the simulation of the waveform in ISE Simulator.

CONCLUSION:

In this experiment, we learnt about how to implement the Behavioural model of JK flip flop in VHDL and also verified the truth table of this flip flop using the waveform generated by ISE Simulator.