EXPERIMENT No.: - 15

Simulation of VHDL Models.

TITLE:

Implementation of Up-down Counter in VHDL using Structural Modelling.

OBJECTIVE:

To implement the Structural model of Up-down Counter using ISE Simulator.

THEORY:

Up counter and down counter are combined together to obtain an UP/DOWN counter. A mode control (M) input is also provided to select either up or down mode. A combinational circuit is required to be designed and used between each pair of flip-flops in order to achieve the up/down operation.

The truth table is as follows: -

COUNT-UP Mode				*COUNT-DOWN Mode*			
States	Q_C	Q_B	Q_A	*States*	Q_C	Q_B	Q_A
0	0	0	0	7	1	1	1
1	0	0	1	6	1	1	0
2	0	1	0	5	1	0	1
3	0	1	1	4	1	0	0
4	1	0	0	3	0	1	1
5	1	0	1	2	0	1	0
6	1	1	0	1	0	0	1
7	1	1	1	0	0	0	0

SOURCE CODE: -

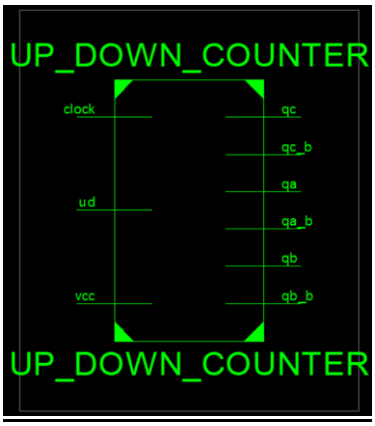
```
library IEEE;

use IEEE.STD_LOGIC_1164.ALL;


-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC_STD.ALL;


-- Uncomment the following library declaration if instantiating
```

```
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity UP_DOWN_COUNTER  is
   Port ( clock : in  STD_LOGIC;
          ud : in  STD_LOGIC;
          vcc : in  STD_LOGIC;
          QC : out  STD_LOGIC;
          QC_bar : out  STD_LOGIC);
end UP_DOWN_COUNTER ;

architecture Structural of UP_DOWN_COUNTER  is

Component jk_flip_flop is
Port(J,K,CLK:in Std_logic;
                    Q,Qbar:out Std_logic);
End Component;

Component andg is
Port(A,B:in Std_logic;
                    C:out Std_logic);
End Component;

Component or_g is
Port(A,B:in Std_logic;
                    C:out Std_logic);
End  Component;

Component notg is
Port(A:in Std_logic;
```

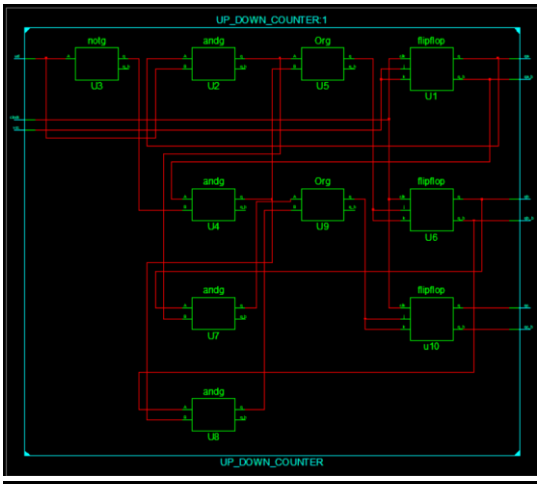
```
                Abar:out Std_logic);
End Component;

Signal qa,qa_bar,QB,QB_bar,A1,A2,A3,A4,O1,O2,N1:Std_logic;

begin

U1:jk_flip_flop Port map(vcc,vcc,clock,qa,qa_bar);
U2:andg Port map(qa,ud,A1);
U3:notg Port map(ud,N1);
U4:andg Port map(qa_bar,N1,A2);
U5:or_g Port map(A1,A2,O1);
U6:jk_flip_flop Port map(O1,O1,clock,QB,QB_bar);
U7:andg Port map(QB,A1,A3);
U8:andg Port map(QB_bar,A2,A4);
U9:or_g Port map(A3,A4,O2);
U10:jk_flip_flop Port map(O2,O2,clock,QC,QC_bar);


end Structural;
```

OUTPUT: -

ENTITY DIAGRAM: -



DETAILED ENTITY DIAGRAM: -



RESULT:

Thus, through structural modelling we have implemented the Up-down Counter in VHDL and we have processed the overview of the basic structure of this entity as a whole using the RTL schematics. The blank square correctly represents the structure of respective input, output Ports signals in Structural Modelling.

CONCLUSION:

In this experiment, we learnt about how to implement the Up-down Counter in VHDL as the structural ports design and placement of the respective model's input and output is correctly represented using structural modelling.