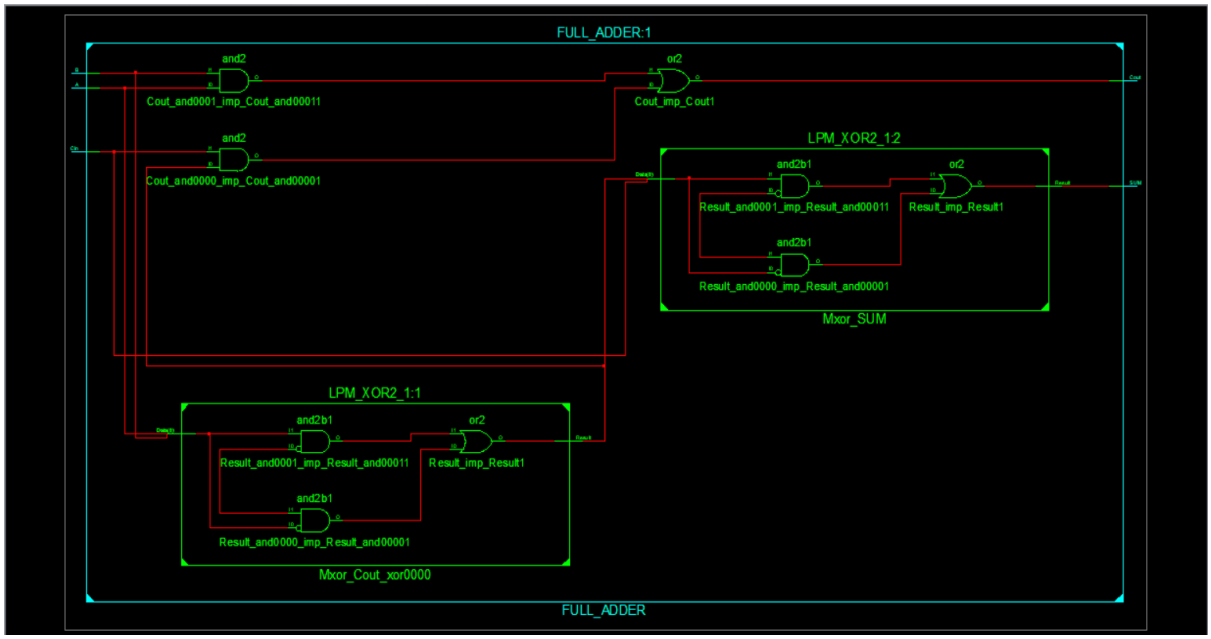
PROGRAM 2: -FULL ADDER

SOURCE CODE: -

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity FULL_ADDER is
    Port ( A : in  STD_LOGIC;
           B : in  STD_LOGIC;
           Cin : in  STD_LOGIC;
           SUM : out  STD_LOGIC;
           Cout : out  STD_LOGIC);
end FULL_ADDER;

architecture Dataflow of FULL_ADDER is

begin
SUM <= ((A XOR B) XOR Cin);

Cout <= (((A XOR B) AND Cin) OR (A AND B));



end Dataflow;
```

OUTPUT: -

Diagram: -



Simulation: -