EXPERIMENT No.: - 8

Simulation of VHDL Models.

TITLE:

Implementation of 3 to 8 decoder in VHDL using CASE Statement.

OBJECTIVE:

To implement the Behavioural model of 3 to 8 decoder using CASE Statement in ISE Simulator.

THEORY:

A decoder is a combinational logic circuit that is used to change the code into a set of signals. It is the reverse process of an encoder. A decoder circuit takes multiple inputs and gives multiple outputs.

A decoder circuit takes binary data of **'n'** inputs into 2^n unique output. In addition to input pins, the decoder has a enable pin. This enables the pin when negated, to make the circuit inactive.

In 3-to-8-line decoder, it includes three inputs and eight outputs. Here the inputs are represented through A, B & C whereas the outputs are represented through D0, D1, D2…D7.

The selection of 8 outputs can be done based on the three inputs. So, the truth table of these 3 lines to 8-line decoder is shown below. From the following truth table, we can observe that simply one of 8 outputs from DO – D7 can be selected depending on 3 select inputs.

A	B	C	D0	D1	D2	D3	D4	D5	D6	D7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	1

From the above truth table of 3 lines to 8-line decoder, the logic expression can be defined as: -

D0 = A'B'C'
D1= A'B'C
D2 = A'BC'
D3 = A'BC
D4 = AB'C'
D5= AB'C
D6 = ABC'
D7 = ABC

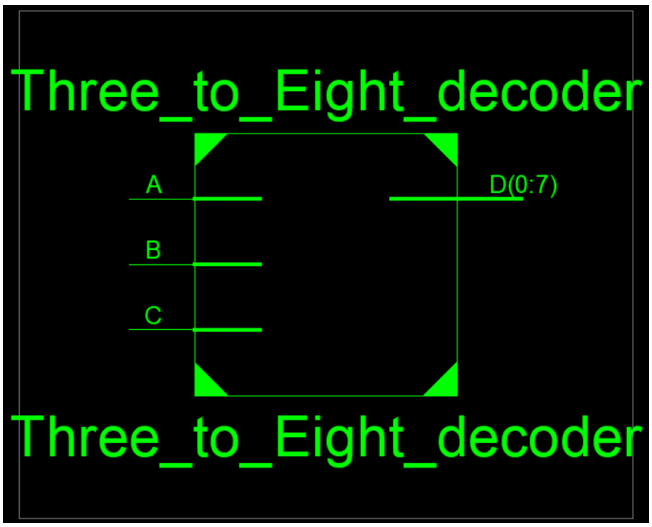
SOURCE CODE: -

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Three_to_Eight_decoder is
   Port ( A,B,C : in  STD_LOGIC;
          D : out  STD_LOGIC_VECTOR(0 TO 7));
end Three_to_Eight_decoder;

architecture Behavioral of Three_to_Eight_decoder is

begin

PROCESS(A,B,C)
          VARIABLE S : STD_LOGIC_VECTOR(0 TO 2);
          begin
          S := A&B&C;
          CASE S IS
                    WHEN "000" => D <="00000001";
                    WHEN "001" => D <="00000010";
                    WHEN "010" => D <="00000100";
                    WHEN "011" => D <="00001000";
```

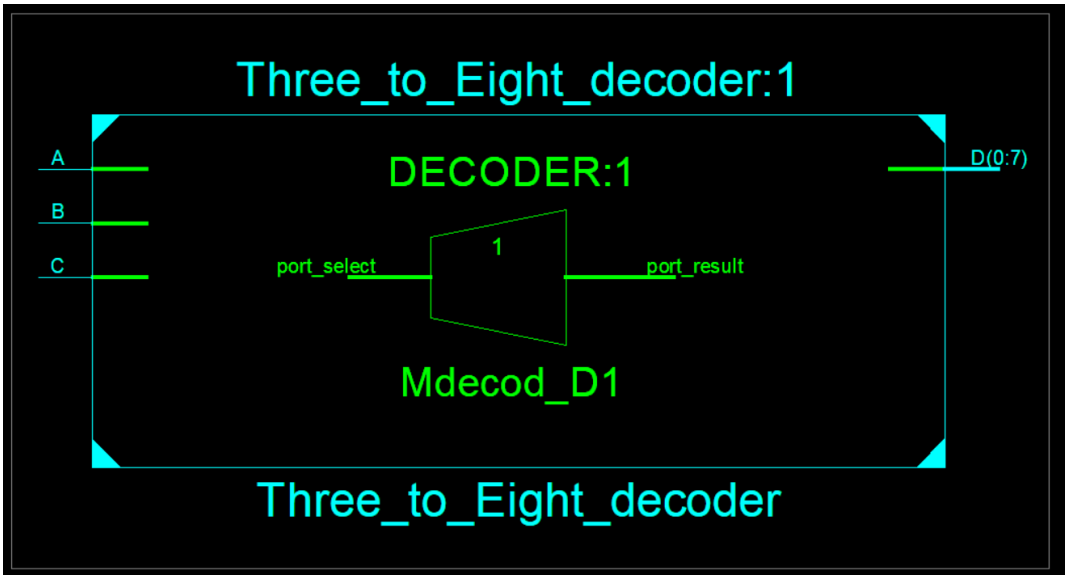
```
            WHEN "100" => D <="00010000";
            WHEN "101" => D <="00100000";
            WHEN "110" => D <="01000000";
            WHEN OTHERS => D <="10000000";
        END CASE;
END PROCESS;


end Behavioral;
```

OUTPUT: -

ENTITY DIAGRAM: -



DETAILED ENTITY DIAGRAM: -



SIMULATION: -

RESULT:

Thus, we have implemented the Behavioural Model of 3-to-8-line decoders in VHDL using CASE Statement, and the Entity Diagram and RTL are shown above. Also, the decoder's truth table has been verified using the simulation of the waveform in ISE Simulator.

CONCLUSION:

In this experiment, we learnt about how to implement the Behavioural model of 3-to-8-line decoders using CASE Statement in VHDL and also verified the truth table of this decoder using the waveform generated by ISE Simulator.