EXPERIMENT No.: - 14

Simulation of VHDL Models.

TITLE:

Implementation of 8-bit Adder in VHDL using Structural Modelling.

OBJECTIVE:

To implement the Structural model of 8-bit Adder using ISE Simulator.

THEORY:

In an 8-bit adder the full adders are connected in a cascade with a 1 carry cascading from a least significant bit to the most significant bit**.** Complete 8-bit Adder: Technically the first Carry-In on the first full adder (also the full adder of the least significant bit) does not have to be there.

The truth table is as follows: -

Inputs			Output	
A	B	C	C_1	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
1	0	0	0	1
0	1	1	1	0
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

SOURCE CODE: -

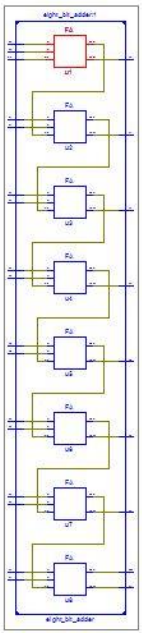
```
library IEEE;

use IEEE.STD_LOGIC_1164.ALL;


-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC_STD.ALL;
```

```
-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity bit8adder is
    Port ( cin : in  STD_LOGIC;
           a0 : in  STD_LOGIC;
           a1 : in  STD_LOGIC;
           a2 : in  STD_LOGIC;
           a3 : in  STD_LOGIC;
           a4 : in  STD_LOGIC;
           a5 : in  STD_LOGIC;
           a6 : in  STD_LOGIC;
           a7 : in  STD_LOGIC;
           b0 : in  STD_LOGIC;
           b1 : in  STD_LOGIC;
           b2 : in  STD_LOGIC;
           b3 : in  STD_LOGIC;
           b4 : in  STD_LOGIC;
           b5 : in  STD_LOGIC;
           b6 : in  STD_LOGIC;
           b7 : in  STD_LOGIC;
           cout : out  STD_LOGIC;
           s0 : out  STD_LOGIC;
           s1 : out  STD_LOGIC;
           s2 : out  STD_LOGIC;
           s3 : out  STD_LOGIC;
           s4 : out  STD_LOGIC;
           s5 : out  STD_LOGIC;
           s6 : out  STD_LOGIC;
```

```
        s7 : out  STD_LOGIC);
end bit8adder;

architecture structural of bit8adder is


component FA is
port(A, B, Cin : in std_logic;
                    Cout, Sum: out std_logic);
end component;

signal c0, c1, c2, c3, c4, c5, c6: std_logic;
begin
u1: FA port map(a0, b0, cin, c0, s0);
u2: FA port map(a1, b1, c0, c1, s1);
u3: FA port map(a2, b2, c1, c2, s2);
u4: FA port map(a3, b3, c2, c3, s3);
u5: FA port map(a4, b4, c3, c4, s4);
u6: FA port map(a5, b5, c4, c5, s5);
u7: FA port map(a6, b6, c5, c6, s6);
u8: FA port map(a7, b7, c6, cout, s7);

end structural;
```

OUTPUT: -

DETAILED ENTITY DIAGRAM: -



RESULT:

Thus, through structural modelling we have implemented the 8-bit Adder in VHDL and we have processed the overview of the basic structure of this entity as a whole using the RTL schematics. The blank square correctly represents the structure of respective input, output Ports signals in Structural Modelling.

CONCLUSION:

In this experiment, we learnt about how to implement the 8-bit Adder in VHDL as the structural ports design and placement of the respective model's input and output is correctly represented using structural modelling.