EXPERIMENT No.: - 11

Simulation of VHDL Models.

TITLE:

Implementation of D flip-flop in VHDL using Behavioural Modelling.

OBJECTIVE:

To implement the Behavioural model of D flip-flop in ISE Simulator.

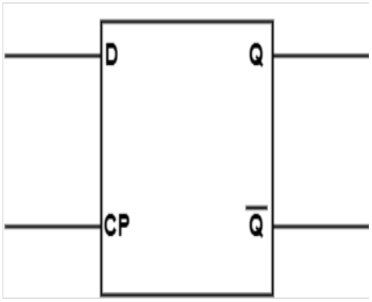
THEORY:

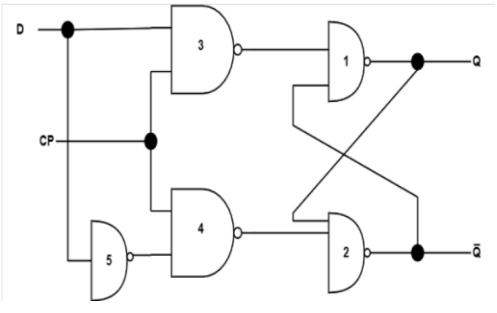
The D flip-flop is a clocked flip-flop with a single digital input 'D'. Each time a D flip-flop is clocked, its output follows the state of 'D'. The D Flip Flop has only two inputs D and CP. The D inputs go precisely to the S input and its complement is used to the R input.

Considering the pulse input is at 0, the outputs of gates 3 and 4 are at the 1 level and the circuit cannot convert state regardless of the value of D. The D input is sampled when CP = 1. If D is 1, the Q output goes to 1, locating the circuit in the set state. If D is 0, output Q goes to 0, and the circuit switches to a clear state.

The D flip flop obtains the destination from its capacity to manage data into its internal storage. This type of flip-flop is known as a gated D-latch. The CP input is provided given the destination G (for gate) to denote that this input allows the gated latch to create applicable data entry into the circuit.

The binary data present at the data input of the D flip flop is changed to the Q output when the CP input is allowed. The output follows the data input considering the pulse continues in its 1 state. When the pulse goes to 0, the binary data that was displayed at the data input at the time the pulse transition appeared is retained at the Q output until the pulse input is allowed again.





The truth table for D flip-flop is as shown in the table.

S	D	Q_{N+1}
0	0	0
0	1	1
1	0	0
1	1	1

The truth table for the D flip flop is displayed in the table. It demonstrates that the next state of the flip flop is independent of the current state since Q_{N+1} is similar to input D whether Q is similar to 0 or 1. This defines that an input pulse will change the value of input D into the output of the flip flop independent of the value of the output earlier the pulse was used.

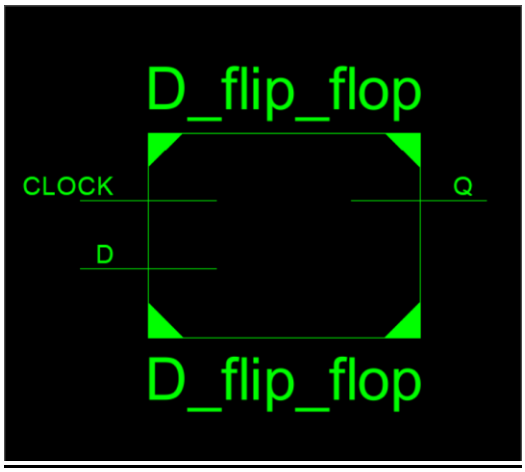
SOURCE CODE: -

```
library IEEE;

use IEEE.STD_LOGIC_1164.ALL;



-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC_STD.ALL;



-- Uncomment the following library declaration if instantiating

-- any Xilinx primitives in this code.

--library UNISIM;

--use UNISIM.VComponents.all;



entity D_flip_flop is

   Port ( D : in  STD_LOGIC;

          CLOCK : in  STD_LOGIC;

          Q : out  STD_LOGIC);

end D_flip_flop;



architecture Behavioral of D_flip_flop is

begin

             process(CLOCK)
```

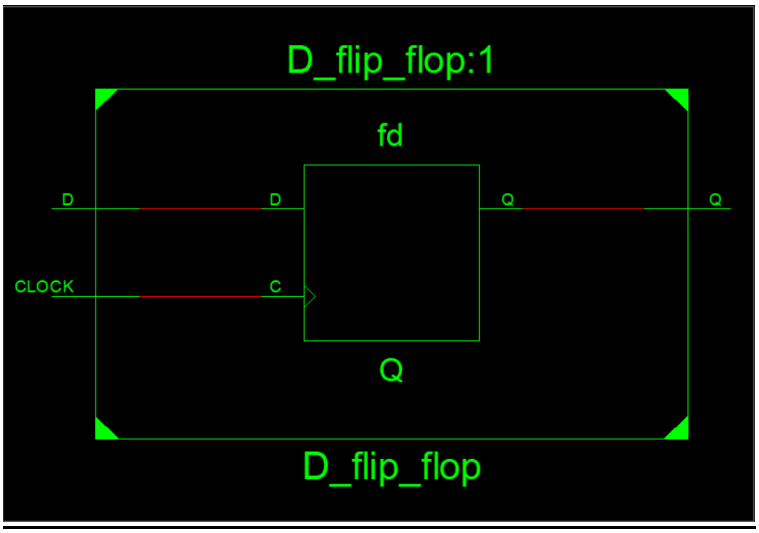
```
        begin
            if(CLOCK='1' and CLOCK'EVENT) then
                Q <= D;
            end if;
    end process;
end Behavioral;
```

OUTPUT: -

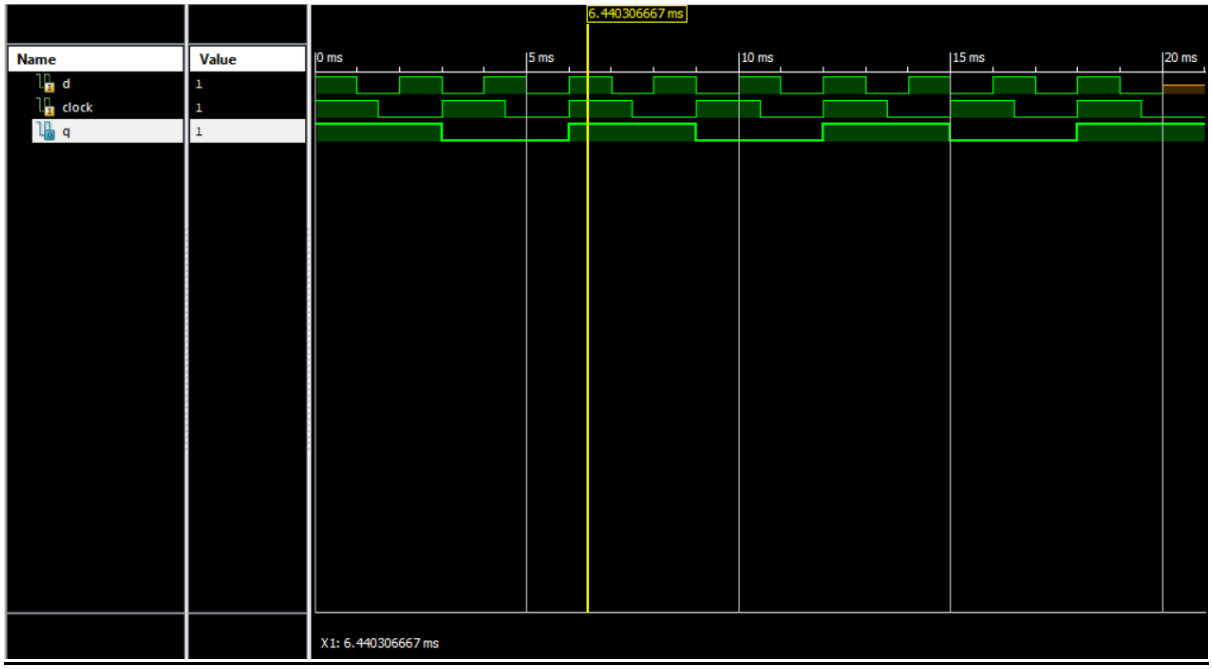
ENTITY DIAGRAM: -



DETAILED ENTITY DIAGRAM: -



SIMULATION: -



RESULT:

Thus, we have implemented the Behavioural Model of D flip flop in VHDL, and the Entity Diagram and RTL are shown above. Also, the flip flop's truth table has been verified using the simulation of the waveform in ISE Simulator.

CONCLUSION:

In this experiment, we learnt about how to implement the Behavioural model of D flip flop in VHDL and also verified the truth table of this flip flop using the waveform generated by ISE Simulator.