EXPERIMENT No.: - 13

Simulation of VHDL Models.

TITLE:

Implementation of T flip-flop in VHDL using Behavioural Modelling.

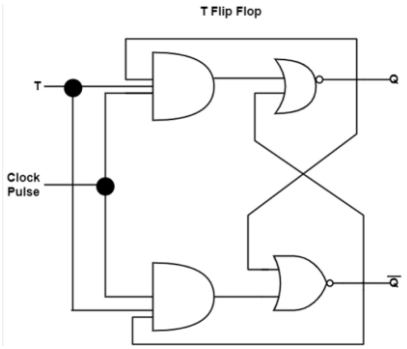
OBJECTIVE:

To implement the Behavioural model of T flip-flop in ISE Simulator.

THEORY:

The T flip-flop is also called toggle flip-flop. It is a change of the JK flip-flop. The T flip flop is received by relating both inputs of a JK flip-flop. The T flip-flop is received by relating the inputs 'J' and 'K'. When T = 0, both AND gates are disabled. Therefore, there is no change in the output. When T= 1, the output toggles.

The diagram demonstrates the circuit diagram of a T flip-flop.



The truth table of T flip-flop is displayed in the table.

Q_N	T	Q_{N+1}
0	0	0
0	1	1
1	0	1
1	1	0

SOURCE CODE: -

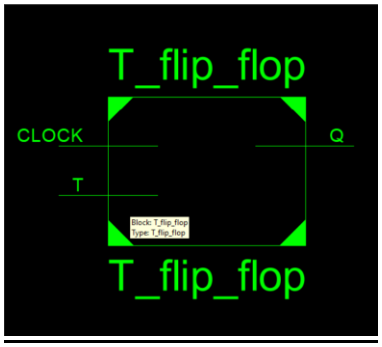
```
library IEEE;

use IEEE.STD_LOGIC_1164.ALL;


-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC_STD.ALL;
```

```
-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity t_flipflop is

        Port(t: in STD_LOGIC;
             clk: in STD_LOGIC;
             q: out STD_LOGIC);

end t_flipflop;

architecture Behavioral of t_flipflop is

begin

        process(clk)
        variable tmp:std_logic:='0';
        begin

            if(clk='1' and clk'event) then
            if T='0' then
            tmp:=tmp;
            else
            tmp:= not tmp;
            end if;
            end if;

            q<=tmp;
```

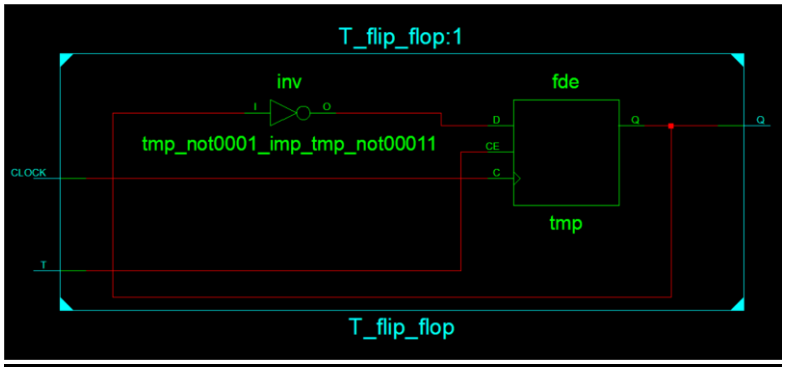
```
        end process;

end Behavioral;
```

OUTPUT: -

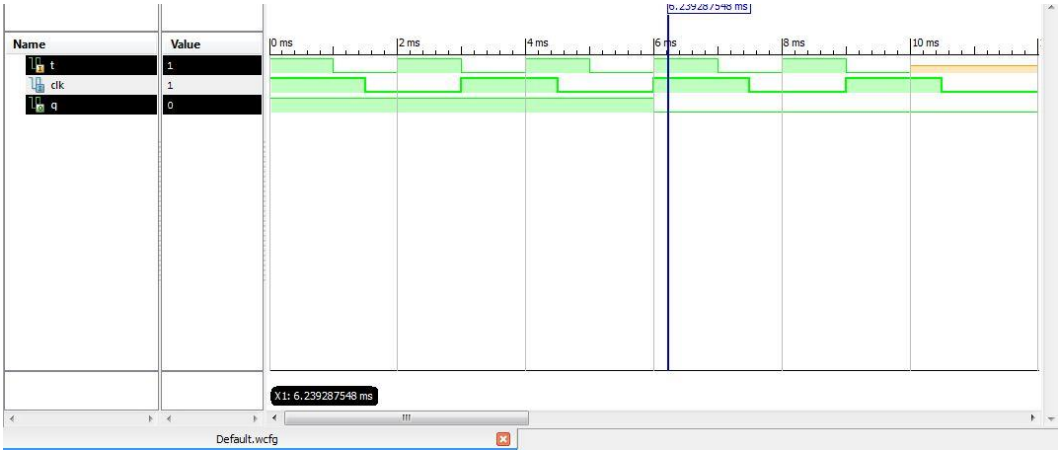
ENTITY DIAGRAM: -



DETAILED ENTITY DIAGRAM: -



SIMULATION: -



RESULT:

Thus, we have implemented the Behavioural Model of T flip flop in VHDL, and the Entity Diagram and RTL are shown above. Also, the flip flop's truth table has been verified using the simulation of the waveform in ISE Simulator.

CONCLUSION:

In this experiment, we learnt about how to implement the Behavioural model of T flip flop in VHDL and also verified the truth table of this flip flop using the waveform generated by ISE Simulator.