Hi3798C V200 Data Sheet

General Information

Issue	**00B02**
Date	**2016-02-03**

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About This Document

Purpose

This document describes the basic information about the Hi3798C V200 intelligent network terminal media processor, including its architecture, boot mode, address space mapping, soldering process, moisture-sensitive specifications, and ordering information.

Related Version

The following table lists the product version related to this document.

Product Name	Version
Hi3798C	V2XX

Intended Audience

This document is intended for:

- Technical support personnel
- Software development engineers

Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
DANGER	Alerts you to a high risk hazard that could, if not avoided, result in serious injury or death.
WARNING	Alerts you to a medium or low risk hazard that could, if not avoided, result in moderate or minor injury.

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Symbol	Description
CAUTION	Alerts you to a potentially hazardous situation that could, if not avoided, result in equipment damage, data loss, performance deterioration, or unanticipated results.
TIP	Provides a tip that may help you solve a problem or save time.
NOTE	Provides additional information to emphasize or supplement important points in the main text.

Register Attributes

The register attributions that may be found in this document are defined as follows.

Symbol	Description	Symbol	Description
RO	The register is read-only.	RW	The register is read/write.
RC	The register is cleared on a read.	WC	The register can be read. The register is cleared when 1 is written. The register keeps unchanged when 0 is written.

Reset Value Conventions

In the register definition tables:

- If the reset value (for the Reset row) of a bit is "?", the reset value is undefined.
- If the reset values of one or multiple bits are "?", the total reset value of a register is undefined and is marked as "-".

Numerical System

The expressions of data capacity, frequency, and data rate are described as follows.

Type	Symbol	Value
Data capacity (such as the RAM capacity)	K	1024
	M	1,048,576
	G	1,073,741,824
Frequency, data rate	k	1000

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Type	Symbol	Value
	M	1,000,000
	G	1,000,000,000

The expressions of addresses and data are described as follows.

Symbol	Example	Description
0x	0xFE04, 0x18	Address or data in hexadecimal
0b	0b000, 0b00 00000000	Data or sequence in binary (register description is excluded.)
X	00X, 1XX	In data expression, X indicates 0 or 1. For example, 00X indicates 000 or 001 and 1XX indicates 100, 101, 110, or 111.

Others

Frequencies in this document all comply with the SDH standard. The shortened frequency names and the corresponding nominal frequencies are as follows.

Shortened Frequency Name	Nominal Frequency
19 M	19.44 MHz
38 M	38.88 MHz
77 M	77.76 MHz
622 M	622.08 MHz

Change History

Changes between document issues are cumulative. Therefore, the latest document issue contains all changes made in previous issues.

Issue 00B02 (2016-02-03)

This issue is the second draft release, which incorporates the following changes:

In Section 2.2.1, description about the master processor is modified.

Table 4-1 in chapter 4 is modified.

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Issue 00B01 (2015-09-30)

This issue is the first draft release.

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Contents

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1 Document Overview

Table 1-1 describes the content of the *Hi3798C V200 Data Sheet*. The highlighted portion outlines information contained in this document.

Table 1-1 Hi3798C V200 Data Sheet overview

Document No.	Document Name	Description
Hi3798C V200 Data Sheet 01	General Information	• Product Overview • Boot Mode • Address Space Mapping • Soldering Process • Moisture-Sensitive Specifications • Ordering Information • Acronyms and Abbreviations
Hi3798C V200 Data Sheet 02	Hardware	• Package and Pins • Electrical Characteristics • Schematic Diagram Design Recommendations • PCB Design Recommendations • Thermal Design Recommendations • Interface Timings
Hi3798C V200 Data Sheet 03	System	• Processor Subsystem • Security Subsystem • Power Management and Low-Power Control • Reset • Clock • System Controller • Peripheral Controller • Interrupt System • Timer

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Document No.	Document Name	Description
		• 64-bit Timer • WDG
Hi3798C V200 Data Sheet 04	Peripherals	• DDRC • FMC • eMMC/SD/SDIO • GSF • GPIO • UART • SCI • I^2C • IR • SPI • LED • USB 2.0 • USB 3.0 • PCIe • SATA • LSADC
Hi3798C V200 Data Sheet 05	Data Stream/Graphics Processing/Audio/Video Interfaces	• TSI • Video Decoder • Video Encoder • TDE • HWC • GPU • VPSS • VDP • AIAO • HDMI TX

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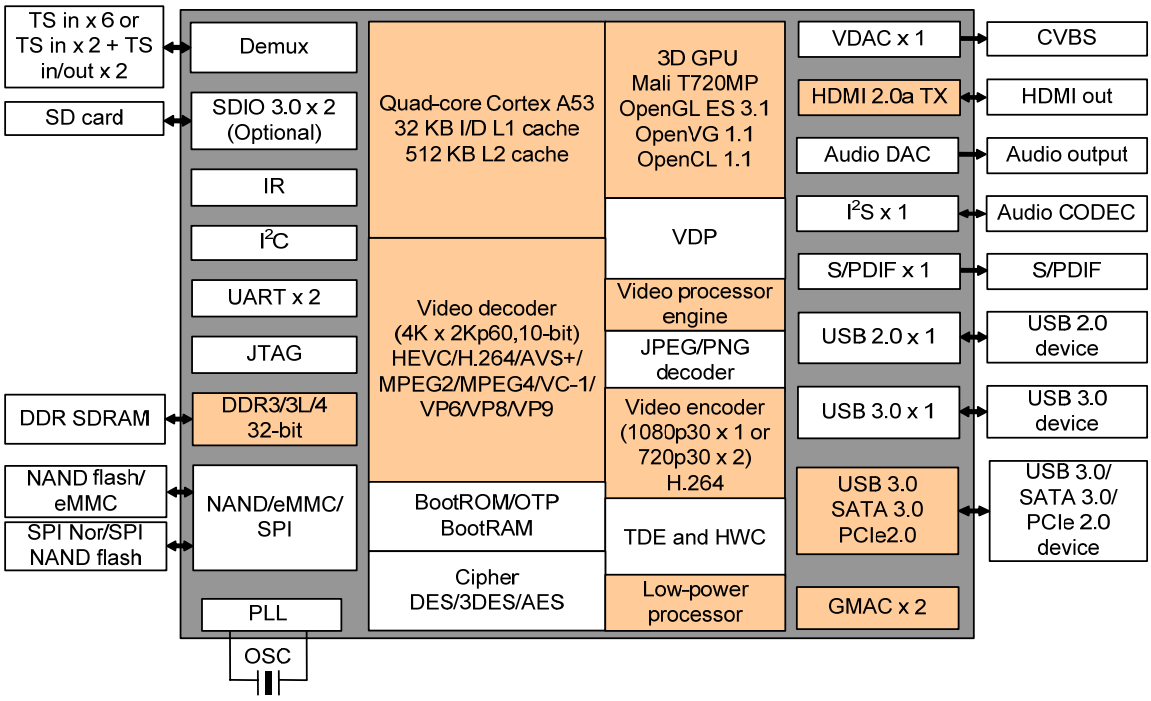
2 Product Overview

2.1 Application Scenario

With an integrated quad-core 64-bit high-performance Cortex A53 processor and embedded NEON, Hi3798C V200 provides powerful CPU processing capabilities that meet differentiated service requirements. It creates the industry's best user experience in stream compatibility, smoothness and picture quality of live video playback, and STB performance. To meet the growing requirements on multimedia playback, video communication, and multi-screen transcoding, Hi3798C V200 supports 4K x 2Kp60@10-bit ultra-HD video decoding and display in various formats (including H.265/HEVC, H.264/AVC, AVS+, MVC, MPEG2, MPEG4, VC-1, VP6, VP8, and VP9) and high-performance H.264 encoding. It also supports Dolby and DTS audio processing. Hi3798C V200 provides a smooth man-machine interface and rich gaming experience with a high-performance multi-core 2D/3D acceleration engine. It also enables flexible connection schemes with multiple Ethernet ports, USB 2.0 ports, USB 3.0 ports, SATA/eSATA ports, PCIe 2.0 ports, and more peripheral interfaces.

Figure 2-1 Application block diagram



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2.2 Architecture

Hi3798C V200 has the following features:

- Master processor
- 3D engine
- Security processing
- Memory interfaces
- Data stream interfaces
- Video CODEC
- Graphics and display processing
- Audio/Video interfaces
- Peripheral interfaces
- Low-power control

2.2.1 Master Processor

Hi3798C V200 integrates a quad-core ARM Cortex A53 processor as the master CPU to implement system functions and some audio and video processing tasks. This processor has the following features:

- Maximum 15000 DMIPS
- Independent 32 KB I-cache and 32 KB D-cache, 512 KB shared L2 cache
- Integrated NEON
- Dynamic power consumption reduction such as dynamic voltage and frequency scaling (DVFS) and adaptive voltage scaling (AVS)

2.2.2 3D Engine

Hi3798C V200 integrates the high-performance multi-core Mali720 GPU to process 3D graphics and videos.

- OpenGL ES 3.1/2.0/1.1/1.0
- OpenVG 1.1
- OpenCL 1.1 full profile/RenderScript
- 1080p60 UI processing capability
- 1080p60 gaming applications

2.2.3 Security Processing

Hi3798C V200 has the following advanced security features:

- Trusted execution environment (TEE)
- Secure video path (SVP)
- Secure boot
- Secure storage
- Secure upgrade
- Protection for Joint Test Action Group (JTAG) and other debugging ports

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- One-time programmable (OTP)
- Digital rights management (DRM)
- Downloadable conditional access (CA) (DCAS) and other mainstream advanced CA
- HDCP 2.2/1.4 protection for HDMI outputs

2.2.4 Memory Interfaces

Hi3798C V200 provides the DDR3/3L/DDR4 SDRAM controller (DDRC), flash memory controller (FMC) that supports the SPI NOR, SPI NAND, and NAND flash, and MMC/SD/SDIO controller.

DDRC

The DDRC controls the access to the DDR3/3L/DDR4 SDRAM. It supports the following features:

- Maximum 2 GB capacity
- 32-bit memory
- Maximum 1066 MHz frequency
- Standby power-down

FMC

The FMC provides memory controller interfaces for connecting to external NAND flash, SPI NAND flash, or SPI NOR flash to access data. It supports the following features:

- Provides one 9 KB (8192 bytes+1024 bytes) on-chip buffer for improving the read speed.
- Supports one external CS (SPI NAND flash, SPI NOR flash, or NAND flash).
- Supports the SPI NOR flash, SPI NAND flash, and NAND flash.
- Supports five types of SPIs, including the standard SPI, dual-output/dual-input SPI, quad-output/quad-input SPI, dual I/O SPI, and quad I/O SPI.
- Supports the SPI NAND flash with the following specifications:
  - 2 KB or 4 KB page size
  - 64 pages/block
  - 3-byte or 4-byte address mode
- Supports the NAND flash with the following specifications:
  - 2 KB, 4 KB, 8 KB, or 16 KB page size
  - 64/128/256/512 pages/block
  - 8-bit width
  - Asynchronous NAND flash
- Supports the error checking and correction (ECC) function for the SPI NAND flash and NAND flash.
  - 8-bit/1 KB, 16-bit/1 KB, 24-bit/1 KB, 28-bit/1 KB, 40-bit/1 KB, and 64-bit/1 KB Bose-Chaudhuri-Hocquenghem (BCH) code ECC (1 KB means the 1 KB level but not exactly 1024 bytes)
  - Enable and disable of the ECC function and ECC code generation
- Supports the randomizer only in non-ECC0 mode when the page size is 8 KB or 16 KB. It is disabled in other modes.

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MMC/SD/SDIO Controller

Hi3798C V200 integrates three high-speed large-capacity SDIO 3.0/MMC 5.0 controllers to control the access to the MMC/SD card. Extended peripherals such as Bluetooth and Wi-Fi devices can be connected over the SDIO interface.

Two controllers support the 1-/4-bit mode. Another one supports the 1-/4-/8-bit mode for boot from the eMMC, and the interface is multiplexed with the NAND flash interface.

2.2.5 Data Stream Interfaces

The data stream interfaces of Hi3798C V200 include the Ethernet port and transport stream interface (TSI).

Ethernet Ports

Hi3798C V200 provides two gigabit Ethernet MACs.

- 10/100/1000 Mbit/s, half-duplex or full-duplex mode
- Two RGMII/RMII interfaces
- Configurable destination MAC address filtering table, which filters the input frames of the Ethernet port
- Traffic control of the CPU interface, protecting the CPU against heavy traffic

TSI

Hi3798C V200 integrates a TSI controller, which supports the following features:

- Parsing and demultiplexing of MPEG2 TSs complying with the standards of the ISO 13818-1 (GB 17975-1) system layer
- Maximum two external standard serial TS inputs and two external standard serial TS inputs/outputs; or six TS inputs without sync signals
- 4-channel playback TSs from the memory
- Maximum 96 hardware PID channels, processing at most 7-channel TSs at the same time

2.2.6 Video CODEC (HiVXE 2.0 Processing Engine)

Hi3798C V200 integrates the HD video and graphics CODEC that supports various protocols (H.265/H.264/AVS+/MVC/VC-1/MPEG2/MPEG4/AVS/VP6/VP8/VP9/JPEG/PNG), providing powerful video/graphics encoding and decoding capabilities.

- H.265/HEVC Main/Main 10 profile@level 5.1 high-tier, maximum 4K x 2K@60 fps and 1x1080p@30 fps simultaneous decoding
- H.264/AVC BP/MP/HP@level 5.1; H.264/AVC MVC, maximum 4K x 2K@30 fps decoding
- VP9, maximum 4K x 2K@60 fps decoding
- VP6/8, maximum 1080p@60 fps decoding
- MPEG1, maximum 1080p@60 fps decoding
- MPEG2 SP@ML, MP@HL, maximum 1080p@60 fps decoding
- MPEG4 SP@level 0−3, ASP@level 0−5, GMC, short header format, maximum 1080p@60 fps decoding
- AVS baseline profile@level 6.0, AVS-P16 (AVS+), maximum 1080p@60 fps decoding

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- VC-1 SP@ML, MP@HL, AP@level 0−3, maximum 1080p@60 fps decoding

2.2.7 Graphics and Display Processing (Imprex 2.0 Processing Engine)

Hi3798C V200 integrates the dedicated two-dimensional engine (TDE), dedicated multi-graphics/video overlapping engine (hardware composer engine), and dedicated display processing engine.

- Hardware overlaying of multiple graphics and video inputs
- 4-layer on-screen display (OSD) and three video layers
- Maximum 4K x 2K image output
- Mosaic and multi-region display
- Mirroring
- 16-bit or 32-bit color depth
- Graphics and video rotation
- LetterBox and PanScan
- 3D video processing and display
- Multi-order vertical and horizontal scaling of videos and graphics; free scaling
- Low-delay display
- Enhanced full-hardware TDE
- Full-hardware anti-aliasing and anti-flicker
- Color space conversion (CSC) with configurable coefficients (including BT2020)
- Image enhancement and noise reduction
- Deinterlacing
- Sharpening
- Chrominance, luminance, contrast, and saturation adjustment
- Db/Dr processing for graphics and videos
- High data rate (HDR)

2.2.8 Audio/Video Interfaces

Hi3798C V200 integrates various audio/video input/output interfaces, providing rich audio/video input/output capabilities.

Video Output Interface

- One 4Kp60 or 1920 x 1080p@60 fps output and one SD output from the same source
- One HDMI 2.0a TX output, supporting HDCP 2.2/1.4, maximum 4K x 2K resolution
- Embedded DAC
  - One composite video broadcasting signal (CVBS) output
  - Rovi and vertical blanking interval (VBI) video output

Audio I/O Interface

- Sony/Philips digital interface format (S/PDIF) audio output interface

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- One embedded DAC, which supports audio-left and audio-right channels (output interface of the RCA type, low impedance, and imbalance)
- One inter-IC sound (I^2S) or pulse code modulation (PCM) digital audio input/output
- One HDMI TX audio output

2.2.9 Peripheral Interfaces

Hi3798C V200 integrates diverse peripheral interfaces for connecting to various peripherals or extending system functions.

IR Interface

The integrated dedicated infrared remoter (IR) receives data through an IR interface. It has the following features:

- Flexible configuration for decoding data in various formats
- Error check for received data
- IR wakeup
- One input interface

LED/Keypad Controller

Hi3798C V200 integrates the LED/keypad controller for controlling the LED display and key scanning.

USB Controller

Hi3798C V200 integrates one USB 2.0 controller and supports two USB 3.0 controllers.

- The USB 2.0 controller supports the host function and supports the Android debug bridge (ADB) debugging (USB1).
- The USB 2.0 ports support the low-speed or high-speed mode and extended hub.
- The USB 3.0 controllers are backward compatible with USB 2.0.

GPIO Controllers

Hi3798C V200 integrates multiple groups of GPIO controllers. Each group provides eight programmable input/output pins.

- Each GPIO pin can be configured as an input or output.
- As an input pin, the GPIO can be an interrupt source.
- As an output pin, the GPIO can be independently set to 1 or 0.

UARTs

Hi3798C V200 integrates two universal asynchronous receiver transmitters (UARTs) for debugging, controlling, or extending external devices such as the Bluetooth and keyboard. One is a 2-wire interface, and the other one is a 4-wire interface.

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I²C Controllers

Hi3798C V200 integrates five inter-integrated circuit (I^2C) controllers, which serve as standard master I^2C devices to transmit or receive data to or from the slave devices over the I^2C bus.

SCI

Hi3798C V200 integrates a smart card interface (SCI) controller and provides one SCI that supports the ISO/IEC 7816-3, ISO/IEC 7816-10 protocols and T0, T1, and T14 asynchronous transmission protocols. The CPU reads data from or writes data to the smart card through the SCI and implements serial-to-parallel conversion (when it reads data from the smart card) and parallel-to-serial conversion (when it writes data to the smart card).

2.2.10 Low-Power Control

Hi3798C V200 supports various low-power modes to dynamically reduce power consumption.

- Various system operating modes, including the normal mode, light standby mode, and passive standby mode
- Module low-power control
- DVFS based on CPU load monitoring
- AVS based on CPU timing monitoring
- Ultra-low-power standby design, including various standby wakeup modes such as remote control wakeup and key wakeup

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3 Boot Modes

After the chip is powered on, the system is reset. The CPU jumps to the internal BOOTROM to execute the boot program after the reset is deasserted. After the internal BOOTROM program is executed, if the external pin USB_BOOT is low level, the chip directly boots from the USB port; otherwise, the CPU copies the U-boot codes stored in the external memory to the DDR to continue executing the boot program.

Hi3798C V200 can boot from any of the following external memories storing the U-boot:

- SPI NOR flash
- NAND flash
- SPI NAND flash
- eMMC
- fSD card

CAUTION

The USB_BOOT pin is pulled high by its internal resistor by default.

The boot_sel pin determines the flash memory from which the chip boots. Figure 3-1 shows the process.

Figure 3-1 shows the boot process.

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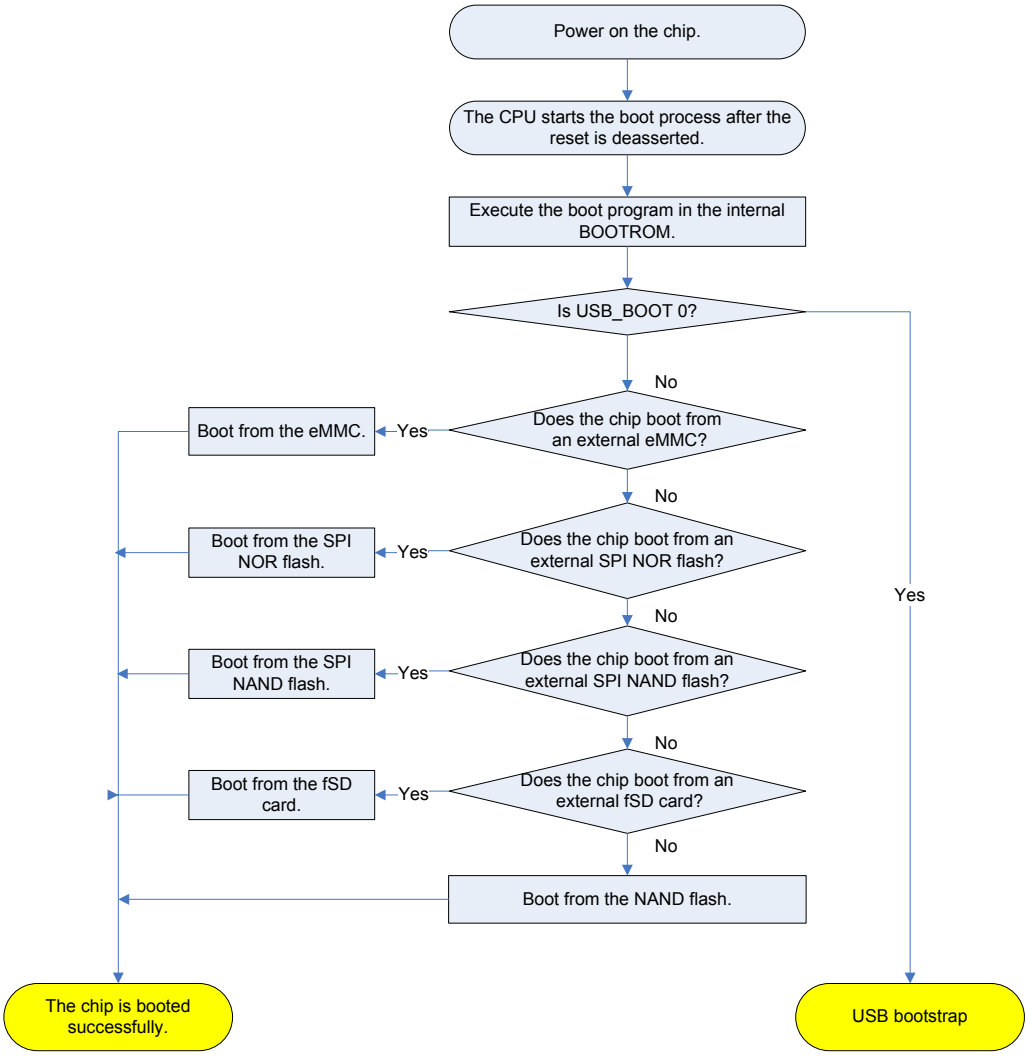
Figure 3-1 Boot process



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4 Address Space Mapping

Table 4-1 describes the address space mapping of Hi3798C V200.

Table 4-1 Address space mapping

Start Address	End Address	Object	Size (Byte)
0x0000_0000	0xEFFF_FFFF	DRAM	3.75 GB
0xF000_0000	0xF000_1FFF	PCIe0 register	8 KB
0xF000_2000	0xF0FF_FFFF	Reserved	16376 KB
0xF100_0000	0xF100_FFFF	Generic interrupt controller (GIC) register	64 KB
0xF101_0000	0xF1FF_FFFF	Reserved	16320 KB
0xF200_0000	0XF4FF_FFFF	PCIe0 register	48 MB
0xF500_0000	0xF7FF_FFFF	Reserved	48 MB
0xF800_0000	0xF800_0FFF	Sysctrl register	4 KB
0xF800_1000	0xF800_1FFF	IR register	4 KB
0xF800_2000	0xF800_2FFF	Timer01 register	4 KB
0xF800_3000	0xF800_3FFF	LEDC register	4 KB
0xF800_4000	0xF800_4FFF	GPIO5 register	4 KB
0xF800_5000	0xF800_7FFF	Reserved	124 KB
0xF800_8000	0xF800_8FFF	SEC Timer01 register	4 KB
0xF800_9000	0xF800_9FFF	SEC Timer23 register	4 KB
0xF800_A000	0xF83F_FFFF	Reserved	4056 KB
0xF840_0000	0xF840_FFFF	8051 local RAM	64 KB
0xF841_0000	0xF8A1_FFFF	Reserved	6208 KB
0xF8A2_0000	0xF8A2_0FFF	PERI_CTRL register	4 KB

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Start Address	End Address	Object	Size (Byte)
0xF8A2_1000	0xF8A2_1FFF	IO_CONFIG register	4 KB
0xF8A2_2000	0xF8A2_2FFF	CRG register	4 KB
0xF8A2_3000	0xF8A2_3FFF	PMC register	4 KB
0xF8A2_4000	0xF8A2_8FFF	Reserved	20 KB
0xF8A2_9000	0xF8A2_9FFF	Timer23 register	4 KB
0xF8A2_A000	0xF8A2_AFFF	Timer45 register	4 KB
0xF8A2_B000	0xF8A2_BFFF	Timer67 register	4 KB
0xF8A2_C000	0xF8A2_CFFF	WDG0 register	4 KB
0xF8A2_D000	0xF8A2_DFFF	WDG1 register	4 KB
0xF8A2_E000	0xF8A2_FFFF	Reserved	8 KB
0xF8A3_0000	0xF8A3_FFFF	MDDRC0 register	64 KB
0xF8A4_0000	0xF8A4_FFFF	Reserved	64 KB
0xF8A5_0000	0xF8A5_FFFF	Reserved	64 KB
0xF8A6_0000	0xF8A6_FFFF	Reserved	64 KB
0xF8A7_0000	0xF8A7_FFFF	Reserved	64 KB
0xF8A8_0000	0xF8A8_0FFF	SEC_CFG register	4 KB
0xF8A8_1000	0xF8A8_1FFF	Reserved	4 KB
0xF8A8_2000	0xF8A8_2FFF	PASTC register	4 KB
0xF8A8_3000	0xF8A8_FFFF	Reserved	52 KB
0xF8A9_0000	0xF8A9_FFFF	MKL	64 KB
0xF8AA_0000	0xF8AA_FFFF	Reserved	64 KB
0xF8AB_0000	0xF8AB_FFFF	OTP register	64 KB
0xF8AC_0000	0xF8AF_FFFF	Reserved	256 KB
0xF8B0_0000	0xF8B0_0FFF	UART0 register	4 KB
0xF8B0_1000	0xF8B0_1FFF	Reserved	4 KB
0xF8B0_2000	0xF8B0_2FFF	UART2 register	4 KB
0xF8B0_3000	0xF8B0_3FFF	Reserved	4 KB
0xF8B0_4000	0xF8B0_4FFF	Reserved	4 KB
0xF8B0_5000	0xF8B0_FFFF	Reserved	44 KB
0xF8B1_0000	0xF8B1_0FFF	I^2C0	4 KB
0xF8B1_1000	0xF8B1_1FFF	I^2C1	4 KB

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Start Address	End Address	Object	Size (Byte)
0xF8B1_2000	0xF8B1_2FFF	I^2C2	4 KB
0xF8B1_3000	0xF8B1_3FFF	I^2C3	4 KB
0xF8B1_4000	0xF8B1_4FFF	I^2C4	4 KB
0xF8B1_5000	0xF8B1_5FFF	Reserved	4 KB
0xF8B1_6000	0xF8B1_6FFF	Reserved	4 KB
0xF8B1_7000	0xF8B1_7FFF	Reserved	4 KB
0xF8B1_8000	0xF8B1_8FFF	SCI0 register	4 KB
0xF8B1_9000	0xF8B1_9FFF	Reserved	4 KB
0xF8B1_A000	0xF8B1_AFFF	SPI0 register	4 KB
0xF8B1_B000	0xF8B1_BFFF	Reserved	4 KB
0xF8B1_C000	0xF8B1_FFFF	Reserved	16 KB
0xF8B2_0000	0xF8B2_0FFF	GPIO0 register	4 KB
0xF8B2_1000	0xF8B2_1FFF	GPIO1 register	4 KB
0xF8B2_2000	0xF8B2_2FFF	GPIO2 register	4 KB
0xF8B2_3000	0xF8B2_3FFF	GPIO3 register	4 KB
0xF8B2_4000	0xF8B2_4FFF	GPIO4 register	4 KB
0xF8B2_5000	0xF8B2_5FFF	Reserved	4 KB
0xF8B2_6000	0xF8B2_6FFF	GPIO6 register	4 KB
0xF8B2_7000	0xF8B2_7FFF	GPIO7 register	4 KB
0xF8B2_8000	0xF8B2_8FFF	GPIO8 register	4 KB
0xF8B2_9000	0xF8B2_9FFF	GPIO9 register	4 KB
0xF8B2_A000	0xF8B2_AFFF	GPIO10 register	4 KB
0xF8B2_B000	0xF8B2_BFFF	GPIO11 register	4 KB
0xF8B2_C000	0xF8B2_CFFF	GPIO12 register	4 KB
0xF8B2_D000	0xF8B2_DFFF	Reserved	4 KB
0xF8B2_E000	0xF8B2_EFFF	Reserved	4 KB
0xF8B2_F000	0xF8B2_FFFF	Reserved	4 KB
0xF8B3_0000	0xF8B3_0FFF	Reserved	4 KB
0xF8B3_1000	0xF8B3_4FFF	Reserved	16 KB
0xF8B3_5000	0xF8B3_5FFF	Reserved	4 KB
0xF8B3_6000	0xF8B3_6FFF	Reserved	4 KB

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Start Address	End Address	Object	Size (Byte)
0xF8B3_7000	0xF8BA_FFFF	Reserved	484 KB
0xF8BB_0000	0xF8BB_FFFF	COUNT register	64 KB
0xF8BC_0000	0xF8C0_FFFF	Reserved	320 KB
0xF8C1_0000	0xF8C1_EFFF	TDE register	640 KB
0xF8C1_F000	0xF8C1_FFFF	TDE MMU register	4 KB
0xF8C2_0000	0xF8C2_EFFF	HWC register	60 KB
0xF8C2_F000	0xF8C2_FFFF	HWC MMU register	4 KB
0xF8C3_0000	0xF8C3_EFFF	VDH register	60 KB
0xF8C3_F000	0xF8C3_FFFF	VDH MMU register	4 KB
0xF8C4_0000	0xF8C4_EFFF	JPGD0 register	60 KB
0xF8C4_F000	0xF8C4_FFFF	JPGD0 MMU register	4 KB
0xF8C5_0000	0xF8C6_FFFF	Reserved	128 KB
0xF8C7_0000	0xF8C7_EFFF	PGD register	60 KB
0xF8C7_F000	0xF8C7_FFFF	PGD MMU register	4 KB
0xF8C8_0000	0xF8C8_EFFF	VEDU register	60 KB
0xF8C8_F000	0xF8C8_FFFF	VEDU MMU register	4 KB
0xF8C9_0000	0xF8C9_FFFF	JPGE register	64 KB
0xF8CA_0000	0xF8CA_FFFF	Reserved	64 KB
0xF8CB_0000	0xF8CB_EFFF	VPSS0 register	60 KB
0xF8CB_F000	0xF8CB_FFFF	VPSS0 MMU register	4 KB
0xF8CC_0000	0xF8CC_EFFF	VDP register	60 KB
0xF8CC_F000	0xF8CC_FFFF	VDP MMU register	4 KB
0xF8CD_0000	0xF8CD_FFFF	AIAO register	64 KB
0xF8CE_0000	0xF8CF_FFFF	HDMI_TX register	128 KB
0xF8D0_0000	0xF8D1_FFFF	Reserved	128 KB
0xF8D2_0000	0xF8D2_FFFF	Reserved	64 KB
0xF8D2_0000	0xF91F_FFFF	Reserved	4928 KB
0xF920_0000	0xF920_FFFF	GPU register	64 KB
0xF924_0000	0xF980_FFFF	Reserved	6080 KB
0xF980_0000	0xF980_FFFF	Reserved	64 KB
0xF981_0000	0xF981_FFFF	Reserved	64 KB

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Start Address	End Address	Object	Size (Byte)
0xF982_0000	0xF982_FFFF	SDIO0 register	64 KB
0xF983_0000	0xF983_FFFF	SDIO2/eMMC/SD card register	64 KB
0xF984_0000	0xF984_FFFF	GSF0 register	64 KB
0xF985_0000	0xF985_FFFF	Reserved	64 KB
0xF986_0000	0xF986_0FFF	PCIe0 peripheral register	4 KB
0xF986_1000	0xF986_1FFF	Reserved	4 KB
0xF986_2000	0xF987_FFFF	Reserved	120 KB
0xF988_0000	0xF988_FFFF	USB2Host0 open host controller interface (OHCI) register	64 KB
0xF989_0000	0xF989_FFFF	USB2Host0 enhanced host controller interface (EHCI) register	64 KB
0xF98A_0000	0xF98A_FFFF	USB3_0 register	64 KB
0xF98B_0000	0xF98B_FFFF	USB3_1 register	64 KB
0xF98C_0000	0xF98F_FFFF	USB2OTG0 register	256 KB
0xF990_0000	0xF990_FFFF	SATA register	64 KB
0xF991_0000	0xF991_FFFF	Reserved	64 KB
0xF992_0000	0xF992_FFFF	Reserved	64 KB
0xF993_0000	0xF993_FFFF	Reserved	64 KB
0xF994_0000	0xF994_FFFF	Reserved	64 KB
0xF995_0000	0xF995_FFFF	FMC register	64 KB
0xF996_0000	0xF99E_FFFF	Reserved	576 KB
0xF99F_0000	0xF99F_0FFF	Multi-cipher MMU register	4 KB
0xF99F_1000	0xF99F_FFFF	Reserved	60 KB
0xF9A0_0000	0xF9A0_FFFF	Multi-cipher register	64 KB
0xF9A1_0000	0xF9A1_FFFF	SHA1 (secure)	64 KB
0xF9A2_0000	0xF9A2_FFFF	SHA2 (non-secure)	64 KB
0xF9A3_0000	0xF9A3_0FFF	RSA register	4 KB
0xF9A3_0000	0xF9BE_FFFF	Reserved	1852 KB
0xF9BF_0000	0xF9BF_0FFF	PVR MMU register	4 KB
0xF9BF_1000	0xF9BF_FFFF	Reserved	60 KB
0xF9C0_0000	0xF9C0_FFFF	PVR0 register	64 KB
0xF9C1_0000	0xF9C1_FFFF	Reserved	64 KB

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Start Address	End Address	Object	Size (Byte)
0xF9C2_0000	0xF9C2_FFFF	Reserved	64 KB
0xF9C3_0000	0xF9C3_FFFF	Reserved	64 KB
0xF9C4_0000	0xF9C4_FFFF	SDIO1 register	64 KB
0xF9C5_0000	0xF9C5_FFFF	Reserved	64 KB
0xF9C6_0000	0xF9C6_FFFF	Reserved	64 KB
0xF9C7_0000	0xF9FF_FFFF	Reserved	3648 KB
0xFA00_0000	0xFBFF_FFFF	Reserved	32 MB
0xFC00_0000	0xFDFF_FFFF	Reserved	32 MB
0xFE00_0000	0xFE0F_FFFF	Reserved	1 MB
0xFE10_0000	0xFE1F_FFFF	Reserved	1 MB
0xFE20_0000	0xFE2F_FFFF	FMC MEM register	1 MB
0xFE30_0000	0xFFEF_FFFF	Reserved	28 MB
0xFFF0_0000	0xFFFD_FFFF	Reserved	896 KB
0xFFFE_0000	0xFFFE_FFFF	BOOTROM (in remap mode) or reserved (in remap clear mode)	64 KB
0xFFFF_0000	0xFFFF_FFFF	BOOTROM (in remap mode) or BOOTRAM (in remap clear mode)	64 KB

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5 Soldering Process

5.1 Overview

Objective

Define the zone temperatures in the surface mounting technology (SMT) phase.

Application Scope

HiSilicon Hi3798C V200

Basic Information

All HiSilicon products for customers comply with the restriction of the use of certain hazardous substances (RoHS) directive. In the part number format Hi*xxxx*RBC V*xxx*, the letter R indicates RoHS. These products are lead-free. The lead-free technology and mixing technology are used in the reflow soldering of HiSilicon chips.

Reflow Chart

Note the following:

- HiSilicon chips: All HiSilicon chips for customers are lead-free RoHS-compliant products.
- Lead-free technology: A technology in which solder paste and all components (including the board, all ICs, capacitors, and resistors) are lead-free.
- Mixing technology: A technology in which lead solder pastes, lead-free BGAs, and lead ICs are used.

5.2 Requirements of Lead-Free Reflow Soldering

Figure 5-1 shows a lead-free reflow soldering curve.

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Figure 5-1 Lead-free reflow soldering curve

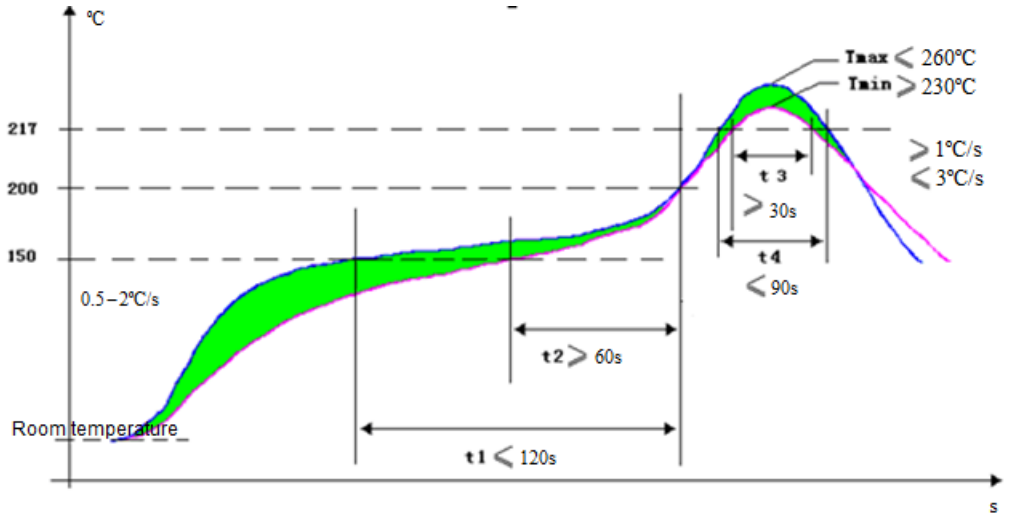

Table 5-1 describes lead-free reflow soldering parameters.

Table 5-1 Lead-free reflow soldering parameters

Zone	Duration	Heating Up Slope	Peak Temperature	Cooling Down Slope
Preheat zone (40–150°C or 104–302°F)	60–150s	≤ 2.0ºC/s (≤ 35.6ºF/s)	None	None
Soak zone (150–200°C or 302–392°F)	60–120s	< 1.0ºC/s (< 33.8ºF/s)	None	None
Reflow zone (> 217°C or 423°F)	60–90s	None	230−260ºC (446−500ºF)	None
Cooling zone (Tmax to 180°C or 356°F)	None	None	None	1.0ºC/s ≤ Slope ≤ 4.0ºC/s (33.8ºF/s ≤ Slope ≤ 39.2ºF/s)

NOTE

- Preheat zone: The temperate range is 40–150°C (104–302°F), the heating up slope must be about 2.0°C/s (36°F/s), and the zone duration must be 50–60s.
- Soak zone: The temperature range is 150–200°C (302–392°F), the heating up slope must be less than 1.0°C/s (34°F/s), and the zone duration must be 60–120s. Slow heating is required; otherwise, soldering is poor.
- Reflow zone: The zone temperature increases from 217°C (423°F) to Tmax, and then decreases from Tmax to 217°C (423°F). The zone duration must be 60–90s.
- Cooling zone: The zone temperature decreases from Tmax to 180°C (356°F). The cooling down slope must be within 4.0°C/s (39°F/s).
- The ambient temperate must increase from 25°C (77°F) to 250°C (482°F) within 6 minutes.

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- The reflow soldering curve shown in Figure 5-1 is recommended. However, you can adjust it as required.
- Typically, the duration of the reflow zone is 60–90s. For the boards with great heat capacity, the duration can be extended to 120s. For details about the requirements on package thermal resistance, see the IPC/JEDEC J-STD-020D standard. For details about the method of measuring the package temperature, see the JEP 140 standard.

Table 5-2 describes the thermal resistance standard for the lead-free package according to the IPC/JEDEC 020D standard.

Table 5-2 Thermal resistance standard for the lead-free package in the IPC/JEDEC 020D standard

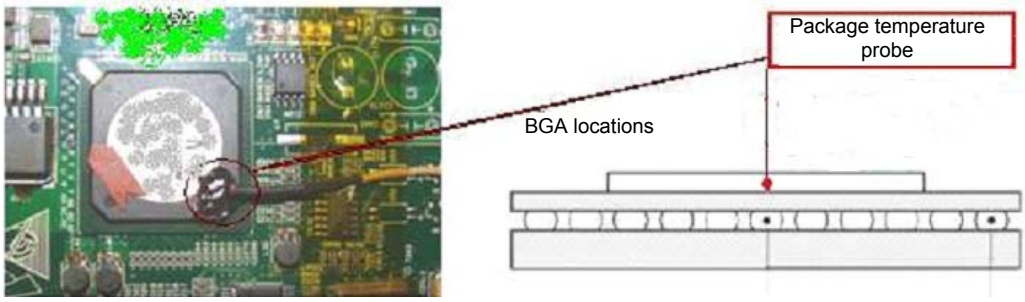
Package Thickness	Temperature 1 (Package Volume < 350 mm^3 or 0.02 $in.^3$)	Temperature 2 (Package Volume = 350–2000 mm^3 or 0.02–0.12 $in.^3$)	Temperature 3 (Package Volume > 2000 mm^3 or 0.12 $in.^3$)
< 1.6 mm (0.06 in.)	260°C (500°F)	260°C (500°F)	260°C (500°F)
1.6–2.5 mm (0.06–0.10 in.)	260°C (500°F)	250°C (482°F)	245°C (473°F)
> 2.5 mm (0.10 in.)	250°C (482°F)	245°C (473°F)	245°C (473°F)

The component soldering terminals (such as the solder ball and pin) and external heat sinks are not taken into account for volume calculation.

The measurement method for the reflow soldering curve is as follows:

According to the JEP140 standard, to measure the package temperature, you are advised to place the temperature probe of the thermocouple close to the chip surface if the package is thin or to drill a hole on the package surface and place the temperature probe of the thermocouple into the hole if the chip package is thick. The second method is recommended based on the thickness of most chip packages. However, this method is not applicable if the chip package is too thin to drill a hole. See Figure 5-2.

Figure 5-2 Measuring the package temperature



5.3 Requirements of Mixing Reflow Soldering

Lead-free components must be properly soldered during mixing reflow soldering. Table 5-3 describes mixing reflow soldering parameters.

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Table 5-3 Mixing reflow soldering parameters

Zone	Item	Lead BGA	Lead-free BGA	Other Components
Preheat zone (40–150°C or 104–302°F)	Duration	60–150s		
	Heating up slope	< 2.5°C/s (37°F/s)		
Soak zone (150–183°C or 302–361°F)	Duration	30–90s		
	Heating up slope	< 1.0°C/s (34°F/s)		
Reflow zone (> 183°C or 361°F)	Peak temperature	210–240°C (410–464°F)	220–240°C (428–464°F)	210–245°C (410–473°F)
	Duration	30–120s	60–120s	30–120s
Cooling zone (Tmax to 150°C or 302°F)	Cooling down slope	1.0°C/s ≤ Slope ≤ 4.0°C/s (34°F/s ≤ Slope ≤ 39°F/s)		

NOTE

The preceding parameter values are provided based on the soldering joint temperature. The maximum and minimum soldering joint temperatures for the board must meet the requirements described in Table 5-3.

When the soldering curve is adjusted, the package thermal resistance requirements on the board components must be met. For details about the requirements on package thermal resistance, see the IPC/JEDEC J-STD-020D standard. For details about the method of measuring the package temperature, see the JEP 140 standard.

Table 5-4 describes the thermal resistance standard for the lead package according to the IPC/JEDEC 020D standard.

Table 5-4 Thermal resistance standard for the lead package

Package Thickness	Temperature 1 (Package Volume < 350 mm^3 or 0.02 $in.^3$)	Temperature 1 (Package Volume ≥ 350 mm^3 or 0.02 $in.^3$)
< 2.5 mm (0.10 in.)	235°C (455°F)	220°C (428°F)
≥ 2.5 mm (0.10 in.)	220°C (428°F)	220°C (428°F)

The component soldering terminals (such as the solder ball and pin) and external heat sinks are not taken into account for volume calculation.

According to the JEP140 standard, the method for measuring the temperature of the package soldered with the mixing technology is the same as that for measuring the temperature of the package soldered with the lead-free technology. For details, see section 5.2 "Requirements of Lead-Free Reflow Soldering."

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6 Moisture-Sensitive Specifications

6.1 Overview

Objective

Define the usage rules for moisture-sensitive ICs, ensuring that ICs are properly used.

Application Scope

All HiSilicon products for external customers

Terminology

- Floor life: time during which a HiSilicon chip can be stored in the workshop at 30°C (86°F) and 60% relative humidity (RH), that is, the time from moisture barrier bag (MBB) unpacking to reflow soldering
- Desiccant: a material for absorbing moisture to keep things dry
- Humidity indicator card (HIC): a card that indicates the humidity status
- Moisture sensitivity level (MSL): a level for measuring the moisture degree. The MSL of Hi3798C V200 is level 3.
- MBB: a vacuum bag for protecting products against moisture
- Solder reflow: reflow soldering
- Shelf life: storage period

6.2 HiSilicon Moisture-proof Packaging

6.2.1 Basic Information

The vacuum packaging materials consist of the following:

- An HIC
- An MBB
- Desiccant

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Figure 6-1 Vacuum packaging materials

6.2.2 Incoming Inspection

When the vacuum bag is unpacked before SMT in the factories of customers or their partners:

- If the largest indicator dot of the HIC is not blue or khaki, rebake the chip by referring to Table 6-1.
- If the 10% RH dot of the HIC is blue or khaki, the chip is dry. In this case, replace the desiccant and pack the chip into a vacuum bag.

If the 10% RH dot is not blue or khaki and the 5% RH dot is red or light green, the chip is moist. In this case, rebake the chip by referring to Table 6-1.

6.2.3 Storage and Usage

Storage Environment

You are advised to store products at 30°C (86°F) or lower and at most 60% RH.

Shelf Life

At 30°C (86°F) or lower and at most 60% RH, the shelf life is greater than or equal to 12 months for vacuum packaging.

Floor Life

Table 6-1 describes the floor life at 30°C (86°F) or lower and at most 60% RH.

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Table 6-1 Floor life

MSL	Floor Life (Out of Bag) at Factory Ambient ≤ 30°C (86°F)/60% RH or As Stated
1	Unlimited at 30°C (86°F) or lower and at most 85% RH
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Mandatory bake before use. After bake, the product must be reflowed within the time limit specified on the label.

Usage

- If a chip has been exposed to air for more than 2 hours at 30°C (86°F) or lower and at most 60% RH, rebake it and pack it into a vacuum bag.
- If a chip has been exposed to air for not more than 2 hours at 30°C (86°F) or lower and at most 60% RH, replace the desiccant and pack the chip into a vacuum bag.

For details about other storage modes and usage rules, see the JEDEC J-STD-033A standard.

6.3 Rebaking

Applicable Products

All moisture-sensitive ICs of HiSilicon

Application Scope

All ICs that need to be rebaked

Rebaking Reference

Table 6-2 Rebaking reference

Body Thickness	Level	Baking at 125°C (257°F)	Baking at 90°C (194°F) ≤ 5% RH	Baking at 40°C (104°F) ≤ 5% RH
≤ 1.4 mm (0.06 in.)	2a	3 hours	11 hours	5 days
	3	7 hours	23 hours	9 days
	4	7 hours	23 hours	9 days

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Body Thickness	Level	Baking at 125°C (257°F)	Baking at 90°C (194°F) ≤ 5% RH	Baking at 40°C (104°F) ≤ 5% RH
	5	7 hours	24 hours	10 days
	5a	10 hours	24 hours	10 days
≤ 2.0 mm (0.08 in.)	2a	16 hours	2 days	22 days
	3	17 hours	2 days	23 days
	4	20 hours	3 days	28 days
	5	25 hours	4 days	35 days
	5a	40 hours	6 days	56 days
≤ 4.5 mm (0.18 in.)	2a	48 hours	7 days	67 days
	3	48 hours	8 days	67 days
	4	48 hours	10 days	67 days
	5	48 hours	10 days	67 days
	5a	48 hours	10 days	67 days

NOTE

- Table 6-2 lists the minimum rebaking time for moist chips.
- Low-temperature rebaking is recommended.
- For details, see the JEDEC standard.

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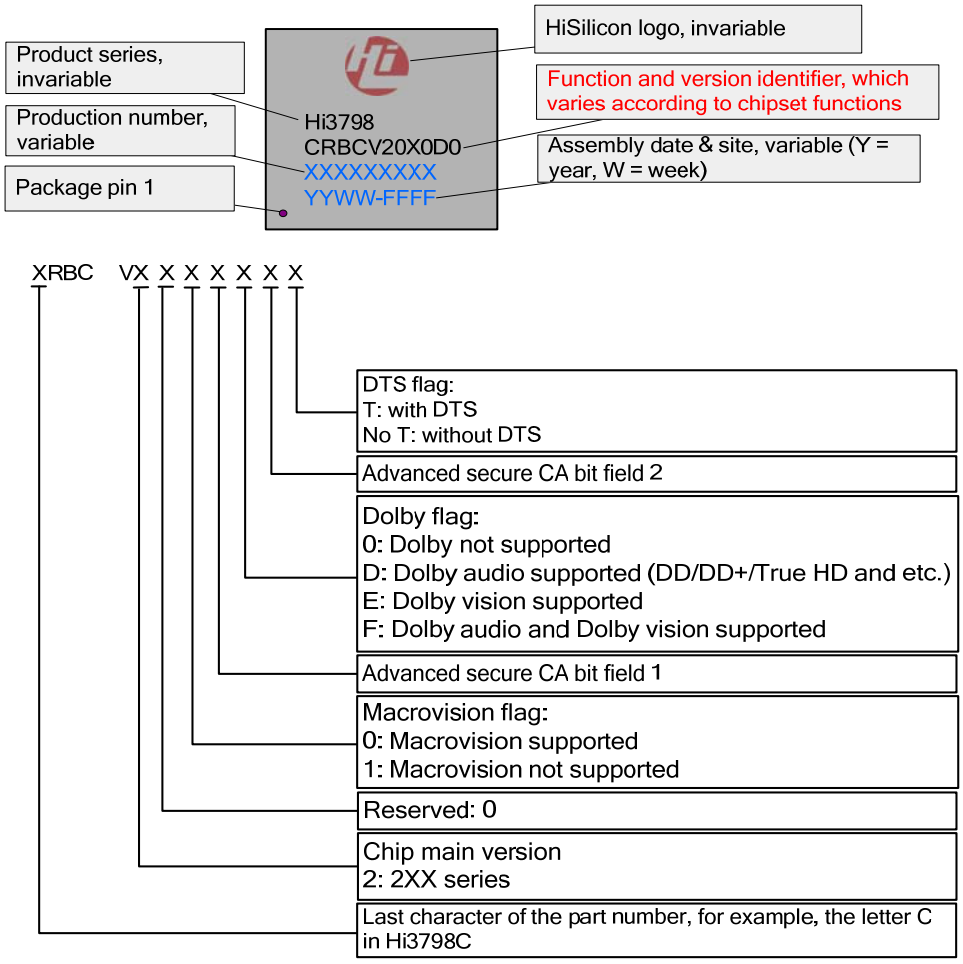
7 Ordering Information

Figure 7-1 illustrates the mark naming convention of Hi3798C V200.

Hi*XXXX* indicates the 6-digit product model before the part number.

Figure 7-1 Mark naming convention



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NOTE

- The letter *X* in the part number indicates variable digits and is only for internal use.
- For details about the conventions for the advanced CA bit field, consult the HiSilicon technical support engineers.

Table 7-1 Packages

Part Number	Package	Body Size	Pitch
Hi3798 CRBC V20X XXX	TFBGA 433	19 mm x 19 mm (0.74 in. x 0.74 in.)	0.8 mm (0.03 in. x 0.03 in.)

For example, if the part number is Hi3798CRBC V2010D0, the chip supports Dolby but not Macrovision (Rovi) and DTS.

CAUTION

According to the technical agreement between HiSilicon and providers of third-party software, HiSilicon has no rights to provide technical samples of the third-party software for other parties. Therefore, if the third-party software or chips that are provided for only authenticated users are involved (including but not limited to DD+ and DTS), ensure that you have obtained authentication from the third party when you place an order for the HiSilicon chip.

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A Acronyms and Abbreviations

A	
AAC	advanced audio coding
AAF	anti-aliasing filter
ABR	average bit rate
AC	alternating current
ACA	accessory charge adapter
ACC	automatic contrast control
ACD	auto command done
ACM	adaptive coding and modulation
ADP	attach detection protocol
ADC	analog-to-digital converter
AE	automatic exposure
AEC	audio echo cancelation
AES	advanced encryption standard
AF	adaption field
AGC	automatic gain control
AHB	advanced high-performance bus
AI	audio input
AIU	audio input unit
ALU	arithmetic logic unit
AMBA	advanced microcontroller bus architecture
AMP	asymmetric multi-processing
ANI	automatic number identification
ANR	automatic noise reduction

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AO	audio output
AOU	audio output unit
AP	access point
APB	advanced peripheral bus
API	application programming interface
APLL	analog phase-locked loop
APSK	amplitude phase shift keying
AQTD	alternate queue transfer descriptor
ARM	advanced RISC machines
ARGB	alpha, red, green, blue
ASF	advanced specification format
ATA	advanced technology attachment
ATAH	ATA host controller
ATAPI	advanced technology attachment packet interface
ATR	answer to reset
ATTR	attribute
AUD	audio
AV	audio & video
AVI	auxiliary video information
AVS	audio video coding standard
AWB	automatic white balance
AXI	advanced extensible interface

B

BB	baseband
BCH	Bose-Chaudhuri-Hocquenghem
BCM	byte counter modified
BEP	boot entrance point
BER	bit error rate
BGA	ball grid array
BIST	built-in self test
BIU	bus interface unit
BMC	bi-phase mark coding

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BND	bayonet nut connector
BOM	bill of material
BPD	bit plan decoder
BPSK	binary phase shift keying
BRG	bridge
BSP	board support package
BVACT	bottom vertical active area
BVBB	bottom vertical back blank
BVFB	bottom vertical front blank

C

CA	conditional access
CABAC	context-based adaptive binary arithmetic coding
CAR	committed access rate
CAS	column address signal.
CAVLC	context adaptive variable length coding
CBC	cipher block chaining
CBR	constant bit rate
CCB	change control board
CCC	command completion coalescing
CCD	charge-coupled device
CCM	constant coding and modulation
CD	command done or collision detection
CDR	clock data recovery
CEC	consumer electronics control
CF	compact flash
CFB	cipher feedback
CFR	crest factor reduction
CGI	common gate interface
CGMS	copy generation management system
CI	common interface
CIC	cascaded integrator comb
CIU	card interface unit

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CL	CAS latency
CLK	clock
CML	current mode logic
CMOS	complementary metal-oxide semiconductor
CN	carrier noise
CNG	comfort noise generator
CODEC	coder/decoder
CP	charge pump
CPL	completion
CPLD	complex programmable logic device
CPU	central processing unit
CR	carrier recovery
CRAMFS	compressed ROM file system
CRC	cyclic redundancy check
CRG	clock and reset generator
CRS	completion retry request
CS	chip select
CSA	common scramble algorithm
CSI	camera serial interface
CSIX	common switch interface
CSMD	carrier sense multiple access
CTI	chroma transient improvement
CTR	counter
CTS	clear to send
CVBS	composite video broadcast signal
CW	cipher word

D

DAC	digital-to-analog converter
DAG	digital automatic gain
DAGC	digital automatic gain control
DAV	DMA of audio and video
DC	direct current

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DCD	data connect detection
DCRC	data CRC error
DCT	discrete cosine transform
DDC	display data channel
DDR	double data-rate
DDRC	double data rate controller
DHCP	dynamic host configuration protocol
DEM	dynamic-element matching
DES	data encryption standard
DFT	design for testability
DIP	dual in-line package
DIS	digital image stabilization
DiSEqC	digital satellite equipment control
DLL	delay locked loop
DM	data mask
DMA	direct memory access
DMAC	direct memory access controller
DNR	digital noise reduction
DP	data path
DPLL	digital phase-locked loop
DQ	data input/output
DQS	data strobe
DR	design requirement
DRAM	dynamic random access memory
DRC	dynamic range compression
DRM	digital rights management
DRTO	data read timeout
DSI	display serial interface
DSU	dedicated scaling unit
DTMF	dual-tone multi-frequency
DTO	data transfer over
DVB	digital video broadcasting
DVB-S	digital video broadcasting-satellite

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DVD	digital versatile disc
DVI	digital visual interface
DVR	digital video recorder
DWA	data weighted averaging

E

E2PROM	electrically erasable programmable read-only memory
EAV	end of active video
EB	eviction buffer
EBE	end-bit error
EBI	external bus interface
ECB	electronic code book
ECC	error correcting code
ECM	entitlement control message
ECS	embedded CPU subsystem
ED	exposed die
EDID	extended display identification data
EEE	energy efficient Ethernet
EHCI	enhanced host controller interface
EMI	electromagnetic interference
EMM	entitlement management message
eMMC	embedded multimedia card
EOP	end of PES
EoS	Ethernet over SONET/SDH
EP	end point
EPG	electronic program guide
EQU	equalizer
ERR	error
ES	element stream
eSATA	external serial advanced technology attachment
ESD	electrostatic discharge
ESR	equivalent series resistance
ETH	Ethernet

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ETU	elementary time unit
F	
FAS	frame aligning signal
FBE	feedback equalizer
FC	switch fabric
FCBGA	flip-chip ball grid array
FCCSP	flip-chip chip scale package
FEC	forward error correction
FER	frame error rate
FFC	flexible flat cable
FFE	feed forward equalizer
FIFO	first in first out
FIQ	fast interrupt request
FIR	finite impulse response
FIS	frame information structure
FOD	field order detect
FPC	flexible printed connector
FPU	floating-point unit
FRUN	FIFO underrun/overrun error
FSK	frequency shift keying
FTP	File Transfer Protocol
G	
GFP-F	frame-mapped generic framing procedure
GFP-T	transparent generic framing procedure
GHB	global history buffer
GIC	generic interrupt controller
GOP	group of picture
GS	generic stream
GMAC	gigabit media access control
GND	ground
GPIO	general purpose input/output

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GPL	GNU general public license
GPU	graphics processing unit

H

HBA	host bus adapter
HBP	horizontal back porch
HD	high definition
HDCP	high-bandwidth digital content protection
HDI	high density interconnector
HDMI	high definition multimedia interface
HFP	horizontal front porch
HIAO	high-performance audio output interface
HPW	horizontal pulse width
HSTL	high speed transceiver logic
HTML	hypertext markup language
HACT	horizontal active area
HFB	horizontal front blank
HL	high level
HLDC	horizontal lens distortion correction
HLE	hardware locked error
HNP	host negotiation protocol
HTO	data starvation-by-host timeout
HP	high profile
HSIC	high-speed inter-chip
HSS	high-speed serializer/deserializer
HTTP	Hypertext Transfer Protocol
HTTPS	Hypertext Transfer Protocol Secure
HVBB	horizontal back blank
HWC	hardware composition

I

I	in-phase
IBIS	input/output buffer information specification

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IC	integrated circuit
I^{2}C	inter-integrated circuit
I^{2}S	inter-IC sound
I/O	input/output
IOC	I/O configuration
IP	Internet Protocol
ISI	input stream identifier
ISP	image signal processor
IDE	integrated device electronic
LDPC	low-density parity check code
IDR	intermediate data rate
IF	intermediate frequency
IGMP	Internet Group Management Protocol
LMS	linear mean square
IPF	IP filter
IPv4	Internet Protocol Version 4
IR	infrared
IRQ	interrupt request
ISI	input stream identifier
ISP	image signal processor
ISR	interrupt service routine
ITCM	instruction tightly coupled memory
ITLA	integrated tunable laser assembly
ITU	International Telecommunication Union
IV	initialization vector

J

JFFS2	journaling flash file system version 2
JPEG	Joint Photographic Experts Group
JPGD	JPEG decoder
JPGE	JPEG encoder
JTAG	Joint Test Action Group

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K

KL	key ladder

L

LCD	liquid crystal display
LDO	low dropout regulator
LDPC	low-density parity check code
LED	light emitting diode
LFB	line fill buffer
LFSR	linear feedback shifting register
LMR	load mode register
LMS	least mean square
LNB	low noise block
LOS	loss of signal
LPI	low-power idle
LRB	line read buffer
LSB	least significant bit
LSP	label switched path
LSN	logic sector number
LTI	luma transient improvement
LVDS	low-voltage differential signaling
LVPECL	low-voltage positive emitter-coupled logic
LVTTL	low-voltage transistor-transistor logic
LVPECL	low-voltage positive emitter-coupled logic

M

MAC	media access control
MBAFF	macroblock adaptive frame field
MCE	media control engine
MCU	microprogrammed control unit
MD	motion detection
MDDRC	multiport DDRC
MDIO	management data input/output

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MDU	motion detect unit
MF	matched filter
MQFN	mapped quad flat non-leaded
MHL	mobile high-definition link
MII	media independent interface
MIPI	mobile industry processor interface
MIPS	microprocessor without interlocked pipeline stages
MLC	multi-level cell
MLF	malformed
MMB	media memory block
MMC	multimedia card
MMU	memory management unit
MMZ	media memory zone
MP	main profile
MPI	MPP programming interface
MPE	media processing engine
MPLL	multiplying phase-locked loop
MPP	media processing platform
MRL	manually-operated retention latch
MSB	most significant bit
MSE	mean square error
MSG	message
MV	motion vector

N

NAL	network abstraction layer
NANDC	NAND flash controller
NC	not connect
NCQ	native command queuing
NLP	non-linear processor
NR	noise reduction
NRZ	non-return-to-zero
NTSC	National Television Systems Committee

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NVR	network video recorder
O	
OCT	on-chip termination
OD	open drain
ODT	on-die termination
OEN	output enable
OFB	output feedback
OHCI	open host controller interface
OOB	out of band
OP	operational amplifier
OR	original requirement
OSC	oscillator
OSD	on screen display
OTG	on-the-go
OTP	one time programmable
OTU	optical transponder unit
P	
PAD	packet assembler/disassembler
PAFF	picture adaptive frame field
PAL	phase alternating line
PCB	printed circuit board
PCI	peripheral component interconnect
PCIe	peripheral component interconnect express
PCIV	PCI view
PCR	program clock reference
PCM	pulse code modulation
PDM	pulse density modulation
PECL	positive emitter coupled logic
PER	packet error rate
PES	packetized elementary stream
PG	power/ground

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PGD	PNG and GIF decoder
PHY	physical
PID	packet ID
PIM-DM	protocol independent multicast dense mode
PIM-SM	protocol independent multicast sparse mode
PIO	programmable input/output
PLL	phase-locked loop
PLS	physical layer signaling
PM	port multiplexer
PMoC	power management of chip
PMP	personal media player
POR	power-on reset
PPP	Point-to-Point Protocol
PPS	picture parameter set
PRBS	pseudo random binary sequence
PRDT	physical region descriptor table
PSI	program specific information
PSK	phase shift keying
PSRAM	pseudo static random access memory
RTCP	Real-time Transport Control Protocol
RTP	Real-time Transport Protocol
PT	packet type
PTS	presentation time stamp
PUB	PHY utility block
PUSI	payload unit start indicator
PWM	pulse width modulation

Q

Q	quadrant
QAM	quadrature amplitude modulation
QDR	quad data rate
QoS	quality of service
QP	quantizer parameter

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QPSK	quaternary phase shift keying
R	
RAM	random access memory
RAS	row address signal
RC	resistor-capacitor
RCA	Radio Corporation of America
RCRC	response CRC error
RE	response error
RF	radio frequency
RGB	red-green-blue
RGMII	reduced gigabit media independent interface
RH	relative humidity
RoHS	restriction of the use of certain hazardous substances
ROI	region of interest
ROM	read-only memory
ROP	raster operation
RPR	resilient packet ring
RLDRAM	reduced latency dynamic random access memory
RMII	reduced media-independent interface
RS	Reed-Solomon
RTC	real-time clock
RTO	response timeout
RTS	request to send
RVDS	RealView development suite
RX	receive
RXDR	receive FIFO data request
S	
SAP	service access point
SAD	sum of absolute difference
SAR	successive approximation
SATA	serial advanced technology attachment

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SAV	start of active video
SBE	start-bit error
SBP	secure boot procedure
SCD	start code detect
SCI	smart card interface
SCL	serial clock
SCR	system clock reference
SCS	secure chipset start-up
SCU	snoop control unit
SD	secure digital
SDA	serial data
SDB	set device bits
SDH	synchronous digital hierarchy
SDHC	secure digital high capacity
SDI	serial digital interface
SDIO	secure digital input/output
SDK	software development kit
SDRAM	synchronous dynamic random access memory
SDV	system design verification
SI	specific information
SIO	sonic input/output
SLC	single-level cell
SMI	static memory interface
SNAP	subnetwork access point
SNR	signal-to-noise ratio
SNTF	serial ATA notification
SOA	semiconductor optical amplifier
SoC	system-on-chip
SONET	synchronous optical network
SOP	start of PES
SP	simple profile
SPDIF	Sony/Philips digital interface
SPI	serial peripheral interface

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SPS	sequence parameter set
SRAM	static random access memory
SRP	Session Request Protocol
SSA	secure software authentication
SSD	secure software download
SSMC	synchronous static memory controller
SSP	synchronous serial port
SSRAM	synchronous static random access memory
SSTL-18	stub series terminated logic for 1.8 V
STA	station
STB	set-top box
STM-1	synchronous transport module level 1
SVB	selective voltage binning
SYNC	synchronization
SYS	system

T

TBD	to be determined
TBGA	tape ball grid array
TC	traffic class
TCP	Transmission Control Protocol
TD	TLP digest
TDES	triple data encryption standard
TDE	two-dimensional engine
TE	tearing effect
TEI	transport error indicator
TFD	task file data
TFPBGA	tape fine-pitch ball grid array
TFT	thin-film technology
TI	Texas Instruments
TLV	type-length-value
TOE	TCP/IP offload engine
TP	transponder

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TPIT	TS packet index table
TR	timing recovery
TS	transport stream
TSI	transport stream interface
TT	teletext
TV	television
TVACT	top vertical active area
TVBB	top vertical back blank
TVFB	top vertical front blank
TVS	transient voltage suppressor
TX	transmit
TXDR	transmit FIFO data request

U

UART	universal asynchronous receiver transmitter
U-boot	universal boot loader
UC	unexpected completion
UDP	User Datagram Protocol
ULPI	UTMI low pin interface
UPnP	universal plug and play
UR	unsupported request
USB	universal serial bus
USIM	universal subscriber identity module
UTMI	USB 2.0 transceiver macrocell interface

V

VACT	vertical active area
VAD	voice activity detector
VAPU	video analysis and process unit
VBB	vertical back blank
VBI	vertical blanking interval
VBR	variable bit rate
VCC	common connector voltage

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VCO	voltage controller oscillator
VCM	variable coding and modulation
VCMP	video compress
VCXO	voltage control crystal oscillator
VDA	video detection analysis
VDH	video decoder for high-definition
VDM	video decoding module
VDEC	video decoding
VDP	video display
VEDU	video encoding/decoding unit
VENC	video encoding
VFB	vertical front blank
VFMW	video firmware
VFP	vertical front porch
VGA	video graphics array
VI	video input
VIC	vector interrupt controller
VICAP	video capture
VIU	video input unit
VLD	valid
VLL	virtual leased line
VO	video output
VOIE	voice encoder
VOU	video output unit
VPP	video pre-processing
VPS	video programming system
VPSS	video process subsystem
VPW	vertical pulse width
VSA	vertical sync start
VQE	voice quality enhancement
VQM	voice quality monitor

W

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WDG	watchdog
WE	write enable
WFE	wait for event
WFI	wait for interrupt
WRED	weighted random early discard
WSS	wide screen signaling

X

XAUI	10 gigabit attachment unit interface

Y

YAFFS	yet another flash file system
YUV	luminance-bandwidth-chrominance

Z

ZME	zoom engine

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