HiKey

USER'S GUIDE

Revision	NOTES	BY	DATE
0.1	Initial Draft	Mihai Nedelcu	2/5/2015
0.2	Corrections from George Grey, Added DSI Switch in list of major components,	Mihai Nedelcu	2/6/2015

Table of Contents

I. TOP SIDE BOARD INTERFACES 5
II. BOTTOM SIDE BOARD INTERFACES 6
1. SETTINGS JUMPER and UART JUMPER 7
2. J2 Low speed expansion connector 8
3. S2 – POWER ON Button 9
4. J12-14 – POWER MEASUREMENTS 10
5. P1 – DC IN JACK 11
6. J8 – ANTENNA Connector 11
7. P2 – uSD CARD Socket 12
8. DISPLAY INTERFACES : P3-HDMI / HS EXP 13
9. J1 – High Speed EXP CNT 14
10. USB INTERFACES: 15
11. System and USER LEDs 16
12. JTAG HEADER 17
III. TOP AND BOTTOM SIDE MAJOR COMPONENTS 18

Table of Figures

Figure 1 – Top side view of the HiKey PCB 5
Figure 2 – Bottom side view of the HiKey PCB 6
Figure 3 – J15 SEL Jumper 7
Figure 4 – UART Debug Header 7
Figure 5 – HiKey LS Expansion Connector 8
Figure 6 – Fan Power Location on LS Expansion 9
Figure 7 – ON/OFF and Reset signals on LS Expansion 9
Figure 8 – Location of Sense Resistors and Headers 10
Figure 9 – DC power jack configuration 11
Figure 10 – HiKey WLAN and BT section and antenna options 11
Figure 11 - SDIO Implementation on HiKey Board 12
Figure 12 - Display Interface Block Diagram 13
Figure 13 – HiKey HS Expansion Connector 14
Figure 14 – USB OTG Connector and WiFi/BT LEDs 15
Figure 15 – WiFi and BT Activity LEDs 16
Figure 16 – User LEDs 16
Figure 17 - Footpring for JTAG header on bottom side of HiKey PCB 17

I. TOP SIDE BOARD interfaces

Figure 1 shows the top side of the HiKey board and lists the main components and interfaces.

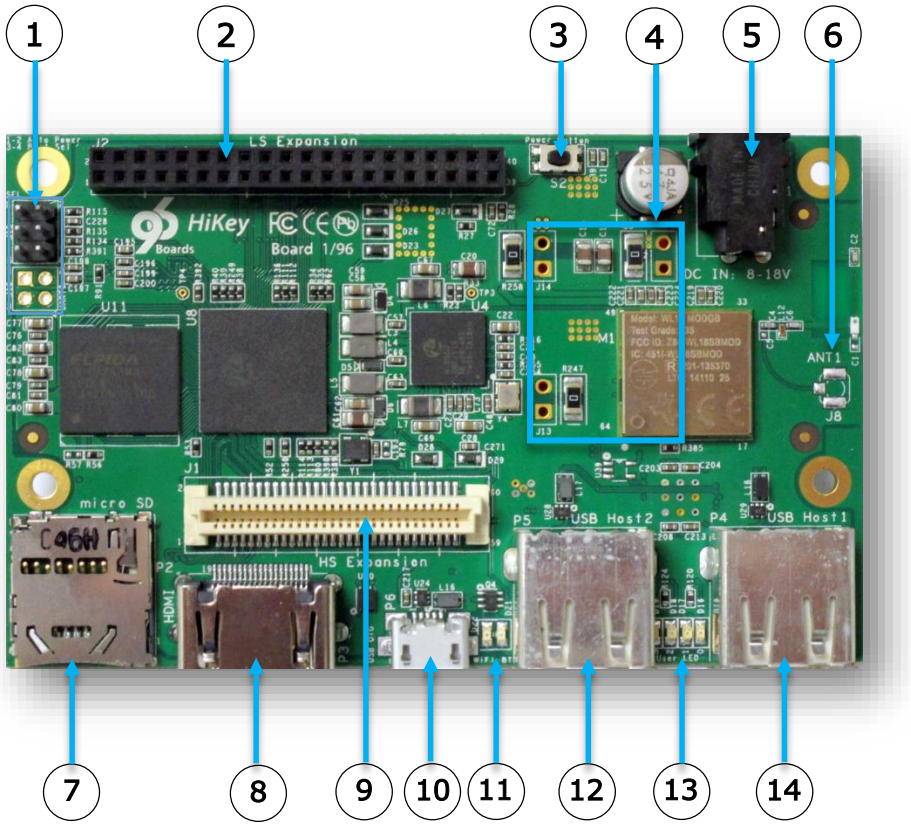

Figure 1 – Top side view of the HiKey PCB

1	**J15/16 - SETTINGS & UART**	Page 4	8	**P3 – HDMI PLUG**	Page 9
2	**J2 - LS EXPANSION CNT**	Page 5	9	**J1 – High Speed EXP CNT**	Page 10
3	**S2 - POWER ON Button**	Page 6	10	**P6 – USB OTG Connector**	Page 11
4	**J12-14 – POWER Measure**	Page 7	11	**D21/22 - WiFi/BT LEDs**	Page 12
5	**P1 - DC IN JACK**	Page 8	12	**P5 – USB HOST Connector 2**	Page 11
6	**J8 – ANTENNA Connector**	Page 8	13	**D16-D19 – USER LEDs**	Page 12
7	**P2 – uSD CARD Socket**	Page 9	14	**P4 – USB HOST Connector 1**	Page 11

II. BOTTOM SIDE BOARD INTERFACES

Figure 2 below shows the header footprint for the JTAG interface.

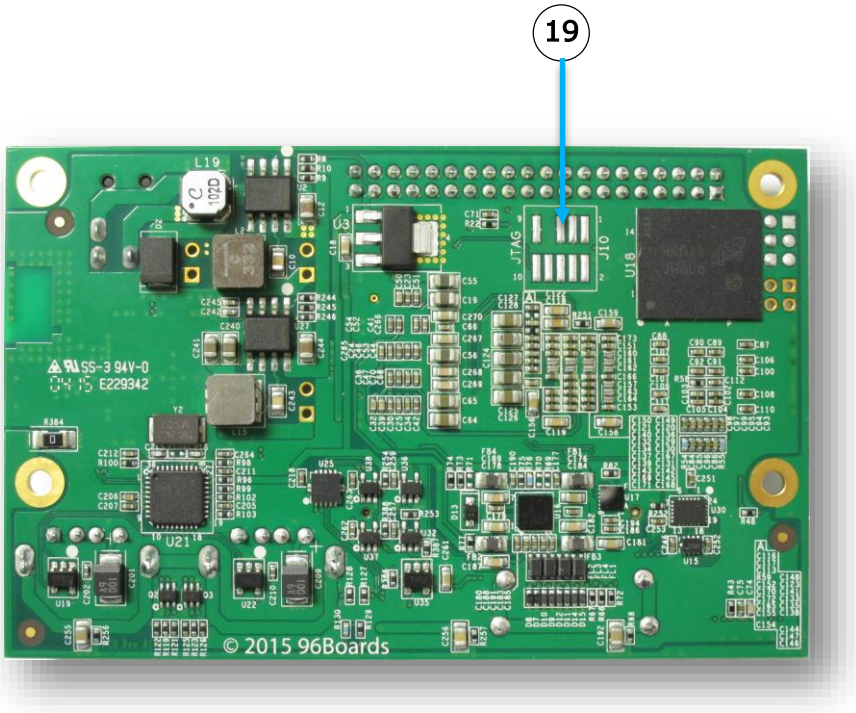

Figure 2 – Bottom side view of the HiKey PCB

19 **J10 JTAG HEADER OPTION** Page 17

1. SETTINGS JUMPER and UART JUMPER

The HiKey board has multiple boot options that are user selectable in hardware and can be set via shunts installed on header J15.

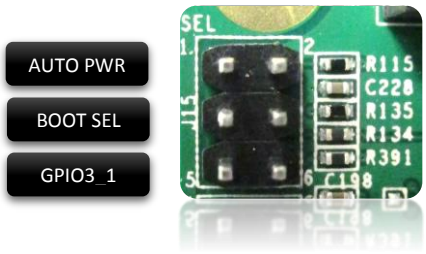

Figure 3 – J15 SEL Jumper

- Auto Power Jumper
  - CLOSED: system will boot up automatically when the power supply is applied.
  - OPEN (default): Pressing the power switch is required to boot up the system.
- Boot Setting Jumper
  - CLOSED: the will attempt to program the eMMC flash from USB OTG source. This should ONLY be used if the first stage bootloader is corrupted or needs to be replaced.
  - OPEN (default): the unit boots from the first stage bootloader installed in the onboard eMMC device.
- User Jumper
  - Connected to GPIO3_1 on the SoC and available to the developer
  - CLOSED: GPIO3_1 will be pulled low
  - OPEN (default): GPIO3_1 will be pulled high

The HiKey board also has an option for a Debug UART Header. This is normally used by the first stage bootloader developers, and is connected to the UART0 port of the SoC. This is available if a 2x2 male header is installed at J16. See below for the pinout of this header.

Figure 4 – UART Debug Header

Table 1 – J16 UART Debug Signals

1.8V	1	2	UART0_RX
DGND	3	4	UART0_TX

2. J2 LOW SPEED EXPANSION Connector

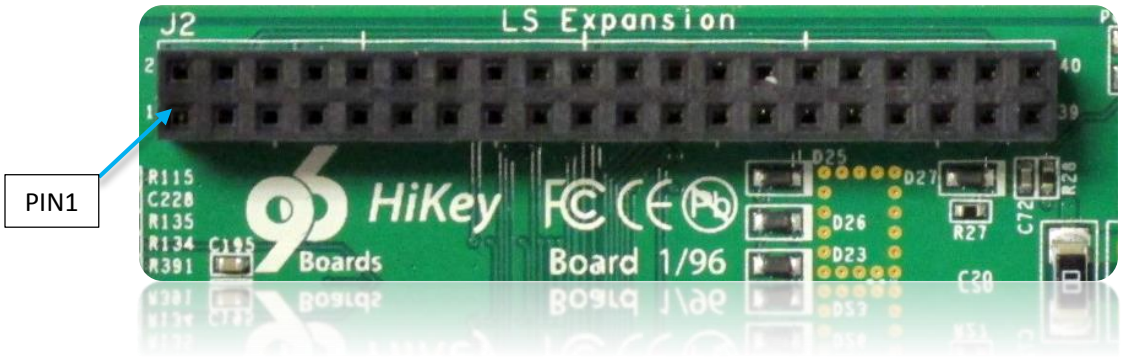

Figure 5 – HiKey LS Expansion Connector

The HiKey board features two expansion connectors: one low speed expansion connector and one high speed. The low speed expansion connector carries GPIO and other low speed interfaces. The connector is a low profile 40 pin female 2mm receptacle (20x2) of a specified height of 4.5mm height.

The low speed expansion brings out 1.8V level SoC signals such as UART2 and UART3, I2C0 and I2C1, GPIO signals as well as SPI, Audio, Reset, 1.8V and Ground. The complete list of SoC signals is shown in **Table 1** below:

Table 2 Low Speed Expansion Connector Signals

DGND	1	2	DGND
UART2_CTS_N	3	4	PMU_PWRON_N
UART2_TX	5	6	EXP_RSTOUT_N
UART2_RX	7	8	SPI0_SCLK
UART2_RTS_N	9	10	SPI0_DI
UART3_TX	11	12	SPI0_CS_N
UART3_RX	13	14	SPI0_DO
I2C0_SCL	15	16	MODEM_PCM_XFS
I2C0_SDA	17	18	MODEM_PCM_XCLK
I2C1_SCL	19	20	MODEM_PCM_DO
I2C1_SDA	21	22	MODEM_PCM_DI
GPIO2_0	23	24	GPIO2_1
GPIO2_2	25	26	GPIO3_3
GPIO2_4	27	28	BL_PWDN0_GPIO9_1
GPIO6_7_DSI_TE0	29	30	GPIO2_7
ISP_RSTB0_GPIO10_2	31	32	ISP_PWDN0_GPIO9_1
GSP_RSTB1_GPIO10_3	33	34	ISP_PWDN1_GPIO9_2
LD021_1V8	35	36	SYSDC_IN
SYS_5V	37	38	SYSDC_IN
DGND	39	40	DGND

The HiKey board can also drive 5V or 12V cooling fans. The power for these is available on the low speed Expansion connector and can be supplied through a 2-pin 2mm male header inserted at pins J2.37-J2.39 or J2.38-J2.40, respectively. **Figure 6** shows details.

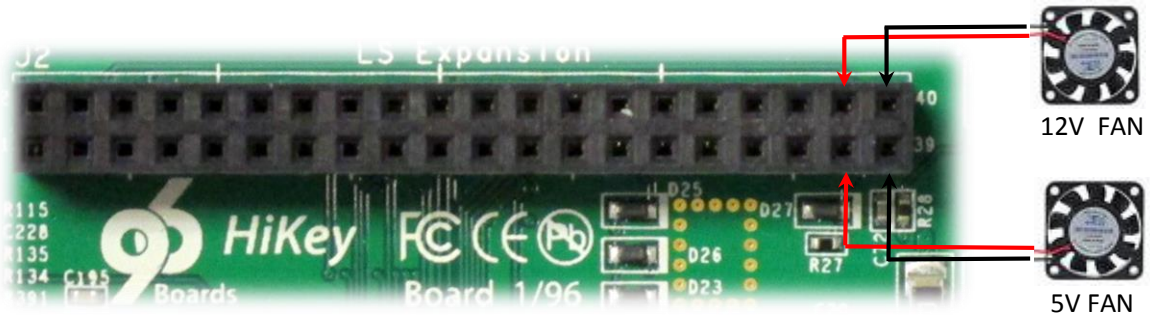

Figure 6 – Fan Power Location on LS Expansion

3. S2 – POWER ON Button

The power button S2 can be used to power up, power down, and reset the system. The circuit is designed such that the user will be able to manually power up, down and reset the board.

- A simple press and release powers ON the board provided the Auto Power Jumper is not installed.
- A press and release will then power OFF the board
- A press and hold for >4 seconds will RESET the board

It is also possible to connect external switches for power on/off and for hard reset. This is implemented by routing the specific power signals to the low speed bus connector as shown in **Figure 7**

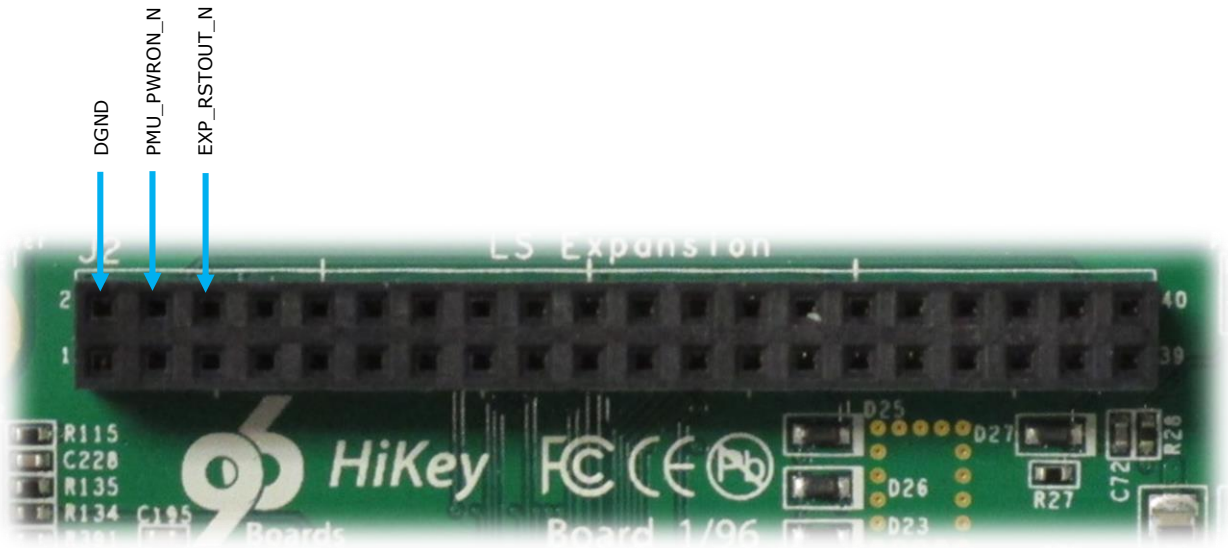

Figure 7 – ON/OFF and Reset signals on LS Expansion

4. J12-14 – POWER MEASUREMENTS

The HiKey board supports power measurements for instrumentation and testing. 1% 1206 sense resistors can be user installed at specific locations in place of the 0Ω resistors currently populated on the board. To connect to these sense resistors, the PCB provides footprints for 100mil 2-pin headers that can be installed. For voltage measurements, digital GND is provided on the low speed expansion connector.

The HiKey board was designed to provide current measurements for the following rails:

Table 3 – Power Measurement Rails

RESISTOR	HEADER	RAIL	MEASUREMENT
R7	J12	DC_IN	Total Base Board Power
R247	J13	VDD_4V2	PMIC
R258	J14	SYS_5V	HDMI, USB

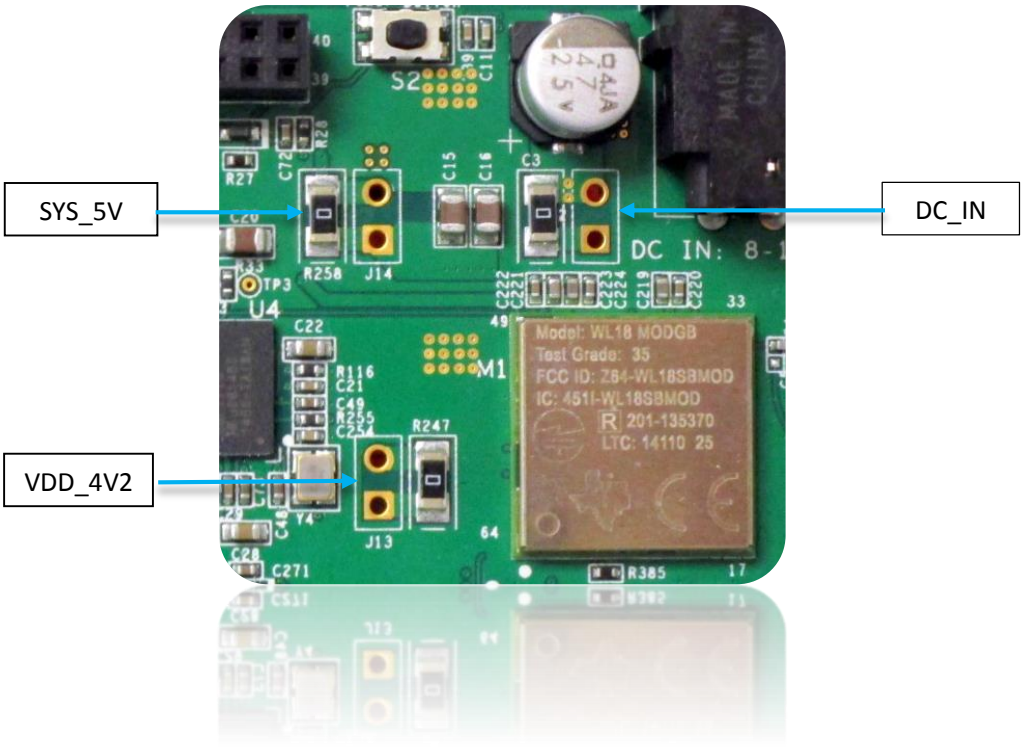

Figure 8 – Location of Sense Resistors and Headers

NOTE: Pin_1 of J12, J13 and J14 is the source, positive terminal.

5. P1 – DC IN JACK

DC Power is provided via the DC jack at P1. This is a CUI PJ-041H connector with a center pin diameter of 1.65mm configured with positive polarity (center +).

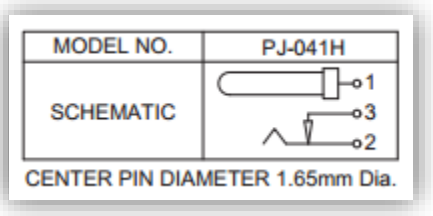

Figure 9 – DC power jack configuration

An 8V up to 18V power supply at a minimum of 2A rating can be used to provide sufficient board power for on system requirements as well as external devices. Additional current rating may be required for mezzanine boards or modules. DC Power can also be supplied via the SYS_DCIN pins on the low speed expansion. See **Table 2**.

NOTE: Power should not be supplied simultaneously from multiple sources

6. J8 – ANTENNA Connector

The HiKey board is equipped with a TI WL1835MOD WLAN Baseband Processor and RF Transceiver which supports IEEE 802.11a, 802.11b, 802.11g and 802.11n WiFi and Bluetooth 4.1.

A PCB chip antenna is available onboard by default but also an external antenna socket option is provided via J8 footprint. A Hirose U.FL-R-SMT connector can be soldered at J8 location.

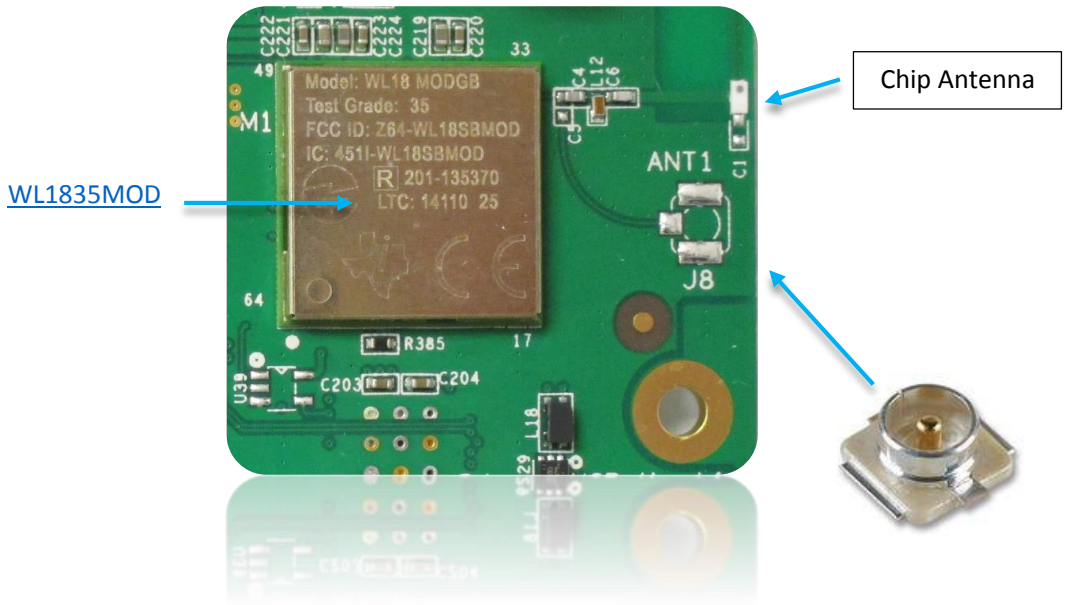

Figure 10 – HiKey WLAN and BT section and antenna options

7. P2 – µSD CARD Socket

An ALPS micro SDHC card socket P2, part number SCHA4B0415, is installed on the HiKey board on the bottom left corner of the PCB. If a suitable bootloader is installed and a bootable microSD card is installed at power up, the HiKey board can boot from software installed on the microSD card and not the default OS stored in the on-board eMMC flash memory.

The SD socket features a push-push eject mechanism and has the following electrical assignment (not including mounting pins):

Table 4 – SD Card Cage pin definition

DATA2	1
CD/DATA3	3
CMD	5
VDD	4
CLOCK	5
VSS	6
DATA0	7
DATA1	8
CD	9
COMMON	10

SD1 signals can be found on the HS Expansion connector in the area shown by the blue rectangle. Please see **Table 5** for details.

The diagram below shows the implementation of the SDIO interface on the HiKey board.

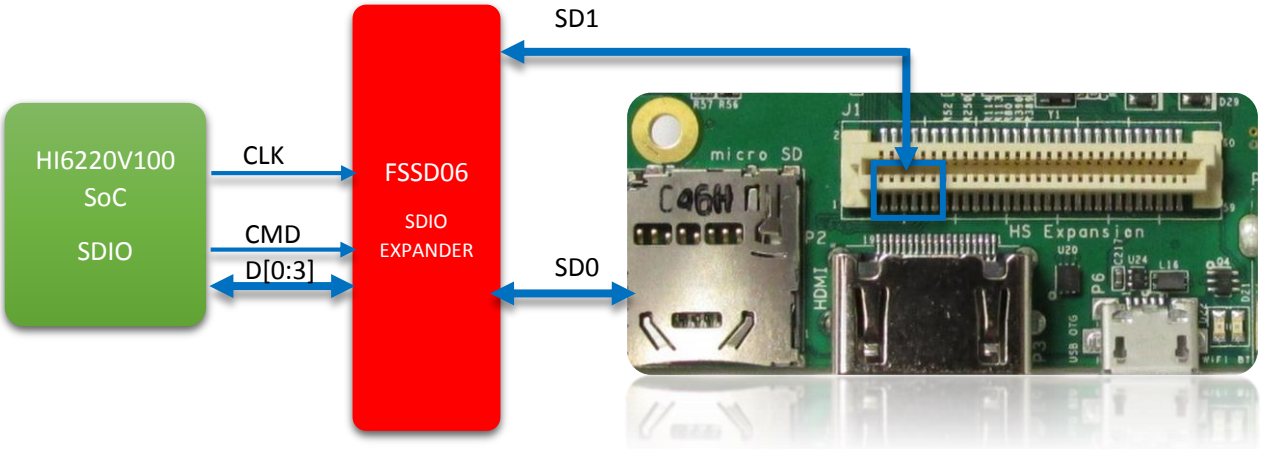

Figure 11 - SDIO Implementation on HiKey Board

8. DISPLAY INTERFACES : P3-HDMI / HS EXP

The on board HDMI is provided via the Analog Devices ADV7533 multifunction video interface chip is available on the Type A HDMI connector mounted at P3. This connector is ESD protected with TI protection diodes.

A 4 lane MIPI/DSI port is provided on the HS Expansion bus interface. Below is a block diagram of the HiKey implementation.

HiKey Display Interface

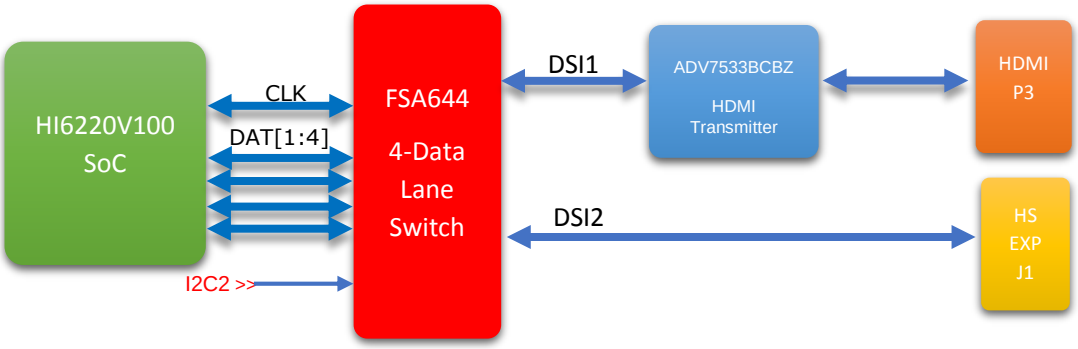

Figure 12 - Display Interface Block Diagram

9. J1 – High Speed EXP CNT

The HS Expansion connector is a board to board low profile 60 pin receptacle TE part number 5177983-2.Pin1 for this header is at the bottom left corner as shown in **Figure 13** below.

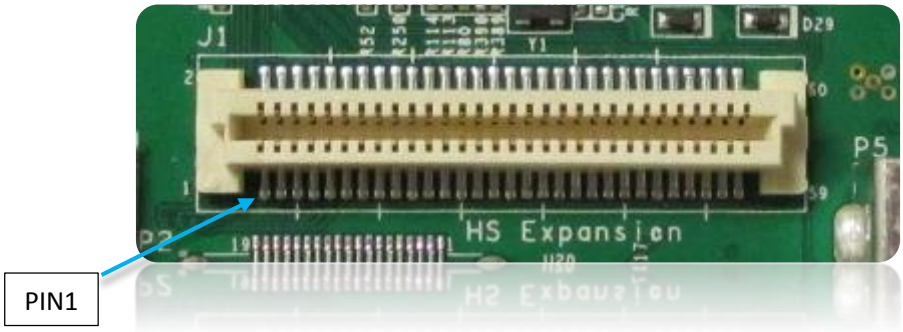

Figure 13 – HiKey HS Expansion Connector

Table 5 – High Speed Expansion SoC Signal Assignments

SD1_DATA0	1	2	CSI0_CLK_P
SD1_DATA1	3	4	CSI0_CLK_N
SD1_DATA2	5	6	DGND
SD1_DATA3	7	8	CSI0_DATA0_P
SD1_CLK	9	10	CSI0_DATA0_N
SD1_CMD	11	12	DGND
DGND	13	14	CSI0_DATA1_P
ISP_CCLK0	15	16	CSI0_DATA1_N
ISP_CCLK1	17	18	DGND
DGND	19	20	CSI0_DATA2_P
DSI2_CLK_P	21	22	CSI0_DATA2_N
DSI2_CLK_N	23	24	DGND
DGND	25	26	CSI0_DATA3_P
DSI2_DATA0_P	27	28	CSI0_DATA3_N
DSI2_DATA0_N	29	30	DGND
DGND	31	32	ISP0_SCL
DSI2_DATA1_P	33	34	ISP0_SDA
DSI2_DATA1_N	35	36	ISP1_SCL
DGND	37	38	ISP1_SDA
DSI2_DATA2_P	39	40	DGND
DSI2_DATA2_N	41	42	CSI1_DATA0_P
DGND	43	44	CSI1_DATA0_N
DSI2_DATA3_P	45	46	DGND
DSI2_DATA3_N	47	48	CSI1_DATA1_P
DGND	49	50	CSI1_DATA1_N
USBDP3	51	52	DGND
USBDM3	53	54	CSI1_CLK_P
DGND	55	56	CSI1_CLK_N
NOT USED	57	58	DGND
NOT USED	59	60	100K PU to LDO5_1V8

Expansion Board Connectors

The following are mezzanine board connectors which can be used with the HiKey receptacle:

Table 6 - Mating connector options for mezzanine board or module

PART NUMBER	MANUFACTURER	SPEED	MATED HEIGHT	TYPE
878314029	MOLEX	LS	2.5mm	TH
57202G5220LF	FCI	LS	2.5mm	SMT
TMMH12001F	SAMTEC	LS	2.0mm	TH
610830-63400LF	FCI	HS	6.7mm	SMT
5179030-2	TE	HS	6.7mm	SMT

Note that the specified connectors provided a board to board spacing of 7.0mm

10. USB INTERFACES:

There are a total of 4 USB ports on the HiKey board. Two Type-A host ports at P4 and P5, one microUSB AB 2.0 host/slave port at P6 and one USB host port available on the High Speed Expansion bus. The following block diagram shows the HiKey board implementation:

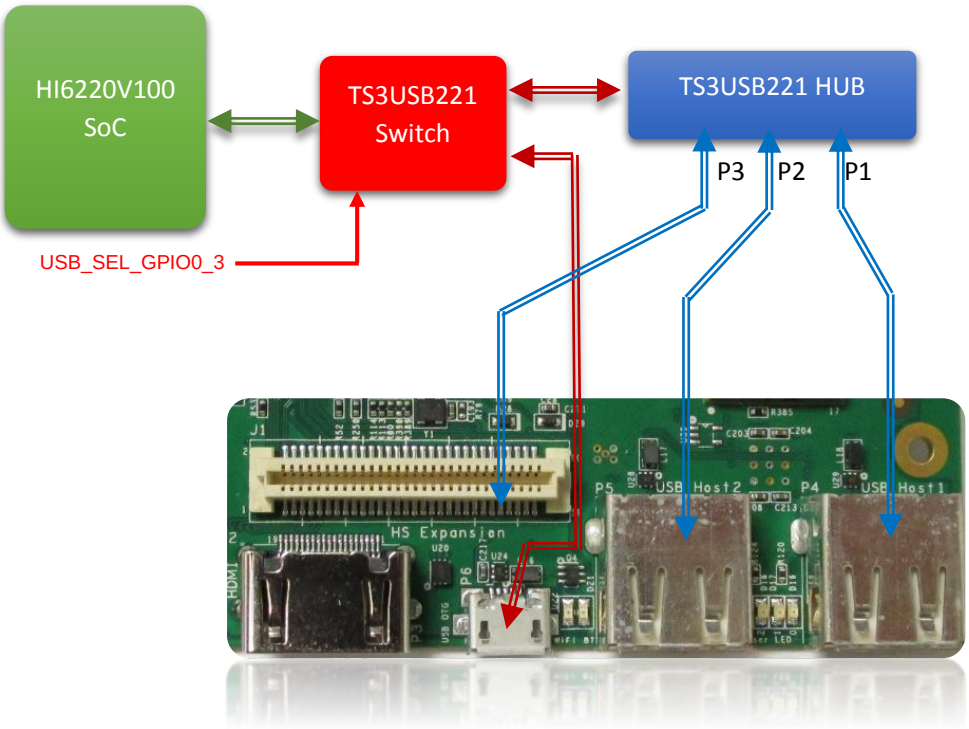

Figure 14 – USB OTG and Type A Connectors

The HiKey board utilizes a single SoC USB interface without USB protocol hardware split transfer support. The USB interfaces are therefore subject to the following restrictions:

1. The microUSB or the Type A/Mezzanine board interfaces may be used depending on the state of USB_SEL_GPIO0_3. Both interfaces may not be used at the same time.
2. The microUSB port supports a single attached device with USB slave operations or USB host high speed, full speed or low speed operations.
3. The Type A/Mezzanine board interfaces cannot support mixed speed devices. All attached devices must be of the same type – high speed, full speed or low speed. Furthermore, the HiKey board must be configured in software to support either full speed/low speed devices (default) or high speed devices on these ports.

11. System and USER LEDs

There are two status LEDs and four User LEDs on the HiKey board. The user LEDs can be programmed by the SoC directly.

D21/22 – WiFi/BT LEDs

- The WiFi activity LED is a Yellow type surface mount 0603 LED.
- The BT activity LED is a Blue Type surface mount 0603 LED.

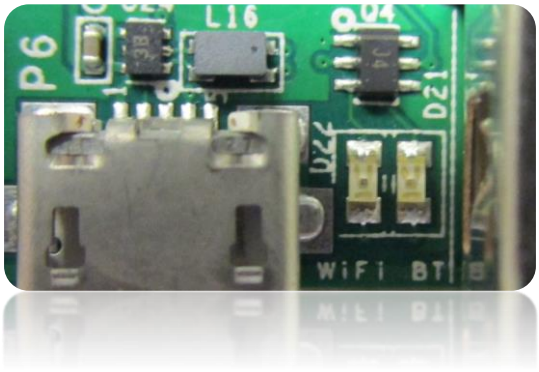

Figure 15 – WiFi and BT Activity LEDs

D16-D19 – USER LEDs

- The four user LEDs are surface mount Green Type 0603 LED.

Figure 16 – User LEDs

12. JTAG HEADER

The HiKey board includes the option for soldering a 10 pin header that brings out the SoC signals for JTAG debug. A **FTSH-105-01-F-DV** header can be populated at J10

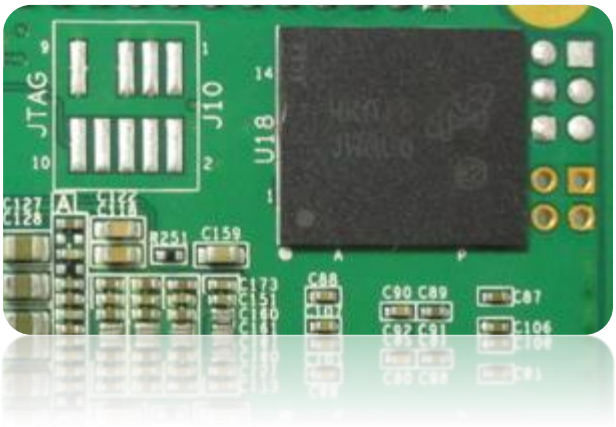

Figure 17 - Footprint for JTAG header on bottom side of HiKey PCB

III. TOP AND BOTTOM SIDE MAJOR COMPONENTS

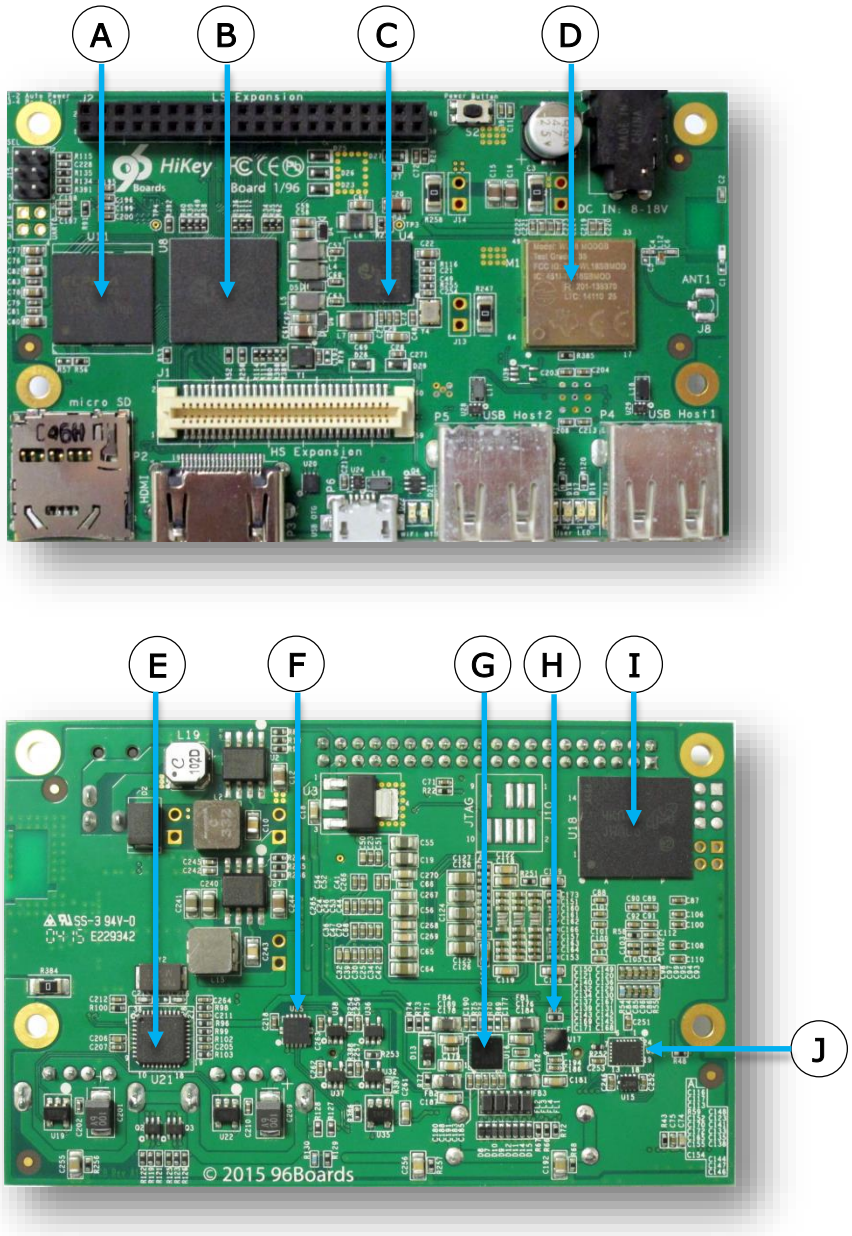

Figure 18 - Top and Bottom side components

- (A) U11 1G LPDDR3 – EDF8132A1MC-GD-F
- (B) U8 SoC – HI6220V100
- (C) U4 PMIC – HI6553V100
- (D) M1 WiLink 8 – WL1835MOD
- (E) U21 USB HUB – USB2513
- (F) U25 USB SWITCH – TS3USB221
- (G) U16 HDMI TRASMITTER – ADV7533
- (H) U17 4-Lane DSI SWITCH – FSA644
- (I) U18 4G EMMC
- (J) U30 SDIO SWITCH – FSSD06UMX