Hi6220V100 Multi-Mode Application Processor

Function Description

Issue 01

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HiSilicon Technologies CO., LIMITED.

About This Document

Purpose

This document describes the function and the basic module of the Hi6220 Soc.

Related Versions

The following table lists the product versions related to this document.

Product Name	Version
Hi6220	V100

Intended Audience

This document is intended for:

- Field application engineers
- Hardware engineers

Update History

Updates between document issues are cumulative. Therefore, the latest document issue contains all updates made in previous issues.

Updates in Issue 01 (2014-12-29)

The first version is released.

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1 Introduction

1.1 Overview

The contents of this document are organized as follows:

- Chapter 1 Introduction. This chapter describes the Hi6220 architecture, which is related to the processor, clock control, reset control, boot mechanism, and memory mapping and allocation.
- Chapter 2 System Control
- Chapter 3 Media System
- Chapter 4 Memory Control
- Chapter 5 Peripheral Interfaces
- Appendix A Interrupt Vectors
- Appendix B: Address Allocation for Registers and Memories

1.2 Architecture

1.2.1 Key Features

Overall Features

- High-pixel photographing, high-definition (HD) video recording, HD video encoding and decoding, and rich multimedia applications such as complex 3D games
- High-speed data communications
- Integrated octa-core 64-bit ARM Cortex-A53 application processor
- Integrated independent Hi-Fi2 audio processor
- ARM TrustZone security mechanism
- Integrated independent hardware encryption and decryption engine
- 533 MHz LPDDR2, 667 MHz LPDDR3, and 800 MHz LPDDR3
- Various peripheral interfaces

- TSMC 28 nm low-power (LP) process
- Ball grid array (BGA) package, 653 pins, 0.48 inch x 0.48 inch body size

Multimedia Features

- 1080p full-HD LCD display
- 1920 x 1080@60 Hz mobile industry processor interface (MIPI) display serial interface (DSI)
- A maximum of 13Mega photograph (13Mega@15 fps and 8Megapixel@30 fps)
- Digital image stabilizer, 4 x 4 digital zoom and multi-area focus
- Dual-stream photographing and preview, zero shutter lag (ZSL)
- Automatic focus (AF), automatic white balance (AWB), and automatic exposure (AE)
- Wide dynamic range (WDR), high dynamic range (HDR), human face detection, and smile recognition
- Embedded video hardware encoder, supporting 1080p@30 fps HD camera
- Embedded video hardware decoder, supporting 1080p@30 fps HD video decoding in the following formats: H.264, SVC, MPEG1/2/4, H.263, VC-1, WMV9, DivX, RV8/9/10, AVS, and VP8
- Embedded Mali450-MP4 GPU, supporting 3D graphics processing, OpenGL ES 1.1/2.0, OpenVG 1.1, 2000Mega@500 MHz, 110M triangle@500 MHz, and 32G flops@500 MHz
- WMA/MP3/AAC/EVS audio encoding and decoding
- Dolby 5.1/7.1, DTS 5.1/7.1 audio channels

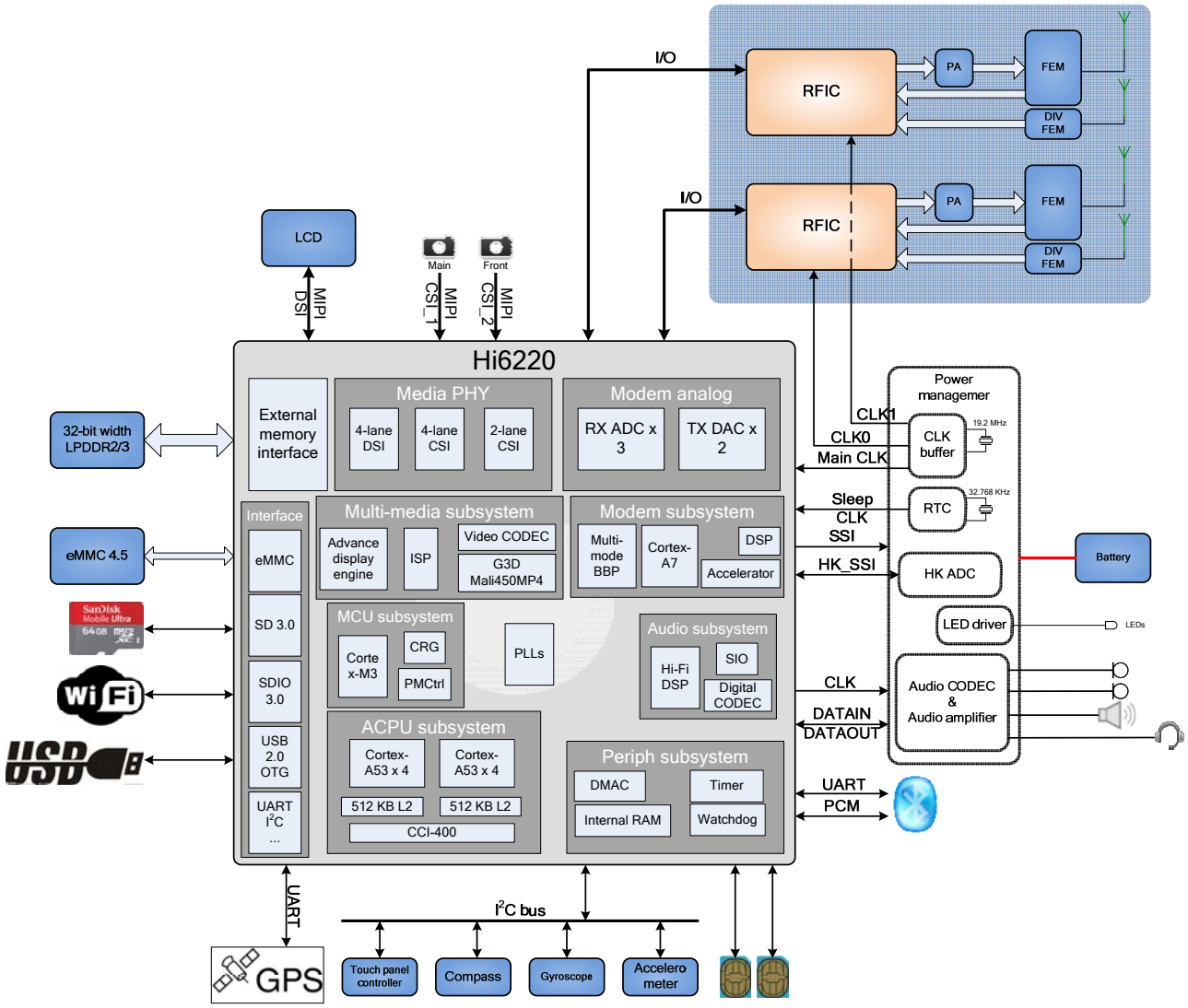
Interface Features

- Six universal asynchronous receiver transmitter (UART) interfaces, among which four are high-speed UART interfaces, connecting to the NAND flash controller (NFC), global positioning system (GPS), Bluetooth (BT), or code division multiple address (CDMA) modem devices or working as debugging interfaces
- Four inter-integrated circuit (I^2C) interfaces, connecting to devices such as the Coulomb counter, charger, camera flash, NFC, touch panel, keypad, or sensor
- One synchronous physical interface (SPI), SPI master and SPI slave
- Three serial input/output (SIO) (I2S/PCM) interfaces, connecting to the digital FM, BT, or CDMA modem devices
- Private audio CODEC interface, connecting to the audio CODEC
- One USB 2.0 on-the-go (OTG) interface
- One embedded multimedia card (eMMC) interface, one SD memory card interface, and one secure digital input/output (SDIO) interface
- Two pulse-width modulation (PWM) interfaces for backlight adjustment
- One 4-lane MIPI DSI
- One 4-lane MIPI camera serial interface (CSI), one 2-lane MIPI CSI
- LPDDR2/LPDDR3 DDR SDRAMs
- 20 general purpose input/output (GPIO) interfaces

1.2.2 Logic Block Diagram

Figure 1-1 shows the logic block diagram of the Hi6220.

Figure 1-1 Logic block diagram



The Hi6220 consists of the application system and communication system, as shown in Figure 1-1. The application system consists of the ACPU subsystem, graphics processing unit (GPU) subsystem, and media subsystem.

1.2.3 Application Scope

The Hi6220 features multicore, multimode, high performance, and high integration. It integrates various multimedia processing and high-speed communications processing functions, applying to multiple products such as smartphones and tablets.

1.3 ACPU

1.3.1 Function

The ACPU uses the ARM Cortex-A53MPCore octa-core64-bit processor which consists of two ARM Cortex-A53MP4 clusters and a CCI400 conformance controller.

- Maximum working frequency of 1.2 GHz
- Four ARM Cortex-A53 processors configured as symmetric multiprocessing (SMP) in the ARM Cortex-A53MP4 cluster
- L1 cache including the 32 KB I cache (2-way set-associative) and 32 KB D cache (4-way set-associative)
- 512 KB L2 cache of the ARM Cortex-A53MP4 cluster, 16-way set-associative
- Integrated generic interrupt controller (GIC) which supports 128 external interrupt sources
- 8-stage pipeline, AArch64 and AArch32 execution states, and ARMv8 architecture
- Management unit (MMU)
- Floating-point processing unit in the processor core, which supports operations with single- or double-precision in compliance with the IEEE754 standard, NEON instruction, and cryptography instruction
- OSs such as Linux and Android
- Connects to the CoreSight test processing unit over the advanced peripheral bus (APB) interface and supports trace and Joint Test Action Group (JTAG) debugging modes

The ARM Cortex-A53 supports the AArch32 execution state and seven operating modes, and complies with the ARMv7 architecture.

The ARM Cortex-A53 also supports the AArch64 execution state.

1.3.2 Interrupt Control

The ARM Cortex-A53 integrates a GIC for controlling interrupts. The GIC supports the following types of interrupts:

- Software generated interrupt (SGI)

  A total of 16 SGIs are supported, and SGIs are controlled by writing to registers.
- Private peripheral interrupt (PPI)

  Each A53 processor corresponds to five PPIs.
- Shared peripheral interrupt (SPI)

  A total of 128 SPIs are supported. The SPIs can interrupt any A53 processor.

The GIC supports TrustZone. Each interrupt source can be set to secure interrupt source or non-secure interrupt source.

For details about interrupt allocation, see Appendix A "Interrupt Vectors."

1.4 Clock Control

1.4.1 Function Description

The digital baseband (DBB) receives external clock inputs and ABB clock inputs, and uses internal phase-locked loops (PLLs) and clock circuits to generate various internal working clocks required by the DBB.

The DBB can work in normal, slow, doze, or sleep mode. The system clock is dynamically switched according to the DBB operating mode. When the DBB works in normal mode, clock gating is supported to dynamically reduce power consumption.

1.4.2 External Clock Inputs

Sleep Clock

The sleep clock is a 32.768 kHz clock.

Crystal Oscillator Clock

The crystal oscillator clock is a 19.2 MHz clock. After shaping and buffering the crystal oscillator clock, the ABB sends it to the DBB. A stable timeout counter is provided for the crystal oscillator clock, and a 32 kHz clock is used as a reference clock for counting.

1.4.3 Internal Clock Configuration

For details, see the clock reset description of each module.

1.5 Reset Control

1.5.1 Function Description

The Hi6220 reset module provides the following functions:

- Receives inputs from external pin reset sources and internal reset sources, and generates reset signals to control the reset of each internal module of the Hi6220.
- Outputs the reset signals to external components.
- Interacts with the power management unit (PMU) and ABB for reset.

All modules in the SoC subsystem use the asynchronous reset and synchronous deassertion modes unless otherwise specified.

1.5.2 External POR Source

The Hi6220 has only one pin input reset source signal, that is, power-on reset (POR) signal RSTIN_N.

When a power-on event is triggered, the PMU inputs the POR signal RSTIN_N to reset all circuits on the Hi6220. RSTIN_N must retain at a low level for more than 100 μs before

release to ensure that the Hi6220 is successfully reset. After dejitter, a 32 kHz clock is sent to various internal clock domains for synchronization.

1.5.3 PMU Reset Indicator Signal PMU_RST_N

During global reset, the Hi6220 outputs a reset indicator signal PMU_RST_N that is sent to the PMU for internal reset. A POR reset signal is triggered again and sent to the Hi6220. A weak pull-up resistor must connect to the PMU_RST_N signal on the board.

1.5.4 JTAG Reset

Hi6220 supports an external JTAG reset signal.

1.5.5 Internal Reset Source

Global Soft Reset

Global soft reset makes the PMU_RST_N output valid and enables the PMU to retrigger POR for the Hi6220.

Global soft reset is triggered in the following scenarios:

- The ACPU watchdog sends a global soft reset request.
- The global watchdog requires global soft reset.
- Over temperature occurs for Tsensor0.

Watchdog Reset

The watchdogs monitor the running status of the processor system. In normal cases, the system software resets the watchdog counters periodically. If watchdog counters are not reset promptly, software is running abnormally, and the watchdogs perform the following operations:

The watchdogs report an exception interrupt, load the initial value for the counters, and recount from the initial value.

If the exception interrupt is not handled (the counters are not reset), the watchdog counters decrease to 0 by step of 1 and then send a watchdog reset request.

1.6 Boot Mechanism

1.6.1 Mapping Among Pin Configurations, eFUSE Configurations, and Boot Addresses

The Hi6220 can boot from the on-chip BOOTROM (bootstrap mode), eMMC, which depends on the inputs of the BOOT_SEL and NAND_BOOT pins and eFUSE configurations.

Table 1-1 describes the mapping among pin configurations, eFUSE configurations, and boot addresses.

Table 1-1 Mapping among pin configurations, eFUSE configurations, and boot addresses

BOOT_SEL	NAND_BOOT	security_boot_flg	Boot Mode	Boot Address
0	x	x	Forcible USB bootstrap	0xFFFF_0000
1	0	x	Booted by the BOOTROM, the system starts from the eMMC.	0xFFFF_0000
1	1	x	Reserved	-

1.6.2 Booting from the eMMC (Booted by the BOOTROM)

The pin configurations are as follows:

- BOOT_SEL: 1
- NAND_BOOT: 0

The eFUSE configuration is as follows:

- security_boot_flg: 0 (non-secure boot)
- 1: secure boot

1.6.3 USB Bootstrap Booting

The USB bootstrap indicates that images are burnt and modified through the USB port without the intervention of any external storage medium.

The Hi6220 supports the USB bootstrap boot mode. This mode applies to R&D commissioning, factory production, software upgrade, or even mobile phone repair without using the external devices such as the JTAG device and chip burner.

The Hi6220 has an external boot pin that provides combined decoded code for instructing the system to boot in bootstrap mode.

The pin configurations are as follows:

The BOOT_SEL pin is set to 0.

1.7 System Debugging

The Hi6220 supports the following system debugging methods:

- The JTAG interface is provided in compliance with the IEEE1149.1 standard. The ACPU can be debugged by connecting the JTAG interface to the emulator.
- ACPU watchdog is provided
- Provides a 16-bit trace interface. The debug system provides pins that output trigger disable signals, and is compatible with various mainstream emulator interfaces such as Trace2, Trace32, and DSTREAM.

1.8 Memory Mapping and Allocation

For details, see Appendix B "Address Allocation for Registers and Memories."

2 System Control

2.1 PERI_SCTRL

2.1.1 Function Description

2.1.1.1 Overview

The PERI_SCTRL supports temperature detection and control module. Detects and controls the temperature by using the TSensor.

2.1.1.2 Temperature Detection Control

The Hi6220 provides a TSensor controller that consists of one local sensor and two remote sensors. The local sensor and remote sensors connect to the TSensor analog parts in the ACPU and G3D and are used to detect and query the working temperatures of the G3D and ACPU respectively. The TSensor controller has a system configuration interface is provided for configuring the TSensor enable status, TSensor temperature threshold, and TSensor temperature interrupt, implementing TSensor temperature correction and hysteresis, reading the temperature, and querying the temperature interrupt status.

2.1.2 Register Description

The base address for PERI_SCTRL registers is 0xF703_0000.

Table 2-1 describes PERI CTRL registers.

Table 2-1 Summary of PERI CTRL registers

Offset Address	Register	Description
0x700	SC_TEMP0_LAG	Tsensor0 temperature comparison lag range register
0x704	SC_TEMP0_TH	Tsensor0 temperature threshold register
0x708	SC_TEMP0_RST_TH	Tsensor0 reset threshold register
0x70C	SC_TEMP0_CFG	Tsensor0 parameter configuration register
0x710	SC_TEMP0_EN	Tsensor0 temperature detection module

Offset Address	Register	Description
		enable register
0x714	SC_TEMP0_INT_EN	Tsensor0 temperature detection interrupt mask register
0x718	SC_TEMP0_INT_CLR	Tsensor0 temperature detection interrupt clear register
0x71C	SC_TEMP0_RST_MSK	Tsensor0 temperature detection reset mask register
0x720	SC_TEMP0_RAW_INT	Tsensor0 temperature detection raw interrupt register
0x724	SC_TEMP0_MSK_INT	Tsensor0 temperature detection mask interrupt register
0x728	SC_TEMP0_VALUE	Detected Tsensor0 temperature register

SC_TEMP0_LAG

SC_TEMP0_LAG is a Tsensor0 temperature comparison lag range register.

Offset Address	Register Name	Total Reset Value
0x700	SC_TEMP0_LAG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												temp0_lag			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RW	reserved	Reserved
[4:0]	RW	temp0_lag	Temperature comparison lag range of Tsensor0. The mapping between the configured value for each step and the temperature is as follows: 200/255 = 0.7843°C (33.41°F). The configured value range is 0°C to 24.3°C (32°F to 75.74°F). The configured value cannot be greater than any value defined by temperature threshold configuration registers. Note: When a temperature is compared with a temperature threshold to generate interrupts, ensure that the temperature does not frequently fluctuate around the temperature threshold. Otherwise, interrupts are frequently generated, and interrupt glitch filtering is required. If the temperature is above the temperature threshold, an interrupt is generated. If the temperature is below the temperature threshold, an interrupt is generated only when the temperature continues to decrease to the value of (temperature threshold – temp0_lag).

SC_TEMP0_TH

SC_TEMP0_TH is a Tsensor0 temperature threshold register.

Offset Address	Register Name	Total Reset Value
0x704	SC_TEMP0_TH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	temp0_3th								temp0_2th								temp0_1th								temp0_0th							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	temp0_3th	Temperature threshold 3 of Tsensor0 The encoding mode is the same as that of temperature threshold 0 of Tsensor0.
[23:16]	RW	temp0_2th	Temperature threshold 2 of Tsensor0 The encoding mode is the same as that of temperature threshold 0 of Tsensor0.
[15:8]	RW	temp0_1th	Temperature threshold 1 of Tsensor0 The encoding mode is the same as that of temperature threshold 0 of Tsensor0.
[7:0]	RW	temp0_0th	Temperature threshold 0 of Tsensor0 0x00: below −60ºC (−76ºF) 0x01: −60ºC (−76ºF) to −59.21569ºC (−74.58824ºF) 0x02: −59.21569ºC (−74.58824ºF) to −58.43137ºC (−73.17647ºF) ... 0xFD: +138.43137ºC (+281.17647ºF) to +139.21569ºC (+282.58824ºF) 0xFE: +139.21569ºC (+282.58824ºF) to +140ºC (+284ºF) 0xFF: above +140ºC (+284ºF) Note: The concept of temperature range is introduced for the 8-bit binary codes. For example, when the temperature is below –60°C (–76°F), the threshold is 0x00. When the temperature ranges from –60°C (–76°F) to −59.21569ºC (−74.58824ºF), the threshold is 0x01. When the temperature ranges from +139.21569ºC (+282.58824ºF) to +140ºC (+284ºF), the threshold is 0xFE. When the temperature is above +140ºC (+284ºF), the threshold is 0xFF. The interval between consecutive thresholds is 0.7843°C (200/255) or 33.41°F.

SC_TEMP0_RST_TH

SC_TEMP0_RST_TH is a Tsensor0 reset threshold register.

Offset Address	Register Name	Total Reset Value
0x708	SC_TEMP0_RST_TH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								temp0_rst_th							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved
[7:0]	RW	temp0_rst_th	Reset threshold of Tsensor0 The encoding mode of reset threshold is the same as that of temperature threshold 0 of Tsensor0. Note: When the configured value is 0xFF, the reset signal cannot be generated. Therefore, the configured value must be less than 0xFF.

SC_TEMP0_CFG

SC_TEMP0_CFG is a Tsensor0 parameter configuration register.

Offset Address	Register Name	Total Reset Value
0x70C	SC_TEMP0_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												temp0_test_raw								reserved							temp0_ct_sel_raw	temp0_trim_raw			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RW	reserved	Reserved
[19:12]	RW	temp0_test_raw	Tsensor0 test mode, for debugging Tsensor0 000: local sensor (default) 001: remote sensor 1 (ACPU cluster 1) 010: remote sensor 2 (ACPU cluster 0) 011: remote sensor 3 (G3D) Other values: reserved
[11:6]	RW	reserved	Reserved

Offset Address	Register Name	Total Reset Value
0x70C	SC_TEMP0_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												temp0_test_raw								reserved							temp0_ct_sel_raw				temp0_trim_raw			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[5:4]	RW	temp0_ct_sel_raw	Tsensor0 HKADC conversion time 00: 0.768 ms 01: 6.144 ms 10: 49.152 ms 11: 393.216 ms
[3:0]	RW	temp0_trim_raw	Reserved

SC_TEMP0_EN

SC_TEMP0_EN is a Tsensor0 temperature detection module enable register.

Offset Address	Register Name	Total Reset Value
0x710	SC_TEMP0_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															temp0_en_raw
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RW	reserved	Reserved
[0]	RW	temp0_en_raw	Tsensor0 temperature detection module enable 0: disabled 1: enabled

SC_TEMP0_INT_EN

SC_TEMP0_INT_EN is a Tsensor0 temperature detection interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x714	SC_TEMP0_INT_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															temp0_int_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RW	reserved	Reserved
[0]	RW	temp0_int_en	Tsensor0 temperature detection interrupt mask 0: masked 1: enabled

SC_TEMP0_INT_CLR

SC_TEMP0_INT_CLR is a Tsensor0 temperature detection interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x718	SC_TEMP0_INT_CLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															temp0_int_clr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RW	reserved	Reserved
[0]	RW	temp0_int_clr	Tsensor0 temperature detection interrupt clear 0: invalid 1: cleared (including the raw interrupt and mask interrupt)

SC_TEMP0_RST_MSK

SC_TEMP0_RST_MSK is a Tsensor0 temperature detection reset mask register.

Offset Address	Register Name	Total Reset Value
0x71C	SC_TEMP0_RST_MSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															temp0_rst_msk
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RW	reserved	Reserved
[0]	RW	temp0_rst_msk	Tsensor0 temperature detection reset mask 0: masked 1: enabled

SC_TEMP0_RAW_INT

SC_TEMP0_RAW_INT is a Tsensor0 temperature detection raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x720	SC_TEMP0_RAW_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															temp0_rawint
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved

Offset Address	Register Name	Total Reset Value
0x720	SC_TEMP0_RAW_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															temp0_rawint
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RO	temp0_rawint	Tsensor0 temperature detection raw interrupt 0: invalid 1: valid

SC_TEMP0_MSK_INT

SC_TEMP0_MSK_INT is a Tsensor0 temperature detection mask interrupt register.

Offset Address	Register Name	Total Reset Value
0x724	SC_TEMP0_MSK_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															temp0_mskint
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RO	temp0_mskint	Tsensor0 temperature detection mask interrupt 0: invalid 1: valid

SC_TEMP0_VALUE

SC_TEMP0_VALUE is a detected Tsensor0 temperature register.

Offset Address	Register Name	Total Reset Value
0x728	SC_TEMP0_VALUE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								temp0_out_s							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved
[7:0]	RO	temp0_out_s	Detected Tsensor0 temperature 00000000: ≤ −60ºC (−76ºF) … 00110011: −20ºC (−4ºF) … 01100110: +20ºC (+68ºF) … 10011001: +60ºC (+140ºF) … 11001100: +100ºC (+212ºF) … 11111111: ≥ +140ºC (+284ºF) Note: The concept of temperature range is introduced for the 8-bit binary codes. The interval between consecutive temperature codes is 0.7843°C (200/255) or 33.41°F.

2.2 RTC

2.2.1 Function Description

The real-time clock (RTC) is used to display time and periodically generate alarms.

The RTC works based on a 32-bit up counter. The initial count value is loaded from RTCLR. The count value increases by 1 on the rising edge of each count clock. When the count value of RTCDR is the same as the value of RTCMR, the RTC generates an interrupt. Then the counter continues to count in incremental mode on the next rising edge of the count clock.

The count clock of the RTC is a 1 Hz clock that is used to convert the count time into a value in the format of year, month, day, hour, minute, and second.

2.2.2 Register Description

- The base address for RTC0 registers is 0xF800_3000.
- The base address for RTC1 registers is 0xF800_4000.

Table 2-2 describes RTC registers.

Table 2-2 Summary of RTC registers

Offset Address	Register	Description
0x000	RTCDR	Data register
0x004	RTCMR	Comparison register
0x008	RTCLR	Load register
0x00C	RTCCR	Control register
0x010	RTCIMSC	Interrupt mask register
0x014	RTCRIS	Raw interrupt status register
0x018	RTCMIS	Masked interrupt status register
0x01C	RTCICR	Interrupt clear register

RTCDR

RTCDR is a data register.

Offset Address	Register Name	Total Reset Value
0x000	RTCDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTCDR																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	RTCDR	Reading this register returns the current count value of the internal counter of the current RTC.

RTCMR

RTCMR is a comparison register.

Offset Address	Register Name	Total Reset Value
0x004	RTCMR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTCMR																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	RTCMR	Write: The written value is converted into the RTC timing interrupt comparison value. When the RTCDR value is the same as the comparison value, an RTC interrupt is generated. Read: The last written value is returned.

RTCLR

RTCLR is a load register.

Offset Address	Register Name	Total Reset Value
0x008	RTCLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTCLR																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	RTCLR	Write: The written value is used to set the initial count value of the RTC. Read: The last written value is returned.

RTCCR

RTCCR is a control register.

Offset Address	Register Name	Total Reset Value
0x00C	RTCCR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															RTCCR
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]		reserved	Reserved
[0]	RW	RTCCR	RTC enable 0: disabled 1: enabled

RTCIMSC

RTCIMSC is an interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x010	RTCIMSC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															RTCIMSC
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]		reserved	Reserved
[0]	RW	RTCIMSC	Interrupt mask 0: cleared 1: enabled

RTCRIS

RTCRIS is a raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x014	RTCRIS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															RTCRIS
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]		reserved	Reserved
[0]	RW	RTCRIS	Raw interrupt status 0: No interrupt is generated. 1: An interrupt is generated.

RTCMIS

RTCMIS is a masked interrupt status register.

Offset Address	Register Name	Total Reset Value
0x018	RTCMIS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															RTCMIS
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]		reserved	Reserved
[0]	RO	RTCMIS	Masked interrupt status 0: No interrupt is generated or the interrupt is masked. 1: An interrupt is generated.

RTCICR

RTCICR is an interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x01C	RTCICR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															RTCICR
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]		reserved	Reserved
[0]	RW	RTCICR	RTC interrupt clear 0: no effect 1: cleared

2.3 Timer

2.3.1 Function Description

The timer implements the timing and counting functions. It serves as the scheduling clock of the operating system and can be used by applications. The timer provides the tick clock for the operating system and wakes the system from the sleep status by using interrupts.

Hi6620 provides 9 dual-timers in the always-on area. During bus DFS, the reference clock of timers must be constant. All timers can be accessed in secure or non-secure mode, which can be configured. Each dual-timer consists of two timers with identical functions and supports the 32 kHz or 19.2 MHz TCXO clock for counting.

Table 2-3 describes the bus clock, working clock, and count cycle of each timer.

Table 2-3 Timer parameters

Module	Clock Signal	Description	Clock Option	Default Value	Software Clock Gating	Maximum Frequency (MHz)	Reset
TIMER0−8	pclk_timer0−8	Timer bus clock	clk_slow	clk_tcxo	√	19.2	preset_timer0−8_n
	clk_timer0−8	Timer working clock	clk_slow	clk_tcxo	√	19.2	preset_timer0−8_n
	clk_en_timer0−8	Timer count enable	Generated by the AO_SC, optional 32 kHz or 19.2 MHz clock	32 kHz	-	-	-

2.3.2 Register Description

The Hi6220 has 9 dual-timers, and each dual-timer has a group of registers. The 9 groups of registers have the same features except for the base addresses and offset addresses. See Table 2-4.

Table 2-4 Base addresses for dual-timer registers

Dual-Timer Register	Base Address
Dual-timer8 registers	0xF8010000
Dual-timer7 registers	0xF800F000
Dual-timer6 registers	0xF800E000
Dual-timer5 registers	0xF800D000
Dual-timer4 registers	0xF800C000
Dual-timer3 registers	0xF800B000
Dual-timer2 registers	0xF800A000
Dual-timer1 registers	0xF8009000
Dual-timer0 registers	0xF8008000

Table 2-5 describes timer registers.

NOTE

n indicates the timer ID and its value is 0 or 1. Each dual-timer has two independent timers.

Table 2-5 Summary of timer registers

Offset Address	Register	Description
0x000 + (0x20 x *n*)	TIMERN_LOAD	Initial count value register of timer *n*
0x004 + (0x20 x *n*)	TIMERN_VALUE	Current count value register of timer *n*
0x008 + (0x20 x *n*)	TIMERN_CONTROL	Timer control register
0x00C + (0x20 x *n*)	TIMERN_INTCLR	Interrupt clear register
0x010 + (0x20 x *n*)	TIMERN_RIS	Raw interrupt status register
0x014 + (0x20 x *n*)	TIMERN_MIS	Masked interrupt status register
0x018	TIMERN_BGLOAD	Initial count value register in periodic mode

TIMERN_LOAD

TIMERN_LOAD is an initial value register of timer *n*. It saves the initial value of a timer.

When a timer is in periodic mode and the count value decreases to 0, the value of TIMERN_LOAD is reloaded to the counter. When a value is written to TIMERN_LOAD, the current count value is changed to the written value on the next rising edge of the TIMCLK enabled by TIMCLKEN*n*.

The minimum valid value of TIMERN_LOAD is 1. If 0 is written to TIMERN_LOAD, a timing interrupt is generated immediately.

When a value is written to TIMERN_BGLOAD, the value of TIMERN_LOAD is overwritten, but the current value of the timer retains.

If values are written to TIMERN_BGLOAD and TIMERN_LOAD before the rising edge of TIMCLK enabled by TIMCLKENn arrives, the value of the counter is changed to the written value of TIMERN_LOAD at the next rising edge of TIMCLK. Then when the counter reaches 0, the last value written to TIMERN_BGLOAD or TIMERN_LOAD is reloaded.

After the TIMERN_BGLOAD and TIMERN_LOAD registers are written twice respectively, reading TIMERN_LOAD returns the written value of TIMERN_BGLOAD. That is, the return value is the valid value loaded when the counter decreases to 0 for the second time in periodic mode.

Offset Address	Register Name	Total Reset Value
0x000 + (0x20 x *n*)	TIMERN_LOAD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	timer0_load																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	timer0_load	Initial count value of timer *n*

TIMERN_VALUE

TIMERN_VALUE is a current count value register of timer *n*.

After a value is written to TIMERN_LOAD, TIMERN_VALUE immediately reflects the newly loaded value of the counter in the PCLK domain without waiting for the next TIMCLK clock edge enabled by TIMCLKENn.

Offset Address	Register Name	Total Reset Value
0x004 + (0x20 x *n*)	TIMERN_VALUE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	timer0_value																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	timer0_value	Current count value of timer *n* that is counting down Note: When the timer is in 16-bit mode, the upper 16 bits of the 32-bit TIMERN_VALUE register are not automatically set to 0. If the timer is switched from 32-bit mode to 16-bit mode and no data is written to TIMERN_LOAD, the upper 16 bits of TIMERN_VALUE may be non-zero.

TIMERN_CONTROL

TIMERN_CONTROL is a timer control register. It is used to control the operating mode of the timer and interrupt generation.

Offset Address	Register Name	Total Reset Value
0x008 + (0x20 x *n*)	TIMERN_CONTROL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								timeren	timermode	intenable	reserved	timerpre		timersize	oneshot
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved
[7]	RW	timeren	Timer enable 0: disabled 1: enabled
[6]	RW	timermode	Timer count mode 0: free-running mode 1: periodic mode
[5]	RW	intenable	TIMERN_RIS interrupt mask 0: masked 1: not masked
[4]	-	reserved	Reserved

Offset Address	Register Name	Total Reset Value
0x008 + (0x20 x *n*)	TIMERN_CONTROL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								timeren	timermode	intenable	reserved	timerpre		timersize	oneshot
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[3:2]	RW	timerpre	Prescaling factor configuration. 00: no prescaling. That is, the clock frequency of the timer is divided by 1. 01: level-4 prescaling. That is, the clock frequency of the timer is divided by 16. 10: level-8 prescaling. That is, the clock frequency of the timer is divided by 256. 11: undefined. If this value is used, the clock frequency of the timer is divided by 256.
[1]	RW	timersize	Counter select 0: 16-bit counter 1: 32-bit counter
[0]	RW	oneshot	Count mode 0: periodic mode or free-running mode 1: one-shot mode

TIMERN_INTCLR

TIMERN_INTCLR is an interrupt clear register. If any data is written to the register, the interrupt status of the corresponding timer is cleared.

Offset Address	Register Name	Total Reset Value
0x00C + (0x20 x *n*)	TIMERN_INTCLR	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	timer0_intclr								timern_intclr
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	-	timer0_intclr	Reserved
[0]	WO	timern_intclr	Interrupt clear Writing 1 clears an interrupt, and writing 0 has no effect.

TIMERN_RIS

TIMERN_RIS is a raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x010 + (0x20 x *n*)	TIMERN_RIS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								timernris
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[0]	RO	timernris	Raw interrupt status of the counter that is returned when the register is read 0: No raw interrupt is generated. 1: A raw interrupt is generated.

TIMERN_MIS

TIMERN_MIS is a masked interrupt status register.

Offset Address	Register Name	Total Reset Value
0x014 + (0x20 x *n*)	TIMERN_MIS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															timernmis
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved
[0]	RO	timernmis	Masked interrupt status of the counter that is returned when the register is read 0: No interrupt is generated. 1: An interrupt is generated.

TIMERN_BGLOAD

TIMERN_BGLOAD is an initial count value register in periodic mode.

In periodic mode, when the value of TIMERN_BGLOAD is updated, the value of TIMERN_LOAD is changed to that of TIMERN_BGLOAD. However, the timer counter does not restart counting. After the counter decreases to 0, the value of TIMERN_LOAD (that is, the value of TIMERN_BGLOAD) is reloaded to the counter.

TIMERN_BGLOAD provides another way for accessing TIMERN_LOAD. The difference is that after a value is written to TIMERN_BGLOAD, the timer does not immediately load the value of TIMERN_LOAD and restart counting.

Offset Address	Register Name	Total Reset Value
0x018	TIMERN_BGLOAD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	timer0bgload																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	timer0bgload	Initial count value of timer *n* Note: This register differs from TIMERN_LOAD. For details, see the description of TIMERN_LOAD.

2.4 Watchdog

2.4.1 Function Description

The watchdog is used to reset the system within a specified period (the count time can be configured) when an exception occurs in the system. When the count value reaches 0 for the first time, the 32-bit down counter in the watchdog generates an interrupt to notify the CPU and automatically reloads the initial count value and counts in decreasing mode. If the CPU does not clear the interrupt and the count value reaches 0 for the second time, the watchdog sends a system reset signal.

Hi6220 provides one watchdog for ACPU.

Table 2-6 Watchdog functions

Watchdog No.	Function	Interrupt Output To	Reset Request Output To
Watchdog0	Monitors the ACPU. The ACPU controls watchdog0, and the MCU processes reset requests or triggers the global reset.	ACPU	MCU

2.4.2 Register Description

The base address for AP Watchdog registers is 0xF800_5000.

Table 2-7 describes watchdog registers.

Table 2-7 Summary of watchdog registers

Offset Address	Register	Description
0x0000	WDG_LOAD	Initial count value register
0x0004	WDG_VALUE	Current count value register
0x0008	WDG_CONTROL	Control register
0x000C	WDG_INTCLR	Interrupt clear register
0x0010	WDG_RIS	Raw interrupt register
0x0014	WDG_MIS	Masked interrupt register
0x0C00	WDG_LOCK	Lock register

WDG_LOAD

WDG_LOAD is an initial count value register. It is used to set the initial value of the internal counter of the watchdog.

Offset Address	Register Name	Total Reset Value
0x0000	WDG_LOAD	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdg_load																															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:0]	RW	wdg_load	Initial count value of the internal watchdog down counter. Once the value is updated, the counter starts to count.

WDG_VALUE

WDG_VALUE is a current count value register. It is used to read the current count value of the internal counter of the watchdog.

Offset Address	Register Name	Total Reset Value
0x0004	WDG_VALUE	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdogvalue																															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:0]	RO	wdogvalue	Current count value of the counter that is counting down

WDG_CONTROL

WDG_CONTROL is a control register. It is used to enable or disable the watchdog and control the interrupt and reset functions.

Offset Address	Register Name	Total Reset Value
0x0008	WDG_CONTROL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														resen	inten
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	-	reserved	Reserved

Offset Address	Register Name	Total Reset Value
0x0008	WDG_CONTROL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														resen	inten
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1]	RW	resen	Output enable for the watchdog reset signal 0: disabled 1: enabled
[0]	RW	inten	Output enable for the watchdog interrupt signal 0: The counter stops counting, the current count value retains, and the watchdog is disabled. 1: Both the counter and the interrupt are enabled, and the watchdog is started. If the interrupt is disabled and then enabled, the counter loads the initial count value from WDG_LOAD and restarts counting.

WDG_INTCLR

WDG_INTCLR is an interrupt clear register. It is used to clear watchdog interrupts so that the watchdog can reload an initial value for counting. This register has only the write property. Writing any value to this register clears the watchdog interrupts. No written value is recorded in this register and no default reset value is defined.

Offset Address	Register Name	Total Reset Value
0x000C	WDG_INTCLR	-

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdg_intclr																															
Reset	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Access	Name	Description
[31:0]	WO	wdg_intclr	The watchdog interrupts are cleared if any value is written to the register. Then the watchdog reloads the initial value from WDG_LOAD and restarts counting.

WDG_RIS

WDG_RIS is a raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x0010	WDG_RIS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								wdogris
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved
[0]	RO	wdogris	Raw watchdog interrupt status. When the count value decreases to 0, this bit is set to 1. 0: No interrupt is generated. 1: An interrupt is generated.

WDG_MIS

WDG_MIS is a masked interrupt register.

Offset Address	Register Name	Total Reset Value
0x0014	WDG_MIS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								wdogmis
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved
[0]	RO	wdogmis	Masked watchdog interrupt status 0: No interrupt is generated or the interrupt is masked. 1: An interrupt is generated.

WDG_LOCK

WDG_LOCK is a lock register. It is used to control the read and write permission for watchdog registers.

Offset Address	Register Name	Total Reset Value
0x0C00	WDG_LOCK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdg_lock																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wdg_lock	Writing 0x1ACC_E551 to this register enables the write permission for all watchdog registers. Writing any value except 0x1ACC_E551 disables the write permission for all watchdog registers. Reading this register returns the lock status but not the value written to this register. 0x0000_0000: The write operation is allowed (unlocked). 0x0000_0001: The write operation is disabled (locked).

2.5 EDMAC

2.5.1 Function Description

2.5.1.1 Overview

The enhanced direct memory access controller (EDMAC) rapidly transfers data between chip modules.

Hi6220 V100 provides one EDMAC for ACPU.

2.5.1.2 DMA Request Configuration

The EDMAC provides 32 DMA request inputs. Table 2-8 describes the DMA input requests corresponding to peripherals.

Table 2-8 DMA requests for the AP EDMAC

DMA Request No.	Peripheral DMA Interface	DMA Request No.	Peripheral DMA Interface
0	SPI RX	16	Reserved
1	SPI TX	17	Reserved
2	I^2C0 RX	18	Reserved
3	I^2C0 TX	19	Reserved
4	I^2C1 RX	20	Reserved
5	I^2C1 TX	21	Reserved

DMA Request No.	Peripheral DMA Interface	DMA Request No.	Peripheral DMA Interface
6	I^2C2 RX	22	Reserved
7	I^2C2 TX	23	Reserved
8	UART1 RX	24	Reserved
9	UART1 TX	25	Reserved
10	UART2 RX	26	I^2C3 RX
11	UART2 TX	27	I^2C3 TX
12	UART3 RX	28	UART0 RX
13	UART3 TX	29	UART0 TX
14	DigACodec_Audio TX	30	UART4 RX
15	DigACodec_Audio RX	31	UART4 TX

2.5.2 Register Description

The base address for AP EDMAC registers is 0xF737_0000.

Table 2-9 describes EDMAC registers.

NOTE

- *in* indicates the number of supported CPU interrupts and its value range is 0−3.
- *cn* indicates the number of supported logcal channels and its value range is 0−15.

Table 2-9 Summary of EDMAC registers

Offset Address	Register	Description
0x0000 + 0x40 x *in*	INT_STAT	Interrupt status register of processor *X*
0x0004 + 0x40 x *in*	INT_TC1	Channel transfer completion interrupt status register of processor *X*
0x0008 + 0x40 x *in*	INT_TC2	Linked list node transfer completion interrupt status register of processor *X*
0x000C + 0x40 x *in*	INT_ERR1	Configuration error interrupt status register of processor *X*
0x0010 + 0x40 x *in*	INT_ERR2	Data transfer error interrupt status register of processor *X*
0x0014 +	INT_ERR3	Linked list read error interrupt status register of

Offset Address	Register	Description
0x40 x *in*		processor *X*
0x0018 + 0x40 x *in*	INT_TC1_MASK	Channel transfer completion interrupt mask register of processor *X*
0x001C + 0x40 x *in*	INT_TC2_MASK	Linked list node transfer completion interrupt mask register of processor *X*
0x0020 + 0x40 x *in*	INT_ERR1_MASK	Configuration error interrupt mask register of processor X
0x0024 + 0x40 x *in*	INT_ERR2_MASK	Data transfer error interrupt mask register of processor *X*
0x0028 + 0x40 x *in*	INT_ERR3_MASK	Linked list read error interrupt mask register of processor *X*
0x0600	INT_TC1_RAW	Raw channel transfer completion interrupt status register
0x0608	INT_TC2_RAW	Raw linked list node transfer completion interrupt status register
0x0610	INT_ERR1_RAW	Raw configuration error interrupt status register
0x0618	INT_ERR2_RAW	Raw data transfer error interrupt status register
0x0620	INT_ERR3_RAW	Raw linked list read error interrupt status register
0x660	SREQ	Single transfer request register
0x664	LSREQ	Last single transfer request register
0x668	BREQ	Burst transfer request register
0x66C	LBREQ	Last burst transfer request register
0x670	FREQ	Flush transfer request register
0x674	LFREQ	Last flush transfer request register
0x688	CH_PRI	Priority control register
0x690	CH_STAT	Global DMA status register
0x0698	DMA_CTRL	DMA global control register

INT_STAT

INT_STAT is an interrupt status register of processor *X*.

Offset Address	Register Name	Total Reset Value
0x0000 + 0x40 x *in* (*in* = 0−3)	INT_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																int_stat															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved
[15:0]	RO	int_stat	Status of the masked interrupts of each DMAC channel. Bits 15−0 correspond to channels 15−0. 0: No interrupt is generated. 1: An interrupt is generated. The interrupt request may be an error interrupt or a transfer completion interrupt.

INT_TC1

INT_TC1 is a channel transfer completion interrupt status register of processor *X*.

Offset Address	Register Name	Total Reset Value
0x0004 + 0x40 x *in* (*in* = 0−3)	INT_TC1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																int_tc1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved
[15:0]	RO	int_tc1	Status of the masked channel transfer completion interrupts of each DMAC channel. Bits 15−0 correspond to channels 15−0. 0: No transfer completion interrupt is generated. 1: A transfer completion interrupt is generated.

INT_TC2

INT_TC2 is a linked list node transfer completion interrupt status register of processor *X*.

Offset Address	Register Name	Total Reset Value
0x0008 + 0x40 x *in* (*in* = 0−3)	INT_TC2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																int_tc2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved
[15:0]	RO	int_tc2	Status of the masked linked list node transfer completion interrupts for each DMAC channel. Bits 15−0 correspond to channels 15−0. 0: No transfer completion interrupt is generated. 1: A transfer completion interrupt is generated.

INT_ERR1

INT_ERR1 is a configuration error interrupt status register of processor *X*.

Offset Address	Register Name	Total Reset Value
0x000C + 0x40 x *in* (*in* = 0−3)	INT_ERR1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																int_err1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved
[15:0]	RO	int_err1	Status of the masked configuration error interrupts for each DMAC channel. Bits 15−0 correspond to channels 15−0. 0: No configuration error interrupt is generated. 1: A configuration error interrupt is generated. This interrupt may be generated for the following reasons: 1. a_count is set to 0. 2. The ID of the linked channel is that of the current channel. 3. The channel connects to a channel that does not exist (this situation happens when the number of channels is less than 16). 4. When narrow transfer is supported, the burst size is set to a reserved value. 5. The configured address is not aligned with the burst size during FIX transfer. 6. flow_ctrl is set to a reserved value.

Offset Address	Register Name	Total Reset Value
0x000C + 0x40 x *in* (*in* = 0−3)	INT_ERR1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																int_err1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
			7. chain_en is set to a reserved value. 8. The configuration error interrupt is generated when the preceding issues occur during the configuration of the linked list node.

INT_ERR2

INT_ERR2 is a data transfer error interrupt status register of processor *X*.

Offset Address	Register Name	Total Reset Value
0x0010 + 0x40 x *in* (*in* = 0−3)	INT_ERR2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																int_err2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved
[15:0]	RO	int_err2	Status of the masked data transfer error interrupts of each DMAC channel. Bits 15−0 correspond to channels 15−0. 0: No interrupt is generated. 1: An interrupt is generated.

INT_ERR3

INT_ERR3 is a linked list read error interrupt status register of processor *X*.

Offset Address	Register Name	Total Reset Value
0x0014 + 0x40 x *in* (*in* = 0−3)	INT_ERR3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																int_err3															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved
[15:0]	RO	int_err3	Status of the masked linked list read error interrupts of each DMAC channel. Bits 15−0 correspond to channels 15−0. 0: No interrupt is generated. 1: An interrupt is generated.

INT_TC1_MASK

INT_TC1_MASK is a channel transfer completion interrupt mask register of processor *X*.

Offset Address	Register Name	Total Reset Value
0x0018 + 0x40 x *in* (*in* = 0−3)	INT_TC1_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																int_tc1_mask															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved
[15:0]	RW	int_tc1_mask	Mask status of the transfer completion interrupts of each DMAC channel. Bits 15−0 correspond to channels 15−0. 0: masked 1: not masked

INT_TC2_MASK

INT_TC2_MASK is a linked list node transfer completion interrupt mask register of processor *X*.

Offset Address	Register Name	Total Reset Value
0x001C + 0x40 x *in* (*in* = 0−3)	INT_TC2_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																int_tc2_mask															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved
[15:0]	RW	int_tc2_mask	Mask status of the linked list node transfer completion interrupts of each DMAC channel. Bits 15−0 correspond to channels 15−0. 0: masked 1: not masked

INT_ERR1_MASK

INT_ERR1_MASK is a configuration error interrupt mask register of processor *X*.

Offset Address	Register Name	Total Reset Value
0x0020 + 0x40 x *in* (*in* = 0−3)	INT_ERR1_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																int_err1_mask															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved
[15:0]	RW	int_err1_mask	Mask status of configuration error interrupts of each DMAC channel. Bits 15−0 correspond to channels 15−0. 0: masked 1: not masked

INT_ERR2_MASK

INT_ERR2_MASK is a data transfer error interrupt mask register of processor *X*.

Offset Address	Register Name	Total Reset Value
0x0024 + 0x40 x *in* (*in* = 0−3)	INT_ERR2_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																int_err2_mask															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved
[15:0]	RW	int_err2_mask	Mask status of data transfer error interrupts of each DMAC channel. Bits 15−0 correspond to channels 15−0. 0: masked 1: not masked

INT_ERR3_MASK

INT_ERR3_MASK is a linked list read error interrupt mask register of processor *X*.

Offset Address	Register Name	Total Reset Value
0x0028 + 0x40 x *in* (*in* = 0−3)	INT_ERR3_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																int_err3_mask															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved
[15:0]	RW	int_err3_mask	Mask status of linked list read error interrupts of each DMAC channel. Bits 15−0 correspond to channels 15−0. 0: masked 1: not masked

INT_TC1_RAW

INT_TC1_RAW is a raw channel transfer completion interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0600	INT_TC1_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																int_tc1_raw															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved
[15:0]	RWC	int_tc1_raw	Raw status of channel transfer completion interrupts of each DMAC channel. Bits 15−0 correspond to channels 15−0. When this register is read: 0: No channel transfer completion interrupt is generated. 1: A channel transfer completion interrupt is generated. When this register is written: 1: The channel transfer completion interrupt is cleared. 0: The original value is retained.

INT_TC2_RAW

INT_TC2_RAW is a raw linked list node transfer completion interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0608	INT_TC2_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																int_tc2_raw															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved
[15:0]	RWC	int_tc2_raw	Raw status of linked list node transfer completion interrupts for each DMAC channel. Bits 15−0 correspond to channels 15−0. When this register is read: 0: No linked list node transfer completion interrupt is generated. 1: A linked list node transfer completion interrupt is generated. When this register is written: 1: The linked list node transfer completion interrupt is cleared. 0: The original value is retained.

INT_ERR1_RAW

INT_ERR1_RAW is a raw configuration error interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0610	INT_ERR1_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																int_err1_raw															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved
[15:0]	RWC	int_err1_raw	Raw status of the configuration error interrupts for each channel. Bits 15−0 correspond to channels 15−0. 0: No configuration error interrupt is generated. 1: A configuration error interrupt is generated. When this register is written: 1: The configuration error interrupt is cleared. 0: The original value is retained.

INT_ERR2_RAW

INT_ERR2_RAW is a raw data transfer error interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0618	INT_ERR2_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																int_err2_raw															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved
[15:0]	RWC	int_err2_raw	Raw status of data transfer error interrupts for each channel. Bits 15−0 correspond to channels 15−0. 0: No data transfer error interrupt is generated. 1: A data transfer error interrupt is generated. When this register is written: 1: The data transfer error interrupt is cleared. 0: The original value is retained.

INT_ERR3_RAW

INT_ERR3_RAW is a raw linked list read error interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0620	INT_ERR3_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																int_err3_raw															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved
[15:0]	RWC	int_err3_raw	Raw status of linked list read error interrupts for each channel. Bits 15−0 correspond to channels 15−0. 0: No linked list read error interrupt is generated. 1: A linked list read error interrupt is generated. When this register is written: 1: The linked list read error interrupt is cleared. 0: The original value is retained.

SREQ

SREQ is a single transfer request register.

Offset Address	Register Name	Total Reset Value
0x660	SREQ	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sreq																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sreq	Whether to generate the DMA single transfer request When this register is written: 0: no effect 1: A DMA single transfer request is generated. When the transfer is complete, the corresponding bit is cleared. When this register is read: 0: The corresponding peripheral does not initiate a single transfer request. 1: The corresponding peripheral initiates a single transfer request.

LSREQ

LSREQ is a last single transfer request register.

Offset Address	Register Name	Total Reset Value
0x664	LSREQ	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lsreq																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	lsreq	Whether to generate the DMA last single transfer request When this register is written: 0: no effect 1: A DMA last single transfer request is generated. When the transfer is complete, the corresponding bit is cleared. When this register is read: 0: The corresponding peripheral does not initiate a last single transfer request. 1: The corresponding peripheral initiates a last single transfer request.

BREQ

BREQ is a burst transfer request register.

Offset Address	Register Name	Total Reset Value
0x668	BREQ	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	breq																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	breq	Whether to generate the DMA burst transfer request When this register is written: 0: no effect 1: A DMA burst transfer request is generated. When the transfer is complete, the corresponding bit is cleared. When this register is read: 0: The corresponding peripheral does not initiate a burst transfer request. 1: The corresponding peripheral initiates a burst transfer request.

LBREQ

LBREQ is a last burst transfer request register.

Offset Address	Register Name	Total Reset Value
0x66C	LBREQ	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lbreq																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	lbreq	Whether to generate the DMA last burst transfer request When this register is written: 0: no effect 1: A DMA last burst transfer request is generated. When the transfer is complete, the corresponding bit is cleared. When this register is read: 0: The corresponding peripheral does not initiate a last burst transfer request. 1: The corresponding peripheral initiates a last burst transfer request.

FREQ

FREQ is a flush transfer request register.

Offset Address	Register Name	Total Reset Value
0x670	FREQ	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	freq																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	freq	Whether to generate the DMA flush transfer request When this register is written: 0: no effect 1: A DMA flush transfer request is generated. When the transfer is complete, the corresponding bit is cleared. When this register is read: 0: The corresponding peripheral does not initiate a flush transfer request.

			1: The corresponding peripheral initiates a flush transfer request.

LFREQ

LFREQ is a last flush transfer request register.

Offset Address	Register Name	Total Reset Value
0x674	LFREQ	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lfreq																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	lfreq	Whether to generate the DMA last flush transfer request When this register is written: 0: no effect 1: A DMA last flush transfer request is generated. When the transfer is complete, the corresponding bit is cleared. When this register is read: 0: The corresponding peripheral does not initiate a last flush transfer request. 1: The corresponding peripheral initiates a last flush transfer request.

CH_PRI

CH_PRI is a priority control register.

Offset Address	Register Name	Total Reset Value
0x688	CH_PRI	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ch15_pri		ch14_pri		ch13_pri		ch12_pri		ch11_pri		ch10_pri		ch9_pri		ch8_pri		ch7_pri		ch6_pri		ch5_pri		ch4_pri		ch3_pri		ch2_pri		ch1_pri		ch0_pri	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RW	ch15_pri	Priority of channel 15 2'b00: priority 0 (highest) 2'b01: priority 1 2'b10: priority 2 2'b11: priority 3 (lowest)
[29:28]	RW	ch14_pri	Priority of channel 14 2'b00: priority 0 (highest) 2'b01: priority 1 2'b10: priority 2 2'b11: priority 3 (lowest)
[27:26]	RW	ch13_pri	Priority of channel 13 2'b00: priority 0 (highest) 2'b01: priority 1 2'b10: priority 2 2'b11: priority 3 (lowest)
[25:24]	RW	ch12_pri	Priority of channel 12 2'b00: priority 0 (highest) 2'b01: priority 1 2'b10: priority 2 2'b11: priority 3 (lowest)
[23:22]	RW	ch11_pri	Priority of channel 11 2'b00: priority 0 (highest) 2'b01: priority 1 2'b10: priority 2 2'b11: priority 3 (lowest)
[21:20]	RW	ch10_pri	Priority of channel 10 2'b00: priority 0 (highest) 2'b01: priority 1 2'b10: priority 2 2'b11: priority 3 (lowest)

Offset Address	Register Name	Total Reset Value
0x688	CH_PRI	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ch15_pri		ch14_pri		ch13_pri		ch12_pri		ch11_pri		ch10_pri		ch9_pri		ch8_pri		ch7_pri		ch6_pri		ch5_pri		ch4_pri		ch3_pri		ch2_pri		ch1_pri		ch0_pri	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[19:18]	RW	ch9_pri	Priority of channel 9 2'b00: priority 0 (highest) 2'b01: priority 1 2'b10: priority 2 2'b11: priority 3 (lowest)
[17:16]	RW	ch8_pri	Priority of channel 8 2'b00: priority 0 (highest) 2'b01: priority 1 2'b10: priority 2 2'b11: priority 3 (lowest)
[15:14]	RW	ch7_pri	Priority of channel 7 2'b00: priority 0 (highest) 2'b01: priority 1 2'b10: priority 2 2'b11: priority 3 (lowest)
[13:12]	RW	ch6_pri	Priority of channel 6 2'b00: priority 0 (highest) 2'b01: priority 1 2'b10: priority 2 2'b11: priority 3 (lowest)
[11:10]	RW	ch5_pri	Priority of channel 5 2'b00: priority 0 (highest) 2'b01: priority 1 2'b10: priority 2 2'b11: priority 3 (lowest)
[9:8]	RW	ch4_pri	Priority of channel 4 2'b00: priority 0 (highest) 2'b01: priority 1 2'b10: priority 2 2'b11: priority 3 (lowest)

Offset Address	Register Name	Total Reset Value
0x688	CH_PRI	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ch15_pri		ch14_pri		ch13_pri		ch12_pri		ch11_pri		ch10_pri		ch9_pri		ch8_pri		ch7_pri		ch6_pri		ch5_pri		ch4_pri		ch3_pri		ch2_pri		ch1_pri		ch0_pri	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	RW	ch3_pri	Priority of channel 3 2'b00: priority 0 (highest) 2'b01: priority 1 2'b10: priority 2 2'b11: priority 3 (lowest)
[5:4]	RW	ch2_pri	Priority of channel 2 2'b00: priority 0 (highest) 2'b01: priority 1 2'b10: priority 2 2'b11: priority 3 (lowest)
[3:2]	RW	ch1_pri	Priority of channel 1 2'b00: priority 0 (highest) 2'b01: priority 1 2'b10: priority 2 2'b11: priority 3 (lowest)
[1:0]	RW	ch0_pri	Priority of channel 0 2'b00: priority 0 (highest) 2'b01: priority 1 2'b10: priority 2 2'b11: priority 3 (lowest)

CH_STAT

CH_STAT is a global DMA status register.

Offset Address	Register Name	Total Reset Value
0x690	CH_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ch_stat															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved
[15:0]	RO	ch_stat	DMAC channel enable 1: The corresponding DMAC channel is working. 0: The corresponding DMAC channel is not working.

DMA_CTRL

DMA_CTRL is a DMA global control register.

Offset Address	Register Name	Total Reset Value
0x0698	DMA_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											conf_out4	reserved		halt_req	halt_ack
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	-	reserved	Reserved
[4]	RW	conf_out4	When the macro definition of the outstanding number is 8: 1: The outstanding number is 4. 0: The outstanding number is 8. When the macro definition of the outstanding number is 4, this bit cannot be written, and the read value is 0. Note: Modification on the outstanding is valid only when all the channels are idle and the corresponding CH_STAT register is set to all 0s. Otherwise, the modification is invalid.
[3:2]	-	reserved	Reserved

Offset Address	Register Name	Total Reset Value
0x0698	DMA_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											conf_out4	reserved		halt_req	halt_ack
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1]	RW	halt_req	DMA halt request configuration register When this bit is read: 1: The DMA has received the halt request but has not entered the halt status. 0: The DMA has not received the halt request or the DMA has entered the halt status. When this bit is written: 1: A DMA halt request is initiated. 0: no effect. The original value is retained.
[0]	RWC	halt_ack	Whether the DMA has entered the halt status When this bit is read: 1: The DMA has entered the halt status. 0: The DMA has not entered the halt status. When this bit is written: 1: The DMA halt status is disabled. 0: no effect. The original value is retained.

3 Media Subsystem

3.1 Overview

The media subsystem provides the following superior functions:

- Captures videos and images.
- Encodes and decodes videos and images.
- Accelerates image 3D processing.
- Supports video post-processing such as scaling, image combination, and image rotation.
- Controls display over various interfaces such as the mobile industry processor interface (MIPI) and parallel port.

The media subsystem consists of:

- Graphics processing unit (GPU) subsystem

  It generates G3D graphics data, combines image data, and implements special effect processing for image data.
- Image signal processor (ISP) subsystem

  It captures images and supports two MIPIs.
- Advanced display engine (ADE) subsystem

  It combines image data, displays images, and supports the screens with the MIPI and parallel port. For details, see section 3.3 "ADE" and section 3.4 "MIPI DSI."
- Video subsystem

  It encodes and decodes videos and images.

3.2 Audio CODEC

3.2.1 Overview

The audio CODEC supports switching of various audio scenarios including the call, MP3 playback, Bluetooth (BT), voice, digital FM, and hybrid scenarios. It has embedded digital-to-analog converter (DAC)/analog-to-digital converter (ADC) digital filter channels and multiple audio peripheral interfaces such as the serial interface, I^2S interface, and DMIC.

3.2.2 Features

The audio CODEC has the following features:

- Flexible configurations for meeting requirements of various application scenarios
- Sampling rate of 8 kHz, 16 kHz, or 48 kHz for the DAC
- Sampling rate of 8 kHz, 16 kHz, or 48 kHz for the ADC
- 16-bit stereo DAC and ADC (data width of 16 bits, 18 bits, 20 bits, or 24 bits)
- Two DAC channels: stereo audio-left and audio-right channels
- Two ADC channels: stereo audio-left and audio-right channels

3.3 ADE

3.3.1 Function Description

As a display channel of the Balong V800R100 chip, the ADE overlays graphics layers, supports display post-processing, and controls display timings. The ADE supports the RGB parallel interface that can connect to display interface IPs such as the MIPI DSI and HDMI.

3.3.2 Register Description

The base address for ADE registers is 0xF410_0000.

Table 3-1 describes ADE registers.

Table 3-1 Summary of ADE registers

Offset Address	Offset Address	Register
0x0000	ADE_VERSION	ADE version register
0x0004	ADE_CTRL	ADE global control register 0
0x0018	ADE_DISP_SRC_CFG	Online display channel data source selection register
0x0040	ADE_CTRAN5_TRANS_CFG	CTRAN5 lower-level channel data transfer enable register
0x0070	ADE_SOFT_RST0	Submodule soft reset register 0
0x0074	ADE_SOFT_RST1	Submodule soft reset register 1
0x0078	ADE_SOFT_RST_SEL0	Submodule soft reset source selection register 0
0x007C	ADE_SOFT_RST_SEL1	Submodule soft reset source selection register 1
0x009C	ADE_AUTO_CLK_GT_EN0	ADE submodule automatic clock gating control register 0
0x00A0	ADE_AUTO_CLK_GT_EN1	ADE submodule automatic clock gating

Offset Address	Offset Address	Register
		control register 1
0x00AC	ADE_RELOAD_DIS0	Submodule hardware sync mask register 0
0x00B0	ADE_RELOAD_DIS1	Submodule hardware sync mask register 1
0x0100	ADE_EN	ADE global enable register
0x0C00	INTR_INIT_STATE_CPU_0	CPU raw interrupt status register 0
0x0C04	INTR_INIT_STATE_CPU_1	CPU raw interrupt status register 1
0x0C08	INTR_MASK_STATE_CPU_0	CPU masked interrupt status register 0
0x0C0C	INTR_MASK_STATE_CPU_1	CPU masked interrupt status register 1
0x1400	RD_CH_DISP_PE	RD_CH_DISP performance control register
0x1404	RD_CH_DISP_CTRL	RD_CH_DISP channel control register
0x1408	RD_CH_DISP_ADDR	RD_CH_DISP data block start address register
0x140C	RD_CH_DISP_SIZE	RD_CH_DISP data block size register
0x1410	RD_CH_DISP_STRIDE	RD_CH_DISP data block stride register
0x1414	RD_CH_DISP_SPACE	RD_CH_DISP data block space size register
0x1420	RD_CH_DISP_BLANK_OFFSET	RD_CH_DISP blank data block offset register
0x1424	RD_CH_DISP_BLANK_SIZE	RD_CH_DISP blank data block size register.
0x1428	RD_CH_DISP_BLANK_SPACE	RD_CH_DISP blank data block space size register
0x142C	RD_CH_DISP_EN	RD_CH_DISP enable register
0x1430	RD_CH_DISP_STATUS	RD_CH_DISP working status register
0x5404	ADE_CTRAN5_DIS	CTRAN5 CSC bypass register
0x5408	ADE_CTRAN5_MODE_CHOOSE	CTRAN5 mode control register
0x540C	ADE_CTRAN5_STAT	CTRAN5 status register
0x5410	ADE_CTRAN5_CHDC0	CTRAN5 transform constant register 0
0x5414	ADE_CTRAN5_CHDC1	CTRAN5 transform constant register 1
0x5418	ADE_CTRAN5_CHDC2	CTRAN5 transform constant register 2
0x541C	ADE_CTRAN5_CHDC3	CTRAN5 transform constant register 3

Offset Address	Offset Address	Register
0x5420	ADE_CTRAN5_CHDC4	CTRAN5 transform constant register 4
0x5424	ADE_CTRAN5_CHDC5	CTRAN5 transform constant register 5
0x5428	ADE_CTRAN5_CSC0	CTRAN5 transform coefficient register 0
0x542C	ADE_CTRAN5_CSC1	CTRAN5 transform coefficient register 1
0x5430	ADE_CTRAN5_CSC2	CTRAN5 transform coefficient register 2
0x5434	ADE_CTRAN5_CSC3	CTRAN5 transform coefficient register 3
0x5438	ADE_CTRAN5_CSC4	CTRAN5 transform coefficient register 4
0x543C	ADE_CTRAN5_IMAGE_SIZE	CTRAN5 image size register
0x5440	ADE_CTRAN5_CFG_OK	CTRAN5 configuration completion indicator register
0x5504	ADE_CTRAN6_DIS	CTRAN6 CSC bypass register
0x5508	ADE_CTRAN6_MODE_CHOOSE	CTRAN6 mode control register
0x550C	ADE_CTRAN6_STAT	CTRAN6 status register
0x5510	ADE_CTRAN6_CHDC0	CTRAN6 transform constant register 0
0x5514	ADE_CTRAN6_CHDC1	CTRAN6 transform constant register 1
0x5518	ADE_CTRAN6_CHDC2	CTRAN6 transform constant register 2
0x551C	ADE_CTRAN6_CHDC3	CTRAN6 transform constant register 3
0x5520	ADE_CTRAN6_CHDC4	CTRAN6 transform constant register 4
0x5524	ADE_CTRAN6_CHDC5	CTRAN6 transform constant register 5
0x5528	ADE_CTRAN6_CSC0	CTRAN6 transform coefficient register 0
0x552C	ADE_CTRAN6_CSC1	CTRAN6 transform coefficient register 1
0x5530	ADE_CTRAN6_CSC2	CTRAN6 transform coefficient register 2
0x5534	ADE_CTRAN6_CSC3	CTRAN6 transform coefficient register 3
0x5538	ADE_CTRAN6_CSC4	CTRAN6 transform coefficient register 4
0x553C	ADE_CTRAN6_IMAGE_SIZE	CTRAN6 image size register
0x5540	ADE_CTRAN6_CFG_OK	CTRAN6 configuration completion indicator register
0x7400	LDI_HRZ_CTRL0	LDI horizontal scanning control register 0
0x7404	LDI_HRZ_CTRL1	LDI horizontal scanning control register 1
0x7408	LDI_VRT_CTRL0	LDI vertical scanning control register 0

Offset Address	Offset Address	Register
0x740C	LDI_VRT_CTRL1	LDI vertical scanning control register 1
0x7410	LDI_PLR_CTRL	LDI signal polarity control register
0x7414	LDI_DSP_SIZE	LDI display size register
0x7418	LDI_3D_CTRL	LDI 3D display control register
0x741C	LDI_INT_EN	LDI interrupt mask register
0x7420	LDI_CTRL	LDI control register
0x7424	LDI_ORG_INT	LDI raw interrupt status register
0x7428	LDI_MSK_INT	LDI masked interrupt status register
0x742C	LDI_INT_CLR	LDI interrupt clear register
0x7430	LDI_WORK_MODE	LDI writeback control register
0x7434	LDI_HDMI_DSI_GT	HDMI/DSI pixel clock gating register
0x7438	LDI_DE_SPACE_LOW	DE signal validity control register for the 3D frame by frame format at the active space stage
0x743C	DSI_CMD_MOD_CTRL	DSI command (CMD) mode control register
0x7440	DSI_TE_CTRL	TE control register in DSI CMD mode
0x7444	DSI_TE_HS_NUM	DSI response line configuration register
0x7448	DSI_TE_HS_WD	Hsync detection width control register in DSI TE pin mode
0x744C	DSI_TE_VS_WD	Vsync detection width control register in DSI TE pin mode
0x7450	LDI_MCU_INTS	MCU interrupt status register
0x7454	LDI_MCU_INTE	MCU interrupt mask register
0x7458	LDI_MCU_INTC	MCU interrupt clear register

Table 3-2 describes the value range and meaning of the variables in the offset addresses for ADE registers.

Table 3-2 Variables in the offset addresses for ADE registers

Variable	Value Range	Description
m	0−64	Number of horizontal filtering phases
n	0−2	Number of horizontal filtering taps/2 (rounding)

Variable	Value Range	Description
i	0–64	Number of vertical filtering phases
j	0–2	Number of vertical filtering taps/2 (rounding)
k	0–39	Number of gamma coefficient registers

ADE_VERSION

ADE_VERSION is an ADE version register.

Offset Address	Register Name	Total Reset Value
0x0000	ADE_VERSION	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	version																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	version	ADE version

ADE_CTRL

ADE_CTRL is ADE global control register 0.

Offset Address	Register Name	Total Reset Value
0x0004	ADE_CTRL	0x4005_000D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dfs_buf_unflow_lev2												dfs_buf_unflow_lev1												rd_ch6_nv	rd_ch5_nv	rot_buf_cfg		dfs_buf_cfg		frm_end_start	
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1

Bits	Access	Name	Description
[31:21]	RW	dfs_buf_unflow_lev2	Increment of the DFS buffer underflow warning threshold. The default value is 512. The underflow warning threshold plus the increment cannot be greater than the size of the allocated DFS buffer. When the filling depth of the DFS buffer is less than the threshold plus the increment, the RDMA QoS needs to be adjusted.

Offset Address	Register Name	Total Reset Value
0x0004	ADE_CTRL	0x4005_000D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dfs_buf_unflow_lev2												dfs_buf_unflow_lev1												rd_ch6_nv	rd_ch5_nv	rot_buf_cfg			dfs_buf_cfg		frm_end_start
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1

Bits	Access	Name	Description
[20:8]	RW	dfs_buf_unflow_lev1	DFS buffer underflow warning threshold. The default value is 1280. The maximum value cannot be greater than the size of the DFS buffer. When the filling depth of the DFS buffer is less than the threshold, an underflow interrupt is reported, and the RDMA QoS is adjusted.
[7]	RW	rd_ch6_nv	Reserved
[6]	RW	rd_ch5_nv	Reserved
[5:3]	RW	rot_buf_cfg	ROT buffer allocation control for channels. The attribute of this field is static, that is, this field cannot be dynamically configured when the ADE is working. 0: channel 1 = N/A; channel 5 = N/A; channel 6 = 16 KB; ROT buffer size = 153.6 KB 1: channel 1 = 16 KB; channel 5 = N/A; channel 6 = 153.6 KB; ROT buffer size = N/A 2: channel 1 = N/A; channel 5 = 153.6 KB; channel 6 =16 KB; ROT buffer size = N/A 3: channel 1 = 16 KB; channel 5 = 76.8 KB; channel 6 =76.8 KB; ROT buffer size = N/A 4: channel 1 = 16 KB; channel 5 = N/A; channel 6 = 76.8 KB; ROT buffer size = 76.8 KB 5: reserved Note: • The ROT must be disabled when no buffer is allocated to the ROT. • The buffer size is the total size of ping-pong buffers. The configured RDMA image block size cannot be greater than the size of a ping buffer.

Offset Address	Register Name	Total Reset Value
0x0004	ADE_CTRL	0x4005_000D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dfs_buf_unflow_lev2												dfs_buf_unflow_lev1												rd_ch6_nv	rd_ch5_nv	rot_buf_cfg			dfs_buf_cfg	frm_end_start	
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1

Bits	Access	Name	Description
[2]	RW	dfs_buf_cfg	DFS buffer allocation control. The attribute of this field is static, that is, this field cannot be dynamically configured when the ADE is working. 0: The DFS buffer depth is 6400, and SCL2 does not support vertical scaling. 1: The DFS buffer depth is 3840, and SCL2 supports vertical scaling. Note: The underflow threshold of the DFS buffer cannot be greater than the allocated buffer depth.
[1:0]	RW	frm_end_start	ADE frame start time, that is, time of refreshing the ADE resource allocation and channel configuration registers 0: Each frame starts when the Vsync signal is received. 1: The first frame starts after the ADE_EN register is configured, and subsequent frames start after frames end (recommended). 2: Frames start immediately after the ADE_EN register is configured. 3: The first frame starts when the Vsync signal is received, and subsequent frames start after frames end.

ADE_DISP_SRC_CFG

ADE_DISP_SRC_CFG is an online display channel data source selection register.

Offset Address	Register Name	Total Reset Value
0x0018	ADE_DISP_SRC_CFG	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														disp_src_cfg	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2:0]	RW	disp_src_cfg	Data source select for the online display channel. The attribute of this field is static, that is, this field cannot be dynamically configured when the ADE is working. 0: disconnected 1: OVLY2 2: readback channel (DISP_RDMA) that is automatically refreshed 3: ROT after OVLY 4: SCL2 after OVLY 5−7: disconnected

ADE_CTRAN5_TRANS_CFG

ADE_CTRAN5_TRANS_CFG is a CTRAN5 lower-level channel data transfer enable register.

Offset Address	Register Name	Total Reset Value
0x0040	ADE_CTRAN5_TRANS_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															ctran5_ovly_trans_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	ctran5_ovly_trans_en	Data transfer enable from CTRAN5 to OVLY1/OVLY2. The attribute of this field is static, that is, this field cannot be dynamically configured when the ADE is working. 0: disabled 1: enabled

ADE_SOFT_RST0

ADE_SOFT_RST0 is submodule soft reset register 0.

Offset Address	Register Name	Total Reset Value
0x0070	ADE_SOFT_RST0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	rot_srst	ctran6_srst	ctran5_srst	ctran4_srst	ctran3_srst	ctran2_srst	ctran1_srst	scl3_srst	scl2_srst	scl1_srst	clip6_srst	clip5_srst	clip4_srst	clip3_srst	clip2_srst	clip1_srst	cmdq_wdma_srst	reserved	ch3_wdma_srst	ch2_wdma_srst	ch1_wdma_srst	reserved	cmdq2_rdma_srst	cmdq1_rdma_srst	disp_rdma_srst	ch6_rdma_srst	ch5_rdma_srst	ch4_rdma_srst	ch3_rdma_srst	ch2_rdma_srst	ch1_rdma_srst
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30]	WC	rot_srst	Submodule soft reset. Writing 0 has no effect, and writing 1 generates a soft reset signal. This bit is automatically cleared.

Offset Address	Register Name	Total Reset Value
0x0070	ADE_SOFT_RST0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	rot_srst	ctran6_srst	ctran5_srst	ctran4_srst	ctran3_srst	ctran2_srst	ctran1_srst	scl3_srst	scl2_srst	scl1_srst	clip6_srst	clip5_srst	clip4_srst	clip3_srst	clip2_srst	clip1_srst	cmdq_wdma_srst	reserved	ch3_wdma_srst	ch2_wdma_srst	ch1_wdma_srst	reserved	cmdq2_rdma_srst	cmdq1_rdma_srst	disp_rdma_srst	ch6_rdma_srst	ch5_rdma_srst	ch4_rdma_srst	ch3_rdma_srst	ch2_rdma_srst	ch1_rdma_srst
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[29]	WC	ctran6_srst	Submodule soft reset. Writing 0 has no effect, and writing 1 generates a soft reset signal. This bit is automatically cleared.
[28]	WC	ctran5_srst	Submodule soft reset. Writing 0 has no effect, and writing 1 generates a soft reset signal. This bit is automatically cleared.
[27]	WC	ctran4_srst	Submodule soft reset. Writing 0 has no effect, and writing 1 generates a soft reset signal. This bit is automatically cleared.
[26]	WC	ctran3_srst	Submodule soft reset. Writing 0 has no effect, and writing 1 generates a soft reset signal. This bit is automatically cleared.
[25]	WC	ctran2_srst	Submodule soft reset. Writing 0 has no effect, and writing 1 generates a soft reset signal. This bit is automatically cleared.
[24]	WC	ctran1_srst	Submodule soft reset. Writing 0 has no effect, and writing 1 generates a soft reset signal. This bit is automatically cleared.
[23]	WC	scl3_srst	Submodule soft reset. Writing 0 has no effect, and writing 1 generates a soft reset signal. This bit is automatically cleared.
[22]	WC	scl2_srst	Submodule soft reset. Writing 0 has no effect, and writing 1 generates a soft reset signal. This bit is automatically cleared.
[21]	WC	scl1_srst	Submodule soft reset. Writing 0 has no effect, and writing 1 generates a soft reset signal. This bit is automatically cleared.
[20]	WC	clip6_srst	Submodule soft reset. Writing 0 has no effect, and writing 1 generates a soft reset signal. This bit is automatically cleared.
[19]	WC	clip5_srst	Submodule soft reset. Writing 0 has no effect, and writing 1 generates a soft reset signal. This bit is automatically cleared.
[18]	WC	clip4_srst	Submodule soft reset. Writing 0 has no effect, and writing 1 generates a soft reset signal. This bit is automatically cleared.
[17]	WC	clip3_srst	Submodule soft reset. Writing 0 has no effect, and writing 1 generates a soft reset signal. This bit is automatically cleared.
[16]	WC	clip2_srst	Submodule soft reset. Writing 0 has no effect, and writing 1 generates a soft reset signal. This bit is automatically cleared.

Offset Address	Register Name	Total Reset Value
0x0070	ADE_SOFT_RST0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	rot_srst	ctran6_srst	ctran5_srst	ctran4_srst	ctran3_srst	ctran2_srst	ctran1_srst	scl3_srst	scl2_srst	scl1_srst	clip6_srst	clip5_srst	clip4_srst	clip3_srst	clip2_srst	clip1_srst	cmdq_wdma_srst	reserved	ch3_wdma_srst	ch2_wdma_srst	ch1_wdma_srst	reserved	cmdq2_rdma_srst	cmdq1_rdma_srst	disp_rdma_srst	ch6_rdma_srst	ch5_rdma_srst	ch4_rdma_srst	ch3_rdma_srst	ch2_rdma_srst	ch1_rdma_srst
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15]	WC	clip1_srst	Submodule soft reset. Writing 0 has no effect, and writing 1 generates a soft reset signal. This bit is automatically cleared.
[14]	WC	cmdq_wdma_srst	Submodule soft reset. Writing 0 has no effect, and writing 1 generates a soft reset signal. This bit is automatically cleared.
[13]	RO	reserved	Reserved
[12]	WC	ch3_wdma_srst	Submodule soft reset. Writing 0 has no effect, and writing 1 generates a soft reset signal. This bit is automatically cleared.
[11]	WC	ch2_wdma_srst	Submodule soft reset. Writing 0 has no effect, and writing 1 generates a soft reset signal. This bit is automatically cleared.
[10]	WC	ch1_wdma_srst	Submodule soft reset. Writing 0 has no effect, and writing 1 generates a soft reset signal. This bit is automatically cleared.
[9]	RO	reserved	Reserved
[8]	WC	cmdq2_rdma_srst	Submodule soft reset. Writing 0 has no effect, and writing 1 generates a soft reset signal. This bit is automatically cleared.
[7]	WC	cmdq1_rdma_srst	Submodule soft reset. Writing 0 has no effect, and writing 1 generates a soft reset signal. This bit is automatically cleared.
[6]	WC	disp_rdma_srst	Submodule soft reset. Writing 0 has no effect, and writing 1 generates a soft reset signal. This bit is automatically cleared.
[5]	WC	ch6_rdma_srst	Submodule soft reset. Writing 0 has no effect, and writing 1 generates a soft reset signal. This bit is automatically cleared.
[4]	WC	ch5_rdma_srst	Submodule soft reset. Writing 0 has no effect, and writing 1 generates a soft reset signal. This bit is automatically cleared.
[3]	WC	ch4_rdma_srst	Submodule soft reset. Writing 0 has no effect, and writing 1 generates a soft reset signal. This bit is automatically cleared.
[2]	WC	ch3_rdma_srst	Submodule soft reset. Writing 0 has no effect, and writing 1 generates a soft reset signal. This bit is automatically cleared.

Offset Address	Register Name	Total Reset Value
0x0070	ADE_SOFT_RST0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	rot_srst	ctran6_srst	ctran5_srst	ctran4_srst	ctran3_srst	ctran2_srst	ctran1_srst	scl3_srst	scl2_srst	scl1_srst	clip6_srst	clip5_srst	clip4_srst	clip3_srst	clip2_srst	clip1_srst	cmdq_wdma_srst	reserved	ch3_wdma_srst	ch2_wdma_srst	ch1_wdma_srst	reserved	cmdq2_rdma_srst	cmdq1_rdma_srst	disp_rdma_srst	ch6_rdma_srst	ch5_rdma_srst	ch4_rdma_srst	ch3_rdma_srst	ch2_rdma_srst	ch1_rdma_srst
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1]	WC	ch2_rdma_srst	Submodule soft reset. Writing 0 has no effect, and writing 1 generates a soft reset signal. This bit is automatically cleared.
[0]	WC	ch1_rdma_srst	Submodule soft reset. Writing 0 has no effect, and writing 1 generates a soft reset signal. This bit is automatically cleared.

ADE_SOFT_RST1

ADE_SOFT_RST1 is submodule soft reset register 1.

Offset Address	Register Name	Total Reset Value
0x0074	ADE_SOFT_RST1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ovly3_srst	ovly2_srst	ovly1_srst	dither_srst	gamma_srst	reserved	cmdq2_srst	cmdq1_srst
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	WC	ovly3_srst	Submodule soft reset. Writing 0 has no effect, and writing 1 generates a soft reset signal. This bit is automatically cleared.
[6]	WC	ovly2_srst	Submodule soft reset. Writing 0 has no effect, and writing 1 generates a soft reset signal. This bit is automatically cleared.
[5]	WC	ovly1_srst	Submodule soft reset. Writing 0 has no effect, and writing 1 generates a soft reset signal. This bit is automatically cleared.

Offset Address	Register Name	Total Reset Value
0x0074	ADE_SOFT_RST1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ovly3_srst	ovly2_srst	ovly1_srst	dither_srst	gamma_srst	reserved	cmdq2_srst	cmdq1_srst
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[4]	WC	dither_srst	Submodule soft reset. Writing 0 has no effect, and writing 1 generates a soft reset signal. This bit is automatically cleared.
[3]	WC	gamma_srst	Submodule soft reset. Writing 0 has no effect, and writing 1 generates a soft reset signal. This bit is automatically cleared.
[2]	RO	reserved	Reserved
[1]	WC	cmdq2_srst	Submodule soft reset. Writing 0 has no effect, and writing 1 generates a soft reset signal. This bit is automatically cleared.
[0]	WC	cmdq1_srst	Submodule soft reset. Writing 0 has no effect, and writing 1 generates a soft reset signal. This bit is automatically cleared.

ADE_SOFT_RST_SEL0

ADE_SOFT_RST_SEL0 is submodule soft reset source selection register 0.

Offset Address	Register Name	Total Reset Value
0x0078	ADE_SOFT_RST_SEL0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	rot_srst_sel	ctran6_srst_sel	ctran5_srst_sel	ctran4_srst_sel	ctran3_srst_sel	ctran2_srst_sel	ctran1_srst_sel	scl3_srst_sel	scl2_srst_sel	scl1_srst_sel	clip6_srst_sel	clip5_srst_sel	clip4_srst_sel	clip3_srst_sel	clip2_srst_sel	clip1_srst_sel	cmdq_wdma_srst_sel	reserved	ch3_wdma_srst_sel	ch2_wdma_srst_sel	ch1_wdma_srst_sel	reserved	cmdq2_rdma_srst_sel	cmdq1_rdma_srst_sel	disp_rdma_srst_sel	ch6_rdma_srst_sel	ch5_rdma_srst_sel	ch4_rdma_srst_sel	ch3_rdma_srst_sel	ch2_rdma_srst_sel	ch1_rdma_srst_sel
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved

Offset Address	Register Name	Total Reset Value
0x0078	ADE_SOFT_RST_SEL0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	rot_srst_sel	ctran6_srst_sel	ctran5_srst_sel	ctran4_srst_sel	ctran3_srst_sel	ctran2_srst_sel	ctran1_srst_sel	scl3_srst_sel	scl2_srst_sel	scl1_srst_sel	clip6_srst_sel	clip5_srst_sel	clip4_srst_sel	clip3_srst_sel	clip2_srst_sel	clip1_srst_sel	cmdq_wdma_srst_sel	reserved	ch3_wdma_srst_sel	ch2_wdma_srst_sel	ch1_wdma_srst_sel	reserved	cmdq2_rdma_srst_sel	cmdq1_rdma_srst_sel	disp_rdma_srst_sel	ch6_rdma_srst_sel	ch5_rdma_srst_sel	ch4_rdma_srst_sel	ch3_rdma_srst_sel	ch2_rdma_srst_sel	ch1_rdma_srst_sel
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[30]	RW	rot_srst_sel	Submodule soft reset source select. This bit must work with frm_end_start. 0: When software configures the corresponding bit in the SOFT_RST register, a soft reset signal is generated, but the submodule does not start to work again. 1: When hardware resources are synchronously updated, a soft reset signal is generated, but the submodule does not start to work again.
[29]	RW	ctran6_srst_sel	Submodule soft reset source select. This bit must work with frm_end_start. 0: When software configures the corresponding bit in the SOFT_RST register, a soft reset signal is generated, but the submodule does not start to work again. 1: When hardware resources are synchronously updated, a soft reset signal is generated, but the submodule does not start to work again.
[28]	RW	ctran5_srst_sel	Submodule soft reset source select. This bit must work with frm_end_start. 0: When software configures the corresponding bit in the SOFT_RST register, a soft reset signal is generated, but the submodule does not start to work again. 1: When hardware resources are synchronously updated, a soft reset signal is generated, but the submodule does not start to work again.

Offset Address	Register Name	Total Reset Value
0x0078	ADE_SOFT_RST_SEL0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	rot_srst_sel	ctran6_srst_sel	ctran5_srst_sel	ctran4_srst_sel	ctran3_srst_sel	ctran2_srst_sel	ctran1_srst_sel	scl3_srst_sel	scl2_srst_sel	scl1_srst_sel	clip6_srst_sel	clip5_srst_sel	clip4_srst_sel	clip3_srst_sel	clip2_srst_sel	clip1_srst_sel	cmdq_wdma_srst_sel	reserved	ch3_wdma_srst_sel	ch2_wdma_srst_sel	ch1_wdma_srst_sel	reserved	cmdq2_rdma_srst_sel	cmdq1_rdma_srst_sel	disp_rdma_srst_sel	ch6_rdma_srst_sel	ch5_rdma_srst_sel	ch4_rdma_srst_sel	ch3_rdma_srst_sel	ch2_rdma_srst_sel	ch1_rdma_srst_sel
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[27]	RW	ctran4_srst_sel	Submodule soft reset source select. This bit must work with frm_end_start. 0: When software configures the corresponding bit in the SOFT_RST register, a soft reset signal is generated, but the submodule does not start to work again. 1: When hardware resources are synchronously updated, a soft reset signal is generated, but the submodule does not start to work again.
[26]	RW	ctran3_srst_sel	Submodule soft reset source select. This bit must work with frm_end_start. 0: When software configures the corresponding bit in the SOFT_RST register, a soft reset signal is generated, but the submodule does not start to work again. 1: When hardware resources are synchronously updated, a soft reset signal is generated, but the submodule does not start to work again.
[25]	RW	ctran2_srst_sel	Submodule soft reset source select. This bit must work with frm_end_start. 0: When software configures the corresponding bit in the SOFT_RST register, a soft reset signal is generated, but the submodule does not start to work again. 1: When hardware resources are synchronously updated, a soft reset signal is generated, but the submodule does not start to work again.

Offset Address	Register Name	Total Reset Value
0x0078	ADE_SOFT_RST_SEL0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	rot_srst_sel	ctran6_srst_sel	ctran5_srst_sel	ctran4_srst_sel	ctran3_srst_sel	ctran2_srst_sel	ctran1_srst_sel	scl3_srst_sel	scl2_srst_sel	scl1_srst_sel	clip6_srst_sel	clip5_srst_sel	clip4_srst_sel	clip3_srst_sel	clip2_srst_sel	clip1_srst_sel	cmdq_wdma_srst_sel	reserved	ch3_wdma_srst_sel	ch2_wdma_srst_sel	ch1_wdma_srst_sel	reserved	cmdq2_rdma_srst_sel	cmdq1_rdma_srst_sel	disp_rdma_srst_sel	ch6_rdma_srst_sel	ch5_rdma_srst_sel	ch4_rdma_srst_sel	ch3_rdma_srst_sel	ch2_rdma_srst_sel	ch1_rdma_srst_sel
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[24]	RW	ctran1_srst_sel	Submodule soft reset source select. This bit must work with frm_end_start. 0: When software configures the corresponding bit in the SOFT_RST register, a soft reset signal is generated, but the submodule does not start to work again. 1: When hardware resources are synchronously updated, a soft reset signal is generated, but the submodule does not start to work again.
[23]	RW	scl3_srst_sel	Submodule soft reset source select. This bit must work with frm_end_start. 0: When software configures the corresponding bit in the SOFT_RST register, a soft reset signal is generated, but the submodule does not start to work again. 1: When hardware resources are synchronously updated, a soft reset signal is generated, but the submodule does not start to work again.
[22]	RW	scl2_srst_sel	Submodule soft reset source select. This bit must work with frm_end_start. 0: When software configures the corresponding bit in the SOFT_RST register, a soft reset signal is generated, but the submodule does not start to work again. 1: When hardware resources are synchronously updated, a soft reset signal is generated, but the submodule does not start to work again.

Offset Address	Register Name	Total Reset Value
0x0078	ADE_SOFT_RST_SEL0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	rot_srst_sel	ctran6_srst_sel	ctran5_srst_sel	ctran4_srst_sel	ctran3_srst_sel	ctran2_srst_sel	ctran1_srst_sel	scl3_srst_sel	scl2_srst_sel	scl1_srst_sel	clip6_srst_sel	clip5_srst_sel	clip4_srst_sel	clip3_srst_sel	clip2_srst_sel	clip1_srst_sel	cmdq_wdma_srst_sel	reserved	ch3_wdma_srst_sel	ch2_wdma_srst_sel	ch1_wdma_srst_sel	reserved	cmdq2_rdma_srst_sel	cmdq1_rdma_srst_sel	disp_rdma_srst_sel	ch6_rdma_srst_sel	ch5_rdma_srst_sel	ch4_rdma_srst_sel	ch3_rdma_srst_sel	ch2_rdma_srst_sel	ch1_rdma_srst_sel
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[21]	RW	scl1_srst_sel	Submodule soft reset source select. This bit must work with frm_end_start. 0: When software configures the corresponding bit in the SOFT_RST register, a soft reset signal is generated, but the submodule does not start to work again. 1: When hardware resources are synchronously updated, a soft reset signal is generated, but the submodule does not start to work again.
[20]	RW	clip6_srst_sel	Submodule soft reset source select. This bit must work with frm_end_start. 0: When software configures the corresponding bit in the SOFT_RST register, a soft reset signal is generated, but the submodule does not start to work again. 1: When hardware resources are synchronously updated, a soft reset signal is generated, but the submodule does not start to work again.
[19]	RW	clip5_srst_sel	Submodule soft reset source select. This bit must work with frm_end_start. 0: When software configures the corresponding bit in the SOFT_RST register, a soft reset signal is generated, but the submodule does not start to work again. 1: When hardware resources are synchronously updated, a soft reset signal is generated, but the submodule does not start to work again.

Offset Address	Register Name	Total Reset Value
0x0078	ADE_SOFT_RST_SEL0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	rot_srst_sel	ctran6_srst_sel	ctran5_srst_sel	ctran4_srst_sel	ctran3_srst_sel	ctran2_srst_sel	ctran1_srst_sel	scl3_srst_sel	scl2_srst_sel	scl1_srst_sel	clip6_srst_sel	clip5_srst_sel	clip4_srst_sel	clip3_srst_sel	clip2_srst_sel	clip1_srst_sel	cmdq_wdma_srst_sel	reserved	ch3_wdma_srst_sel	ch2_wdma_srst_sel	ch1_wdma_srst_sel	reserved	cmdq2_rdma_srst_sel	cmdq1_rdma_srst_sel	disp_rdma_srst_sel	ch6_rdma_srst_sel	ch5_rdma_srst_sel	ch4_rdma_srst_sel	ch3_rdma_srst_sel	ch2_rdma_srst_sel	ch1_rdma_srst_sel
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[18]	RW	clip4_srst_sel	Submodule soft reset source select. This bit must work with frm_end_start. 0: When software configures the corresponding bit in the SOFT_RST register, a soft reset signal is generated, but the submodule does not start to work again. 1: When hardware resources are synchronously updated, a soft reset signal is generated, but the submodule does not start to work again.
[17]	RW	clip3_srst_sel	Submodule soft reset source select. This bit must work with frm_end_start. 0: When software configures the corresponding bit in the SOFT_RST register, a soft reset signal is generated, but the submodule does not start to work again. 1: When hardware resources are synchronously updated, a soft reset signal is generated, but the submodule does not start to work again.
[16]	RW	clip2_srst_sel	Submodule soft reset source select. This bit must work with frm_end_start. 0: When software configures the corresponding bit in the SOFT_RST register, a soft reset signal is generated, but the submodule does not start to work again. 1: When hardware resources are synchronously updated, a soft reset signal is generated, but the submodule does not start to work again.

Offset Address	Register Name	Total Reset Value
0x0078	ADE_SOFT_RST_SEL0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	rot_srst_sel	ctran6_srst_sel	ctran5_srst_sel	ctran4_srst_sel	ctran3_srst_sel	ctran2_srst_sel	ctran1_srst_sel	scl3_srst_sel	scl2_srst_sel	scl1_srst_sel	clip6_srst_sel	clip5_srst_sel	clip4_srst_sel	clip3_srst_sel	clip2_srst_sel	clip1_srst_sel	cmdq_wdma_srst_sel	reserved	ch3_wdma_srst_sel	ch2_wdma_srst_sel	ch1_wdma_srst_sel	reserved	cmdq2_rdma_srst_sel	cmdq1_rdma_srst_sel	disp_rdma_srst_sel	ch6_rdma_srst_sel	ch5_rdma_srst_sel	ch4_rdma_srst_sel	ch3_rdma_srst_sel	ch2_rdma_srst_sel	ch1_rdma_srst_sel
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15]	RW	clip1_srst_sel	Submodule soft reset source select. This bit must work with frm_end_start. 0: When software configures the corresponding bit in the SOFT_RST register, a soft reset signal is generated, but the submodule does not start to work again. 1: When hardware resources are synchronously updated, a soft reset signal is generated, but the submodule does not start to work again.
[14]	RW	cmdq_wdma_srst_sel	Submodule soft reset source select. This bit must work with frm_end_start. 0: When software configures the corresponding bit in the SOFT_RST register, a soft reset signal is generated, but the submodule does not start to work again. 1: When hardware resources are synchronously updated, a soft reset signal is generated, but the submodule does not start to work again.
[13]	RO	reserved	Reserved
[12]	RW	ch3_wdma_srst_sel	Submodule soft reset source select. This bit must work with frm_end_start. 0: When software configures the corresponding bit in the SOFT_RST register, a soft reset signal is generated, but the submodule does not start to work again. 1: When hardware resources are synchronously updated, a soft reset signal is generated, but the submodule does not start to work again.

Offset Address	Register Name	Total Reset Value
0x0078	ADE_SOFT_RST_SEL0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	rot_srst_sel	ctran6_srst_sel	ctran5_srst_sel	ctran4_srst_sel	ctran3_srst_sel	ctran2_srst_sel	ctran1_srst_sel	scl3_srst_sel	scl2_srst_sel	scl1_srst_sel	clip6_srst_sel	clip5_srst_sel	clip4_srst_sel	clip3_srst_sel	clip2_srst_sel	clip1_srst_sel	cmdq_wdma_srst_sel	reserved	ch3_wdma_srst_sel	ch2_wdma_srst_sel	ch1_wdma_srst_sel	reserved	cmdq2_rdma_srst_sel	cmdq1_rdma_srst_sel	disp_rdma_srst_sel	ch6_rdma_srst_sel	ch5_rdma_srst_sel	ch4_rdma_srst_sel	ch3_rdma_srst_sel	ch2_rdma_srst_sel	ch1_rdma_srst_sel
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[11]	RW	ch2_wdma_srst_sel	Submodule soft reset source select. This bit must work with frm_end_start. 0: When software configures the corresponding bit in the SOFT_RST register, a soft reset signal is generated, but the submodule does not start to work again. 1: When hardware resources are synchronously updated, a soft reset signal is generated, but the submodule does not start to work again.
[10]	RW	ch1_wdma_srst_sel	Submodule soft reset source select. This bit must work with frm_end_start. 0: When software configures the corresponding bit in the SOFT_RST register, a soft reset signal is generated, but the submodule does not start to work again. 1: When hardware resources are synchronously updated, a soft reset signal is generated, but the submodule does not start to work again.
[9]	RO	reserved	Reserved
[8]	RW	cmdq2_rdma_srst_sel	Submodule soft reset source select. This bit must work with frm_end_start. 0: When software configures the corresponding bit in the SOFT_RST register, a soft reset signal is generated, but the submodule does not start to work again. 1: When hardware resources are synchronously updated, a soft reset signal is generated, but the submodule does not start to work again.

Offset Address	Register Name	Total Reset Value
0x0078	ADE_SOFT_RST_SEL0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	rot_srst_sel	ctran6_srst_sel	ctran5_srst_sel	ctran4_srst_sel	ctran3_srst_sel	ctran2_srst_sel	ctran1_srst_sel	scl3_srst_sel	scl2_srst_sel	scl1_srst_sel	clip6_srst_sel	clip5_srst_sel	clip4_srst_sel	clip3_srst_sel	clip2_srst_sel	clip1_srst_sel	cmdq_wdma_srst_sel	reserved	ch3_wdma_srst_sel	ch2_wdma_srst_sel	ch1_wdma_srst_sel	reserved	cmdq2_rdma_srst_sel	cmdq1_rdma_srst_sel	disp_rdma_srst_sel	ch6_rdma_srst_sel	ch5_rdma_srst_sel	ch4_rdma_srst_sel	ch3_rdma_srst_sel	ch2_rdma_srst_sel	ch1_rdma_srst_sel
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7]	RW	cmdq1_rdma_srst_sel	Submodule soft reset source select. This bit must work with frm_end_start. 0: When software configures the corresponding bit in the SOFT_RST register, a soft reset signal is generated, but the submodule does not start to work again. 1: When hardware resources are synchronously updated, a soft reset signal is generated, but the submodule does not start to work again.
[6]	RW	disp_rdma_srst_sel	Submodule soft reset source select. This bit must work with frm_end_start. 0: When software configures the corresponding bit in the SOFT_RST register, a soft reset signal is generated, but the submodule does not start to work again. 1: When hardware resources are synchronously updated, a soft reset signal is generated, but the submodule does not start to work again.
[5]	RW	ch6_rdma_srst_sel	Submodule soft reset source select. This bit must work with frm_end_start. 0: When software configures the corresponding bit in the SOFT_RST register, a soft reset signal is generated, but the submodule does not start to work again. 1: When hardware resources are synchronously updated, a soft reset signal is generated, but the submodule does not start to work again.

Offset Address	Register Name	Total Reset Value
0x0078	ADE_SOFT_RST_SEL0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	rot_srst_sel	ctran6_srst_sel	ctran5_srst_sel	ctran4_srst_sel	ctran3_srst_sel	ctran2_srst_sel	ctran1_srst_sel	scl3_srst_sel	scl2_srst_sel	scl1_srst_sel	clip6_srst_sel	clip5_srst_sel	clip4_srst_sel	clip3_srst_sel	clip2_srst_sel	clip1_srst_sel	cmdq_wdma_srst_sel	reserved	ch3_wdma_srst_sel	ch2_wdma_srst_sel	ch1_wdma_srst_sel	reserved	cmdq2_rdma_srst_sel	cmdq1_rdma_srst_sel	disp_rdma_srst_sel	ch6_rdma_srst_sel	ch5_rdma_srst_sel	ch4_rdma_srst_sel	ch3_rdma_srst_sel	ch2_rdma_srst_sel	ch1_rdma_srst_sel
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[4]	RW	ch5_rdma_srst_sel	Submodule soft reset source select. This bit must work with frm_end_start. 0: When software configures the corresponding bit in the SOFT_RST register, a soft reset signal is generated, but the submodule does not start to work again. 1: When hardware resources are synchronously updated, a soft reset signal is generated, but the submodule does not start to work again.
[3]	RW	ch4_rdma_srst_sel	Submodule soft reset source select. This bit must work with frm_end_start. 0: When software configures the corresponding bit in the SOFT_RST register, a soft reset signal is generated, but the submodule does not start to work again. 1: When hardware resources are synchronously updated, a soft reset signal is generated, but the submodule does not start to work again.
[2]	RW	ch3_rdma_srst_sel	Submodule soft reset source select. This bit must work with frm_end_start. 0: When software configures the corresponding bit in the SOFT_RST register, a soft reset signal is generated, but the submodule does not start to work again. 1: When hardware resources are synchronously updated, a soft reset signal is generated, but the submodule does not start to work again.

Offset Address	Register Name	Total Reset Value
0x0078	ADE_SOFT_RST_SEL0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	rot_srst_sel	ctran6_srst_sel	ctran5_srst_sel	ctran4_srst_sel	ctran3_srst_sel	ctran2_srst_sel	ctran1_srst_sel	scl3_srst_sel	scl2_srst_sel	scl1_srst_sel	clip6_srst_sel	clip5_srst_sel	clip4_srst_sel	clip3_srst_sel	clip2_srst_sel	clip1_srst_sel	cmdq_wdma_srst_sel	reserved	ch3_wdma_srst_sel	ch2_wdma_srst_sel	ch1_wdma_srst_sel	reserved	cmdq2_rdma_srst_sel	cmdq1_rdma_srst_sel	disp_rdma_srst_sel	ch6_rdma_srst_sel	ch5_rdma_srst_sel	ch4_rdma_srst_sel	ch3_rdma_srst_sel	ch2_rdma_srst_sel	ch1_rdma_srst_sel
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1]	RW	ch2_rdma_srst_sel	Submodule soft reset source select. This bit must work with frm_end_start. 0: When software configures the corresponding bit in the SOFT_RST register, a soft reset signal is generated, but the submodule does not start to work again. 1: When hardware resources are synchronously updated, a soft reset signal is generated, but the submodule does not start to work again.
[0]	RW	ch1_rdma_srst_sel	Submodule soft reset source select. This bit must work with frm_end_start. 0: When software configures the corresponding bit in the SOFT_RST register, a soft reset signal is generated, but the submodule does not start to work again. 1: When hardware resources are synchronously updated, a soft reset signal is generated, but the submodule does not start to work again.

ADE_SOFT_RST_SEL1

ADE_SOFT_RST_SEL1 is submodule soft reset source selection register 1.

Offset Address	Register Name	Total Reset Value
0x007C	ADE_SOFT_RST_SEL1	0x0000_0018

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ovly3_srst_sel	ovly2_srst_sel	ovly1_srst_sel	dither_srst_sel	gamma_srst_sel	reserved	cmdq2_srst_sel	cmdq1_srst_sel
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	ovly3_srst_sel	Submodule soft reset source select. This bit must work with frm_end_start. 0: When software configures the corresponding bit in the SOFT_RST register, a soft reset signal is generated, but the submodule does not start to work again. 1: When hardware resources are synchronously updated, a soft reset signal is generated, but the submodule does not start to work again.
[6]	RW	ovly2_srst_sel	Submodule soft reset source select. This bit must work with frm_end_start. 0: When software configures the corresponding bit in the SOFT_RST register, a soft reset signal is generated, but the submodule does not start to work again. 1: When hardware resources are synchronously updated, a soft reset signal is generated, but the submodule does not start to work again.
[5]	RW	ovly1_srst_sel	Submodule soft reset source select. This bit must work with frm_end_start. 0: When software configures the corresponding bit in the SOFT_RST register, a soft reset signal is generated, but the submodule does not start to work again. 1: When hardware resources are synchronously updated, a soft reset signal is generated, but the submodule does not start to work again.

Offset Address	Register Name	Total Reset Value
0x007C	ADE_SOFT_RST_SEL1	0x0000_0018

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ovly3_srst_sel	ovly2_srst_sel	ovly1_srst_sel	dither_srst_sel	gamma_srst_sel	reserved	cmdq2_srst_sel	cmdq1_srst_sel
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0

Bits	Access	Name	Description
[4]	RW	dither_srst_sel	Submodule soft reset source select. This bit must work with frm_end_start. 0: When software configures the corresponding bit in the SOFT_RST register, a soft reset signal is generated, but the submodule does not start to work again. 1: When hardware resources are synchronously updated, a soft reset signal is generated, but the submodule does not start to work again.
[3]	RW	gamma_srst_sel	Submodule soft reset source select. This bit must work with frm_end_start. 0: When software configures the corresponding bit in the SOFT_RST register, a soft reset signal is generated, but the submodule does not start to work again. 1: When hardware resources are synchronously updated, a soft reset signal is generated, but the submodule does not start to work again.
[2]	RO	reserved	Reserved
[1]	RW	cmdq2_srst_sel	Submodule soft reset source select. This bit must work with frm_end_start. 0: When software configures the corresponding bit in the SOFT_RST register, a soft reset signal is generated, but the submodule does not start to work again. 1: When hardware resources are synchronously updated, a soft reset signal is generated, but the submodule does not start to work again.

Offset Address	Register Name	Total Reset Value
0x007C	ADE_SOFT_RST_SEL1	0x0000_0018

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ovly3_srst_sel	ovly2_srst_sel	ovly1_srst_sel	dither_srst_sel	gamma_srst_sel	reserved	cmdq2_srst_sel	cmdq1_srst_sel
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0

Bits	Access	Name	Description
[0]	RW	cmdq1_srst_sel	Submodule soft reset source select. This bit must work with frm_end_start. 0: When software configures the corresponding bit in the SOFT_RST register, a soft reset signal is generated, but the submodule does not start to work again. 1: When hardware resources are synchronously updated, a soft reset signal is generated, but the submodule does not start to work again.

ADE_AUTO_CLK_GT_EN0

ADE_AUTO_CLK_GT_EN0 is ADE submodule automatic clock gating control register 0.

Offset Address	Register Name	Total Reset Value
0x009C	ADE_AUTO_CLK_GT_EN0	0x7FFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	rot_auto_clk_gt_en	ctran6_auto_clk_gt_en	ctran5_auto_clk_gt_en	ctran4_auto_clk_gt_en	ctran3_auto_clk_gt_en	ctran2_auto_clk_gt_en	ctran1_auto_clk_gt_en	scl3_auto_clk_gt_en	scl2_auto_clk_gt_en	scl1_auto_clk_gt_en	clip6_auto_clk_gt_en	clip5_auto_clk_gt_en	clip4_auto_clk_gt_en	clip3_auto_clk_gt_en	clip2_auto_clk_gt_en	clip1_auto_clk_gt_en	cmdq_wdma_auto_clk_gt_en	reserved	ch3_wdma_auto_clk_gt_en	ch2_wdma_auto_clk_gt_en	ch1_wdma_auto_clk_gt_en	reserved	cmdq2_rdma_auto_clk_gt_en	cmdq1_rdma_auto_clk_gt_en	disp_rdma_auto_clk_gt_en	ch6_rdma_auto_clk_gt_en	ch5_rdma_auto_clk_gt_en	ch4_rdma_auto_clk_gt_en	ch3_rdma_auto_clk_gt_en	ch2_rdma_auto_clk_gt_en	ch1_rdma_auto_clk_gt_en
Reset	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30]	RW	rot_auto_clk_gt_en	Submodule automatic clock gating enable (valid only when global automatic clock gating is enabled) 0: disabled 1: enabled
[29]	RW	ctran6_auto_clk_gt_en	Submodule automatic clock gating enable (valid only when global automatic clock gating is enabled) 0: disabled 1: enabled
[28]	RW	ctran5_auto_clk_gt_en	Submodule automatic clock gating enable (valid only when global automatic clock gating is enabled) 0: disabled 1: enabled
[27]	RW	ctran4_auto_clk_gt_en	Submodule automatic clock gating enable (valid only when global automatic clock gating is enabled) 0: disabled 1: enabled
[26]	RW	ctran3_auto_clk_gt_en	Submodule automatic clock gating enable (valid only when global automatic clock gating is enabled) 0: disabled 1: enabled
[25]	RW	ctran2_auto_clk_gt_en	Submodule automatic clock gating enable (valid only when global automatic clock gating is enabled) 0: disabled 1: enabled

Offset Address	Register Name	Total Reset Value
0x009C	ADE_AUTO_CLK_GT_EN0	0x7FFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	rot_auto_clk_gt_en	ctran6_auto_clk_gt_en	ctran5_auto_clk_gt_en	ctran4_auto_clk_gt_en	ctran3_auto_clk_gt_en	ctran2_auto_clk_gt_en	ctran1_auto_clk_gt_en	scl3_auto_clk_gt_en	scl2_auto_clk_gt_en	scl1_auto_clk_gt_en	clip6_auto_clk_gt_en	clip5_auto_clk_gt_en	clip4_auto_clk_gt_en	clip3_auto_clk_gt_en	clip2_auto_clk_gt_en	clip1_auto_clk_gt_en	cmdq_wdma_auto_clk_gt_en	reserved	ch3_wdma_auto_clk_gt_en	ch2_wdma_auto_clk_gt_en	ch1_wdma_auto_clk_gt_en	reserved	cmdq2_rdma_auto_clk_gt_en	cmdq1_rdma_auto_clk_gt_en	disp_rdma_auto_clk_gt_en	ch6_rdma_auto_clk_gt_en	ch5_rdma_auto_clk_gt_en	ch4_rdma_auto_clk_gt_en	ch3_rdma_auto_clk_gt_en	ch2_rdma_auto_clk_gt_en	ch1_rdma_auto_clk_gt_en
Reset	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[24]	RW	ctran1_auto_clk_gt_en	Submodule automatic clock gating enable (valid only when global automatic clock gating is enabled) 0: disabled 1: enabled
[23]	RW	scl3_auto_clk_gt_en	Submodule automatic clock gating enable (valid only when global automatic clock gating is enabled) 0: disabled 1: enabled
[22]	RW	scl2_auto_clk_gt_en	Submodule automatic clock gating enable (valid only when global automatic clock gating is enabled) 0: disabled 1: enabled
[21]	RW	scl1_auto_clk_gt_en	Submodule automatic clock gating enable (valid only when global automatic clock gating is enabled) 0: disabled 1: enabled
[20]	RW	clip6_auto_clk_gt_en	Submodule automatic clock gating enable (valid only when global automatic clock gating is enabled) 0: disabled 1: enabled
[19]	RW	clip5_auto_clk_gt_en	Submodule automatic clock gating enable (valid only when global automatic clock gating is enabled) 0: disabled 1: enabled

Offset Address	Register Name	Total Reset Value
0x009C	ADE_AUTO_CLK_GT_EN0	0x7FFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	rot_auto_clk_gt_en	ctran6_auto_clk_gt_en	ctran5_auto_clk_gt_en	ctran4_auto_clk_gt_en	ctran3_auto_clk_gt_en	ctran2_auto_clk_gt_en	ctran1_auto_clk_gt_en	scl3_auto_clk_gt_en	scl2_auto_clk_gt_en	scl1_auto_clk_gt_en	clip6_auto_clk_gt_en	clip5_auto_clk_gt_en	clip4_auto_clk_gt_en	clip3_auto_clk_gt_en	clip2_auto_clk_gt_en	clip1_auto_clk_gt_en	cmdq_wdma_auto_clk_gt_en	reserved	ch3_wdma_auto_clk_gt_en	ch2_wdma_auto_clk_gt_en	ch1_wdma_auto_clk_gt_en	reserved	cmdq2_rdma_auto_clk_gt_en	cmdq1_rdma_auto_clk_gt_en	disp_rdma_auto_clk_gt_en	ch6_rdma_auto_clk_gt_en	ch5_rdma_auto_clk_gt_en	ch4_rdma_auto_clk_gt_en	ch3_rdma_auto_clk_gt_en	ch2_rdma_auto_clk_gt_en	ch1_rdma_auto_clk_gt_en
Reset	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[18]	RW	clip4_auto_clk_gt_en	Submodule automatic clock gating enable (valid only when global automatic clock gating is enabled) 0: disabled 1: enabled
[17]	RW	clip3_auto_clk_gt_en	Submodule automatic clock gating enable (valid only when global automatic clock gating is enabled) 0: disabled 1: enabled
[16]	RW	clip2_auto_clk_gt_en	Submodule automatic clock gating enable (valid only when global automatic clock gating is enabled) 0: disabled 1: enabled
[15]	RW	clip1_auto_clk_gt_en	Submodule automatic clock gating enable (valid only when global automatic clock gating is enabled) 0: disabled 1: enabled
[14]	RW	cmdq_wdma_auto_clk_gt_en	Submodule automatic clock gating enable (valid only when global automatic clock gating is enabled) 0: disabled 1: enabled
[13]	RO	reserved	Reserved
[12]	RW	ch3_wdma_auto_clk_gt_en	Submodule automatic clock gating enable (valid only when global automatic clock gating is enabled) 0: disabled 1: enabled

Offset Address	Register Name	Total Reset Value
0x009C	ADE_AUTO_CLK_GT_EN0	0x7FFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	rot_auto_clk_gt_en	ctran6_auto_clk_gt_en	ctran5_auto_clk_gt_en	ctran4_auto_clk_gt_en	ctran3_auto_clk_gt_en	ctran2_auto_clk_gt_en	ctran1_auto_clk_gt_en	scl3_auto_clk_gt_en	scl2_auto_clk_gt_en	scl1_auto_clk_gt_en	clip6_auto_clk_gt_en	clip5_auto_clk_gt_en	clip4_auto_clk_gt_en	clip3_auto_clk_gt_en	clip2_auto_clk_gt_en	clip1_auto_clk_gt_en	cmdq_wdma_auto_clk_gt_en	reserved	ch3_wdma_auto_clk_gt_en	ch2_wdma_auto_clk_gt_en	ch1_wdma_auto_clk_gt_en	reserved	cmdq2_rdma_auto_clk_gt_en	cmdq1_rdma_auto_clk_gt_en	disp_rdma_auto_clk_gt_en	ch6_rdma_auto_clk_gt_en	ch5_rdma_auto_clk_gt_en	ch4_rdma_auto_clk_gt_en	ch3_rdma_auto_clk_gt_en	ch2_rdma_auto_clk_gt_en	ch1_rdma_auto_clk_gt_en
Reset	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[11]	RW	ch2_wdma_auto_clk_gt_en	Submodule automatic clock gating enable (valid only when global automatic clock gating is enabled) 0: disabled 1: enabled
[10]	RW	ch1_wdma_auto_clk_gt_en	Submodule automatic clock gating enable (valid only when global automatic clock gating is enabled) 0: disabled 1: enabled
[9]	RO	reserved	Reserved
[8]	RW	cmdq2_rdma_auto_clk_gt_en	Submodule automatic clock gating enable (valid only when global automatic clock gating is enabled) 0: disabled 1: enabled
[7]	RW	cmdq1_rdma_auto_clk_gt_en	Submodule automatic clock gating enable (valid only when global automatic clock gating is enabled) 0: disabled 1: enabled
[6]	RW	disp_rdma_auto_clk_gt_en	Submodule automatic clock gating enable (valid only when global automatic clock gating is enabled) 0: disabled 1: enabled
[5]	RW	ch6_rdma_auto_clk_gt_en	Submodule automatic clock gating enable (valid only when global automatic clock gating is enabled) 0: disabled 1: enabled

Offset Address	Register Name	Total Reset Value
0x009C	ADE_AUTO_CLK_GT_EN0	0x7FFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	rot_auto_clk_gt_en	ctran6_auto_clk_gt_en	ctran5_auto_clk_gt_en	ctran4_auto_clk_gt_en	ctran3_auto_clk_gt_en	ctran2_auto_clk_gt_en	ctran1_auto_clk_gt_en	scl3_auto_clk_gt_en	scl2_auto_clk_gt_en	scl1_auto_clk_gt_en	clip6_auto_clk_gt_en	clip5_auto_clk_gt_en	clip4_auto_clk_gt_en	clip3_auto_clk_gt_en	clip2_auto_clk_gt_en	clip1_auto_clk_gt_en	cmdq_wdma_auto_clk_gt_en	reserved	ch3_wdma_auto_clk_gt_en	ch2_wdma_auto_clk_gt_en	ch1_wdma_auto_clk_gt_en	reserved	cmdq2_rdma_auto_clk_gt_en	cmdq1_rdma_auto_clk_gt_en	disp_rdma_auto_clk_gt_en	ch6_rdma_auto_clk_gt_en	ch5_rdma_auto_clk_gt_en	ch4_rdma_auto_clk_gt_en	ch3_rdma_auto_clk_gt_en	ch2_rdma_auto_clk_gt_en	ch1_rdma_auto_clk_gt_en
Reset	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[4]	RW	ch5_rdma_auto_clk_gt_en	Submodule automatic clock gating enable (valid only when global automatic clock gating is enabled) 0: disabled 1: enabled
[3]	RW	ch4_rdma_auto_clk_gt_en	Submodule automatic clock gating enable (valid only when global automatic clock gating is enabled) 0: disabled 1: enabled
[2]	RW	ch3_rdma_auto_clk_gt_en	Submodule automatic clock gating enable (valid only when global automatic clock gating is enabled) 0: disabled 1: enabled
[1]	RW	ch2_rdma_auto_clk_gt_en	Submodule automatic clock gating enable (valid only when global automatic clock gating is enabled) 0: disabled 1: enabled
[0]	RW	ch1_rdma_auto_clk_gt_en	Submodule automatic clock gating enable (valid only when global automatic clock gating is enabled) 0: disabled 1: enabled

ADE_AUTO_CLK_GT_EN1

ADE_AUTO_CLK_GT_EN1 is ADE submodule automatic clock gating control register 1.

Offset Address	Register Name	Total Reset Value
0x00A0	ADE_AUTO_CLK_GT_EN1	0x0000_01FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							top_auto_clk_gt_en	ovly3_auto_clk_gt_en	ovly2_auto_clk_gt_en	ovly1_auto_clk_gt_en	dither_auto_clk_gt_en	gamma_auto_clk_gt_en	reserved	cmdq2_auto_clk_gt_en	cmdq1_auto_clk_gt_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved
[8]	RW	top_auto_clk_gt_en	Submodule automatic clock gating enable (valid only when global automatic clock gating is enabled) 0: disabled 1: enabled
[7]	RW	ovly3_auto_clk_gt_en	Submodule automatic clock gating enable (valid only when global automatic clock gating is enabled) 0: disabled 1: enabled
[6]	RW	ovly2_auto_clk_gt_en	Submodule automatic clock gating enable (valid only when global automatic clock gating is enabled) 0: disabled 1: enabled
[5]	RW	ovly1_auto_clk_gt_en	Submodule automatic clock gating enable (valid only when global automatic clock gating is enabled) 0: disabled 1: enabled
[4]	RW	dither_auto_clk_gt_en	Submodule automatic clock gating enable (valid only when global automatic clock gating is enabled) 0: disabled 1: enabled
[3]	RW	gamma_auto_clk_gt_en	Submodule automatic clock gating enable (valid only when global automatic clock gating is enabled) 0: disabled 1: enabled
[2]	RO	reserved	Reserved

Offset Address	Register Name	Total Reset Value
0x00A0	ADE_AUTO_CLK_GT_EN1	0x0000_01FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							top_auto_clk_gt_en	ovly3_auto_clk_gt_en	ovly2_auto_clk_gt_en	ovly1_auto_clk_gt_en	dither_auto_clk_gt_en	gamma_auto_clk_gt_en	reserved	cmdq2_auto_clk_gt_en	cmdq1_auto_clk_gt_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[1]	RW	cmdq2_auto_clk_gt_en	Submodule automatic clock gating enable (valid only when global automatic clock gating is enabled) 0: disabled 1: enabled
[0]	RW	cmdq1_auto_clk_gt_en	Submodule automatic clock gating enable (valid only when global automatic clock gating is enabled) 0: disabled 1: enabled

ADE_RELOAD_DIS0

ADE_RELOAD_DIS0 is submodule hardware sync mask register 0.

Offset Address	Register Name	Total Reset Value
0x00AC	ADE_RELOAD_DIS0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	rot_reload_dis	ctran6_reload_dis	ctran5_reload_dis	ctran4_reload_dis	ctran3_reload_dis	ctran2_reload_dis	ctran1_reload_dis	scl3_reload_dis	scl2_reload_dis	scl1_reload_dis	clip6_reload_dis	clip5_reload_dis	clip4_reload_dis	clip3_reload_dis	clip2_reload_dis	clip1_reload_dis	cmdq_wdma_reload_dis	reserved	ch3_wdma_reload_dis	ch2_wdma_reload_dis	ch1_wdma_reload_dis	reserved	cmdq2_rdma_reload_dis	cmdq1_rdma_reload_dis	disp_rdma_reload_dis	ch6_rdma_reload_dis	ch5_rdma_reload_dis	ch4_rdma_reload_dis	ch3_rdma_reload_dis	ch2_rdma_reload_dis	ch1_rdma_reload_dis
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30]	RW	rot_reload_dis	Submodule hardware sync mask. This bit must work with ADE_SOFT_RST_SEL. 0: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule reloads programs and starts to work after soft reset. 1: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule does not reload and start to work after soft reset.
[29]	RW	ctran6_reload_dis	Submodule hardware sync mask. This bit must work with ADE_SOFT_RST_SEL. 0: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule reloads programs and starts to work after soft reset. 1: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule does not reload and start to work after soft reset.
[28]	RW	ctran5_reload_dis	Submodule hardware sync mask. This bit must work with ADE_SOFT_RST_SEL. 0: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule reloads programs and starts to work after soft reset. 1: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule does not reload and start to work after soft reset.
[27]	RW	ctran4_reload_dis	Submodule hardware sync mask. This bit must work with ADE_SOFT_RST_SEL. 0: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule reloads programs and starts to work after soft reset. 1: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule does not reload and start to work after soft reset.

Offset Address	Register Name	Total Reset Value
0x00AC	ADE_RELOAD_DIS0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	rot_reload_dis	ctran6_reload_dis	ctran5_reload_dis	ctran4_reload_dis	ctran3_reload_dis	ctran2_reload_dis	ctran1_reload_dis	scl3_reload_dis	scl2_reload_dis	scl1_reload_dis	clip6_reload_dis	clip5_reload_dis	clip4_reload_dis	clip3_reload_dis	clip2_reload_dis	clip1_reload_dis	cmdq_wdma_reload_dis	reserved	ch3_wdma_reload_dis	ch2_wdma_reload_dis	ch1_wdma_reload_dis	reserved	cmdq2_rdma_reload_dis	cmdq1_rdma_reload_dis	disp_rdma_reload_dis	ch6_rdma_reload_dis	ch5_rdma_reload_dis	ch4_rdma_reload_dis	ch3_rdma_reload_dis	ch2_rdma_reload_dis	ch1_rdma_reload_dis
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[26]	RW	ctran3_reload_dis	Submodule hardware sync mask. This bit must work with ADE_SOFT_RST_SEL. 0: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule reloads programs and starts to work after soft reset. 1: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule does not reload and start to work after soft reset.
[25]	RW	ctran2_reload_dis	Submodule hardware sync mask. This bit must work with ADE_SOFT_RST_SEL. 0: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule reloads programs and starts to work after soft reset. 1: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule does not reload and start to work after soft reset.
[24]	RW	ctran1_reload_dis	Submodule hardware sync mask. This bit must work with ADE_SOFT_RST_SEL. 0: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule reloads programs and starts to work after soft reset. 1: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule does not reload and start to work after soft reset.
[23]	RW	scl3_reload_dis	Submodule hardware sync mask. This bit must work with ADE_SOFT_RST_SEL. 0: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule reloads programs and starts to work after soft reset. 1: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule does not reload and start to work after soft reset.

Offset Address	Register Name	Total Reset Value
0x00AC	ADE_RELOAD_DIS0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	rot_reload_dis	ctran6_reload_dis	ctran5_reload_dis	ctran4_reload_dis	ctran3_reload_dis	ctran2_reload_dis	ctran1_reload_dis	scl3_reload_dis	scl2_reload_dis	scl1_reload_dis	clip6_reload_dis	clip5_reload_dis	clip4_reload_dis	clip3_reload_dis	clip2_reload_dis	clip1_reload_dis	cmdq_wdma_reload_dis	reserved	ch3_wdma_reload_dis	ch2_wdma_reload_dis	ch1_wdma_reload_dis	reserved	cmdq2_rdma_reload_dis	cmdq1_rdma_reload_dis	disp_rdma_reload_dis	ch6_rdma_reload_dis	ch5_rdma_reload_dis	ch4_rdma_reload_dis	ch3_rdma_reload_dis	ch2_rdma_reload_dis	ch1_rdma_reload_dis
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[22]	RW	scl2_reload_dis	Submodule hardware sync mask. This bit must work with ADE_SOFT_RST_SEL. 0: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule reloads programs and starts to work after soft reset. 1: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule does not reload and start to work after soft reset.
[21]	RW	scl1_reload_dis	Submodule hardware sync mask. This bit must work with ADE_SOFT_RST_SEL. 0: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule reloads programs and starts to work after soft reset. 1: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule does not reload and start to work after soft reset.
[20]	RW	clip6_reload_dis	Submodule hardware sync mask. This bit must work with ADE_SOFT_RST_SEL. 0: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule reloads programs and starts to work after soft reset. 1: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule does not reload and start to work after soft reset.
[19]	RW	clip5_reload_dis	Submodule hardware sync mask. This bit must work with ADE_SOFT_RST_SEL. 0: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule reloads programs and starts to work after soft reset. 1: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule does not reload and start to work after soft reset.

Offset Address	Register Name	Total Reset Value
0x00AC	ADE_RELOAD_DIS0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	rot_reload_dis	ctran6_reload_dis	ctran5_reload_dis	ctran4_reload_dis	ctran3_reload_dis	ctran2_reload_dis	ctran1_reload_dis	scl3_reload_dis	scl2_reload_dis	scl1_reload_dis	clip6_reload_dis	clip5_reload_dis	clip4_reload_dis	clip3_reload_dis	clip2_reload_dis	clip1_reload_dis	cmdq_wdma_reload_dis	reserved	ch3_wdma_reload_dis	ch2_wdma_reload_dis	ch1_wdma_reload_dis	reserved	cmdq2_rdma_reload_dis	cmdq1_rdma_reload_dis	disp_rdma_reload_dis	ch6_rdma_reload_dis	ch5_rdma_reload_dis	ch4_rdma_reload_dis	ch3_rdma_reload_dis	ch2_rdma_reload_dis	ch1_rdma_reload_dis
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[18]	RW	clip4_reload_dis	Submodule hardware sync mask. This bit must work with ADE_SOFT_RST_SEL. 0: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule reloads programs and starts to work after soft reset. 1: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule does not reload and start to work after soft reset.
[17]	RW	clip3_reload_dis	Submodule hardware sync mask. This bit must work with ADE_SOFT_RST_SEL. 0: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule reloads programs and starts to work after soft reset. 1: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule does not reload and start to work after soft reset.
[16]	RW	clip2_reload_dis	Submodule hardware sync mask. This bit must work with ADE_SOFT_RST_SEL. 0: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule reloads programs and starts to work after soft reset. 1: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule does not reload and start to work after soft reset.
[15]	RW	clip1_reload_dis	Submodule hardware sync mask. This bit must work with ADE_SOFT_RST_SEL. 0: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule reloads programs and starts to work after soft reset. 1: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule does not reload and start to work after soft reset.

Offset Address	Register Name	Total Reset Value
0x00AC	ADE_RELOAD_DIS0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	rot_reload_dis	ctran6_reload_dis	ctran5_reload_dis	ctran4_reload_dis	ctran3_reload_dis	ctran2_reload_dis	ctran1_reload_dis	scl3_reload_dis	scl2_reload_dis	scl1_reload_dis	clip6_reload_dis	clip5_reload_dis	clip4_reload_dis	clip3_reload_dis	clip2_reload_dis	clip1_reload_dis	cmdq_wdma_reload_dis	reserved	ch3_wdma_reload_dis	ch2_wdma_reload_dis	ch1_wdma_reload_dis	reserved	cmdq2_rdma_reload_dis	cmdq1_rdma_reload_dis	disp_rdma_reload_dis	ch6_rdma_reload_dis	ch5_rdma_reload_dis	ch4_rdma_reload_dis	ch3_rdma_reload_dis	ch2_rdma_reload_dis	ch1_rdma_reload_dis
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[14]	RW	cmdq_wdma_reload_dis	Submodule hardware sync mask. This bit must work with ADE_SOFT_RST_SEL. 0: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule reloads programs and starts to work after soft reset. 1: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule does not reload and start to work after soft reset.
[13]	RO	reserved	Reserved
[12]	RW	ch3_wdma_reload_dis	Submodule hardware sync mask. This bit must work with ADE_SOFT_RST_SEL. 0: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule reloads programs and starts to work after soft reset. 1: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule does not reload and start to work after soft reset.
[11]	RW	ch2_wdma_reload_dis	Submodule hardware sync mask. This bit must work with ADE_SOFT_RST_SEL. 0: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule reloads programs and starts to work after soft reset. 1: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule does not reload and start to work after soft reset.
[10]	RW	ch1_wdma_reload_dis	Submodule hardware sync mask. This bit must work with ADE_SOFT_RST_SEL. 0: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule reloads programs and starts to work after soft reset. 1: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule does not reload and start to work after soft reset.
[9]	RO	reserved	Reserved

Offset Address	Register Name	Total Reset Value
0x00AC	ADE_RELOAD_DIS0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	rot_reload_dis	ctran6_reload_dis	ctran5_reload_dis	ctran4_reload_dis	ctran3_reload_dis	ctran2_reload_dis	ctran1_reload_dis	scl3_reload_dis	scl2_reload_dis	scl1_reload_dis	clip6_reload_dis	clip5_reload_dis	clip4_reload_dis	clip3_reload_dis	clip2_reload_dis	clip1_reload_dis	cmdq_wdma_reload_dis	reserved	ch3_wdma_reload_dis	ch2_wdma_reload_dis	ch1_wdma_reload_dis	reserved	cmdq2_rdma_reload_dis	cmdq1_rdma_reload_dis	disp_rdma_reload_dis	ch6_rdma_reload_dis	ch5_rdma_reload_dis	ch4_rdma_reload_dis	ch3_rdma_reload_dis	ch2_rdma_reload_dis	ch1_rdma_reload_dis
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[8]	RW	cmdq2_rdma_reload_dis	Submodule hardware sync mask. This bit must work with ADE_SOFT_RST_SEL. 0: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule reloads programs and starts to work after soft reset. 1: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule does not reload and start to work after soft reset.
[7]	RW	cmdq1_rdma_reload_dis	Submodule hardware sync mask. This bit must work with ADE_SOFT_RST_SEL. 0: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule reloads programs and starts to work after soft reset. 1: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule does not reload and start to work after soft reset.
[6]	RW	disp_rdma_reload_dis	Submodule hardware sync mask. This bit must work with ADE_SOFT_RST_SEL. 0: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule reloads programs and starts to work after soft reset. 1: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule does not reload and start to work after soft reset.
[5]	RW	ch6_rdma_reload_dis	Submodule hardware sync mask. This bit must work with ADE_SOFT_RST_SEL. 0: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule reloads programs and starts to work after soft reset. 1: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule does not reload and start to work after soft reset.

Offset Address	Register Name	Total Reset Value
0x00AC	ADE_RELOAD_DIS0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	rot_reload_dis	ctran6_reload_dis	ctran5_reload_dis	ctran4_reload_dis	ctran3_reload_dis	ctran2_reload_dis	ctran1_reload_dis	scl3_reload_dis	scl2_reload_dis	scl1_reload_dis	clip6_reload_dis	clip5_reload_dis	clip4_reload_dis	clip3_reload_dis	clip2_reload_dis	clip1_reload_dis	cmdq_wdma_reload_dis	reserved	ch3_wdma_reload_dis	ch2_wdma_reload_dis	ch1_wdma_reload_dis	reserved	cmdq2_rdma_reload_dis	cmdq1_rdma_reload_dis	disp_rdma_reload_dis	ch6_rdma_reload_dis	ch5_rdma_reload_dis	ch4_rdma_reload_dis	ch3_rdma_reload_dis	ch2_rdma_reload_dis	ch1_rdma_reload_dis
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[4]	RW	ch5_rdma_reload_dis	Submodule hardware sync mask. This bit must work with ADE_SOFT_RST_SEL. 0: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule reloads programs and starts to work after soft reset. 1: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule does not reload and start to work after soft reset.
[3]	RW	ch4_rdma_reload_dis	Submodule hardware sync mask. This bit must work with ADE_SOFT_RST_SEL. 0: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule reloads programs and starts to work after soft reset. 1: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule does not reload and start to work after soft reset.
[2]	RW	ch3_rdma_reload_dis	Submodule hardware sync mask. This bit must work with ADE_SOFT_RST_SEL. 0: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule reloads programs and starts to work after soft reset. 1: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule does not reload and start to work after soft reset.
[1]	RW	ch2_rdma_reload_dis	Submodule hardware sync mask. This bit must work with ADE_SOFT_RST_SEL. 0: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule reloads programs and starts to work after soft reset. 1: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule does not reload and start to work after soft reset.

Offset Address	Register Name	Total Reset Value
0x00AC	ADE_RELOAD_DIS0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	rot_reload_dis	ctran6_reload_dis	ctran5_reload_dis	ctran4_reload_dis	ctran3_reload_dis	ctran2_reload_dis	ctran1_reload_dis	scl3_reload_dis	scl2_reload_dis	scl1_reload_dis	clip6_reload_dis	clip5_reload_dis	clip4_reload_dis	clip3_reload_dis	clip2_reload_dis	clip1_reload_dis	cmdq_wdma_reload_dis	reserved	ch3_wdma_reload_dis	ch2_wdma_reload_dis	ch1_wdma_reload_dis	reserved	cmdq2_rdma_reload_dis	cmdq1_rdma_reload_dis	disp_rdma_reload_dis	ch6_rdma_reload_dis	ch5_rdma_reload_dis	ch4_rdma_reload_dis	ch3_rdma_reload_dis	ch2_rdma_reload_dis	ch1_rdma_reload_dis
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	ch1_rdma_reload_dis	Submodule hardware sync mask. This bit must work with ADE_SOFT_RST_SEL. 0: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule reloads programs and starts to work after soft reset. 1: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule does not reload and start to work after soft reset.

ADE_RELOAD_DIS1

ADE_RELOAD_DIS1 is submodule hardware sync mask register 1.

Offset Address	Register Name	Total Reset Value
0x00B0	ADE_RELOAD_DIS1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ovly3_reload_dis	ovly2_reload_dis	ovly1_reload_dis	dither_reload_dis	gamma_reload_dis	reserved	cmdq2_reload_dis	cmdq1_reload_dis
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved

Offset Address	Register Name	Total Reset Value
0x00B0	ADE_RELOAD_DIS1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ovly3_reload_dis	ovly2_reload_dis	ovly1_reload_dis	dither_reload_dis	gamma_reload_dis	reserved	cmdq2_reload_dis	cmdq1_reload_dis
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7]	RW	ovly3_reload_dis	Submodule hardware sync mask. This bit must work with ADE_SOFT_RST_SEL. 0: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule reloads programs and starts to work after soft reset. 1: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule does not reload and start to work after soft reset.
[6]	RW	ovly2_reload_dis	Submodule hardware sync mask. This bit must work with ADE_SOFT_RST_SEL. 0: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule reloads programs and starts to work after soft reset. 1: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule does not reload and start to work after soft reset.
[5]	RW	ovly1_reload_dis	Submodule hardware sync mask. This bit must work with ADE_SOFT_RST_SEL. 0: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule reloads programs and starts to work after soft reset. 1: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule does not reload and start to work after soft reset.
[4]	RW	dither_reload_dis	Submodule hardware sync mask. This bit must work with ADE_SOFT_RST_SEL. 0: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule reloads programs and starts to work after soft reset. 1: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule does not reload and start to work after soft reset.
[3]	RW	gamma_reload_dis	Submodule hardware sync mask. This bit must work with ADE_SOFT_RST_SEL. 0: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule reloads programs and starts to work after soft reset. 1: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule does not reload and start to work after soft reset.

Offset Address	Register Name	Total Reset Value
0x00B0	ADE_RELOAD_DIS1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ovly3_reload_dis	ovly2_reload_dis	ovly1_reload_dis	dither_reload_dis	gamma_reload_dis	reserved	cmdq2_reload_dis	cmdq1_reload_dis
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[2]	RO	reserved	Reserved
[1]	RW	cmdq2_reload_dis	Submodule hardware sync mask. This bit must work with ADE_SOFT_RST_SEL. 0: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule reloads programs and starts to work after soft reset. 1: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule does not reload and start to work after soft reset.
[0]	RW	cmdq1_reload_dis	Submodule hardware sync mask. This bit must work with ADE_SOFT_RST_SEL. 0: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule reloads programs and starts to work after soft reset. 1: When the corresponding bit in ADE_SOFT_RST_SEL is 1, the submodule does not reload and start to work after soft reset.

ADE_EN

ADE_EN is an ADE global enable register.

Offset Address	Register Name	Total Reset Value
0x0100	ADE_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															ade_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved

Offset Address	Register Name	Total Reset Value
0x0100	ADE_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															ade_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	ade_en	ADE global enable. Writing any value to this field triggers a Config OK interrupt. 0: disabled 1: enabled

INTR_INIT_STATE_CPU_0

INTR_INIT_STATE_CPU_0 is CPU raw interrupt status register 0.

Offset Address	Register Name	Total Reset Value
0x0C00	INTR_INIT_STATE_CPU_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	intr_init_state_cpu0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	intr_init_state_cpu0	Raw interrupt status reported to the CPU. This field corresponds to interrupt sources 0−31.

INTR_INIT_STATE_CPU_1

INTR_INIT_STATE_CPU_1 is CPU raw interrupt status register 1.

Offset Address	Register Name	Total Reset Value
0x0C04	INTR_INIT_STATE_CPU_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	intr_init_state_cpu1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	intr_init_state_cpu1	Raw interrupt status reported to the CPU. This field corresponds to interrupt sources 32−63.

INTR_MASK_STATE_CPU_0

INTR_MASK_STATE_CPU_0 is CPU masked interrupt status register 0.

Offset Address	Register Name	Total Reset Value
0x0C08	INTR_MASK_STATE_CPU_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	intr_mask_state_cpu0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	intr_mask_state_cpu0	Masked interrupt status reported to the CPU. This field corresponds to interrupt sources 0−31.

INTR_MASK_STATE_CPU_1

INTR_MASK_STATE_CPU_1 is CPU masked interrupt status register 1.

Offset Address	Register Name	Total Reset Value
0x0C0C	INTR_MASK_STATE_CPU_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	intr_mask_state_cpu1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	intr_mask_state_cpu1	Masked interrupt status reported to the CPU. This field corresponds to interrupt sources 32−63.

RD_CH_DISP_PE

RD_CH_DISP_PE is an RD_CH_DISP performance control register.

Offset Address	Register Name	Total Reset Value
0x1400	RD_CH_DISP_PE	0x0300_0777

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				rd_ch_disp_min_burst_len				reserved											rd_ch_disp_qos_cfg	rd_ch_disp_qos_thd				rd_ch_disp_qos_sec				rd_ch_disp_qos			
Reset	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	0	1	1	1

Bits	Access	Name	Description
[31:28]	RW	reserved	Reserved
[27:24]	RW	rd_ch_disp_min_burst_len	Typical burst length
[23:13]	RW	reserved	Reserved
[12]	RW	rd_ch_disp_qos_cfg	QoS configuration mode 0: The QoS is configured by software. 1: The QoS is configured based on the threshold of the lower-level buffer.
[11:8]	RW	rd_ch_disp_qos_thd	QoS value of threshold area 3 of the lower-level buffer (the maximum value is 7 and the upper bits are reserved)
[7:4]	RW	rd_ch_disp_qos_sec	QoS value of threshold area 2 of the lower-level buffer (the maximum value is 7 and the upper bits are reserved)
[3:0]	RW	rd_ch_disp_qos	rd_ch_disp_qos_cfg = 0: QoS value of the TX operation of the current channel rd_ch_disp_qos_cfg = 1: QoS value of threshold area 1 of the lower-level buffer (the maximum value is 7 and the upper bits are reserved)

RD_CH_DISP_CTRL

RD_CH_DISP_CTRL is an RD_CH_DISP channel control register.

Offset Address	Register Name	Total Reset Value
0x1404	RD_CH_DISP_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				reserved				reserved				rd_ch_disp_format				reserved										rd_ch_disp_fsh_int_disable	rd_ch_disp_axi_fsh_int_disable	rd_ch_disp_rd_dir	rd_ch_disp_partial				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:24]	RO	reserved	Reserved
[23:21]	RO	reserved	Reserved
[20:16]	RW	rd_ch_disp_format	Data format 00000: RGB565 00001: BGR565 00010: XRGB8888 00011: XBGR8888 00100: ARGB8888 00101: ABGR8888 00110: RGBA8888 00111: BGRA8888 01000: RGB888 01001: BGR888 01010−01111: reserved 10000: YUYV 10001: YVYU 10010: UYVY 10011: VYUY 10100: YUV444 10101−11111: reserved
[15:6]	RO	reserved	Reserved

Offset Address	Register Name	Total Reset Value
0x1404	RD_CH_DISP_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				reserved				reserved				rd_ch_disp_format				reserved										rd_ch_disp_fsh_int_disable		rd_ch_disp_axi_fsh_int_disable		rd_ch_disp_rd_dir		rd_ch_disp_partial	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[5]	RW	rd_ch_disp_fsh_int_disable	DMA channel completion interrupt mask 0: The interrupt is not masked when 0 is written. 1: The interrupt is masked when 1 is written.
[4]	RW	rd_ch_disp_axi_fsh_int_disable	DMA channel AXI completion interrupt mask 0: The interrupt is not masked when 0 is written. 1: The interrupt is masked when 1 is written.
[3:2]	RW	rd_ch_disp_rd_dir	Data block read direction after secondary division 00: start from the upper left data block 01: start from the lower left data block 10: start from the upper right data block 11: start from the lower right data block
[1:0]	RW	rd_ch_disp_partial	Division mode 00: non-secondary division 01: secondary division (horizontal and then vertical) 10: secondary division (vertical and then horizontal) 11: reserved

RD_CH_DISP_ADDR

RD_CH_DISP_ADDR is an RD_CH_DISP data block start address register.

Offset Address	Register Name	Total Reset Value
0x1408	RD_CH_DISP_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rd_ch_disp_start_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	rd_ch_disp_start_addr	Start address (in byte) for the data block

RD_CH_DISP_SIZE

RD_CH_DISP_SIZE is an RD_CH_DISP data block size register.

Offset Address	Register Name	Total Reset Value
0x140C	RD_CH_DISP_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rd_ch_disp_height																rd_ch_disp_width															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	rd_ch_disp_height	Data block height (in line)
[15:0]	RW	rd_ch_disp_width	Data block width (in byte)

RD_CH_DISP_STRIDE

RD_CH_DISP_STRIDE is an RD_CH_DISP data block stride register.

Offset Address	Register Name	Total Reset Value
0x1410	RD_CH_DISP_STRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															rd_ch_disp_stride_dir	rd_ch_disp_stride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	RW	rd_ch_disp_stride_dir	Stride sign bit 0: positive 1: negative
[15:0]	RW	rd_ch_disp_stride	Distance (in byte) between the start points of two scanning lines

RD_CH_DISP_SPACE

RD_CH_DISP_SPACE is an RD_CH_DISP data block space size register.

Offset Address	Register Name	Total Reset Value
0x1414	RD_CH_DISP_SPACE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rd_ch_disp_space																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	rd_ch_disp_space	Offset (in byte) of the lower left corner of the data block = rd_chx_height x Stride If rd_chx_height is 0, the offset is set to 0.

RD_CH_DISP_BLANK_OFFSET

RD_CH_DISP_BLANK_OFFSET is an RD_CH_DISP blank data block offset register.

Offset Address	Register Name	Total Reset Value
0x1420	RD_CH_DISP_BLANK_OFFSET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rd_ch_disp_blank_offset_height																rd_ch_disp_blank_offset_width															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	rd_ch_disp_blank_offset_height	Height offset (in line) of the blank data block
[15:0]	RW	rd_ch_disp_blank_offset_width	Width offset (in byte) of the blank data block

RD_CH_DISP_BLANK_SIZE

RD_CH_DISP_BLANK_SIZE is an RD_CH_DISP blank data block size register.

Offset Address	Register Name	Total Reset Value
0x1424	RD_CH_DISP_BLANK_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rd_ch_disp_blank_height																rd_ch_disp_blank_width															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	rd_ch_disp_blank_height	Height (in line) of the blank data block
[15:0]	RW	rd_ch_disp_blank_width	Width (in byte) of the blank data block

RD_CH_DISP_BLANK_SPACE

RD_CH_DISP_BLANK_SPACE is an RD_CH_DISP blank data block space size register.

Offset Address	Register Name	Total Reset Value
0x1428	RD_CH_DISP_BLANK_SPACE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rd_ch_disp_blank_space																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	rd_ch_disp_blank_	Size (in byte) of the data block space = blank_height x Stride

Offset Address	Register Name	Total Reset Value
0x1428	RD_CH_DISP_BLANK_SPACE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rd_ch_disp_blank_space																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
		space	

RD_CH_DISP_EN

RD_CH_DISP_EN is an RD_CH_DISP enable register.

Offset Address	Register Name	Total Reset Value
0x142C	RD_CH_DISP_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															rd_ch_disp_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	rd_ch_disp_en	DMA channel enable 0: Writing 0 has no effect. 1: Writing 1 enables the channel.

RD_CH_DISP_STATUS

RD_CH_DISP_STATUS is an RD_CH_DISP working status register.

Offset Address	Register Name	Total Reset Value
0x1430	RD_CH_DISP_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														rd_ch_disp_status	rd_ch_disp_axi_status
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RO	rd_ch_disp_status	DMA channel status 0: After the DMA channel transfers data, the AXI interface and buffer are idle. 1: When the DMA channel is transferring data, the AXI interface or buffer is working.
[0]	RO	rd_ch_disp_axi_status	DMA channel AXI interface status 0: After the DMA channel transfers data, the AXI interface is idle. 1: When the DMA channel is transferring data, the AXI interface is working.

ADE_CTRAN5_DIS

ADE_CTRAN5_DIS is a **CTRAN5 CSC bypass register.**

Offset Address	Register Name	Total Reset Value
0x5404	ADE_CTRAN5_DIS	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															ctran_bypass
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	ctran_bypass	CSC bypass 1: bypassed 0: not bypassed (working)

ADE_CTRAN5_MODE_CHOOSE

ADE_CTRAN5_MODE_CHOOSE is a CTRAN5 mode control register.

Offset Address	Register Name	Total Reset Value
0x5408	ADE_CTRAN5_MODE_CHOOSE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														ctran_mode	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1:0]	RW	ctran_mode	CTRAN5 working mode 0: YUV444 —> ARGB8888 1: ARGB8888 —> YUV422 2: ARGB8888 —> YUV444 3: ARGB8888 —> ARGB8888

ADE_CTRAN5_STAT

ADE_CTRAN5_STAT is a CTRAN5 status register.

Offset Address	Register Name	Total Reset Value
0x540C	ADE_CTRAN5_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															ctran_idle_indicate
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RO	ctran_idle_indicate	CTRAN5 status 1: idle 0: busy

ADE_CTRAN5_CHDC0

ADE_CTRAN5_CHDC0 is CTRAN5 transform constant register 0.

Offset Address	Register Name	Total Reset Value
0x5410	ADE_CTRAN5_CHDC0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								ch0dc1								reserved								ch0dc0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24:16]	RW	ch0dc1	Transform constant 1 of channel 0 This 9-bit constant is a signed number and is expressed by two's complement.
[15:9]	RO	reserved	Reserved
[8:0]	RW	ch0dc0	Transform constant 0 of channel 0 This 9-bit constant is a signed number and is expressed by two's

Offset Address	Register Name	Total Reset Value
0x5410	ADE_CTRAN5_CHDC0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								ch0dc1								reserved								ch0dc0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
			complement.

ADE_CTRAN5_CHDC1

ADE_CTRAN5_CHDC1 is CTRAN5 transform constant register 1.

Offset Address	Register Name	Total Reset Value
0x5414	ADE_CTRAN5_CHDC1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								ch0dc3								reserved								ch0dc2							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24:16]	RW	ch0dc3	Transform constant 3 of channel 0 This 9-bit constant is a signed number and is expressed by two's complement.
[15:9]	RO	reserved	Reserved
[8:0]	RW	ch0dc2	Transform constant 2 of channel 0 This 9-bit constant is a signed number and is expressed by two's complement.

ADE_CTRAN5_CHDC2

ADE_CTRAN5_CHDC2 is CTRAN5 transform constant register 2.

Offset Address	Register Name	Total Reset Value
0x5418	ADE_CTRAN5_CHDC2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								ch1dc1								reserved								ch1dc0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24:16]	RW	ch1dc1	Transform constant 1 of channel 1 This 9-bit constant is a signed number and is expressed by two's complement.
[15:9]	RO	reserved	Reserved
[8:0]	RW	ch1dc0	Transform constant 0 of channel 1 This 9-bit constant is a signed number and is expressed by two's complement.

ADE_CTRAN5_CHDC3

ADE_CTRAN5_CHDC3 is CTRAN5 transform constant register 3.

Offset Address	Register Name	Total Reset Value
0x541C	ADE_CTRAN5_CHDC3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								ch1dc3								reserved								ch1dc2							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24:16]	RW	ch1dc3	Transform constant 3 of channel 1 This 9-bit constant is a signed number and is expressed by two's complement.
[15:9]	RO	reserved	Reserved
[8:0]	RW	ch1dc2	Transform constant 2 of channel 1 This 9-bit constant is a signed number and is expressed by two's complement.

ADE_CTRAN5_CHDC4

ADE_CTRAN5_CHDC4 is CTRAN5 transform constant register 4.

Offset Address	Register Name	Total Reset Value
0x5420	ADE_CTRAN5_CHDC4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								ch2dc1								reserved								ch2dc0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24:16]	RW	ch2dc1	Transform constant 1 of channel 2 This 9-bit constant is a signed number and is expressed by two's complement.
[15:9]	RO	reserved	Reserved
[8:0]	RW	ch2dc0	Transform constant 0 of channel 2 This 9-bit constant is a signed number and is expressed by two's complement.

ADE_CTRAN5_CHDC5

ADE_CTRAN5_CHDC5 is CTRAN5 transform constant register 5.

Offset Address	Register Name	Total Reset Value
0x5424	ADE_CTRAN5_CHDC5	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								ch2dc3								reserved								ch2dc2							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24:16]	RW	ch2dc3	Transform constant 3 of channel 2 This 9-bit constant is a signed number and is expressed by two's complement.
[15:9]	RO	reserved	Reserved
[8:0]	RW	ch2dc2	Transform constant 2 of channel 2 This 9-bit constant is a signed number and is expressed by two's complement.

ADE_CTRAN5_CSC0

ADE_CTRAN5_CSC0 is CTRAN5 transform coefficient register 0.

Offset Address	Register Name	Total Reset Value
0x5428	ADE_CTRAN5_CSC0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				csc01												reserved				csc00											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	csc01	Channel transform coefficient 01 This 13-bit coefficient is a signed number and is expressed by two's complement.
[15:13]	RO	reserved	Reserved
[12:0]	RW	csc00	Channel transform coefficient 00 This 13-bit coefficient is a signed number and is expressed by two's complement.

ADE_CTRAN5_CSC1

ADE_CTRAN5_CSC1 is CTRAN5 transform coefficient register 1.

Offset Address	Register Name	Total Reset Value
0x542C	ADE_CTRAN5_CSC1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				csc10												reserved				csc02											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	csc10	Channel transform coefficient 10 This 13-bit coefficient is a signed number and is expressed by two's complement.
[15:13]	RO	reserved	Reserved

Offset Address	Register Name	Total Reset Value
0x542C	ADE_CTRAN5_CSC1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				csc10												reserved				csc02											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[12:0]	RW	csc02	Channel transform coefficient 02 This 13-bit coefficient is a signed number and is expressed by two's complement.

ADE_CTRAN5_CSC2

ADE_CTRAN5_CSC2 is CTRAN5 transform coefficient register 2.

Offset Address	Register Name	Total Reset Value
0x5430	ADE_CTRAN5_CSC2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				csc12												reserved				csc11											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	csc12	Channel transform coefficient 12 This 13-bit coefficient is a signed number and is expressed by two's complement.
[15:13]	RO	reserved	Reserved
[12:0]	RW	csc11	Channel transform coefficient 11 This 13-bit coefficient is a signed number and is expressed by two's complement.

ADE_CTRAN5_CSC3

ADE_CTRAN5_CSC3 is CTRAN5 transform coefficient register 3.

Offset Address	Register Name	Total Reset Value
0x5434	ADE_CTRAN5_CSC3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				csc21												reserved				csc20											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	csc21	Channel transform coefficient 21 This 13-bit coefficient is a signed number and is expressed by two's complement.
[15:13]	RO	reserved	Reserved
[12:0]	RW	csc20	Channel transform coefficient 20 This 13-bit coefficient is a signed number and is expressed by two's complement.

ADE_CTRAN5_CSC4

ADE_CTRAN5_CSC4 is CTRAN5 transform coefficient register 4.

Offset Address	Register Name	Total Reset Value
0x5438	ADE_CTRAN5_CSC4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				csc22											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12:0]	RW	csc22	Channel transform coefficient 22 This 13-bit coefficient is a signed number and is expressed by two's complement.

ADE_CTRAN5_IMAGE_SIZE

ADE_CTRAN5_IMAGE_SIZE is a CTRAN5 image size register.

Offset Address	Register Name	Total Reset Value
0x543C	ADE_CTRAN5_IMAGE_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												image_size																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved
[21:0]	RW	image_size	Number of image pixels. The value is a 22-bit unsigned number and is expressed by two's complement. Note: The configured value is the actual value minus 1. For example, if an image has 80 pixels, the configured value is 79 pixels. When the ARGB888 format is converted into the YUV422 format, the number of pixels must be an even number. When the YUV444 format is converted into the ARGB888 format, there is no such restriction.

ADE_CTRAN5_CFG_OK

ADE_CTRAN5_CFG_OK is a CTRAN5 configuration completion indicator register.

Offset Address	Register Name	Total Reset Value
0x5440	ADE_CTRAN5_CFG_OK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															ctran_cfg_ok
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	ctran_cfg_ok	CTRAN5 register configuration completion indicator

ADE_CTRAN6_DIS

ADE_CTRAN6_DIS is a **CTRAN6 CSC bypass register.**

Offset Address	Register Name	Total Reset Value
0x5504	ADE_CTRAN6_DIS	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														ctran_bypass	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	ctran_bypass	CSC bypass 1: bypassed 0: not bypassed (working)

ADE_CTRAN6_MODE_CHOOSE

ADE_CTRAN6_MODE_CHOOSE is a CTRAN6 mode control register.

Offset Address	Register Name	Total Reset Value
0x5508	ADE_CTRAN6_MODE_CHOOSE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														ctran_mode	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1:0]	RW	ctran_mode	CTRAN6 working mode 0: YUV444 —> ARGB8888 1: ARGB8888 —> YUV422 2: ARGB8888 —> YUV444 3: ARGB8888 —> ARGB8888

ADE_CTRAN6_STAT

ADE_CTRAN6_STAT is a CTRAN6 status register.

Offset Address	Register Name	Total Reset Value
0x550C	ADE_CTRAN6_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															ctran_idle_indicate
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RO	ctran_idle_indicate	CTRAN6 status 1: idle 0: busy

ADE_CTRAN6_CHDC0

ADE_CTRAN6_CHDC0 is CTRAN6 transform constant register 0.

Offset Address	Register Name	Total Reset Value
0x5510	ADE_CTRAN6_CHDC0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								ch0dc1								reserved								ch0dc0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24:16]	RW	ch0dc1	Transform constant 1 of channel 0 This 9-bit constant is a signed number and is expressed by two's complement.
[15:9]	RO	reserved	Reserved
[8:0]	RW	ch0dc0	Transform constant 0 of channel 0 This 9-bit constant is a signed number and is expressed by two's

Offset Address	Register Name	Total Reset Value
0x5510	ADE_CTRAN6_CHDC0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								ch0dc1								reserved								ch0dc0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
			complement.

ADE_CTRAN6_CHDC1

ADE_CTRAN6_CHDC1 is CTRAN6 transform constant register 1

Offset Address	Register Name	Total Reset Value
0x5514	ADE_CTRAN6_CHDC1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								ch0dc3								reserved								ch0dc2							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24:16]	RW	ch0dc3	Transform constant 3 of channel 0 This 9-bit constant is a signed number and is expressed by two's complement.
[15:9]	RO	reserved	Reserved
[8:0]	RW	ch0dc2	Transform constant 2 of channel 0 This 9-bit constant is a signed number and is expressed by two's complement.

ADE_CTRAN6_CHDC2

ADE_CTRAN6_CHDC2 is CTRAN6 transform constant register 2

Offset Address	Register Name	Total Reset Value
0x5518	ADE_CTRAN6_CHDC2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								ch1dc1								reserved								ch1dc0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24:16]	RW	ch1dc1	Transform constant 1 of channel 1 This 9-bit constant is a signed number and is expressed by two's complement.
[15:9]	RO	reserved	Reserved
[8:0]	RW	ch1dc0	Transform constant 0 of channel 1 This 9-bit constant is a signed number and is expressed by two's complement.

ADE_CTRAN6_CHDC3

ADE_CTRAN6_CHDC3 is CTRAN6 transform constant register 3

Offset Address	Register Name	Total Reset Value
0x551C	ADE_CTRAN6_CHDC3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								ch1dc3								reserved								ch1dc2							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24:16]	RW	ch1dc3	Transform constant 3 of channel 1 This 9-bit constant is a signed number and is expressed by two's complement.
[15:9]	RO	reserved	Reserved
[8:0]	RW	ch1dc2	Transform constant 2 of channel 1 This 9-bit constant is a signed number and is expressed by two's complement.

ADE_CTRAN6_CHDC4

ADE_CTRAN6_CHDC4 is CTRAN6 transform constant register 4

Offset Address	Register Name	Total Reset Value
0x5520	ADE_CTRAN6_CHDC4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								ch2dc1								reserved								ch2dc0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24:16]	RW	ch2dc1	Transform constant 1 of channel 2 This 9-bit constant is a signed number and is expressed by two's complement.
[15:9]	RO	reserved	Reserved
[8:0]	RW	ch2dc0	Transform constant 0 of channel 2 This 9-bit constant is a signed number and is expressed by two's complement.

ADE_CTRAN6_CHDC5

ADE_CTRAN6_CHDC5 is CTRAN6 transform constant register 5

Offset Address	Register Name	Total Reset Value
0x5524	ADE_CTRAN6_CHDC5	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								ch2dc3								reserved								ch2dc2							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24:16]	RW	ch2dc3	Transform constant 3 of channel 2 This 9-bit constant is a signed number and is expressed by two's complement.
[15:9]	RO	reserved	Reserved
[8:0]	RW	ch2dc2	Transform constant 2 of channel 2 This 9-bit constant is a signed number and is expressed by two's complement.

ADE_CTRAN6_CSC0

ADE_CTRAN6_CSC0 is CTRAN6 transform coefficient register 0.

Offset Address	Register Name	Total Reset Value
0x5528	ADE_CTRAN6_CSC0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				csc01												reserved				csc00											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	csc01	Channel transform coefficient 01 This 13-bit coefficient is a signed number and is expressed by two's complement.
[15:13]	RO	reserved	Reserved
[12:0]	RW	csc00	Channel transform coefficient 00 This 13-bit coefficient is a signed number and is expressed by two's complement.

ADE_CTRAN6_CSC1

ADE_CTRAN6_CSC1 is CTRAN6 transform coefficient register 1.

Offset Address	Register Name	Total Reset Value
0x552C	ADE_CTRAN6_CSC1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				csc10												reserved				csc02											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	csc10	Channel transform coefficient 10 This 13-bit coefficient is a signed number and is expressed by two's complement.
[15:13]	RO	reserved	Reserved

Offset Address	Register Name	Total Reset Value
0x552C	ADE_CTRAN6_CSC1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				csc10												reserved				csc02											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[12:0]	RW	csc02	Channel transform coefficient 02 This 13-bit coefficient is a signed number and is expressed by two's complement.

ADE_CTRAN6_CSC2

ADE_CTRAN6_CSC2 is CTRAN6 transform coefficient register 2.

Offset Address	Register Name	Total Reset Value
0x5530	ADE_CTRAN6_CSC2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				csc12												reserved				csc11											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	csc12	Channel transform coefficient 12 This 13-bit coefficient is a signed number and is expressed by two's complement.
[15:13]	RO	reserved	Reserved
[12:0]	RW	csc11	Channel transform coefficient 11 This 13-bit coefficient is a signed number and is expressed by two's complement.

ADE_CTRAN6_CSC3

ADE_CTRAN6_CSC3 is CTRAN6 transform coefficient register 3.

Offset Address	Register Name	Total Reset Value
0x5534	ADE_CTRAN6_CSC3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				csc21												reserved				csc20											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	csc21	Channel transform coefficient 21 This 13-bit coefficient is a signed number and is expressed by two's complement.
[15:13]	RO	reserved	Reserved
[12:0]	RW	csc20	Channel transform coefficient 20 This 13-bit coefficient is a signed number and is expressed by two's complement.

ADE_CTRAN6_CSC4

ADE_CTRAN6_CSC4 is CTRAN6 transform coefficient register 4.

Offset Address	Register Name	Total Reset Value
0x5538	ADE_CTRAN6_CSC4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				csc22											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12:0]	RW	csc22	Channel transform coefficient 22 This 13-bit coefficient is a signed number and is expressed by two's complement.

ADE_CTRAN6_IMAGE_SIZE

ADE_CTRAN6_IMAGE_SIZE is a CTRAN6 image size register.

Offset Address	Register Name	Total Reset Value
0x553C	ADE_CTRAN6_IMAGE_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												image_size																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved
[21:0]	RW	image_size	Number of image pixels. The value is a 22-bit unsigned number and is expressed by two's complement. Note: The configured value is the actual value minus 1. For example, if an image has 80 pixels, the configured value is 79 pixels. When the ARGB888 format is converted into the YUV422 format, the number of pixels must be an even number. When the YUV444 format is converted into the ARGB888 format, there is no such restriction.

ADE_CTRAN6_CFG_OK

ADE_CTRAN6_CFG_OK is a CTRAN6 configuration completion indicator register.

Offset Address	Register Name	Total Reset Value
0x5540	ADE_CTRAN6_CFG_OK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															ctran_cfg_ok
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	ctran_cfg_ok	CTRAN6 register configuration completion indicator

LDI_HRZ_CTRL0

LDI_HRZ_CTRL0 is LDI horizontal scanning control register 0.

Offset Address	Register Name	Total Reset Value
0x7400	LDI_HRZ_CTRL0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hbp												reserved								hfp											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RW	hbp	Horizontal back porch (HBP). Its value range is 0–4095.
[19:12]	RO	reserved	Reserved
[11:0]	RW	hfp	Horizontal front porch (HFP). Its value range is 0–4095. The HFP indicates the number of pixel clocks in the period from the end of a line of valid data to the valid horizontal sync signal ldi_hsync.

LDI_HRZ_CTRL1

LDI_HRZ_CTRL1 is LDI horizontal scanning control register 1.

Offset Address	Register Name	Total Reset Value
0x7404	LDI_HRZ_CTRL1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				hsw											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	hsw	Horizontal sync width (HSW). The configured value is the actual width minus 1. The unit of the HSW is pixel clock, and its value range is 1−4096.

LDI_VRT_CTRL0

LDI_VRT_CTRL0 is LDI vertical scanning control register 0.

Offset Address	Register Name	Total Reset Value
0x7408	LDI_VRT_CTRL0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vbp												reserved								vfp											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RW	vbp	Vertical back porch (VBP). Its value range is 0−4095. The VBP indicates the number of scanned blanking lines in the period from the invalid frame sync signal ldi_vsync to the start of a frame of valid data.
[19:12]	RO	reserved	Reserved
[11:0]	RW	vfp	Vertical front porch (VFP). Its value range is 0−4095. The VFP indicates the number of scanned blanking lines in the period from the end of valid data to the valid frame sync signal ldi_vsync.

LDI_VRT_CTRL1

LDI_VRT_CTRL1 is LDI vertical scanning control register 1.

Offset Address	Register Name	Total Reset Value
0x740C	LDI_VRT_CTRL1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				vsw											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	vsw	Vertical sync width (VSW). The configured value is the actual width minus 1. The unit of the VSW is scanned line, and its value range is 1−4096.

LDI_PLR_CTRL

LDI_PLR_CTRL is an LDI signal polarity control register.

Offset Address	Register Name	Total Reset Value
0x7410	LDI_PLR_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												data_en_plr	pixel_clk_plr	hsync_plr	vsync_plr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RW	data_en_plr	Polarity of the data valid signal ldi_data_en_o 0: active high 1: active low
[2]	RW	pixel_clk_plr	Polarity of the pixel clock ldi_pixel_clk 0: active at the rising edge 1: active at the falling edge
[1]	RW	hsync_plr	Polarity of the horizontal sync signal ldi_hsync_o 0: active high 1: active low
[0]	RW	vsync_plr	Polarity of the vertical sync signal ldi_vsync_o 0: active high 1: active low

LDI_DSP_SIZE

LDI_DSP_SIZE is an LDI display size register.

Offset Address	Register Name	Total Reset Value
0x7414	LDI_DSP_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vsize												reserved								hsize											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RW	vsize	Number of vertical pixels of the display. The configured value is the number of actual pixels minus 1, and the value range is 1−4096.

[19:12]	RO	reserved	Reserved
[11:0]	RW	hsize	Number of horizontal pixels of the display. The configured value is the number of actual pixels minus 1, and the value range is 1−4096.

LDI_3D_CTRL

LDI_3D_CTRL is an LDI 3D display control register.

Offset Address	Register Name	Total Reset Value
0x7418	LDI_3D_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				active_space											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	active_space	Active space between frames. Its value range is 0−4095. The active space applies only to the frame by frame format of the 3D display, and its unit is scanned line.

LDI_INT_EN

LDI_INT_EN is an LDI interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x741C	LDI_INT_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vactive_line_int_en	dsi_te1_pin_int_en	dsi_te0_pin_int_en	dsi_te_tri_int_en	vfrontporch_end_int_en	vactive1_end_int_en	vactive1_start_int_en	vactive0_end_int_en	vactive0_start_int_en	vbackporch_int_en	vfrontporch_int_en	vsync_int_en	edc_afifo_underflow_int_en	frame_end_int_en	frame_start_int_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved
[14]	RW	vactive_line_int_en	Specific line interrupt enable for frame valid data 0: masked 1: enabled
[13]	RW	dsi_te1_pin_int_en	Tearing effect pin TE1 interrupt enable 0: masked 1: enabled
[12]	RW	dsi_te0_pin_int_en	Tearing effect pin TE0 interrupt enable 0: masked 1: enabled
[11]	RW	dsi_te_tri_int_en	Tearing effect trigger interrupt enable 0: masked 1: enabled
[10]	RW	vfrontporch_end_int_en	VFP end interrupt enable 0: masked 1: enabled
[9]	RW	vactive1_end_int_en	Valid data end interrupt enable for the right eye frame (applicable only to the 3D mode) 0: masked 1: enabled

Offset Address	Register Name	Total Reset Value
0x741C	LDI_INT_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vactive_line_int_en	dsi_te1_pin_int_en	dsi_te0_pin_int_en	dsi_te_tri_int_en	vfrontporch_end_int_en	vactive1_end_int_en	vactive1_start_int_en	vactive0_end_int_en	vactive0_start_int_en	vbackporch_int_en	vfrontporch_int_en	vsync_int_en	edc_afifo_underflow_int_en	frame_end_int_en	frame_start_int_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[8]	RW	vactive1_start_int_en	Valid data start interrupt enable for the right eye frame (applicable only to the 3D mode) 0: masked 1: enabled
[7]	RW	vactive0_end_int_en	Frame valid data end interrupt enable (2D mode) or valid data end interrupt enable for the left eye frame (3D mode) 0: masked 1: enabled
[6]	RW	vactive0_start_int_en	Frame valid data start interrupt enable (2D mode) or valid data start interrupt enable for the left eye frame (3D mode) 0: masked 1: enabled
[5]	RW	vbackporch_int_en	VBP start interrupt enable 0: masked 1: enabled
[4]	RW	vfrontporch_int_en	VFP start interrupt enable 0: masked 1: enabled
[3]	RW	vsync_int_en	Vertical sync start interrupt enable 0: masked 1: enabled

Offset Address	Register Name	Total Reset Value
0x741C	LDI_INT_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vactive_line_int_en	dsi_te1_pin_int_en	dsi_te0_pin_int_en	dsi_te_tri_int_en	vfrontporch_end_int_en	vactive1_end_int_en	vactive1_start_int_en	vactive0_end_int_en	vactive0_start_int_en	vbackporch_int_en	vfrontporch_int_en	vsync_int_en	edc_afifo_underflow_int_en	frame_end_int_en	frame_start_int_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[2]	RW	edc_afifo_underflow_int_en	Comparison interrupt enable 0: masked 1: enabled
[1]	RW	frame_end_int_en	Frame end interrupt enable 0: masked 1: enabled
[0]	RW	frame_start_int_en	Frame start interrupt enable 0: masked 1: enabled

LDI_CTRL

LDI_CTRL is an LDI control register.

Offset Address	Register Name	Total Reset Value
0x7420	LDI_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved			ldi_en_self_clr	vactive_line												shutdown	color_mode	bgr	corlorbar_width					wait_vsync_en	bpp		date_gate_en	disp_mode_buf	ldi_en	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28]	RW	ldi_en_self_clr	LDI_EN self-clear enable 0: disabled 1: enabled. The LDI automatically stops after a frame is displayed.
[27:16]	RW	vactive_line	Number of specific Vactive lines. The minimum value is 0, and the maximum value is the LCD height minus 1. If the number of scanned lines reaches the value in the Vactive period, a vactive_line_int interrupt is triggered.
[15]	RW	shutdown	Shutdown signal of the DSI DPI interface 0: The LCD works properly. 1: The LCD enters the sleep mode.
[14]	RW	color_mode	Color mode of the DSI DPI interface 0: full color mode 1: reduced color mode
[13]	RW	bgr	RGB output format 0: common RGB output format 1: BGR output format (the B and R components are exchanged)
[12:6]	RW	corlorbar_width	RGB color bar width. The configured value is the number of actual width minus 1, and the value range is 1−128.
[5]	RW	wait_vsync_en	Wait ldi_vsync_other enable 0: disabled 1: enabled
[4:3]	RW	bpp	Input pixel format 00: RGB565 01: RGB666 10: RGB888 11: reserved

Offset Address	Register Name	Total Reset Value
0x7420	LDI_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved			ldi_en_self_clr	vactive_line												shutdown	color_mode	bgr	corlorbar_width					wait_vsync_en	bpp			date_gate_en	disp_mode_buf	ldi_en	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[2]	RW	date_gate_en	Data valid signal gating enable 0: disabled 1: enabled
[1]	RW	disp_mode_buf	Display mode 0: 2D display mode or non-frame by frame mode during 3D displaying (default value) 1: 3D frame by frame mode
[0]	RW	ldi_en	LDI enable

LDI_ORG_INT

LDI_ORG_INT is an LDI raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x7424	LDI_ORG_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vactive_line_int	dsi_te1_pin_int	dsi_te0_pin_int	dsi_te_tri_int	vfrontporch_end_int	vactive1_end_int	vactive1_start_int	vactive0_end_int	vactive0_start_int	vbackporch_int	vfrontporch_int	vsync_int	edc_afifo_underflow_int	frame_end_int	frame_start_int
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved
[14]	RO	vactive_line_int	Raw status of the specific line interrupt of frame valid data This bit is not masked by the interrupt enable bit. When the number of scanned lines reaches the number of specific Vactive lines, this bit is set to 1.
[13]	RO	dsi_te1_pin_int	Raw status of the tearing effect pin TE1 interrupt This bit is not masked by the interrupt enable bit. When the TE1 pin detects a valid tearing effect signal, this bit is set to 1.
[12]	RO	dsi_te0_pin_int	Raw status of the tearing effect pin TE0 interrupt This bit is not masked by the interrupt enable bit. When the TE0 pin detects a valid tearing effect signal, this bit is set to 1.
[11]	RO	dsi_te_tri_int	Raw status of the tearing effect trigger interrupt This bit is not masked by the interrupt enable bit. When the DSI host receives a tearing effect trigger signal and sends an indicator to the LDI, this bit is set to 1.
[10]	RO	vfrontporch_end_int	Raw status of the VFP end interrupt This bit is not masked by the interrupt enable bit. When the VBP ends, this bit is set to 1.
[9]	RO	vactive1_end_int	Raw status of the valid data end interrupt of the right eye frame (applicable only to the 3D mode) This bit is not masked by the interrupt enable bit. When the valid data of the right eye frame ends, this bit is set to 1.
[8]	RO	vactive1_start_int	Raw status of the valid data start interrupt of the right eye frame (applicable only to the 3D mode) This bit is not masked by the interrupt enable bit. When the valid data of the right eye frame starts, this bit is set to 1.

Offset Address	Register Name	Total Reset Value
0x7424	LDI_ORG_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vactive_line_int	dsi_te1_pin_int	dsi_te0_pin_int	dsi_te_tri_int	vfrontporch_end_int	vactive1_end_int	vactive1_start_int	vactive0_end_int	vactive0_start_int	vbackporch_int	vfrontporch_int	vsync_int	edc_afifo_underflow_int	frame_end_int	frame_start_int
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7]	RO	vactive0_end_int	Raw status of the frame valid data end interrupt (2D mode) or raw status of the valid data end interrupt of the left eye frame (3D mode) This bit is not masked by the interrupt enable bit. When the frame valid data ends, this bit is set to 1.
[6]	RO	vactive0_start_int	Raw status of the frame valid data start interrupt (2D mode) or raw status of the valid data start interrupt of the left eye frame (3D mode) This bit is not masked by the interrupt enable bit. When the frame valid data starts, this bit is set to 1.
[5]	RO	vbackporch_int	Raw status of the VBP last line start interrupt This bit is not masked by the interrupt enable bit. When the VFP starts, this bit is set to 1.
[4]	RO	vfrontporch_int	Raw status of the VFP start interrupt This bit is not masked by the interrupt enable bit. When the VBP starts, this bit is set to 1.
[3]	RO	vsync_int	Raw status of the vertical sync start interrupt This bit is not masked by the interrupt enable bit. When frame sync starts, this bit is set to 1.
[2]	RO	edc_afifo_underflow_int	Raw status of the AFIFO underflow interrupt This bit is not masked by the interrupt enable bit. When the AFIFO underflows, this bit is set to 1.
[1]	RO	frame_end_int	Raw status of the frame end interrupt This bit is not masked by the interrupt enable bit. When the frame ends, this bit is set to 1.

Offset Address	Register Name	Total Reset Value
0x7424	LDI_ORG_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vactive_line_int	dsi_te1_pin_int	dsi_te0_pin_int	dsi_te_tri_int	vfrontporch_end_int	vactive1_end_int	vactive1_start_int	vactive0_end_int	vactive0_start_int	vbackporch_int	vfrontporch_int	vsync_int	edc_afifo_underflow_int	frame_end_int	frame_start_int
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RO	frame_start_int	Raw status of the frame start interrupt This bit is not masked by the interrupt enable bit. When the frame starts, this bit is set to 1.

LDI_MSK_INT

LDI_MSK_INT is an LDI masked interrupt status register.

Offset Address	Register Name	Total Reset Value
0x7428	LDI_MSK_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vactive_line_int	dsi_te1_pin_int	dsi_te0_pin_int	dsi_te_tri_int	vfrontporch_end_int	vactive1_end_int	vactive1_start_int	vactive0_end_int	vactive0_start_int	vbackport_int	vfrontporch_int	vsync_int	edc_afifo_underflow_int	frame_end_int	frame_start_int
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved
[14]	RO	vactive_line_int	Masked status of the specific line interrupt of frame valid data

Offset Address	Register Name	Total Reset Value
0x7428	LDI_MSK_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vactive_line_int	dsi_te1_pin_int	dsi_te0_pin_int	dsi_te_tri_int	vfrontporch_end_int	vactive1_end_int	vactive1_start_int	vactive0_end_int	vactive0_start_int	vbackport_int	vfrontporch_int	vsync_int	edc_afifo_underflow_int	frame_end_int	frame_start_int
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[13]	RO	dsi_te1_pin_int	Raw status of the tearing effect pin TE1 interrupt
[12]	RO	dsi_te0_pin_int	Raw status of the tearing effect pin TE0 interrupt
[11]	RO	dsi_te_tri_int	Raw status of the tearing effect trigger interrupt
[10]	RO	vfrontporch_end_int	Raw status of the VFP end interrupt
[9]	RO	vactive1_end_int	Masked status of the valid data end interrupt of the right eye frame (applicable only to the 3D mode)
[8]	RO	vactive1_start_int	Masked status of the valid data start interrupt of the right eye frame (applicable only to the 3D mode)
[7]	RO	vactive0_end_int	Masked status of the frame valid data end interrupt (2D mode) or masked status of the valid data end interrupt of the left eye frame (3D mode)
[6]	RO	vactive0_start_int	Masked status of the frame valid data start interrupt (2D mode) or masked status of the valid data start interrupt of the left eye frame (3D mode)
[5]	RO	vbackport_int	Masked status of the VBP last line start interrupt
[4]	RO	vfrontporch_int	Masked status of the VFP start interrupt
[3]	RO	vsync_int	Masked status of the vertical sync start interrupt
[2]	RO	edc_afifo_underflow_int	Masked status of the EDC AFIFO underflow interrupt
[1]	RO	frame_end_int	Masked status of the frame end interrupt
[0]	RO	frame_start_int	Masked status of the frame start interrupt

LDI_INT_CLR

LDI_INT_CLR is an LDI interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x742C	LDI_INT_CLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vactive_line_int_clr	dsi_te1_pin_int_clr	dsi_te0_pin_int_clr	dsi_te_tri_int_clr	vfrontporch_end_int_clr	vactive1_end_int_clr	vactive1_start_int_clr	vactive0_end_int_clr	vactive0_start_int_clr	vfrontporch_int_clr	vbackporch_int_clr	vsync_int_clr	edc_afifo_underflow_int_clr	frame_end_int_clr	frame_start_int_clr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved
[14]	RW	vactive_line_int_clr	Specific line interrupt clear for the frame valid data. Writing 1 clears the interrupt, and writing 0 has no effect.
[13]	RW	dsi_te1_pin_int_clr	Tearing effect pin TE1 interrupt clear Writing 1 clears the interrupt.
[12]	RW	dsi_te0_pin_int_clr	Tearing effect pin TE0 interrupt clear Writing 1 clears the interrupt.
[11]	RW	dsi_te_tri_int_clr	Tearing effect trigger interrupt clear Writing 1 clears the interrupt.
[10]	RW	vfrontporch_end_int_clr	VFP end interrupt clear Writing 1 clears the interrupt.
[9]	RW	vactive1_end_int_clr	Valid data end interrupt clear for the right eye frame Writing 1 clears the interrupt.
[8]	RW	vactive1_start_int_clr	Valid data start interrupt clear for the right eye frame Writing 1 clears the interrupt.
[7]	RW	vactive0_end_int_clr	Frame valid data end interrupt clear (2D mode) or valid data end interrupt clear for the left eye frame (3D mode) Writing 1 clears the interrupt.

Offset Address	Register Name	Total Reset Value
0x742C	LDI_INT_CLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vactive_line_int_clr	dsi_te1_pin_int_clr	dsi_te0_pin_int_clr	dsi_te_tri_int_clr	vfrontporch_end_int_clr	vactive1_end_int_clr	vactive1_start_int_clr	vactive0_end_int_clr	vactive0_start_int_clr	vfrontporch_int_clr	vbackporch_int_clr	vsync_int_clr	edc_afifo_underflow_int_clr	frame_end_int_clr	frame_start_int_clr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[6]	RW	vactive0_start_int_clr	Frame valid data start interrupt clear (2D mode) or valid data start interrupt clear for the left eye frame (3D mode) Writing 1 clears the interrupt.
[5]	RW	vfrontporch_int_clr	VFP start interrupt clear Writing 1 clears the interrupt.
[4]	RW	vbackporch_int_clr	VBP start interrupt clear Writing 1 clears the interrupt.
[3]	RW	vsync_int_clr	Vertical sync start interrupt clear Writing 1 clears the interrupt.
[2]	RW	edc_afifo_underflow_int_clr	EDC AFIFO underflow interrupt clear Writing 1 clears the interrupt.
[1]	RW	frame_end_int_clr	Frame end interrupt clear Writing 1 clears the interrupt.
[0]	RW	frame_start_int_clr	Frame start interrupt clear Writing 1 clears the interrupt.

LDI_WORK_MODE

LDI_WORK_MODE is an LDI writeback control register.

Offset Address	Register Name	Total Reset Value
0x7430	LDI_WORK_MODE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													colorbar_en	wback_en	work_mode
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2]	RW	colorbar_en	Color bar enable. When this signal is high, the LDI automatically generates red, green, and blue color bars to test the LCD. This field is valid only in test mode.
[1]	RW	wback_en	Writeback enable
[0]	RW	work_mode	Working mode 0: test mode 1: normal mode

LDI_HDMI_DSI_GT

LDI_HDMI_DSI_GT is an HDMI/DSI pixel clock gating register.

Offset Address	Register Name	Total Reset Value
0x7434	LDI_HDMI_DSI_GT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														hdmi_pclk_off	dsi_pclk_off
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved

Offset Address	Register Name	Total Reset Value
0x7434	LDI_HDMI_DSI_GT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														hdmi_pclk_off	dsi_pclk_off
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1]	RW	hdmi_pclk_off	HDMI pixel clock disable 0: enabled 1: disabled
[0]	RW	dsi_pclk_off	DSI pixel clock disable 0: enabled 1: disabled

LDI_DE_SPACE_LOW

LDI_DE_SPACE_LOW is a DE signal validity control register for the 3D frame by frame format at the active space stage.

Offset Address	Register Name	Total Reset Value
0x7438	LDI_DE_SPACE_LOW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															de_space_low
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RW	reserved	Reserved
[0]	RW	de_space_low	Whether the DE signal is valid at the active space stage 0: The DE signal is high at the active space stage. 1: The DE signal is low at the active space stage. This field is valid only in 3D frame by frame format.

DSI_CMD_MOD_CTRL

DSI_CMD_MOD_CTRL is a DSI CMD mode control register.

Offset Address	Register Name	Total Reset Value
0x743C	DSI_CMD_MOD_CTRL	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2	1	0
Name	reserved								dsi_wms_3d_mode	dsi_halt_video_en	dsi_halt_cmd_en
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RW	reserved	Reserved
[2]	RW	dsi_wms_3d_mode	WMS signal mode in 3D mode (frame by frame) 0: separated WMS mode 1: continuous WMS mode
[1]	RW	dsi_halt_video_en	HALT signal enable in video mode. This bit is used to enable last line extension. 0: disabled. This signal is ignored internally. 1: enabled
[0]	RW	dsi_halt_cmd_en	HALT signal enable in CMD mode 0: disabled. This signal is ignored internally. 1: enabled

DSI_TE_CTRL

DSI_TE_CTRL is a TE control register in DSI CMD mode.

Offset Address	Register Name	Total Reset Value
0x7440	DSI_TE_CTRL	0x0000_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																dsi_te_pin_en	dsi_te_mask_und					dsi_te_mask_dis				dsi_te_mask_en	dsi_te_pin_hd_sel	dsi_te_hard_sel	dsi_te1_pin_p	dsi_te0_pin_p	dsi_te_hard_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RW	reserved	Reserved
[14]	RW	dsi_te_pin_en	TE pin detection enable in CMD mode 0: The TE pin detection logic is disabled. This setting applies when the TE pin is not used in video mode or CMD mode. 1: The TE pin detection logic is enabled. This setting applies when the TE pin is used in CMD mode.
[13:10]	RW	dsi_te_mask_und	Number of masked TE signals when TE signals are masked
[9:6]	RW	dsi_te_mask_dis	Number of displayed TE signals when TE signals are masked
[5]	RW	dsi_te_mask_en	TE mask enable. This function is required only in hardware mode. In software mode, ignore the interrupt. 0: The TE mask function is disabled. 1: The TE mask function is enabled.
[4]	RW	dsi_te_pin_hd_sel	TE pin select in TE hardware mode 0: TE0 pin 1: TE1 pin
[3]	RW	dsi_te_hard_sel	Source select in TE hardware mode 0: TE pin source input from pins 1: TE trigger source read over the MIPI
[2]	RW	dsi_te1_pin_p	TE1 polarity select 0: The input polarity is retained. 1: The input polarity is reversed.
[1]	RW	dsi_te0_pin_p	TE0 polarity select 0: The input polarity is retained. 1: The input polarity is reversed.

Offset Address	Register Name	Total Reset Value
0x7440	DSI_TE_CTRL	0x0000_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																dsi_te_pin_en	dsi_te_mask_und			dsi_te_mask_dis				dsi_te_mask_en	dsi_te_pin_hd_sel	dsi_te_hard_sel	dsi_te1_pin_p	dsi_te0_pin_p	dsi_te_hard_en		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	dsi_te_hard_en	TE hardware mode enable 0: disabled 1: enabled This bit must be disabled before you perform frame rate conversion (FRC) at a ratio when TE mask is enabled.

DSI_TE_HS_NUM

DSI_TE_HS_NUM is a DSI response line configuration register.

Offset Address	Register Name	Total Reset Value
0x7444	DSI_TE_HS_NUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved						dsi_te1_hs_num														dsi_te0_hs_num												
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RW	reserved	Reserved
[25:13]	RW	dsi_te1_hs_num	This field is used to configure the HS at which data is transmitted when the TE1 signal is in mode 2 (VS+HS). If this field is set to 0, only VS is used to transmit data and HS is ignored. The data of (DSI_TE1_HS_NUM + 1) lines is transmitted in practice.
[12:0]	RW	dsi_te0_hs_num	This field is used to configure the HS at which data is transmitted when the TE0 signal is in mode 2 (VS+HS). If this field is set to 0, only VS is used to transmit data and HS is ignored. The data of (DSI_TE1_HS_NUM + 1) lines is transmitted in

			practice.

DSI_TE_HS_WD

DSI_TE_HS_WD is an Hsync detection width control register in DSI TE pin mode.

Offset Address	Register Name	Total Reset Value
0x7448	DSI_TE_HS_WD	0x0000_3003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								dsi_te1_hs_wd												dsi_te0_hs_wd											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:24]	RW	reserved	Reserved
[23:12]	RW	dsi_te1_hs_wd	This field is used to determine the HS signal when the TE1 signal is in mode 2 (VS+HS). A TE signal is an HS signal when the active region of the TE signal is greater than the field value. The field value must be less than the value of DSI_TE0_VS_WD.
[11:0]	RW	dsi_te0_hs_wd	This field is used to determine the HS signal when the TE0 signal is in mode 2 (VS+HS). A TE signal is an HS signal when the active region of the TE signal is greater than the field value. The field value must be less than the value of DSI_TE1_VS_WD.

DSI_TE_VS_WD

DSI_TE_VS_WD is a Vsync detection width control register in DSI TE pin mode.

Offset Address	Register Name	Total Reset Value
0x744C	DSI_TE_VS_WD	0x0008_0080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								dsi_te1_vs_wd												dsi_te0_vs_wd											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	reserved	Reserved
[23:12]	RW	dsi_te1_vs_wd	This field is used to determine the VS signal when the TE1 signal is in mode 2 (VS+HS). A TE signal is a VS signal when the active region of the TE signal is greater than the field value. The field value must be greater than the value of DSI_TE1_HS_WD.
[11:0]	RW	dsi_te0_vs_wd	This field is used to determine the VS signal when the TE0 signal is in mode 2 (VS+HS). A TE signal is a VS signal when the active

			region of the TE signal is greater than the field value.

LDI_MCU_INTS

LDI_MCU_INTS is an MCU interrupt status register.

Offset Address	Register Name	Total Reset Value
0x7450	LDI_MCU_INTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															mcu_frm_end_ints
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RO	mcu_frm_end_ints	Status of the frame end interrupt

LDI_MCU_INTE

LDI_MCU_INTE is an MCU interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x7454	LDI_MCU_INTE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															mcu_frm_end_int_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved

Offset Address	Register Name	Total Reset Value
0x7454	LDI_MCU_INTE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															mcu_frm_end_int_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	mcu_frm_end_int_en	Frame end interrupt enable 0: masked 1: enabled

LDI_MCU_INTC

LDI_MCU_INTC is an MCU interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x7458	LDI_MCU_INTC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															mcu_frm_end_clr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	WO	mcu_frm_end_clr	Frame end interrupt clear. Writing 1 clears the interrupt.

3.4 MIPI DSI

3.4.1 Function Description

The MIPI DSI interface (DSI for short) of the display subsystem has the following features:

- Supports the following protocols:
  - MIPI® Alliance Specification for Display Serial Interface (DSI) v1.1 - 14 March 2012
  - MIPI® Alliance Specification for Display Command Set (DCS) v1.1 - 14 March 2012
  - MIPI® Alliance Standard for Display Pixel Interface v2.00 (DPI-2) - 23 Jan 2006
  - MIPI® Alliance Specification for Stereoscopic Display Formats (SDF) v1.0 - 14 March 2012
  - MIPI® Alliance Specification for D-PHY v1.1 - 16 Dec 2011
  - AMBA 2.0 Specification (APB) from ARM
- Supports the enhanced DPI (eDPI) input interface. The polarity of the interface control signal can be configured.
- Transmits a large amount of pixel data by running the memory write start (MWS) and memory write continue (MWC) commands and supports the high-definition command mode LCD.
- Supports the pixel formats such as RGB565, RGB666 packed, RGB666 loosely packed, and RGB888.
- Supports the configurable display resolution. The maximum resolution is WUXGA (1920 x 1200).
- Supports the configurable number of D-PHY data lanes. One to four data lanes are allowed.
- Supports the configurable transfer rate of the data lane. The maximum transfer rate is 1.5 Gbit/s.
- Supports bidirectional transfer and escape mode for data lane 0.
- Allows the virtual channel IDs for the video mode data packet, command mode data packet, and generic data packet to be separately configured.
- Supports all DCS commands and generic commands.
- Supports error correcting code (ECC) check and cyclic redundancy check (CRC).
- Supports the high speed (HS) or low power (LP) command transfer in video mode.
- Transmits and receives the end of transmission packet (EoTp).
- Supports the ultra-low power state (ULPS).
- Supports the error detection and recovery mechanism.
- Supports the 3D image format.
- Supports the peripheral response timeout mechanism.
- Supports the non-continuous clock.

3.4.2 Register Description

The DSI Controller core used in Hi6220 is build from Synopsys IP(1.20a). Details about the block can be found in DWC_mipi_dsi_host_databook.pdf and DWC_mipi_dsi_host_user.pdf (Which can also be downloaded from http://www.synopsys.com/dw/ipdir.php?ds=mipi_dsi)

The base address for DSI registers is 0xF410_7800.

4 Memory Control

4.1 Overview

This chapter describes the major memory control modules of the Hi6220.

- Multimedia card (MMC)/Secure digital (SD)/Secure digital input/output (SDIO)

  The Hi6220 has three independent MMC modules that support the SD card, embedded multimedia card (eMMC), peer device (such as a Wi-Fi chip) with an SDIO interface respectively.

4.2 SD/SDIO/MMC Host Controller

4.2.1 Function

The SD/SDIO/MMC host is the host controller in the SD, SDIO, or MMC (including the eMMC) system. The host controls the following cards:

- SD 3.0 card
- SDIO 3.0 card
- MMC 4.41 & eMMC 4.5

The SD card and MMC are massive-storage devices with embedded flash memories. The SDIO card is used for data transfer and can contain flash memories.

Hi6220 V100 integrates the following three MMC modules:

- MMC0: Connects to eMMC and supports 1-bit, 4-bit, and 8-bit modes.
- MMC1: Connects to the SD 3.0 card and supports 1-bit and 4-bit modes (3 V and 1.8 V supported for the I/O device).
- MMC2: Connects to the slave device and supports 1-bit and 4-bit modes.

The SD/SDIO/MMC host controller has the following features:

- Supports SD, SDIO, MMC card interface protocols.
- Provides a slave advanced microcontroller bus architecture (AMBA) advanced high-performance bus (AHB) interface for transmitting data and accessing internal registers.
- Provides an internal DMA controller (IDMAC) dedicated for transmitting data.

- Supports separate card interface clocks and bus interface clocks.

Card Interface Features

- SD 3.0 protocol
- SDIO 3.00 protocol
- MMC 4.41 and eMMC 4.5 protocols
- Cyclic redundancy check (CRC) and error detection
- Programmable baud rate
- Clock control circuit for enabling and disabling the card clock
- SDIO interrupt (eSDIO) in 1-bit and 4-bit data bus width modes
- SDIO suspend and resume operations
- SDIO read wait
- Block size ranging from 1 to 65535 bytes
- 4-bit DDR transfers defined in the SD 3.0 and MMC 4.41 protocols
- UHS-1 SD or SDIO card with the maximum rates of SDR50 and DDR50
- 4-bit and 8-bit HS200 modes defined in the eMMC 4.5 protocol, maximum interface frequency of 150 MHz
- Voltage switching between the SD and SDIO cards
- Card clock stop for preventing the FIFO overrun and underrun
- Busy status interrupt reported during write operations

4.2.2 Register Description

The EMMC/SD core used in Hi6220 is build from Synopsys IP(2.60a). Details about the block can be found in dwc_mobile_storage_db.pdf (Which can also be downloaded from https://www.synopsys.com/dw/ipdir.php?c=dwc_mobile_storage)

The base address for MMC0 registers is 0xF723_D000.

The base address for MMC1 registers is 0xF723_E000.

The base address for MMC2 registers is 0xF723_F000.

5 Peripheral Interfaces

5.1 GPIO

5.1.1 Function Description

The Hi6220 has 20 groups of general-purpose input/output (GPIO) pins, including GPIO0−GPIO2 in the power-on area of the system-on-chip (SoC) system and GPIO3−GPIO19 in the power-off area of the SoC system. Each GPOP group has eight programmable GPIO pins, and there are 160 GPIO pins in total. The GPIO pins are used to generate output signals or collect input signals for specific applications. The GPIO3−GPIO19 pins are multiplexed with other functional pins.

The GPIO has the following features:

- The GPIO complies with the advanced microcontroller bus architecture 2.0 (AMBA 2.0) advanced peripheral bus (APB) interface standard, and all register configuration interfaces and internal registers can be accessed.
- The GPIO supports only one bus clock and one reset signal but not separate soft reset.
- Each GPIO group provides eight independent input/output pins, which can be separately controlled by software. The pin direction during power-on reset is input by default.
- Any number of input pins can be configured as external interrupt signal sources over the interrupt interface, which is controlled by software.
- The interrupt triggering mode can be set to high-level-triggered, low-level-triggered, rising-edge-triggered, falling-edge-triggered, or dual-edge-triggered, which is controlled by software.
- Interrupts can be combined for output.
- The input interrupts of the eight pins in each GPIO group can be distributed by processor.
- The GPIO security operation feature can be configured.
- Except some pads in the power-on area, the GPIO can wake up the ACPU in sleep mode by using interrupts only during power-on. The ACPU can be woken up by using GPIO0−GPIO19.
- GPIO0−GPIO2 are located in the system power-on area.
- GPIO3−GPIO19 are located in the system power-off area.
- The GPIO supports only software control.

5.1.2 Register Description

Table 5-1 lists the base addresses for GPIO0 to GPIO19 registers.

Table 5-1 Base addresses for GPIO0 to GPIO19 registers

Register	Base Address
GPIO0 registers	0xF801_1000
GPIO1 registers	0xF801_2000
GPIO2 registers	0xF801_3000
GPIO3 registers	0xF801_4000
GPIO4 registers	0xF702_0000
GPIO5 registers	0xF702_1000
GPIO6 registers	0xF702_2000
GPIO7 registers	0xF702_3000
GPIO8 registers	0xF702_4000
GPIO9 registers	0xF702_5000
GPIO10 registers	0xF702_6000
GPIO11 registers	0xF702_7000
GPIO12 registers	0xF702_8000
GPIO13 registers	0xF702_9000
GPIO14 registers	0xF702_A000
GPIO15 registers	0xF702_B000
GPIO16 registers	0xF702_C000
GPIO17 registers	0xF702_D000
GPIO18 registers	0xF702_E000
GPIO19 registers	0xF702_F000

Table 5-2 describes GPIO registers.

Table 5-2 Summary of GPIO registers

Offset Address	Register	Description
0x0004	GPIODATA_0	GPIO data register 0
0x0008	GPIODATA_1	GPIO data register 1

Offset Address	Register	Description
0x0010	GPIODATA_2	GPIO data register 2
0x0020	GPIODATA_3	GPIO data register 3
0x0040	GPIODATA_4	GPIO data register 4
0x0080	GPIODATA_5	GPIO data register 5
0x0100	GPIODATA_6	GPIO data register 6
0x0200	GPIODATA_7	GPIO data register 7
0x400	GPIODIR	GPIO direction control register
0x404	GPIOIS	Edge- or level-sensitive mode selection register
0x408	GPIOIBE	Single- or dual-edge-sensitive mode selection register
0x40C	GPIOIEV	Rising/Falling edge or high/low level trigger mode selection register
0x410	GPIOIE	Interrupt mask register
0x500	GPIOIE2	Interrupt mask register
0x504	GPIOIE3	Interrupt mask register
0x414	GPIORIS	Raw interrupt status register
0x418	GPIOMIS	Masked interrupt status register
0x530	GPIOMIS2	Masked interrupt status register
0x534	GPIOMIS3	Masked interrupt status register
0x41C	GPIOIC	Interrupt clear register
0x420	GPIOAFSEL	Hardware/Software mode control register

GPIODATA_0

GPIODATA_0 is GPIO data register 0. It is used to buffer input/output data.

If the corresponding bit of GPIO_DIR is configured as output, the value written to the GPIO_DATA register is output to the corresponding pin (ensure that the pin multiplexing configuration is correct). If the bit is configured as input, the value of the corresponding input pin is read.

CAUTION

If the corresponding bit of GPIO_DIR is configured as input, the pin values are returned if the read operations are valid; if the corresponding bit is configured as output, the written values are returned if the read operations are valid.

The GPIO_DATA register masks the read and write operations on bits by using PADDR[9:2]. This register corresponds to 256 address spaces. PADDR[9:2] correspond to GPIO_DATA bit[7:0]. When a PADDR bit is high, the corresponding bit in GPIO_DATA can be read or written; when the corresponding bit is low, the read or write operation is not allowed. For example:

- If the address is 0x3FC (0b11_1111_1100), operations on all the eight bits of GPIO_DATA bit[7:0] are valid.
- If the address is 0x200 (0b10_0000_0000), only the operation on GPIO_DATA bit[7] is valid.

Offset Address	Register Name	Total Reset Value
0x0004	GPIODATA_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								data_register							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved
[7:0]	RW	data_register	Data register

GPIODATA_1

GPIODATA_1 is GPIO data register 1. Its function is similar to GPIODATA_0.

Offset Address	Register Name	Total Reset Value
0x0008	GPIODATA_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								data_register							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved
[7:0]	RW	data_register	Data register

GPIODATA_2

GPIODATA_2 is GPIO data register 2. Its function is similar to GPIODATA_0.

Offset Address	Register Name	Total Reset Value
0x0010	GPIODATA_2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								data_register							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved
[7:0]	RW	data_register	Data register

GPIODATA_3

GPIODATA_3 is GPIO data register 3. Its function is similar to GPIODATA_0.

Offset Address	Register Name	Total Reset Value
0x0020	GPIODATA_3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								data_register							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved
[7:0]	RW	data_register	Data register

GPIODATA_4

GPIODATA_4 is GPIO data register 4. Its function is similar to GPIODATA_0.

Offset Address	Register Name	Total Reset Value
0x0040	GPIODATA_4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								data_register							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved

Offset Address	Register Name	Total Reset Value
0x0040	GPIODATA_4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								data_register							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	data_register	Data register

GPIODATA_5

GPIODATA_5 is GPIO data register 5. Its function is similar to GPIODATA_0.

Offset Address	Register Name	Total Reset Value
0x0080	GPIODATA_5	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								data_register							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved
[7:0]	RW	data_register	Data register

GPIODATA_6

GPIODATA_6 is GPIO data register 6. Its function is similar to GPIODATA_0.

Offset Address	Register Name	Total Reset Value
0x0100	GPIODATA_6	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								data_register							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved
[7:0]	RW	data_register	Data register

GPIODATA_7

GPIODATA_7 is GPIO data register 7. Its function is similar to GPIODATA_0.

Offset Address	Register Name	Total Reset Value
0x0200	GPIODATA_7	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								data_register							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved
[7:0]	RW	data_register	Data register

GPIODIR

GPIODIR is a GPIO direction control register.

Offset Address	Register Name	Total Reset Value
0x400	GPIODIR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								data_direct							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved
[7:0]	RW	data_direct	Data direction 0: input 1: output

GPIOIS

GPIOIS is an edge- or level-sensitive mode selection register.

Offset Address	Register Name	Total Reset Value
0x404	GPIOIS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								interrupt_sense							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved
[7:0]	RW	interrupt_sense	Edge- or level-sensitive mode select 0: edge-sensitive mode 1: level-sensitive mode

GPIOIBE

GPIOIBE is a single- or dual-edge-sensitive mode selection register.

Offset Address	Register Name	Total Reset Value
0x408	GPIOIBE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								interrupt_sense							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved
[7:0]	RW	interrupt_sense	Single- or dual-edge-sensitive mode select 0: single-edge-sensitive mode. The GPIOIEV register determines whether the interrupt is triggered by the rising edge or falling edge. 1: The interrupt is triggered by either the rising edge or falling edge.

GPIOIEV

GPIOIEV is a rising/falling edge or high/low level trigger mode selection register.

Offset Address	Register Name	Total Reset Value
0x40C	GPIOIEV	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								interrupt_event							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved
[7:0]	RW	interrupt_event	Rising/Falling edge or high/low level trigger mode select 0: The interrupt is triggered by the falling edge or low level. 1: The interrupt is triggered by the rising edge or high level.

GPIOIE

GPIOIE is a GPIO interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x410	GPIOIE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								interrupt_mask							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved
[7:0]	RW	interrupt_mask	Interrupt mask 0: The interrupt of the corresponding pin is masked. 1: The interrupt of the corresponding pin is enabled.

GPIOIE2

GPIOIE2 is a GPIO interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x500	GPIOIE2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								interrupt2_mask							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved
[7:0]	RW	interrupt2_mask	Interrupt mask 0: The interrupt of the corresponding pin is masked. 1: The interrupt of the corresponding pin is enabled.

GPIOIE3

GPIOIE3 is a GPIO interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x504	GPIOIE3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								interrupt3_mask							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved
[7:0]	RW	interrupt3_mask	Interrupt mask 0: The interrupt of the corresponding pin is masked. 1: The interrupt of the corresponding pin is enabled.

GPIORIS

GPIORIS is a raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x414	GPIORIS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								raw_interrupt_status							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved
[7:0]	RO	raw_interrupt_status	Raw interrupt status 0: The corresponding pin does not trigger an interrupt. 1: The corresponding pin has triggered an interrupt.

GPIOMIS

GPIOMIS is a masked interrupt status register.

Offset Address	Register Name	Total Reset Value
0x418	GPIOMIS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								masked_interrupt_status							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved
[7:0]	RO	masked_interrupt_status	Masked interrupt status 0: The corresponding pin does not trigger an interrupt. 1: The corresponding pin has triggered an interrupt.

GPIOMIS2

GPIOMIS2 is a masked interrupt status register.

Offset Address	Register Name	Total Reset Value
0x530	GPIOMIS2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								masked_interrupt2_status							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved
[7:0]	RO	masked_interrupt2_status	Masked interrupt status 0: The corresponding pin does not trigger an interrupt. 1: The corresponding pin has triggered an interrupt.

GPIOMIS3

GPIOMIS3 is a masked interrupt status register.

Offset Address	Register Name	Total Reset Value
0x534	GPIOMIS3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								masked_interrupt3_status							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved
[7:0]	RO	masked_interrupt3_status	Masked interrupt status 0: The corresponding pin does not trigger an interrupt. 1: The corresponding pin has triggered an interrupt.

GPIOIC

GPIOIC is a GPIO interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x41C	GPIOIC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								interrupt_status_clear							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved
[7:0]	WO	interrupt_status_clear	Interrupt clear 0: no effect 1: cleared

GPIOAFSEL

GPIOAFSEL is a hardware/software mode control register.

Offset Address	Register Name	Total Reset Value
0x420	GPIOAFSEL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								mode_control_select_register							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved
[7:0]	RW	mode_control_select_register	Control mode select 0: software-controlled mode 1: hardware-controlled mode

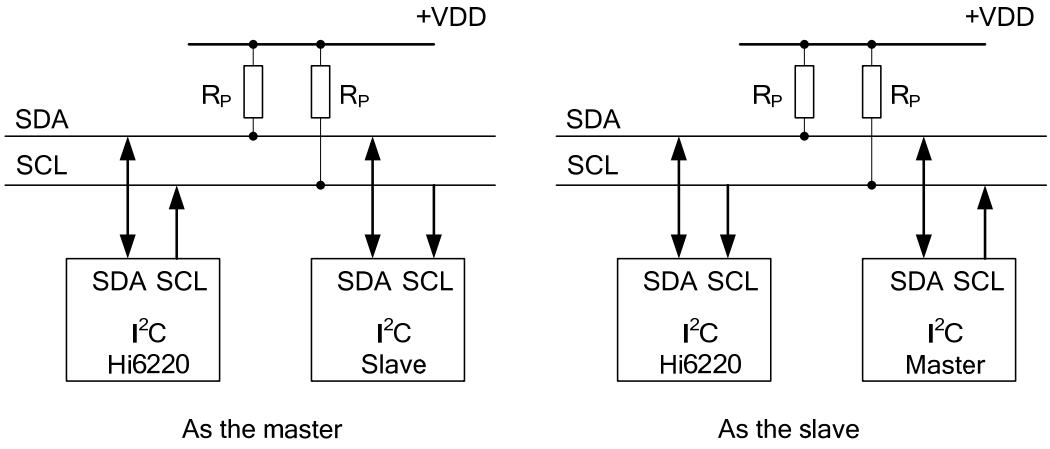
5.2 I²C

5.2.1 Function Description

The inter-integrated circuit (I^2C) module of the DesignWare mainly acts as a master (both master and slave modes are supported). The I^2C controller communicates with an external device with the I^2C interface through the serial clock (SCL) and serial data (SDA) signal lines. The I^2C interfaces can transmit/receive data to/from the slave on the I^2C bus in compliance with I^2C specifications V2.0.

Figure 5-1 shows the typical I^2C application circuit.

Figure 5-1 Typical I²C application circuit



The I²C module has the following features:

- Supports the I²C bus protocol V2.0.
- Serves as a master or slave on the I²C bus, and supports bus arbitration for multiple masters when serving as a master.
- Servers as the transceiver on the I²C bus to transmit or receive data between the master and the slave.
- Supports the 7-bit standard slave address or 10-bit extended slave address when serving as a master.
- Supports the standard mode (100 kbit/s), fast mode (400 kbit/s), and high-speed mode (3.4 Mbit/s).
- Reports interrupts and queries the status of raw and masked interrupts.
- Does not support the CBUS component on the I²C bus. The CBUS bus consists of the shared I²C bus and an additional line, and the CBUS component implements communication through the CBUS bus.
- Suppresses glitches for the received SDA and SCL signals.

5.2.2 Register Description

The following are the base addresses for I²C registers:

- The base address for I²C0 registers is 0xF710_0000.
- The base address for I²C1 registers is 0xF710_1000.
- The base address for I²C2 registers is 0xF710_2000.
- The base address for I²C3 registers is 0xF710_3000.

Table 5-3 describes I²C registers.

Table 5-3 Summary of I²C registers

Offset Address	Register	Description
0x0000	I2C_CON	I²C control register

Offset Address	Register	Description
0x0004	I2C_TAR	I^2C access slave device address register
0x0008	I2C_SAR	I^2C slave address register
0x000C	I2C_HS_MADDR	I^2C high-speed master code address register
0x0010	I2C_DATA_CMD	I^2C data channel register
0x0014	I2C_SS_SCL_HCNT	High level time configuration register for the SCL clock at standard speed
0x0018	I2C_SS_SCL_LCNT	Low level time configuration register for the SCL clock at standard speed
0x001C	I2C_FS_SCL_HCNT	High level time configuration register for the SCL clock at fast speed
0x0020	I2C_FS_SCL_LCNT	Low level time configuration register for the SCL clock at fast speed
0x0024	I2C_HS_SCL_HCNT	High level time configuration register for the SCL clock at high speed
0x0028	I2C_HS_SCL_LCNT	Low level time configuration register for the SCL clock at high speed
0x002C	I2C_INTR_STAT	Interrupt status register
0x0030	I2C_INTR_MASK	Interrupt mask register
0x0034	I2C_RAW_INTR_STAT	Raw interrupt status register
0x0038	I2C_RX_TL	RX FIFO threshold configuration register
0x003C	I2C_TX_TL	TX FIFO threshold configuration register
0x0040	I2C_CLR_INTR	Combined and independent interrupt clear register
0x0044	I2C_CLR_RX_UNDER	RX_UNDER interrupt clear register
0x0048	I2C_CLR_RX_OVER	RX_OVER interrupt clear register
0x004C	I2C_CLR_TX_OVER	TX_OVER interrupt clear register
0x0050	I2C_CLR_RD_REQ	RD_REQ interrupt clear register
0x0054	I2C_CLR_TX_ABRT	ABRT interrupt clear register
0x0058	I2C_CLR_RX_DONE	RX_DONE interrupt clear register
0x005C	I2C_CLR_ACTIVITY	ACTIVITY status register
0x0060	I2C_CLR_STOP_DET	STOP_DET interrupt clear register
0x0064	I2C_CLR_START_DET	START_DET interrupt clear register
0x0068	I2C_CLR_GEN_CALL	GEN_CALL interrupt clear register

Offset Address	Register	Description
0x006C	I2C_ENABLE	I^2C enable register
0x0070	I2C_STATUS	I^2C status register
0x0074	I2C_TXFLR	TX FIFO data count indicator register
0x0078	I2C_RXFLR	RX FIFO data count indicator register
0x007C	I2C_SDA_HOLD	Serial data (SDA) hold time register
0x0080	I2C_TX_ABRT_SOURCE	TX_ABRT source interrupt register
0x0088	I2C_DMA_CR	I^2C direct memory access (DMA) channel enable control register
0x008C	I2C_DMA_TDLR	TX FIFO threshold configuration register for DMA operations
0x0090	I2C_DMA_RDLR	RX FIFO threshold configuration register for DMA operations
0x0094	I2C_SDA_SETUP	SDA setup time register
0x0098	I2C_ACK_GENERAL_CALL	General call response register
0x009C	I2C_ENABLE_STATUS	I^2C enable status register
0x00A0	I2C_FS_SPKLEN	Standard- and full-speed glitch suppression length register
0x00A4	I2C_HS_SPKLEN	High-speed glitch suppression length register
0x00F4	I2C_COMP_PARAM_1	Parameter register
0x00F8	I2C_COMP_VERSION	Version register
0x00FC	I2C_COMP_TYPE	DesignWareIP type register

I2C_CON

I2C_CON is an I^2C control register.

CAUTION

I2C_CON can be configured only when the I^2C is disabled (I2C_ENABLE[enable] is 0).

Offset Address	Register Name	Total Reset Value
0x0000	I2C_CON	0x007F

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved									i2c_slave_disable	i2c_restart_en	i2c_10bitaddr_master	i2c_10bitaddr_slave	speed		master_mode
Reset	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[15:7]	-	reserved	Reserved
[6]	RW	i2c_slave_disable	Reserved Note that the bit must be 1.
[5]	RW	i2c_restart_en	Restart condition enable 0: disabled, meaning that the restart condition function is unavailable 1: enabled
[4]	RW	i2c_10bitaddr_master	TX 7-bit or 10-bit address select 0: 7-bit address 1: 10-bit address
[3]	RW	i2c_10bitaddr_slave	Reserved
[2:1]	RW	speed	I^2C operation speed select 00: invalid 01: standard speed (0−100 kbit/s) 10: fast speed (≤ 400 kbit/s) 11: high speed (≤ 3.4 Mbit/s)
[0]	RW	master_mode	Master mode enable 0: disabled 1: enabled

I2C_TAR

I2C_TAR is an I^2C access slave device address register.

CAUTION

I2C_TAR can be configured only when the I²C is disabled (I2C_ENABLE[enable] is 0).

Offset Address	Register Name	Total Reset Value
0x0004	I2C_TAR	0x0055

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved			i2c_10bit_addr_master	special	gc_or_start	i2c_tar									
Reset	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1

Bits	Access	Name	Description
[15:13]	-	reserved	Reserved
[12]	RW	i2c_10bit_addr_master	7-bit or 10-bit addressing mode when DW_apb_i2c acts as a master 0: 7-bit addressing 1: 10-bit addressing
[11]	RW	special	General call and start byte function enable 0: disabled 1: enabled
[10]	RW	gc_or_start	Whether to implement the general call or start byte function when bit 11 is 1. 0: general call 1: start byte
[9:0]	RW	i2c_tar	Slave address that is accessed by the I²C when I²C acts as a master device

I2C_SAR

I2C_SAR is a slave I²C address register.

CAUTION

I2C_SAR can be configured only when the I^2C is disabled (I2C_ENABLE[enable] is 0).

Offset Address	Register Name	Total Reset Value
0x0008	I2C_SAR	0x0055

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved						i2c_sar									
Reset	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1

Bits	Access	Name	Description
[15:10]	-	reserved	Reserved
[9:0]	RW	i2c_sar	Address of the slave I^2C. For the 7-bit addressing, only I2C_SAR bit[6:0] are used.

I2C_HS_MADDR

I2C_HS_MADDR is an I^2C high-speed master code address register. It can be configured only when the I^2C is disabled (I2C_ENABLE[enable] is 0).

Offset Address	Register Name	Total Reset Value
0x000C	I2C_HS_MADDR	0x0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														i2c_hs_mar	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[15:3]	-	reserved	Reserved
[2:0]	RW	i2c_hs_mar	Master code of the I^2C in high-speed mode Each master has its independent master code. An I^2C system supports a maximum of eight high-speed masters.

I2C_DATA_CMD

I2C_DATA_CMD is an I^2C data channel register.

Offset Address	Register Name	Total Reset Value
0x0010	I2C_DATA_CMD	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					restart	stop	cmd	dat							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:11]	-	reserved	Reserved
[10]	WO	restart	1: A RESTART is generated before the next transfer no matter whether the current transfer direction is the same as the previous one. 0: A RESTART is generated before the next transfer only if the current transfer direction is different from the previous one.
[9]	WO	stop	1: A STOP is generated after the current bytes are transferred no matter whether the TX FIFO is empty. If the TX FIFO is not empty, the master immediately generates a START and requests bus arbitration for a new transfer attempt. 0: No STOP is generated after the current bytes are transferred no matter whether the TX FIFO is empty. If the TX FIFO is not empty, the master continues the current transfer and transmits or receives data based on the direction command word configuration. If the TX FIFO is empty, the master pulls SCL down until the TX FIFO receives a new command.
[8]	WO	cmd	Read/Write control bit 0: write operation. It indicates that the I^2C controller will transmit data to the I^2C bus. In this case, the lower eight bits (DAT) will be transmitted to the I^2C bus by the I^2C controller. 1: Read operation. It indicates that the I^2C controller will read data from the I^2C bus.
[7:0]	RW	dat	Data to be transmitted or received through the I^2C bus The data received through the I^2C bus is obtained if these eight bits are read. The written data is transmitted to the I^2C bus if these eight bits are written.

I2C_SS_SCL_HCNT

I2C_SS_SCL_HCNT is a high level width configuration register for the SCL clock at standard speed.

CAUTION

I2C_SS_SCL_HCNT can be configured only when the I^2C is disabled (I2C_ENABLE[enable] is 0).

Offset Address	Register Name	Total Reset Value
0x0014	I2C_SS_SCL_HCNT	0x0190

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	i2c_ss_scl_hcnt															
Reset	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0

Bits	Access	Name	Description
[15:0]	RW	i2c_ss_scl_hcnt	Number of ic_clk clock cycles for the high-level SCL signal in standard mode Note that the minimum value is 6 and any written value less than 6 is regarded as 6.

I2C_SS_SCL_LCNT

I2C_SS_SCL_LCNT is a low level width configuration register for the SCL clock at standard speed.

CAUTION

I2C_SS_SCL_LCNT can be configured only when the I^2C is disabled (I2C_ENABLE[enable] is 0).

Offset Address	Register Name	Total Reset Value
0x0018	I2C_SS_SCL_LCNT	0x01D6

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	i2c_ss_scl_lcnt															
Reset	0	0	0	0	0	0	0	1	1	1	0	1	0	1	1	0

Bits	Access	Name	Description
[15:0]	RW	i2c_ss_scl_lcnt	Number of ic_clk clock cycles for the low-level SCL signal in standard mode Note that the minimum value is 8 and any written value less than 8 is regarded as 8.

I2C_FS_SCL_HCNT

I2C_FS_SCL_HCNT is a high level width configuration register for the SCL clock at fast speed.

CAUTION

I2C_FS_SCL_HCNT can be configured only when the I^2C is disabled (I2C_ENABLE[enable] is 0).

Offset Address	Register Name	Total Reset Value
0x001C	I2C_FS_SCL_HCNT	0x003C

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	i2c_fs_scl_hcnt															
Reset	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0

Bits	Access	Name	Description
[15:0]	RW	i2c_fs_scl_hcnt	Number of ic_clk clock cycles for the high-level SCL signal in fast mode Note that the minimum value is 6 and any written value less than 6 is regarded as 6.

I2C_FS_SCL_LCNT

I2C_FS_SCL_LCNT is the low level width configuration register for the SCL clock at fast speed.

CAUTION

I2C_FS_SCL_LCNT can be configured only when the I^2C is disabled (I2C_ENABLE[enable] is 0).

Offset Address	Register Name	Total Reset Value
0x0020	I2C_FS_SCL_LCNT	0x0082

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	i2c_fs_scl_lcnt															
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0

Bits	Access	Name	Description
[15:0]	RW	i2c_fs_scl_lcnt	Number of ic_clk clock cycles for the low-level SCL signal in fast mode Note that the minimum value is 8 and any written value less than 8 is regarded as 8.

I2C_HS_SCL_HCNT

I2C_HS_SCL_HCNT is a high level time configuration register for the SCL clock at the high speed.

CAUTION

I2C_HS_SCL_HCNT can be configured only when the I^2C is disabled (I2C_ENABLE[enable] is 0).

Offset Address	Register Name	Total Reset Value
0x0024	I2C_HS_SCL_HCNT	0x0006

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	i2c_hs_scl_hcnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

Bits	Access	Name	Description
[15:0]	RW	i2c_hs_scl_hcnt	Number of ic_clk clock cycles for the high-level SCL signal in high-speed mode

			Note that the minimum value is 6 and any written value less than 6 is regarded as 6.

I2C_HS_SCL_LCNT

I2C_HS_SCL_LCNT is a low-level time configuration register for the SCL clock at the high speed.

CAUTION

I2C_HS_SCL_HCNT can be configured only when the I^2C is disabled (I2C_ENABLE[enable] is 0).

Offset Address	Register Name	Total Reset Value
0x0028	I2C_HS_SCL_LCNT	0x0010

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	i2c_hs_scl_lcnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[15:0]	RW	i2c_hs_scl_lcnt	Number of ic_clk clock cycles for the low-level SCL signal in high-speed mode Note that the minimum value is 8 and any written value less than 8 is regarded as 8.

I2C_INTR_STAT

I2C_INTR_STAT is an interrupt status register.

Offset Address	Register Name	Total Reset Value
0x002C	I2C_INTR_STAT	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				gen_call	start_det	stop_det	activity	rx_done	tx_abrt	rd_req	tx_empty	tx_over	rx_full	rx_over	rx_under
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:12]	-	reserved	Reserved
[11]	RO	gen_call	GEN_CALL interrupt, indicating whether a general call request is received 0: No general call request is received. 1: A general call request is received. The I^2C stores the received data in the RX buffer.
[10]	RO	start_det	START_DET interrupt, indicating whether the start condition is met on the I^2C bus 0: The start condition is not met. 1: The start condition is met.
[9]	RO	stop_det	STOP_DET interrupt, indicating whether the stop condition is met on the I^2C bus 0: The stop condition is not met. 1: The stop condition is met.
[8]	RO	activity	ACTIVITY interrupt, indicating the activity status of the I^2C 0: idle 1: busy
[7]	RO	rx_done	RX_DONE interrupt. When the I^2C acts as the slave device, this bit indicates whether data reception is complete. 0: not completed 1: completed
[6]	RO	tx_abrt	TX_ABRT interrupt. The interrupt can be triggered in multiple cases. For details, see I2C_TX_ABRT_SOURCE.
[5]	RO	rd_req	RD_REQ interrupt. When the I^2C acts as the slave device, this bit indicates whether a data read request is initiated by a master device. 0: No request is initiated. 1: A request is initiated.

Offset Address	Register Name	Total Reset Value
0x002C	I2C_INTR_STAT	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				gen_call	start_det	stop_det	activity	rx_done	tx_abrt	rd_req	tx_empty	tx_over	rx_full	rx_over	rx_under
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[4]	RO	tx_empty	ITX_EMPTY interrupt, indicating whether the data in the TX FIFO reaches or is below the threshold 0: The data in the TX FIFO is above the threshold. 1: The data in the TX FIFO reaches or is below the threshold.
[3]	RO	tx_over	TX_OVER interrupt, indicating whether the data in the TX FIFO overflows 0: no 1: yes
[2]	RO	rx_full	RX_FULL interrupt, indicating whether the data in the RX FIFO reaches or is above the threshold 0: The data in the RX FIFO is below the threshold. 1: The data in the RX FIFO reaches or is above the threshold
[1]	RO	rx_over	RX_OVER interrupt, indicating whether the data in the RX FIFO overflows 0: no 1: yes
[0]	RO	rx_under	RX_UNDER interrupt. When the RX FIFO is empty, the internal bus interface initiates a request to read I2C_DATA_CMD. 0: This bit is meaningless. 1: When the RX FIFO is empty, the CPU reads I2C_DATA_CMD.

I2C_INTR_MASK

I2C_INTR_MASK is an interrupt mask register. The value 0 indicates that the interrupt is masked, and the value 1 indicates that the interrupt is not masked.

Offset Address	Register Name	Total Reset Value
0x0030	I2C_INTR_MASK	0x08FF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				m_gen_call	m_start_det	m_stop_det	m_activity	m_rx_done	m_tx_abrt	m_rd_req	m_tx_empty	m_tx_over	m_rx_full	m_rx_over	m_rx_under
Reset	0	0	0	0	1	0	0	0	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[15:12]	-	reserved	Reserved
[11]	RW	m_gen_call	GEN_CALL interrupt mask
[10]	RW	m_start_det	START_DET interrupt mask
[9]	RW	m_stop_det	STOP_DET interrupt mask
[8]	RW	m_activity	ACTIVITY interrupt mask
[7]	RW	m_rx_done	RX_DONE interrupt mask
[6]	RW	m_tx_abrt	TX_ABRT interrupt mask
[5]	RW	m_rd_req	RD_REQ interrupt mask
[4]	RW	m_tx_empty	TX_EMPTY interrupt mask
[3]	RW	m_tx_over	TX_OVER interrupt mask
[2]	RW	m_rx_full	RX_FULL interrupt mask
[1]	RW	m_rx_over	RX_OVER interrupt mask
[0]	RW	m_rx_under	RX_UNDER interrupt mask

I2C_RAW_INTR_STAT

I2C_RAW_INTR_STAT is a raw interrupt status register. The value 0 indicates that no interrupt is generated, and the value 1 indicates that an interrupt is generated.

Offset Address	Register Name	Total Reset Value
0x0034	I2C_RAW_INTR_STAT	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				r_gen_call	r_start_det	r_stop_det	r_activity	r_rx_done	r_tx_abrt	r_rd_req	r_tx_empty	r_tx_over	r_rx_full	r_rx_over	r_rx_under
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:12]	-	reserved	Reserved
[11]	RO	r_gen_call	GEN_CALL raw interrupt status
[10]	RO	r_start_det	START_DET raw interrupt status
[9]	RO	r_stop_det	STOP_DET raw interrupt status
[8]	RO	r_activity	ACTIVITY raw interrupt status
[7]	RO	r_rx_done	RX_DONE raw interrupt status
[6]	RO	r_tx_abrt	TX_ABRT raw interrupt status
[5]	RO	r_rd_req	RD_REQ raw interrupt status
[4]	RO	r_tx_empty	TX_EMPTY raw interrupt status
[3]	RO	r_tx_over	TX_OVER raw interrupt status
[2]	RO	r_rx_full	RX_FULL raw interrupt status
[1]	RO	r_rx_over	RX_OVER raw interrupt status
[0]	RO	r_rx_under	RX_UNDER raw interrupt status

I2C_RX_TL

I2C_RX_TL is an RX FIFO threshold configuration register.

Offset Address	Register Name	Total Reset Value
0x0038	I2C_RX_TL	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								rx_tl							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:8]	-	reserved	Reserved

[7:0]	RW	rx_tl	RX FIFO threshold. The actual value is equal to the configured value plus 1. Note that any configured value greater than 8 is considered as 8.

I2C_TX_TL

I2C_TX_TL is a TX FIFO threshold configuration register.

Offset Address	Register Name	Total Reset Value
0x003C	I2C_TX_TL	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								tx_tl							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:8]	-	reserved	Reserved
[7:0]	RW	tx_tl	TX FIFO threshold Note that any configured value greater than 8 is considered as 8.

I2C_CLR_INTR

I2C_CLR_INTR is a combined and independent interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x0040	I2C_CLR_INTR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															clr_intr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:1]	-	reserved	Reserved

Offset Address	Register Name	Total Reset Value
0x0040	I2C_CLR_INTR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															clr_intr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RO	clr_intr	Reading this register clears all combined interrupts and independent interrupts as well as the I2C_TX_ABRT_SOURCE register. Note that I2C_TX_ABRT_SOURCE[abrt_sbyte_norstrt] and the combined interrupts triggered by I2C_TX_ABRT_SOURCE[abrt_sbyte_norstrt] cannot be cleared.

I2C_CLR_RX_UNDER

I2C_CLR_RX_UNDER is an RX_UNDER interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x0044	I2C_CLR_RX_UNDER	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															clr_rx_under
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:1]	-	reserved	Reserved
[0]	RO	clr_rx_under	Reading this register clears the RX_UNDER interrupt.

I2C_CLR_RX_OVER

I2C_CLR_RX_OVER is an RX_OVER interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x0048	I2C_CLR_RX_OVER	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															clr_rx_over
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:1]	-	reserved	Reserved
[0]	RO	clr_rx_over	Reading this register clears the RX_OVER interrupt.

I2C_CLR_TX_OVER

I2C_CLR_TX_OVER is a TX_OVER interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x004C	I2C_CLR_TX_OVER	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															clr_tx_over
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:1]	-	reserved	Reserved
[0]	RO	clr_tx_over	Reading this register clears the TX_OVER interrupt.

I2C_CLR_RD_REQ

I2C_CLR_RD_REQ is an RD_REQ interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x0050	I2C_CLR_RD_REQ	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															clr_rd_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:1]	-	reserved	Reserved
[0]	RO	clr_rd_req	Reading this register clears the RD_REQ interrupt.

I2C_CLR_TX_ABRT

I2C_CLR_TX_ABRT is an ABRT interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x0054	I2C_CLR_TX_ABRT	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															clr_tx_abrt
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:1]	-	reserved	Reserved
[0]	RO	clr_tx_abrt	Reading this register clears the TX_ABRT interrupt and the I2C_TX_ABRT_SOURCE register.

I2C_CLR_RX_DONE

I2C_CLR_RX_DONE is an RX_DONE interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x0058	I2C_CLR_RX_DONE	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															clr_rx_done
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:1]	-	reserved	Reserved
[0]	RO	clr_rx_done	Reading this register clears the RX_DONE interrupt.

I2C_CLR_ACTIVITY

I2C_CLR_ACTIVITY is an ACTIVITY status register.

Offset Address	Register Name	Total Reset Value
0x005C	I2C_CLR_ACTIVITY	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															clr_activity
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:1]	-	reserved	Reserved
[0]	RO	clr_activity	When this register is read, the ACTIVITY interrupt status can be obtained and this bit is cleared automatically by hardware.

I2C_CLR_STOP_DET

I2C_CLR_STOP_DET is a STOP_DET interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x0060	I2C_CLR_STOP_DET	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															clr_stop_det
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:1]	-	reserved	Reserved
[0]	RO	clr_stop_det	Reading this register clears the STOP_DET interrupt.

I2C_CLR_START_DET

I2C_CLR_START_DET is a START_DET interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x0064	I2C_CLR_START_DET	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															clr_start_det
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:1]	-	reserved	Reserved
[0]	RO	clr_start_det	Reading this register clears the START_DET interrupt.

I2C_CLR_GEN_CALL

I2C_CLR_GEN_CALL is a GEN_CALL interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x0068	I2C_CLR_GEN_CALL	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															clr_gen_call
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:1]	-	reserved	Reserved
[0]	RO	clr_gen_call	Reading this register clears the GEN_CALL interrupt.

I2C_ENABLE

I2C_ENABLE is an I^2C enable register for enabling or disabling the I^2C.

When the I^2C is transferring data (I2C_STATUS[activity] is 1), the I^2C can be disabled. Note the following:

- If the I^2C is disabled when it is transmitting data, data transmission is stopped after the current byte is transmitted and data in the TX FIFO is cleared.
- If the I^2C is disabled when it is receiving data, it does not respond to the current transfer and sends NACK after the current byte is received.

Offset Address	Register Name	Total Reset Value
0x006C	I2C_ENABLE	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															i2c_enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:1]	-	reserved	Reserved
[0]	RW	i2c_enable	I^2C enable 0: disabled 1: enabled

I2C_STATUS

I2C_STATUS is an I^2C status register.

Offset Address	Register Name	Total Reset Value
0x0070	I2C_STATUS	0x0006

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved									slv_activity	mst_activity	rff	rfne	tfe	tfnf	activity
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

Bits	Access	Name	Description
[15:7]	-	reserved	Reserved
[6]	RO	slv_activity	Activity of the slave state machine 0: The slave state machine is idle, and the slave part of DW_apb_i2c is inactive. 1: The slave state machine is not idle, and the slave part of DW_apb_i2c is active.
[5]	RO	mst_activity	Activity of the master state machine 0: The master state machine is idle, and the master part of DW_apb_i2c is inactive. 1: The master state machine is not idle, and the master part of DW_apb_i2c is active.
[4]	RO	rff	RX FIFO full indicator 0: not full 1: full
[3]	RO	rfne	RX FIFO empty indicator 0: empty 1: not empty
[2]	RO	tfe	TX FIFO empty indicator 0: not empty 1: empty
[1]	RO	tfnf	TX FIFO full indicator 0: full 1: not full
[0]	RO	activity	I^2C bus status 0: idle 1: busy

I2C_TXFLR

I2C_TXFLR is a TX FIFO data count indicator register.

Offset Address	Register Name	Total Reset Value
0x0074	I2C_TXFLR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved									txflr						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:7]	-	reserved	Reserved
[6:0]	RO	txflr	Number of data segments in the TX FIFO

I2C_RXFLR

I2C_RXFLR is an RX FIFO data count indicator register.

Offset Address	Register Name	Total Reset Value
0x0078	I2C_RXFLR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved									rxflr						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:7]	-	reserved	Reserved
[6:0]	RO	rxflr	Number of data segments in the RX FIFO

I2C_SDA_HOLD

I2C_SDA_HOLD is an SDA hold time register.

Offset Address	Register Name	Total Reset Value
0x007C	I2C_SDA_HOLD	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																i2c_sda_hold															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved
[15:0]	RW	i2c_sda_hold	SDA hold time (in ic_clk cycle)

I2C_TX_ABRT_SOURCE

I2C_TX_ABRT_SOURCE is a TX_ABRT source interrupt register.

Offset Address	Register Name	Total Reset Value
0x0080	I2C_TX_ABRT_SOURCE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																abrt_slvrd_intx	abrt_slv_arblost	abrt_slvflush_txfifo	abrt_lost	abrt_master_dis	abrt_10b_rd_norstrt	abrt_sbyte_norstrt	abrt_hs_norstrt	abrt_sbyte_ackdet	abrt_hs_ackdet	abrt_gcall_read	abrt_gcall_noack	abrt_txdata_noack	abrt_10addr2_noack	abrt_10addr1_noack	abrt_7b_addr_noack
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved
[15]	RO	abrt_slvrd_intx	0: reset value 1: An interrupt is generated when the CPU responds to a request from the slave to transfer data to the remote host but the user writes 1 to the command register.
[14]	RO	abrt_slv_arblost	0: reset value 1: Bus arbitration is lost when the slave is transferring data to the remote master, and I2C_TX_ABRT_SOURCE bit[14] is set.
[13]	RO	abrt_slvflush_txfifo	0: reset value 1: When the slave receives a read command and duplicate data exists in the TX FIFO, the slave sends a TX_ARBT interrupt to flush the original data in the TX FIFO.

Offset Address	Register Name	Total Reset Value
0x0080	I2C_TX_ABRT_SOURCE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																abrt_slvrd_intx	abrt_slv_arblost	abrt_slvflush_txfifo	abrt_lost	abrt_master_dis	abrt_10b_rd_norstrt	abrt_sbyte_norstrt	abrt_hs_norstrt	abrt_sbyte_ackdet	abrt_hs_ackdet	abrt_gcall_read	abrt_gcall_noack	abrt_txdata_noack	abrt_10addr2_noack	abrt_10addr1_noack	abrt_7b_addr_noack
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[12]	RO	abrt_lost	Bus arbitration loss interrupt 0: reset value 1: Arbitration for the master is lost, or arbitration for the slave transfer is lost when I2C_TX_ABRT_SOURCE bit[14] is set.
[11]	RO	abrt_master_dis	Error interrupt cause 0: reset value 1: When the master functionality is disabled, a master operation is initiated.
[10]	RO	abrt_10b_rd_norstrt	Error interrupt cause 0: reset value 1: When the master does not support the restart function, a read command is sent to the slave with a 10-bit address.
[9]	RO	abrt_sbyte_norstrt	Error interrupt cause 0: reset value 1: When the master does not support the restart function, a start byte is sent.
[8]	RO	abrt_hs_norstrt	Error interrupt cause 0: reset value 1: When the master does not support the restart function, high-speed operations are performed.
[7]	RO	abrt_sbyte_ackdet	Error interrupt cause 0: reset value 1: The start byte transmitted from the master is acknowledged.
[6]	RO	abrt_hs_ackdet	Error interrupt cause 0: reset value 1: When the master is transferring data at a high speed, the high-speed host code is acknowledged.

Offset Address	Register Name	Total Reset Value
0x0080	I2C_TX_ABRT_SOURCE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																abrt_slvrd_intx	abrt_slv_arblost	abrt_slvflush_txfifo	abrt_lost	abrt_master_dis	abrt_10b_rd_norstrt	abrt_sbyte_norstrt	abrt_hs_norstrt	abrt_sbyte_ackdet	abrt_hs_ackdet	abrt_gcall_read	abrt_gcall_noack	abrt_txdata_noack	abrt_10addr2_noack	abrt_10addr1_noack	abrt_7b_addr_noack
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[5]	RO	abrt_gcall_read	Error interrupt cause 0: reset value 1: After the master initiates a general call, the CPU sends a read command to the I^2C.
[4]	RO	abrt_gcall_noack	Error interrupt cause 0: reset value 1: The general call initiated by the master is not acknowledged.
[3]	RO	abrt_txdata_noack	Error interrupt cause 0: reset value 1: The address transmitted from the master is acknowledged by the slave, but the transmitted data is not acknowledged.
[2]	RO	abrt_10addr2_noack	Error interrupt cause 0: reset value 1: The second byte in the 10-bit address transmitted from the master is not acknowledged.
[1]	RO	abrt_10addr1_noack	Error interrupt cause 0: reset value 1: The first byte in the 10-bit address transmitted from the master is not acknowledged.
[0]	RO	abrt_7b_addr_noack	Error interrupt cause 0: reset value 1: The 7-bit address transmitted from the master is not acknowledged.

I2C_DMA_CR

I2C_DMA_CR is an I^{2}C DMA channel enable control register.

Offset Address	Register Name	Total Reset Value
0x0088	I2C_DMA_CR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														tdmae	rdmae
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:2]	-	reserved	Reserved
[1]	RW	tdmae	TX FIFO DMA channel enable 0: no 1: yes
[0]	RW	rdmae	RX FIFO DMA channel enable 0: no 1: yes

I2C_DMA_TDLR

I2C_DMA_TDLR is a TX FIFO threshold configuration register for DMA operations.

Offset Address	Register Name	Total Reset Value
0x008C	I2C_DMA_TDLR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										dmatdl					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:6]	-	reserved	Reserved
[5:0]	RW	dmatdl	Threshold for the DMA operation on the TX FIFO

I2C_DMA_RDLR

I2C_DMA_RDLR is an RX FIFO threshold configuration register for DMA operations.

Offset Address	Register Name	Total Reset Value
0x0090	I2C_DMA_RDLR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										dmardl					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:6]	-	reserved	Reserved
[5:0]	RW	dmardl	Threshold for the DMA operation on the RX FIFO. The actual value is equal to the configured value plus 1.

I2C_SDA_SETUP

I2C_SDA_SETUP is an SDA setup time register.

Offset Address	Register Name	Total Reset Value
0x0094	I2C_SDA_SETUP	0x0000_0064

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								i2c_sda_setup							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved
[7:0]	RW	i2c_sda_setup	SDA hold time

I2C_ACK_GENERAL_CALL

I2C_ACK_GENERAL_CALL is a general call response register.

Offset Address	Register Name	Total Reset Value
0x0098	I2C_ACK_GENERAL_CALL	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															ack_gen_call
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved
[0]	RW	ack_gen_call	General call response 0: No general call interrupt is generated when a general call is received. 1: An ACK signal is generated when a general call is received.

I2C_ENABLE_STATUS

I2C_ENABLE_STATUS is an I^2C enable status register.

Offset Address	Register Name	Total Reset Value
0x009C	I2C_ENABLE_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													slv_rx_data_lost	slv_disabled_while_busy	i2c_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	-	reserved	Reserved
[2]	RO	slv_rx_data_lost	This bit indicates whether data reception on the slave stops if I2C_ENABLE changes from 1 to 0 when at least 1 byte has been received.

Offset Address	Register Name	Total Reset Value
0x009C	I2C_ENABLE_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													slv_rx_data_lost	slv_disabled_while_busy	i2c_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1]	RO	slv_disabled_while_busy	This bit indicates whether data reception on the slave stops if I2C_ENABLE changes from 1 to 0.
[0]	RO	i2c_en	DW_apb_i2c enable status

5.3 SPI

5.3.1 Function Description

Features

The serial peripheral interface (SPI) implements serial-to-parallel conversion and parallel-to-serial conversion, and serves as a master or slave to communicate with peripherals in synchronous serial mode.

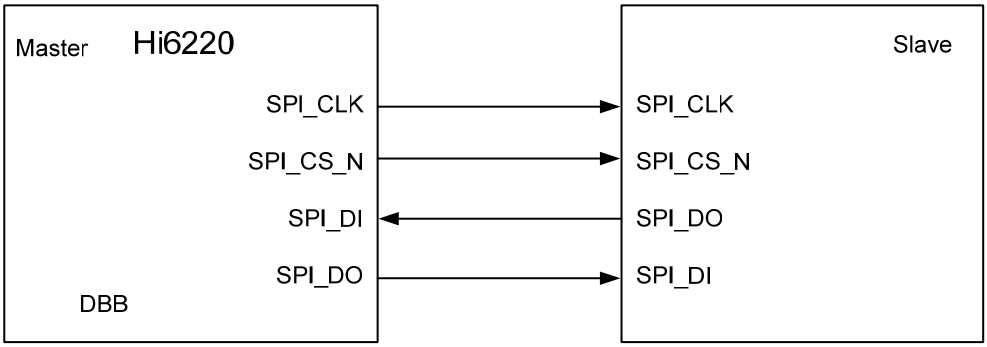
The Hi6220 integrates an SPI module as the master or slave.

The SPI has the following features:

- Supports the programmable interface clock frequency.
- Supports SPI frame formats.
- Supports the programmable serial data frame length ranging from 4 bits to 16 bits.
- Supports TX and RX FIFO interrupts, RX overrun interrupts, and RX timeout interrupts; separately masks each interrupt.
- Supports the internal loopback test mode.
- Supports the DMA operation.
- Acts as the master or slave.

Figure 5-2 shows the application block diagram when the SPI connects to a slave.

Figure 5-2 Application block diagram when the SPI connects to a slave



Operating Modes

The SPI operates in two modes:

- Data transfer in interrupt or query mode
- Data transfer in DMA mode

5.3.2 Register Description

The SPI core used in Hi6220 is build from ARM IP(PL022). Details about the block can be found in DDI0194G_ssp_pl022_r1p3_trm.pdf (Which can also be downloaded from http://infocenter.arm.com/help/topic/com.arm.doc.ddi0194g/DDI0194G_ssp_pl022_r1p3_trm.pdf)

The base address for SPI registers is 0xF710_6000.

5.4 UART

5.4.1 Function Description

The universal asynchronous receiver/transmitter (UART) performs serial-to-parallel conversion on the data from peripherals and parallel-to-serial conversion on the data transmitted to peripherals.

The UART has the following features:

- Supports the configurable data bit width and stop bit width.
  - The width of the data bit can be set to 5 bits, 6 bits, 7 bits, or 8 bits.
  - The width of the stop bit can be set to 1 bit or 2 bits.
- Supports parity check or no check.
- Supports the programmable transfer rate.
- Supports the modem status interrupt, RX FIFO interrupt, TX FIFO interrupt, RX timeout interrupt, and error interrupt.
- Supports flow control for UART1−UART4.

Table 5-4 describes the features of the five UART modules.

Table 5-4 UART features

UART No.	Working Clock	Flow Control	Interrupt	DMA
UART0	19.2 MHz	Supported	Supported	Supported
UART1	150 MHz/19.2 MHz	Supported	Supported	Supported
UART2	150 MHz/19.2 MHz	Supported	Supported	Supported
UART3	150 MHz/19.2 MHz	Supported	Supported	Supported
UART4	150 MHz/19.2 MHz	Supported	Supported	Supported

5.4.2 Register Description

- The base address for UART0 registers is 0xF801_5000.
- The base address for UART1 registers is 0xF711_1000.
- The base address for UART2 registers is 0xF711_2000.
- The base address for UART3 registers is 0xF711_3000.
- The base address for UART4 registers is 0xF711_4000.

Table 5-5 describes UART registers.

Table 5-5 Summary of UART registers

Offset Address	Register	Description
0x000	UART_DR	UART data register
0x004	UART_RSR	RX status register or error clear register
0x018	UART_FR	UART flag register
0x024	UART_IBRD	Integral baud rate register
0x028	UART_FBRD	Decimal baud rate register
0x02C	UART_LCR_H	Transfer mode control register
0x030	UART_CR	UART control register
0x034	UART_IFLS	Interrupt FIFO threshold selection register
0x038	UART_IMSC	Interrupt mask register
0x03C	UART_RIS	Raw interrupt status register
0x040	UART_MIS	Masked interrupt status register
0x044	UART_ICR	Interrupt clear register
0x048	UART_DMACR	DMA control register

UART_DR

UART_DR is a UART data register. It is used to store the data to be received and transmitted. The RX status can be queried by reading this register.

Offset Address	Register Name	Total Reset Value
0x000	UART_DR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				oe	be	pe	fe	data							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:12]	-	reserved	Reserved
[11]	RO	oe	Overflow error 0: No overflow error occurs. 1: An overflow error occurs. The RX FIFO is full and a data segment has been received.
[10]	RO	be	Break error 0: No break error occurs. 1: A break error occurs. That is, the RX data input signal retains low longer than a full word transfer. A full word consists of a start bit, data bits, a parity bit, and a stop bit.
[9]	RO	pe	Parity error 0: No parity error occurs. 1: A parity error occurs in the received data.
[8]	RO	fe	Frame error 0: No frame error occurs. 1: A frame error occurs in the received data (incorrect stop bit).
[7:0]	RW	data	Data to be transmitted and received

UART_RSR

UART_RSR is an RX status register or error clear register.

- It acts as the RX status register when being read.
- It acts as the error clear register when being written.

The RX status can also be obtained by reading UART_DR. The status information about the break, frame, and parity read from UART_DR takes priority over that read from UART_RSR. That is, the status information in UART_DR changes faster than that in UART_RSR.

Writing any value to UART_RSR resets it.

Offset Address	Register Name	Total Reset Value
0x004	UART_RSR	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved				oe	be	pe	fe
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:4]	-	reserved	Reserved
[3]	RW	oe	Overflow error 0: No overflow error occurs. 1: An overflow error occurs. When the FIFO is full, the contents in the FIFO remain valid. No data will be written to the FIFO and the shift register overflows. In this case, the CPU must read data immediately to spare the FIFO.
[2]	RW	be	Break error 0: No break error occurs. 1: A break error occurs. If the RX data input signal remains low longer than a full word transfer, a break error is considered. A full word consists of a start bit, data bits, a parity bit, and a stop bit.
[1]	RW	pe	Parity error 0: No parity error occurs. 1: A parity error occurs in the received data. In FIFO mode, the error is associated with the data at the top of the FIFO.
[0]	RW	fe	Frame error 0: No frame error occurs. 1: An error occurs in the stop bit of the received data. The valid stop bit is 1.

UART_FR

UART_FR is a UART flag register.

Offset Address	Register Name	Total Reset Value
0x018	UART_FR	0x0010

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								txfe	rxff	txff	rxfe	busy	reserved		cts
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[15:8]	-	reserved	Reserved
[7]	RO	txfe	This bit depends on the status of UART_LCR_H[fen]. If UART_LCR_H[fen] is 0, the bit is set to 1 when the TX holding register is empty. If UART_LCR_H[fen] is 1, the bit is set to 1 when the TX FIFO is empty.
[6]	RO	rxff	This bit depends on the status of UART_LCR_H[fen]. If UART_LCR_H[fen] is 0, the bit is set to 1 when the RX holding register is full. If UART_LCR_H[fen] is 1, the bit is set to 1 when the RX FIFO is full.
[5]	RO	txff	This bit depends on the status of UART_LCR_H[fen]. If UART_LCR_H[fen] is 0, the bit is set to 1 when the TX holding register is full. If UART_LCR_H[fen] is 1, the bit is set to 1 when the TX FIFO is full.
[4]	RO	rxfe	This bit depends on the status of UART_LCR_H[fen]. If UART_LCR_H[fen] is 0, the bit is set to 1 when the RX holding register is empty. If UART_LCR_H[fen] is 1, the bit is set to 1 when the RX FIFO is empty.
[3]	RO	busy	UART busy/idle status 0: The UART is idle or data transmission is complete. 1: The UART is busy transmitting data. If this bit is set to 1, the status is retained until the entire byte (including all stop bits) is transmitted from the shift register. No matter whether the UART is enabled, this bit is set to 1 when the TX FIFO is not empty.
[2:1]	-	reserved	Reserved
[0]	-	cts	Inversion of nUARTCTS (UARTx_CTS_N). If the modem status input is 0, the bit is 1.

UART_IBRD

UART_IBRD is an integral baud rate register.

Offset Address	Register Name	Total Reset Value
0x024	UART_IBRD	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	bauddivint															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:0]	RW	bauddivint	Clock divider corresponding to the integral part of the baud rate. All bits are cleared during reset.

UART_FBRD

UART_FBRD is a decimal baud rate register.

CAUTION

- The values of UART_IBRD and UART_FBRD can be updated until the current data is transmitted and received completely.
- The minimum clock divider is 1, and the maximum clock divider is 65,535 ($2^{16} - 1$). That is, UART_IBRD cannot be 0 and UART_FBRD is ignored if UART_IBRD is 0. If UART_IBRD is equal to 65,535 (0xFFFF), UART_FBRD must be 0. If UART_FBRD is greater than 0, data transmission and data reception fail.
- Assume that UART_FBRD is set to 0x1E and UART_IBRD is set to 0x01. In this case, the integral part of the clock divider is 30, and the decimal part of the clock divider is 0.015625. Therefore, the clock divider is 30.015625.
- UART baud rate = Internal bus frequency/(16 x Clock divider) = Internal bus frequency/(16 x 30.015625)

Offset Address	Register Name	Total Reset Value
0x028	UART_FBRD	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	banddivfrac															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:0]	RW	banddivfrac	Clock divider corresponding to the decimal part of the baud rate

UART_LCR_H

UART_LCR_H is a transfer mode control register. UART_LCR_H, UART_IBRD, and UART_FBRD constitute a 30-bit register. If UART_IBRD and UART_FBRD are updated, UART_LCR_H must be updated at the same time.

Offset Address	Register Name	Total Reset Value
0x02C	UART_LCR_H	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								sps	wlen		fen	stp2	eps	pen	brk
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:8]	-	reserved	Reserved
[7]	RW	sps	Parity select When bit 1, bit 2, and bit 7 of this register are set to 1, the parity bit is 0 during transmission and detection. When bit 1 and bit 7 are set to 1 and bit 2 is set to 0, the parity bit is 1 during transmission and detection. When bit 1, bit 2, and bit 7 are cleared, the stick parity bit is disabled.
[6:5]	RW	wlen	Count of bits in a transmitted or received frame 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits
[4]	RW	fen	TX/RX FIFO enable 0: disabled 1: enabled
[3]	RW	stp2	Whether a 2-bit stop bit exists at the end of a transmitted frame 0: There is no 2-bit stop bit at the end of the transmitted frame. 1: There is a 2-bit stop bit at the end of the transmitted frame. The RX logic does not check for the 2-bit stop bit during data reception.
[2]	RW	eps	Parity bit select during data transmission and reception 0: The odd parity bit is generated or checked during data transmission and reception. 1: The even parity bit is generated or checked during data transmission and reception. This bit is invalid when UART_LCR_H[fen] is 0.

Offset Address	Register Name	Total Reset Value
0x02C	UART_LCR_H	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								sps	wlen		fen	stp2	eps	pen	brk
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1]	RW	pen	Parity check enable 0: The parity check is disabled. 1: The parity bit is generated at the TX end and checked at the RX end.
[0]	RW	brk	TX break 0: invalid 1: After the current data transmission is complete, the UTXD outputs low level continuously. Note: This bit must retain 1 for at least two full frames to ensure that the break command is executed properly. In normal cases, this bit must be set to 0.

UART_CR

UART_CR is a UART control register.

To configure UART_CR, perform the following steps:

Step 1 Write 0 to UART_CR bit[0] to disable the UART.

Step 2 Wait until the current data transmission or reception is complete.

Step 3 Clear UART_LCR_H[fen].

Step 4 Configure UART_CR.

Step 5 Write 1 to UART_CR bit[0] to enable the UART.

----End

Offset Address	Register Name	Total Reset Value
0x030	UART_CR	0x0300

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ctsen	rtsen	reserved		rts	dtr	rxe	txe	lbe	reserved						uarten
Reset	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15]	RW	ctsen	CTS hardware flow control enable 0: disabled 1: enabled. Data can be transmitted only when the nUARTCTS signal is valid.
[14]	RW	rtsen	RTS hardware flow control enable 0: disabled 1: enabled. The data RX request can be sent only when the RX FIFO has free space.
[13:12]	-	reserved	Reserved
[11]	RW	rts	Request TX This bit is the inversion of the status output signal nUARTRTS of the UART modem. 0: The output signal is retained. 1: The output signal is 0.
[10]	RW	dtr	Data TX ready This bit is the inversion of the status output signal nUARTDTR of the UART modem. 0: The output signal is retained. 1: The output signal is 0.
[9]	RW	rxe	UART RX enable 0: disabled 1: enabled If the UART is disabled during data reception, the current data reception ends before data is received completely.
[8]	RW	txe	UART TX enable 0: disabled 1: enabled If the UART is disabled during data transmission, the current data transmission ends before the data is transmitted completely.

Offset Address	Register Name	Total Reset Value
0x030	UART_CR	0x0300

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ctsen	rtsen	reserved		rts	dtr	rxe	txe	lbe	reserved						uarten
Reset	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7]	RW	lbe	Loopback enable 0: disabled 1: UARTTXD output is looped back to UARTRXD.
[6:1]	-	reserved	Reserved
[0]	RW	uarten	UART enable 0: disabled 1: enabled If the UART is disabled during data reception and transmission, the current data transfer ends before data is transmitted and received completely.

UART_IFLS

UART_IFLS is an interrupt FIFO threshold selection register. It is used to set the threshold for triggering the FIFO interrupt (UART_TXINTR or UART_RXINTR).

Offset Address	Register Name	Total Reset Value
0x034	UART_IFLS	0x0012

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved							rtsflsel			rxiflsel			txiflsel		
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0

Bits	Access	Name	Description
[15:9]	-	reserved	Reserved

Offset Address	Register Name	Total Reset Value
0x034	UART_IFLS	0x0012

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved							rtsflsel			rxiflsel			txiflsel		
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0

Bits	Access	Name	Description
[8:6]	RW	rtsflsel	RX FIFO level corresponding to the RTS flow control. The RTS is triggered when any of the following conditions is met: 000: RX FIFO ≥ 1/8 full 001: RX FIFO ≥ 1/4 full 010: RX FIFO ≥ 1/2 full 011: RX FIFO ≥ 3/4 full 100: RX FIFO ≥ 7/8 full 101: RX FIFO ≥ full − 2 110−111: reserved Note: The RTS flow control threshold must be greater than or equal to the RX interrupt threshold. The value 101 is recommended. The bit applies only to the UART1/2 interrupt.
[5:3]	RW	rxiflsel	RX interrupt FIFO threshold. An RX interrupt is triggered when any of the following conditions is met: 000: RX FIFO ≥ 1/8 full 001: RX FIFO ≥ 1/4 full 010: RX FIFO ≥ 1/2 full 011: receive FIFO ≥ 3/4 full 100: RX FIFO ≥ 7/8 full 101−111: reserved
[2:0]	RW	txiflsel	TX interrupt FIFO threshold. A TX interrupt is triggered when any of the following conditions is met: 000: TX FIFO ≤ 1/8 full 001: TX FIFO ≤ 1/4 full 011: TX FIFO ≤ 3/4 full 010: TX FIFO ≤ 1/2 full 100: TX FIFO ≤ 7/8 full 101−111: reserved

UART_IMSC

UART_IMSC is an interrupt mask register. The value 0 indicates that the interrupt is masked, and the value 1 indicates that the interrupt is not masked.

Offset Address	Register Name	Total Reset Value
0x038	UART_IMSC	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					oeim	beim	peim	feim	rtim	txim	rxim	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:11]	-	reserved	Reserved
[10]	RW	oeim	Overflow error interrupt mask
[9]	RW	beim	Break error interrupt mask
[8]	RW	peim	Parity check interrupt mask
[7]	RW	feim	Frame error interrupt mask
[6]	RW	rtim	RX timeout interrupt mask
[5]	RW	txim	TX interrupt mask
[4]	RW	rxim	RX interrupt mask
[3:0]	-	reserved	Reserved

UART_RIS

UART_RIS is a raw interrupt status register. The contents of this register are not affected by the UART_IMSC register. The value 0 indicates that no interrupt is generated, and the value 1 indicates that an interrupt is generated.

Offset Address	Register Name	Total Reset Value
0x03C	UART_RIS	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					oeris	beris	peris	feris	rtris	txris	rxris	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:11]	-	reserved	Reserved

Offset Address	Register Name	Total Reset Value
0x03C	UART_RIS	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					oeris	beris	peris	feris	rtris	txris	rxris	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[10]	RO	oeris	Raw overflow error interrupt status
[9]	RO	beris	Raw break error interrupt status
[8]	RO	peris	Raw parity check interrupt status
[7]	RO	feris	Raw error interrupt status
[6]	RO	rtris	Raw RX timeout interrupt status
[5]	RO	txris	Raw TX interrupt status
[4]	RO	rxris	Raw RX interrupt status
[3:0]	-	reserved	Reserved

UART_MIS

UART_MIS is a masked interrupt status register. The values of this register are the results obtained after UART_RIS is ANDed with UART_IMSC. The value 0 indicates that no interrupt is generated, and the value 1 indicates that an interrupt is generated.

Offset Address	Register Name	Total Reset Value
0x040	UART_MIS	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					oemis	bemis	pemis	femis	rtmis	txmis	rxmis	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:11]	-	reserved	Reserved
[10]	RO	oemis	Masked overflow error interrupt status
[9]	RO	bemis	Masked break error interrupt status
[8]	RO	pemis	Masked parity check interrupt status
[7]	RO	femis	Masked error interrupt status

Offset Address	Register Name	Total Reset Value
0x040	UART_MIS	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					oemis	bemis	pemis	femis	rtmis	txmis	rxmis	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[6]	RO	rtmis	Masked RX timeout interrupt status
[5]	RO	txmis	Masked TX interrupt status
[4]	RO	rxmis	Masked RX interrupt status
[3:0]	-	reserved	Reserved

UART_ICR

UART_ICR is an interrupt clear register. Writing 1 clears the corresponding interrupt, and writing 0 has no effect.

Offset Address	Register Name	Total Reset Value
0x044	UART_ICR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					oeic	beic	peic	feic	rtic	txic	rxic	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:11]	-	reserved	Reserved
[10]	WO	oeic	Overflow error interrupt clear
[9]	WO	beic	Break error interrupt clear
[8]	WO	peic	Parity check interrupt clear
[7]	WO	feic	Error interrupt clear
[6]	WO	rtic	RX timeout interrupt clear
[5]	WO	txic	TX interrupt clear
[4]	WO	rxic	RX interrupt clear
[3:0]	-	reserved	Reserved

UART_DMACR

UART_DMACR is a DMA control register. It is used to enable or disable the DMAs of the TX and RX FIFOs.

Offset Address	Register Name	Total Reset Value
0x048	UART_DMACR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													dmaonerr	txdmae	rxdmae
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:3]	-	reserved	Reserved
[2]	RW	dmaonerr	DMA enable control for the RX channel when the UART error interrupt (UARTEINTR) occurs. 0: When UARTEINTR is valid, the DMA output request (UARTRXDMASREQ or UARRTXDMABREQ) of the RX channel is valid. 1: When UARTEINTR is valid, the DMA output request (UARTRXDMASREQ or UARRTXDMABREQ) of the RX channel is invalid.
[1]	RW	txdmae	TX FIFO DMA enable 0: disabled 1: enabled
[0]	RW	rxdmae	RX FIFO DMA enable 0: disabled 1: enabled

5.5 USB 2.0

5.5.1 OTG Subsystem

5.5.1.1 Function Description

The Hi6220 USB on-the-go (OTG) consists of the USB 2.0 controller and USB PHY. It can act as a host, device, or OTG 2.0. As a device or OTG-B, the USB OTG connects to the PC or other USB host. As a host or OTG-A, the USB OTG connects to the USB flash drive or other USB device.

The USB OTG has the following features:

- Complies with the USB 2.0 and OTG 2.0 protocols.
- Supports the HS, FS, and LS in host/OTG-A mode.
- Supports the HS and FS in device/OTG-B mode.
- Supports the Session Request Protocol (SRP), Host Negotiation Protocol (HNP), and Attach Detection Protocol (ADP) of OTGA 2.0, which is downward compatible with OTG 1.3.
- Supports the Link Power Management (LPM) protocol.
- Supports the Battery Charging 1.1/1.2 protocol.
- Supports a maximum of 16 IN endpoints and 16 OUT endpoints when acting as a device or OTG-B.
- Uses endpoint 0 as the control endpoint when acting as a device or OTG-B. The type of endpoint 1 to endpoint 15 can be set to control, bulk, isochronous, or interrupt.
- Provides a separate TX FIFO for each endpoint when acting as a device or OTG-B. The FIFO size can be dynamically configured, and all endpoints share an RX FIFO.
- Supports a maximum of 16 channels when acting as a host or OTG-A.
- Configures the sizes of the periodic TX FIFO, non-periodic TX FIFO, and RX FIFO when acting as a host or OTG-A.
- Provides a built-in DMAC that can be operated in scatter/gather or buffer DMA mode.
- The controller supports the application of point to point and doesn't support split and hub transfer when acting as a host or OTG-A.

DMA Features

The USB 2.0 OTG supports the built-in DMA in buffer or linked list (scatter or gather) DMA mode.

As a host or OTG-A, the USB 2.0 OTG supports a maximum of 16 DMA channels. Each transfer channel corresponds to a DMA channel.

When the USB 2.0 OTG acts as a device or OTG-B, each IN endpoint or OUT endpoint has an independent DMA channel.

5.5.2 Register Description

The USB core used in Hi6220 is build from Synopsys IP(3.00a). Details about the block can be found in DWC_otg_databook.pdf and DWC_otg_programming .pdf(Which can also be downloaded from https://www.synopsys.com/dw/ipdir.php?ds=dwc_usb_2_0_hs_otg)

The base address for USB registers is 0xF72C_0000.

A ACPU Interrupts

Table A-1 describes the ACPU interrupts of the Hi6220.

- 0−15: software generated interrupts (SGIs)
- 16−31: private peripheral interrupts (PPIs)
- 32−159: shared peripheral interrupts

Table A-1 ACPU interrupt vectors

ID	Interrupt Source	Interrupt Description
0−7	SGI_NS_intr	Software configuration interrupts of the ARM core In the system supporting the security extension, it is strongly recommended that ID0−ID7 be used for non-secure interrupts and ID8−ID15 be used for secure interrupts for all processors.
8−15	SGI_S_intr	
16−26	Reserved	Reserved interrupt of the ARM core
27−31	CoreInter_intrs	Internal timer/watchdog interrupts of the ARM core
32-38	Reserved	Reserved
39	Tsensor_intr	Temperature sensor interrupt
40	RTC1_intr	RTC1 interrupt
41-43	Reserved	Reserved
44	RTC0_intr	RTC0 interrupt
45	WDog0_intr	ACPU watchdog interrupt
46	Timer0_intr	AP Dual_Timer0_0 interrupt
47	Timer1_intr	AP Dual_Timer0_1 interrupt
48	Timer2_intr	AP Dual_Timer1_0 interrupt
49	Timer3_intr	AP Dual_Timer1_1 interrupt

ID	Interrupt Source	Interrupt Description
50	Timer4_intr	AP Dual_Timer2_0 interrupt
51	Timer5_intr	AP Dual_Timer2_1 interrupt
52	Timer6_intr	AP Dual_Timer3_0 interrupt
53	Timer7_intr	AP Dual_Timer3_1 interrupt
54	Timer8_intr	AP Dual_Timer4_0 interrupt
55	Timer9_intr	AP Dual_Timer4_1 interrupt
56	Timer10_intr	AP Dual_Timer5_0 interrupt
57	Timer11_intr	AP Dual_Timer5_1 interrupt
58	Timer12_intr	AP Dual_Timer6_0 interrupt
59	Timer13_intr	AP Dual_Timer6_1 interrupt
60	Timer14_intr	AP Dual_Timer7_0 interrupt
61	Timer15_intr	AP Dual_Timer7_1 interrupt
62	Timer16_intr	AP Dual_Timer8_0 interrupt
63	Timer17_intr	AP Dual_Timer8_1 interrupt
64-67	Reserved	Reserved
68	UART0_intr	UART0 interrupt, for product line calibration and software debugging
69	UART1_intr	UART1 interrupt, for the BT (shared with the Hi1101 BT and GPS)
70	UART2_intr	UART2 interrupt, for the separate GPS and debugging
71	UART3_intr	UART3 interrupt, for the third-party modem and CL interoperation
72	UART4_intr	UART4 interrupt, for the third-party modem loading
73-75	Reserved	Reserved
76	I2C0_intr	I^2C0 interrupt, for the camera flash, NFC, and charger
77	I2C1_intr	I^2C1 interrupt, for the touch key, keypad (KP), and touch panel (TP)
78	I2C2_intr	I^2C2 interrupt, for sensors (magnetic sensor/acceleration sensor/gyroscope/ambient light sensor+proximity sensor/barometer)
79	I2C3_intr	Backup

ID	Interrupt Source	Interrupt Description
80-81	Reserved	Reserved
82	SSP_intr	SPI interrupt
83	Reserved	Reserved
84	GPIO0_intr0	GPIO0-to-APCU combined interrupt (8 bits)
85	GPIO1_intr0	GPIO1-to-APCU combined interrupt (8 bits)
86	GPIO2_intr0	GPIO2-to-APCU combined interrupt (8 bits)
87	GPIO3_intr0	GPIO3-to-APCU combined interrupt (8 bits)
88	GPIO4_intr0	GPIO4-to-APCU combined interrupt (8 bits)
89	GPIO5_intr0	GPIO5-to-APCU combined interrupt (8 bits)
90	GPIO6_intr0	GPIO6-to-APCU combined interrupt (8 bits)
91	GPIO7_intr0	GPIO7-to-APCU combined interrupt (8 bits)
92	GPIO8_intr0	GPIO8-to-APCU combined interrupt (8 bits)
93	GPIO9_intr0	GPIO9-to-APCU combined interrupt (8 bits)
94	GPIO10_intr0	GPIO10-to-APCU combined interrupt (8 bits)
95	GPIO11_intr0	GPIO11-to-APCU combined interrupt (8 bits)
96	GPIO12_intr0	GPIO12-to-APCU combined interrupt (8 bits)
97	GPIO13_intr0	GPIO13-to-APCU combined interrupt (8 bits)
98	GPIO14_intr0	GPIO14-to-APCU combined interrupt (8 bits)
99	GPIO15_intr0	GPIO15-to-APCU combined interrupt (8 bits)
100	GPIO16_intr0	GPIO16-to-APCU combined interrupt (8 bits)
101	GPIO17_intr0	GPIO17-to-APCU combined interrupt (8 bits)
102	GPIO18_intr0	GPIO18-to-APCU combined interrupt (8 bits)
103	GPIO19_intr0	GPIO19-to-APCU combined interrupt (8 bits)
104	eMMC_intr	eMMC card controller interrupt (SDMMC0)
105	SDMMC_intr	SD card controller interrupt (SDMMC1)
106	SDIOMMC_intr	SDIO card controller interrupt (SDMMC2)
107-108	Reserved	Reserved
109	USB2OTG_intr	USB 2.0 OTG interrupt
110	USB2OTG_BC_intr	Battery charge interrupt (from the SC)

ID	Interrupt Source	Interrupt Description
111	ADE_SEC_intr	ADE secure interrupt
112	DDRC_intr	Combined interrupt of the MDDRC qos_buf interrupt, traffic statistics period reach interrupt, and debug interrupt
113	AEDMAC0_NS_intr	AP EDMAC non-secure interrupt 0
114-115	Reserved	Reserved
116	AEDMAC0_S_intr	AP EDMAC non-secure interrupt 0
117-130	Reserved	Reserved
131	ACPU_PMUIRQ_intr	Combined interrupt of the eight core performance monitoring unit interrupts of the two clusters of the ACPU
132	ACPU_Cluster0_AXI_Error_intr	ACPU cluster 0 AXI bus error interrupt
133	ACPU_Cluster1_AXI_Error_intr	ACPU cluster 1 AXI bus error interrupt
134	Reserved	Reserved
135	ACPU_CTIIRQ_intr	Combined interrupt of the eight core CoreSight interrupts of the two clusters of the ACPU
136	Reserved	Reserved
137	Reserved	Reserved
138	Reserved	Reserved
139	Reserved	Reserved
140	ACPU_COMM_RXTX_COMB_intr	Combined interrupt of the eight core COMMRX and COMMTX interrupts of the two clusters of the ACPU
141	ACPU_SOFT_FIQ_intr	Soft FIQ interrupt from the secure the AO_SC to the ACPU
142	G3D_intr	G3D interrupt
143-145	Reserved	Reserved
146	ADE_intr	ADE interrupt
147	ADE_LDI_intr	ADE_LDI interrupt
148	MIPI_DSI_intr	MIPI_DSI interrupt

ID	Interrupt Source	Interrupt Description
149-151	Reserved	Reserved
152	ISP_intr	ISP interrupt
153	MIPI_CSI0_intr	MIPI_CSI0 interrupt
154	MIPI_CSI1_intr	MIPI_CSI1 interrupt
155	DigACodec_intr	Audio CODEC digital part interrupt
156	ACPU_Cluster0_IRQFIQOUT_CORE0_intr	Combined interrupt of the wakeup interrupts of the four cores of cluster 0 (for ACPU cluster 0 core 0)
157	ACPU_Cluster1_IRQFIQOUT_CORE0_intr	Combined interrupt of the wakeup interrupts of the four cores of cluster 1 (for ACPU cluster 1 core 0)
158-159	Reserved	Reserved

B Address Allocation for Registers and Memories

Table B-1 describes the base addresses for the DBB registers of the SoC.

Table B-1 Address ranges of register groups and memories

Functional Module	Width	Start Address	Bit Width
BOOTROM	32K	0xFFFF0000	32
SRAM_OFF	72K	0xFFF80000	32
UART0	4KB	0xF8015000	32
GPIO3	4KB	0xF8014000	32
GPIO2	4KB	0xF8013000	32
GPIO1	4KB	0xF8012000	32
GPIO0	4KB	0xF8011000	32
Timer8	4KB	0xF8010000	32
Timer7	4KB	0xF800F000	32
Timer6	4KB	0xF800E000	32
Timer5	4KB	0xF800D000	32
Timer4	4KB	0xF800C000	32
Timer3	4KB	0xF800B000	32
Timer2	4KB	0xF800A000	32
Timer1	4KB	0xF8009000	32
Timer0	4KB	0xF8008000	32
Watchdog0	4KB	0xF8005000	32
RTC1	4KB	0xF8004000	32

Functional Module	Width	Start Address	Bit Width
RTC0	4KB	0xF8003000	32
AP_DMAC	4KB	0xF7370000	32
USB	256KB	0xF72C0000	32
SDIOMMC	4KB	0xF723F000	32
SDMMC	4KB	0xF723E000	32
eMMC	4KB	0xF723D000	32
UART4	4KB	0xF7114000	32
UART3	4KB	0xF7113000	32
UART2	4KB	0xF7112000	32
UART1	4KB	0xF7111000	32
SSP	4KB	0xF7106000	32
I2C3	4KB	0xF7103000	32
I2C2	4KB	0xF7102000	32
I2C1	4KB	0xF7101000	32
I2C0	4KB	0xF7100000	32
PERI_SCTRL	8KB	0xF7030000	32
GPIO19	4KB	0xF702F000	32
GPIO18	4KB	0xF702E000	32
GPIO17	4KB	0xF702D000	32
GPIO16	4KB	0xF702C000	32
GPIO15	4KB	0xF702B000	32
GPIO14	4KB	0xF702A000	32
GPIO13	4KB	0xF7029000	32
GPIO12	4KB	0xF7028000	32
GPIO11	4KB	0xF7027000	32
GPIO10	4KB	0xF7026000	32
GPIO9	4KB	0xF7025000	32
GPIO8	4KB	0xF7024000	32
GPIO7	4KB	0xF7023000	32
GPIO6	4KB	0xF7022000	32
GPIO5	4KB	0xF7021000	32

Functional Module	Width	Start Address	Bit Width
GPIO4	4KB	0xF7020000	32
ACPU_CCI	64KB	0xF6E00000	32
ACPU_GIC	32KB	0xF6800000	32
ACPU_CLUSTER0	128KB	0xF6580000	32
ACPU_CLUSTER1	128KB	0xF65c0000	32
MEDIA_XG2RAM_ADE	256K	0xF5000000	32
MEDIA_XG2RAM_HARQ	1M	0xF5000000	32
CSI	4KB	0xF4510000	32
MEDIA_SCTRL	4KB	0xF4410000	32
VPU_S	4KB	0xF4311000	32
JPU_S	4KB	0xF4310000	32
SMMU_S	64KB	0xF4210000	32
ADE_S	64KB	0xF4100000	32
G3D_S	192KB	0xF4080000	32
ISP_S	512KB	0xF4000000	32

