

Project Name :Bubblegum96_S900

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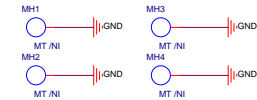
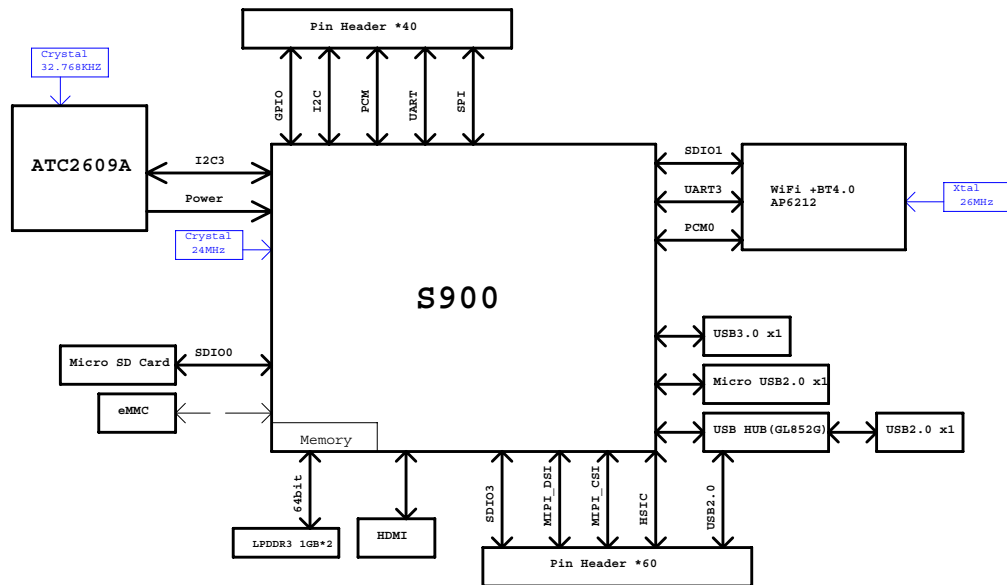
Revision History :

Rev.	Description	Editor	Date
0.9	Initial		2015.04.17
1.0	UPDATE		2015.11.06



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Bubblegum-96 Block_Diagram

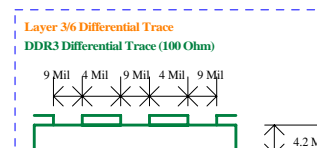
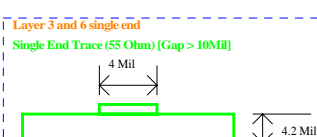
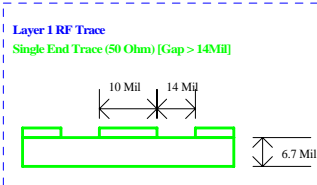
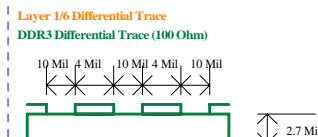
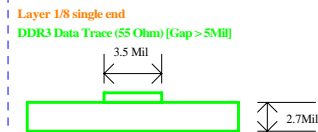
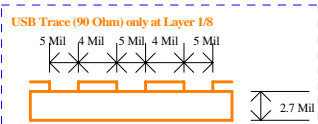
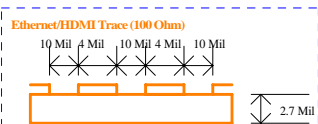


- Operating Temp:
- Storage Temp:
- Dimension: 90mmx60 mm
- Thickness : 8L/1.6mm

PCB Stack 8 layers Tg 150

1 OZ	pp 1080	1.3-1.6 Mil	0.4-1.2 Mil (Solder Mask thickness)
1 OZ	core	2.7 Mil	1.2-1.4 Mil (without copper thickness)
1 OZ	core	4 Mil	1.2-1.4 Mil (without copper thickness)
1 OZ	core	39.9 Mil	1.2-1.4 Mil (with copper thickness)
1 OZ	core	4 Mil	1.2-1.4 Mil (without copper thickness)
1 OZ	pp 1080	2.7 Mil	1.2-1.4 Mil (without copper thickness)
1 OZ	pp 1080	1.3-1.6 Mil	0.4-1.2 Mil (Solder Mask thickness)

63.4 mil +/-10%



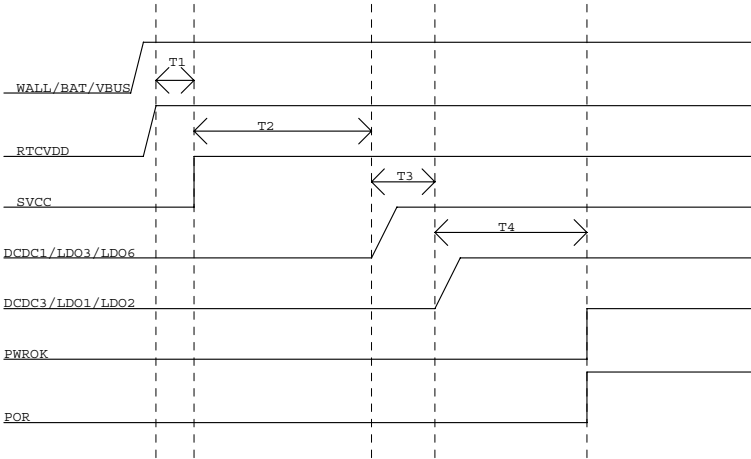
ATC2609 Application frame

1. PMU(ATC2609) Power on Status

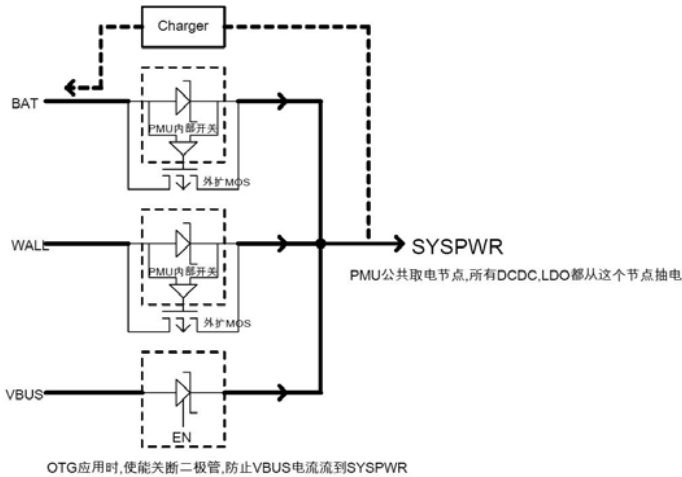
V:Power ON O:Power ON form SW Control X:Power OFF

		Assignment	Imax@Vout	Default Power State @Diff SYS Mode			
				S1:Working Mode	S2:Standby Mode	S3:Sleep Mode	S4:DeepSleep Mode
DC-DC 類	DC-DC0	VDD_CORE	2000mA@0.9V	O	O	X	X
	DC-DC1	CPU_VDD	3000mA@0.9V	O	O	X	X
	DC-DC2	LP_VDDQ_1V2	2000mA@1.2V	O	O	X	X
	DC-DC3	VCC3V1	1200mA@3.1V	O	O	X	X
	DC-DC4		2000mA@0.9V	O	O	X	X
LDO類	LDO0	SD_VCC	500mA@3.1V	O	O	X	X
	LDO1	WiFi_3V3	500mA@3.3V	O	O	X	X
	LDO2	AVCC3V1	500mA@3.1V	V		X	X
	LDO4	AVCC1V8#	2000mA@1.8V	O	O	X	X
	LDO6	AVDD1V0	2000mA@1.0V	O	O	X	X
	LDO7	VCC1V8_IO	200mA@1.2/1.5/1.8V	O	O	X	X
	LDO8	TPVCC3V1	2000mA@3.1V	O	O	X	X

2. PMU(ATC2609) Power On Sequence



3. PMU(ATC2609) APDS frame



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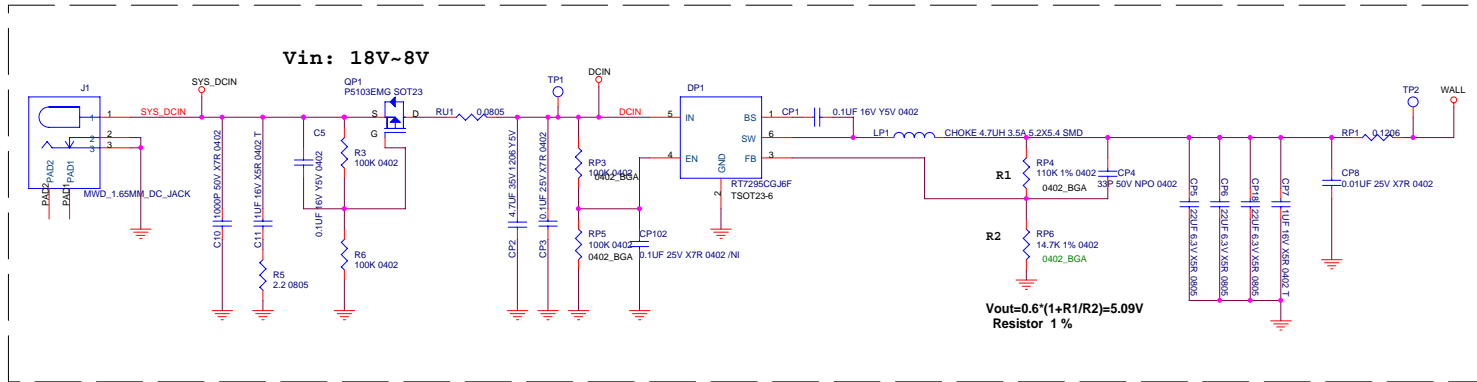
DC Adapter IN

PCB Layout Trace Width

80Mil

50Mil

20Mil



PCB



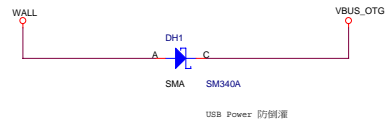
96BOARDS_S900_V1.0

HEATSINK

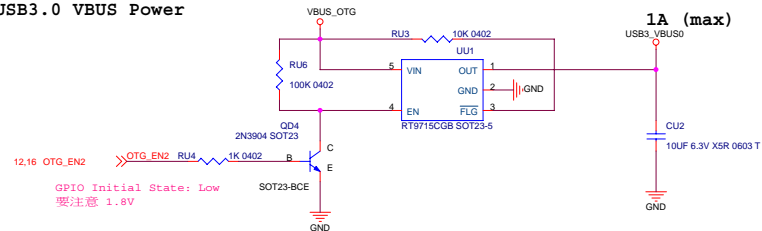


HEATSINK 21x21x5.2(B)

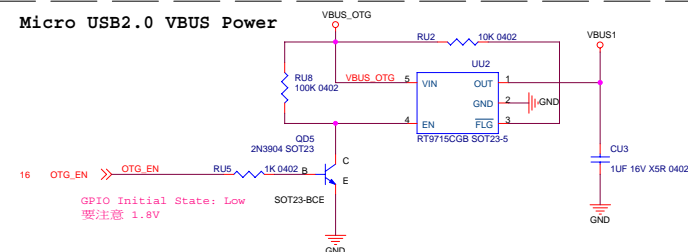
USB1/USB2/USB3 HOST Power



USB3.0 VBUS Power

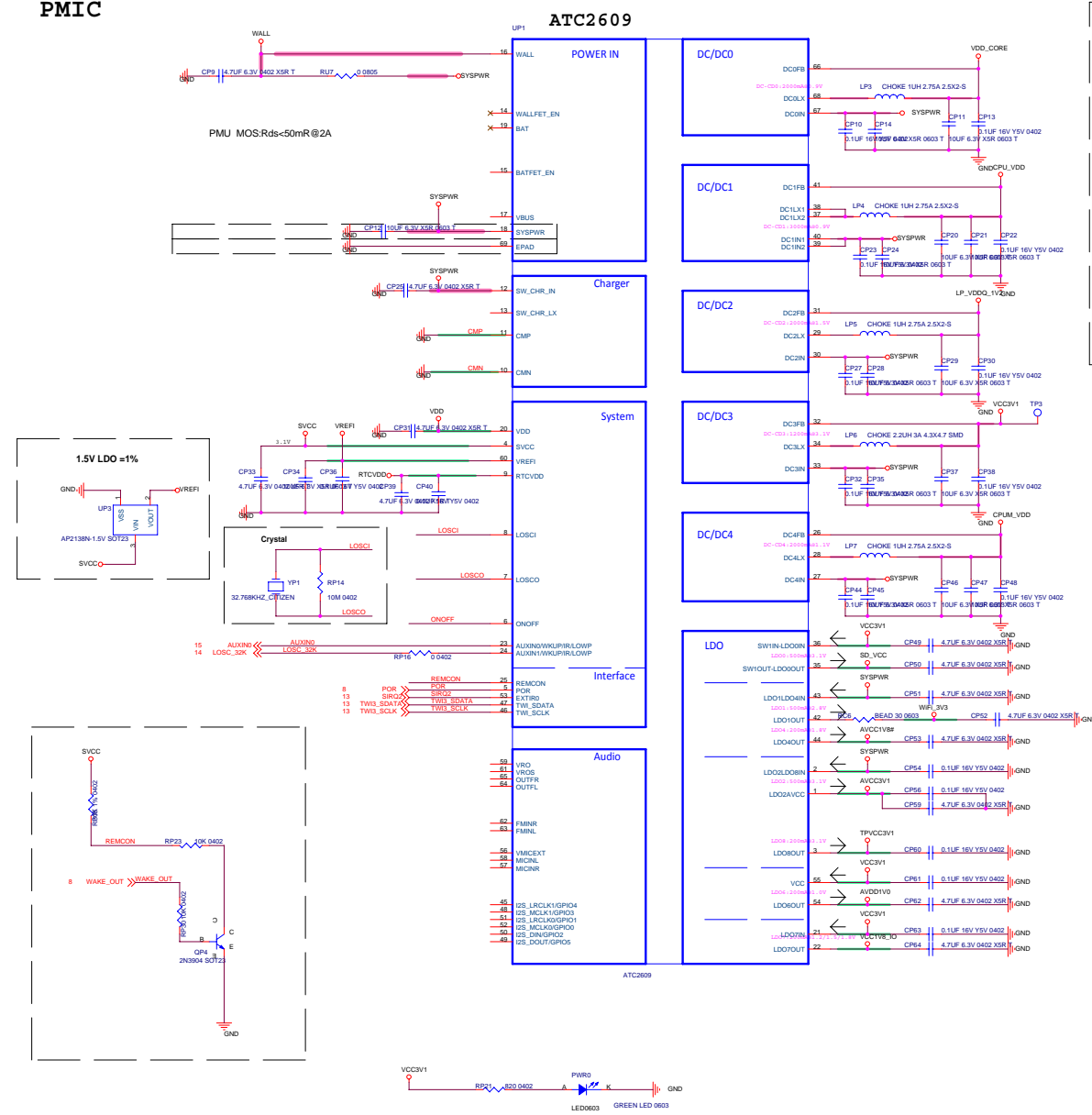


Micro USB2.0 VBUS Power

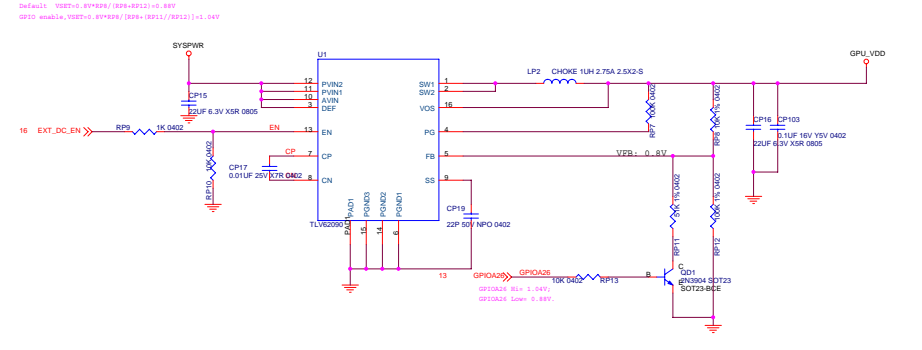


PMIC

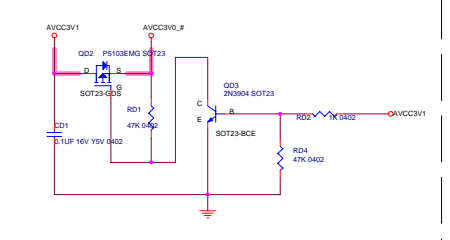
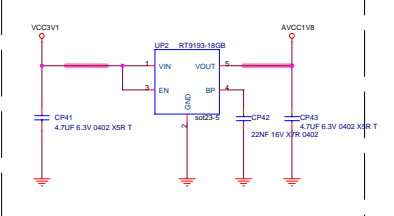
ATC2609



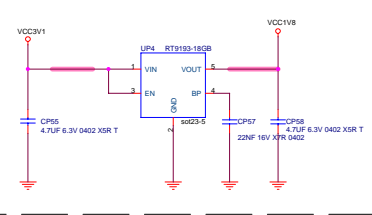
GPUVDD:TLV62090 Imax=3A



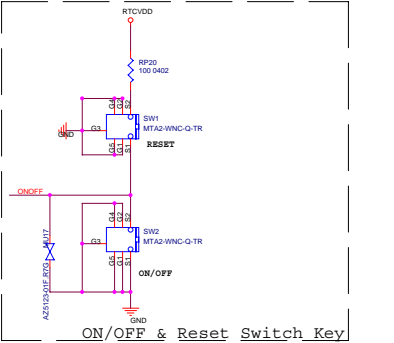
AVCC1V8

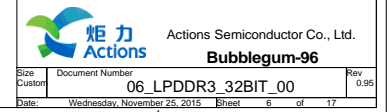
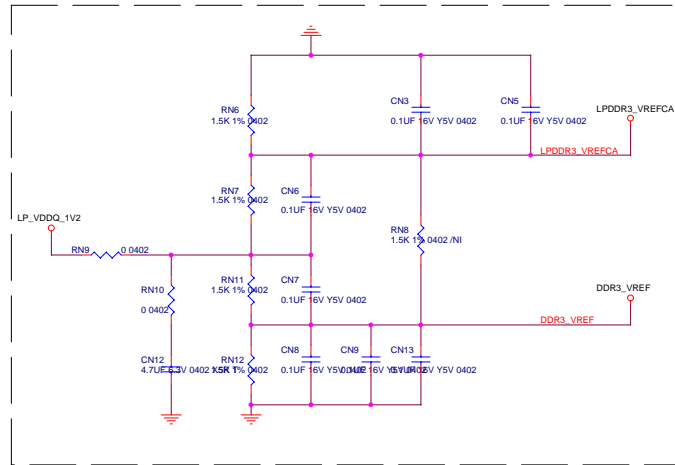


VCC1V8

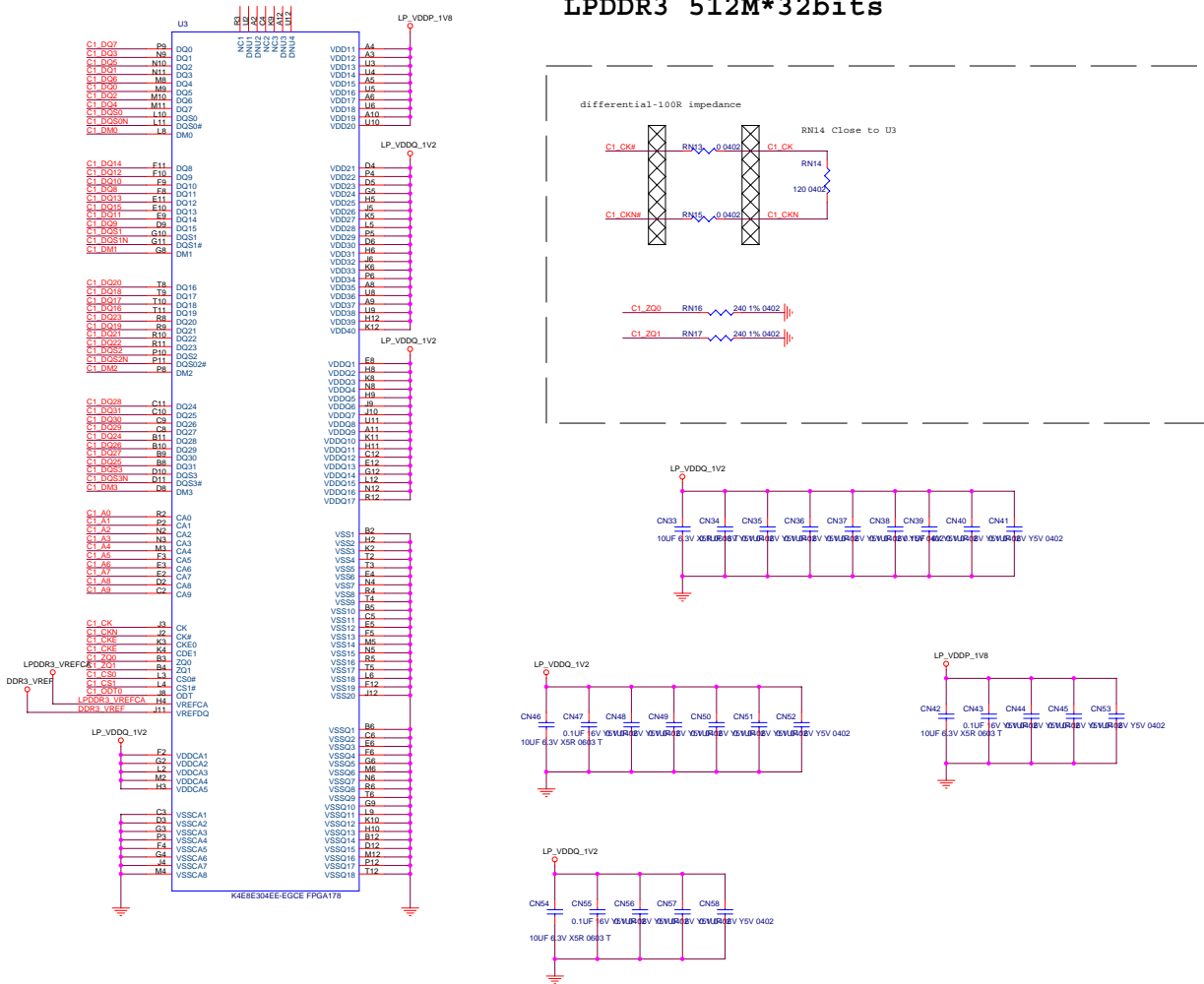


PCB Layout Trace Width



[illegible]

LPDDR3 512M*32bits



CPU LPDDR3 Interface

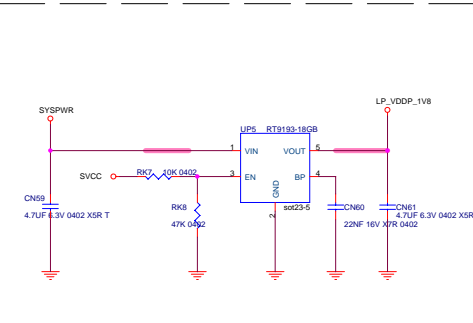
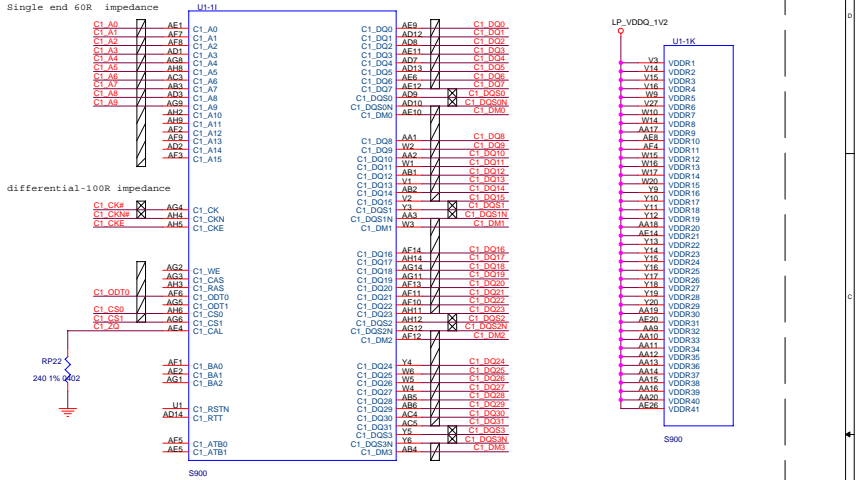


Figure 10: Pin connections for the 100-pin package. The diagram shows two pin headers, U1-U16 and U17-U32, connected to various components. U1-U16 is connected to CPU_VDD1, CPU_VDD2, CPU_VDD3, CPU_VDD4, CPU_VDD5, CPU_VDD6, CPU_VDD7, CPU_VDD8, CPU_VDD9, CPU_VDD10, CPU_VDD11, CPU_VDD12, CPU_VDD13, CPU_VDD14, CPU_VDD15, CPU_VDD16, CPU_VDD17, CPU_VDD18, CPU_VDD19, CPU_VDD20, CPU_VDD21, CPU_VDD22, CPU_VDD23, CPU_VDD24, CPU_VDD25, CPU_VDD26, CPU_VDD27, CPU_VDD28, CPU_VDD29, CPU_VDD30, CPU_VDD31, CPU_VDD32, CPU_VDD33, CPU_VDD34, CPU_VDD35, CPU_VDD36, CPU_VDD37, CPU_VDD38, CPU_VDD39, CPU_VDD40, CPU_VDD41, CPU_VDD42, CPU_VDD43, CPU_VDD44, CPU_VDD45, CPU_VDD46, CPU_VDD47, CPU_VDD48, CPU_VDD49, CPU_VDD50, CPU_VDD51, CPU_VDD52, CPU_VDD53, CPU_VDD54, CPU_VDD55, CPU_VDD56, CPU_VDD57, CPU_VDD58, CPU_VDD59, CPU_VDD60, CPU_VDD61, CPU_VDD62, CPU_VDD63, CPU_VDD64, CPU_VDD65, CPU_VDD66, CPU_VDD67, CPU_VDD68, CPU_VDD69, CPU_VDD70, CPU_VDD71, CPU_VDD72, CPU_VDD73, CPU_VDD74, CPU_VDD75, CPU_VDD76, CPU_VDD77, CPU_VDD78, CPU_VDD79, CPU_VDD80, CPU_VDD81, CPU_VDD82, CPU_VDD83, CPU_VDD84, CPU_VDD85, CPU_VDD86, CPU_VDD87, CPU_VDD88, CPU_VDD89, CPU_VDD90, CPU_VDD91, CPU_VDD92, CPU_VDD93, CPU_VDD94, CPU_VDD95, CPU_VDD96, CPU_VDD97, CPU_VDD98, CPU_VDD99, CPU_VDD100. U17-U32 is connected to CPU_VDD101, CPU_VDD102, CPU_VDD103, CPU_VDD104, CPU_VDD105, CPU_VDD106, CPU_VDD107, CPU_VDD108, CPU_VDD109, CPU_VDD110, CPU_VDD111, CPU_VDD112, CPU_VDD113, CPU_VDD114, CPU_VDD115, CPU_VDD116, CPU_VDD117, CPU_VDD118, CPU_VDD119, CPU_VDD120, CPU_VDD121, CPU_VDD122, CPU_VDD123, CPU_VDD124, CPU_VDD125, CPU_VDD126, CPU_VDD127, CPU_VDD128, CPU_VDD129, CPU_VDD130, CPU_VDD131, CPU_VDD132, CPU_VDD133, CPU_VDD134, CPU_VDD135, CPU_VDD136, CPU_VDD137, CPU_VDD138, CPU_VDD139, CPU_VDD140, CPU_VDD141, CPU_VDD142, CPU_VDD143, CPU_VDD144, CPU_VDD145, CPU_VDD146, CPU_VDD147, CPU_VDD148, CPU_VDD149, CPU_VDD150, CPU_VDD151, CPU_VDD152, CPU_VDD153, CPU_VDD154, CPU_VDD155, CPU_VDD156, CPU_VDD157, CPU_VDD158, CPU_VDD159, CPU_VDD160, CPU_VDD161, CPU_VDD162, CPU_VDD163, CPU_VDD164, CPU_VDD165, CPU_VDD166, CPU_VDD167, CPU_VDD168, CPU_VDD169, CPU_VDD170, CPU_VDD171, CPU_VDD172, CPU_VDD173, CPU_VDD174, CPU_VDD175, CPU_VDD176, CPU_VDD177, CPU_VDD178, CPU_VDD179, CPU_VDD180, CPU_VDD181, CPU_VDD182, CPU_VDD183, CPU_VDD184, CPU_VDD185, CPU_VDD186, CPU_VDD187, CPU_VDD188, CPU_VDD189, CPU_VDD190, CPU_VDD191, CPU_VDD192, CPU_VDD193, CPU_VDD194, CPU_VDD195, CPU_VDD196, CPU_VDD197, CPU_VDD198, CPU_VDD199, CPU_VDD200. The diagram also shows connections to VDD_CORE, GPU_VDD, and VDD_CORE2.

[illegible]

The diagram illustrates the ESD protection circuit for a USB3.0 single-core board. It shows the connection between the USB3.0 connector pins (VCONN, DM+, DP-, RX1+, RX1-, TX1+, TX1-) and the internal IC pins (SS_EVDN, SS_TXDN, SS_RXDN, SS_TAPN, SS_EVUP, SS_TXUP, SS_RXUP, SS_TAPUP). The circuit is designed for differential 90Ω and differential 100Ω impedances. It also shows the connection to the USB3.0 CONN block and the USB3.0 CONN block. The diagram is labeled "ESD PROTECT".

[illegible]

Freq.Tolerance<40ppm
ESR <50 ohm
PLS Place Near CPU

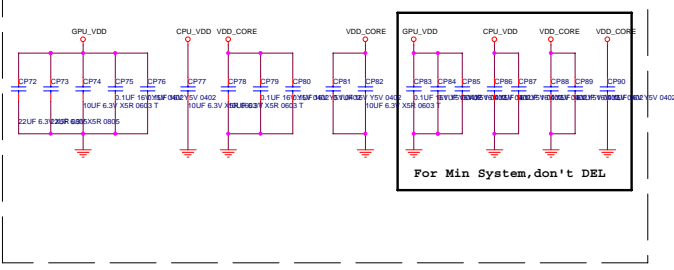
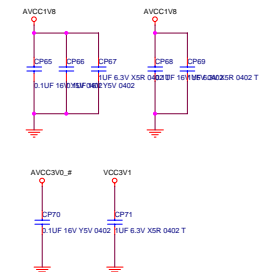
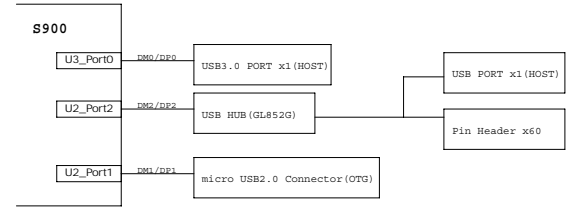
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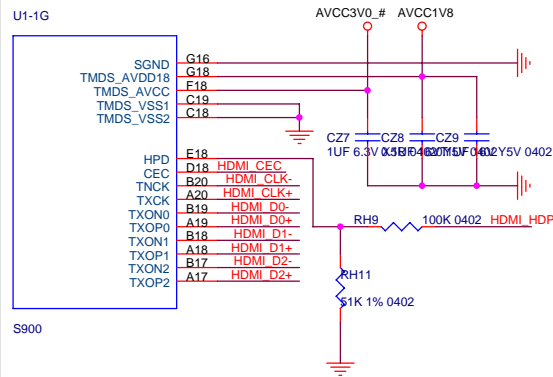
24MHZ 12PF 30PPM 3.2X2.5

18P 50V 0402 NPO

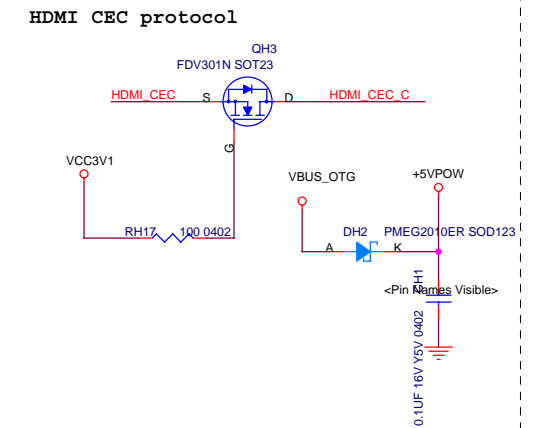
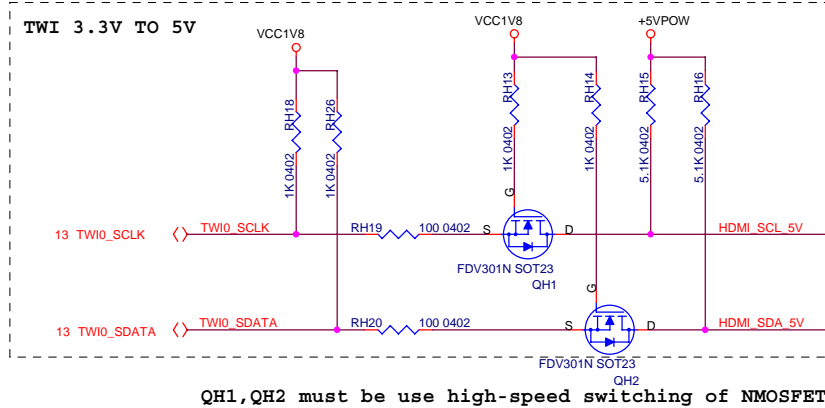
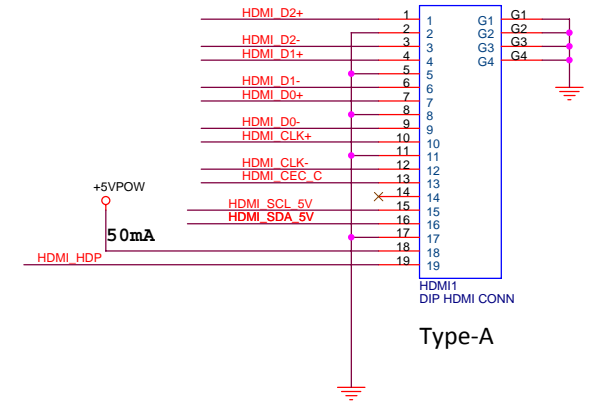
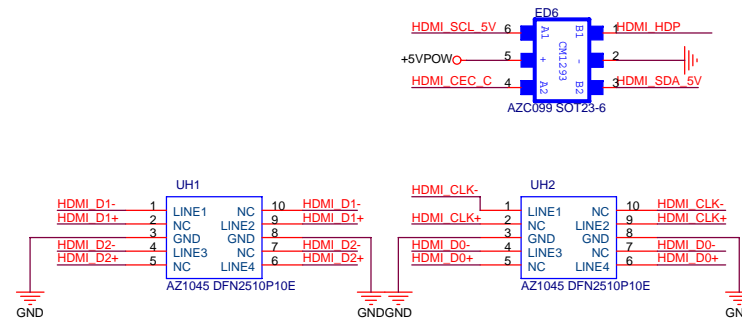
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GND

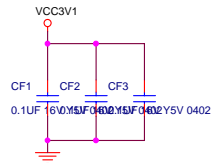
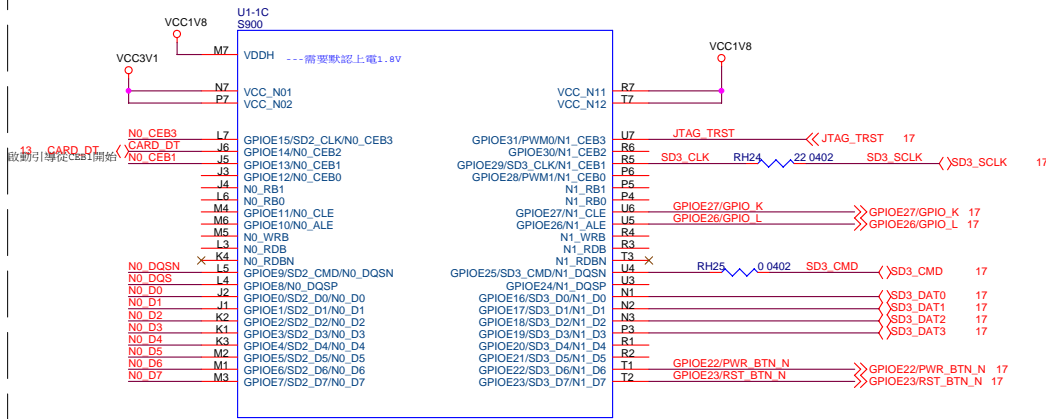


CPU HDMI
Interface

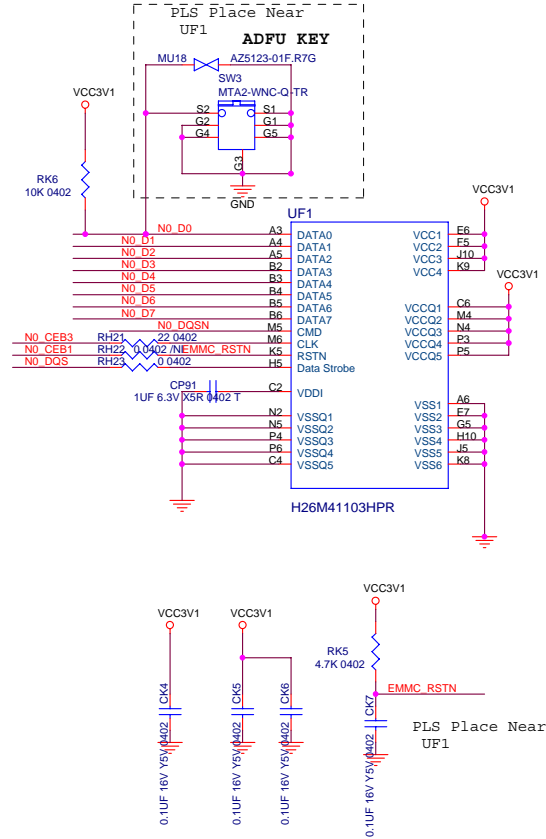
HDMI



CPU NAND/eMMC Interface



eMMC(Optional)

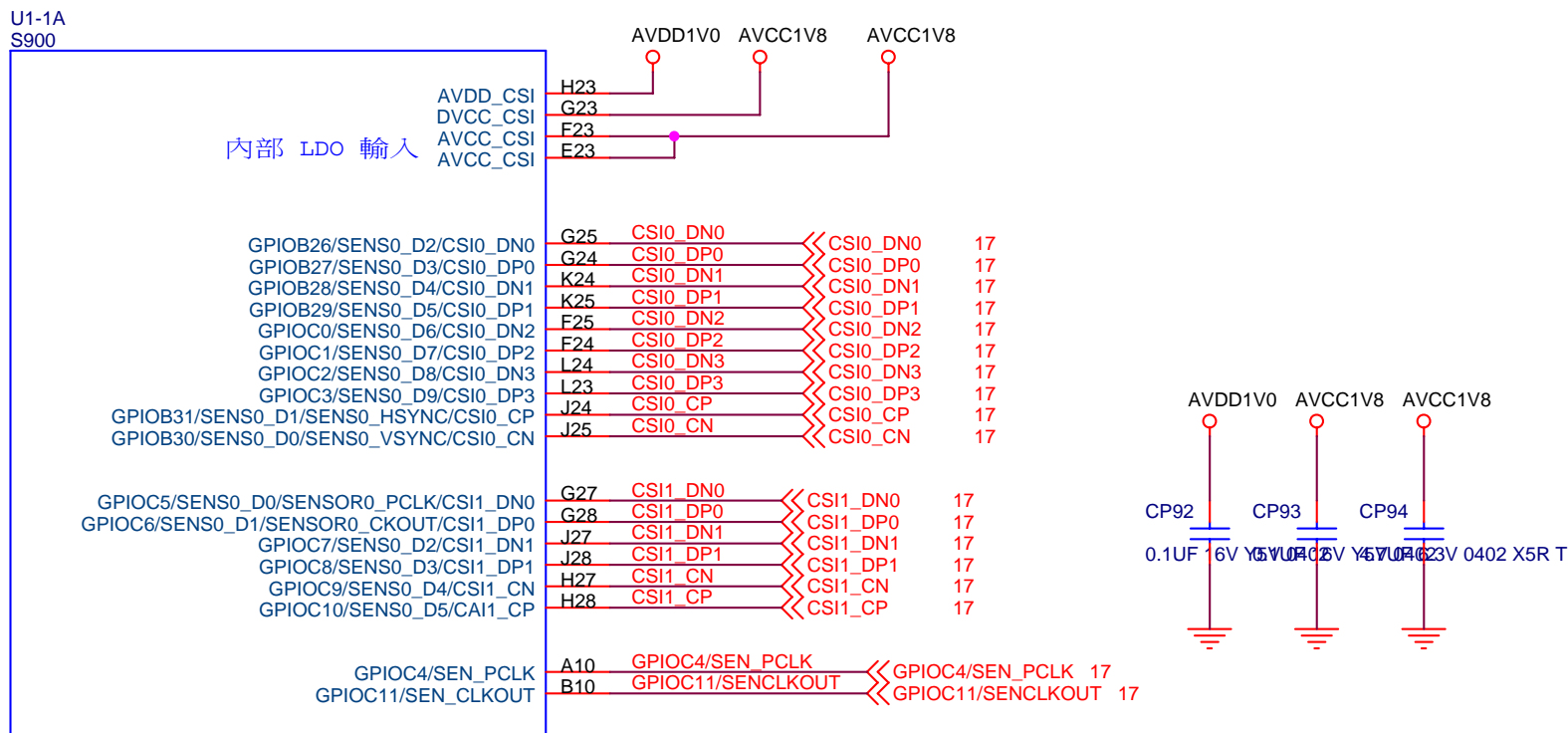


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MIPI_CSI



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Size
A

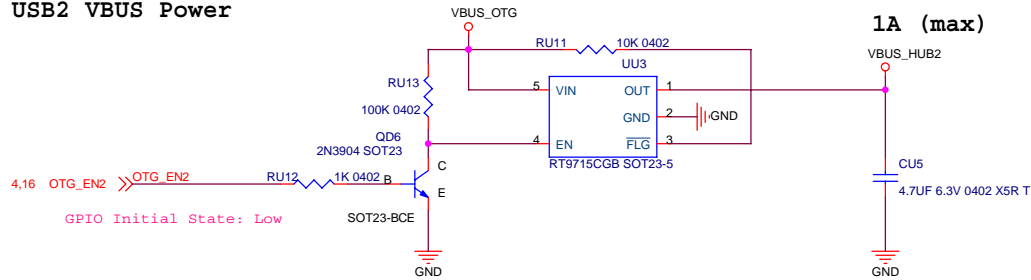
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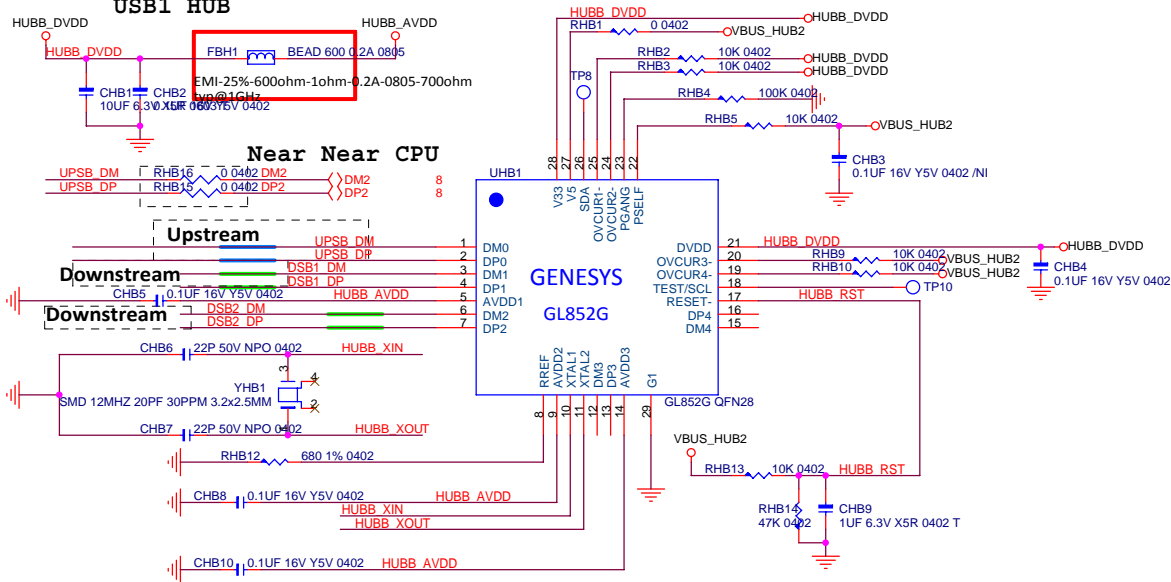
Rev	0.95
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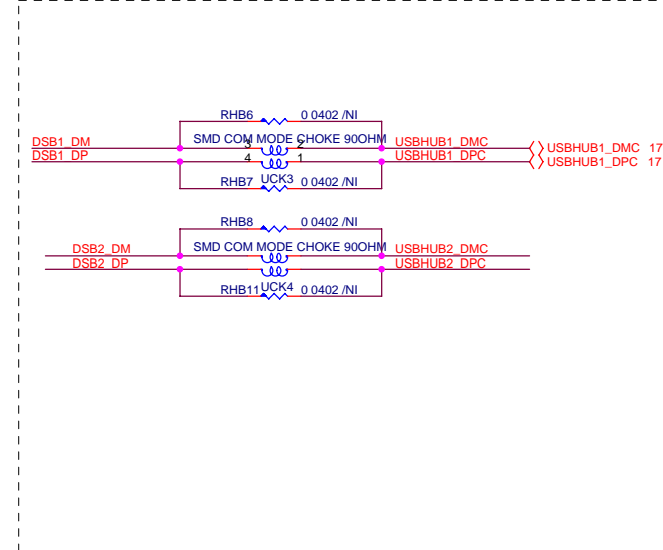
USB2 VBUS Power



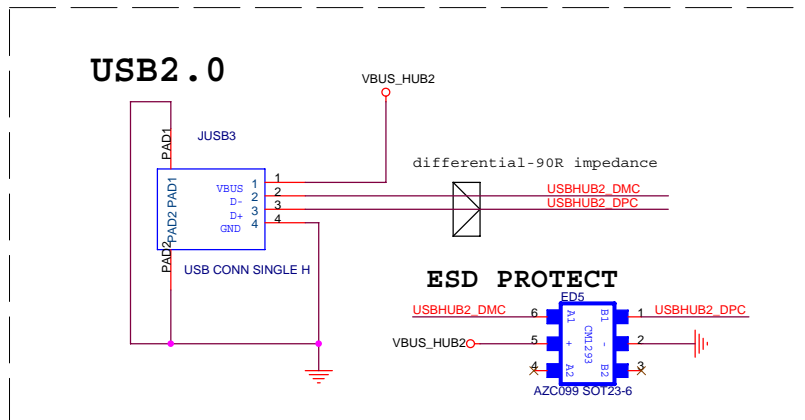
USB1 HUB



EMI COMMODE CHOKE



USB2.0

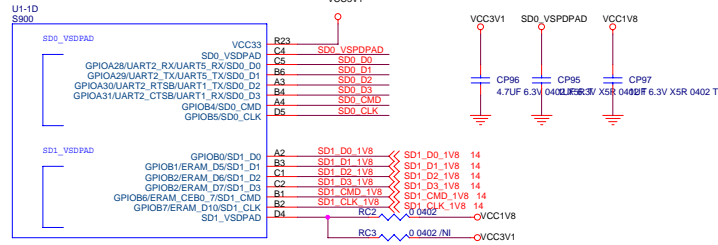


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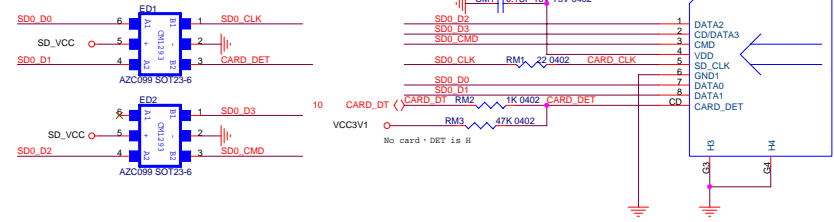
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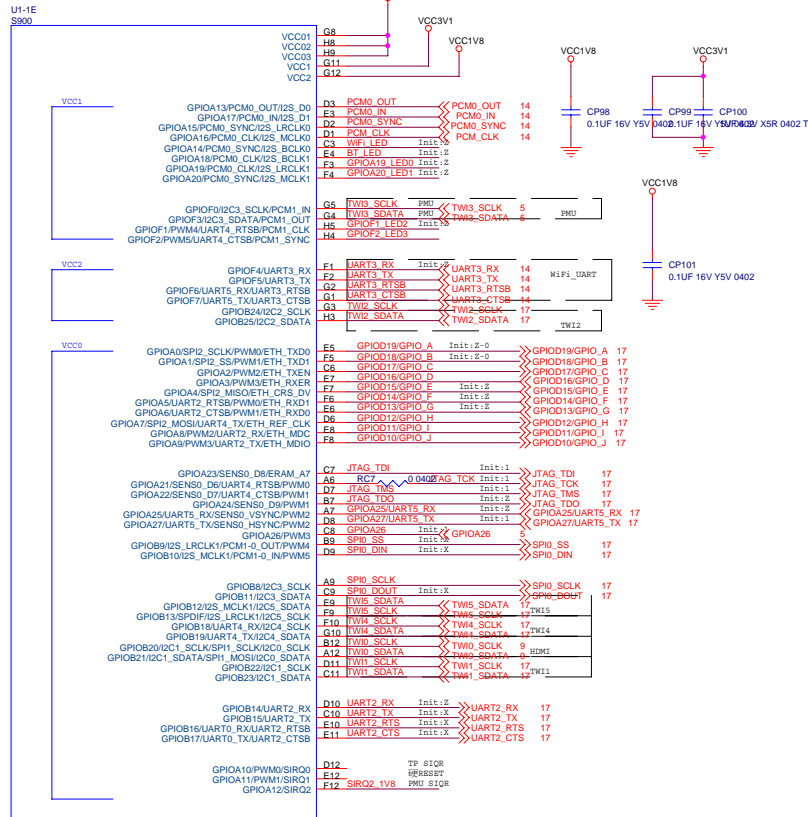
CPU TF_Card Interface



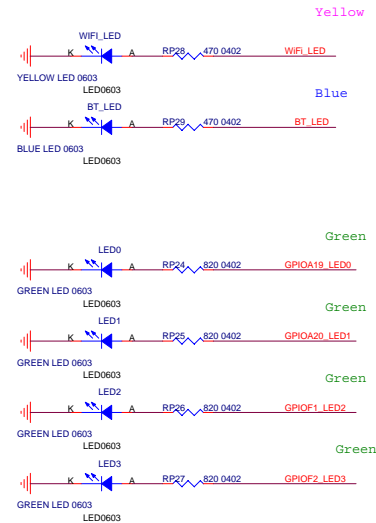
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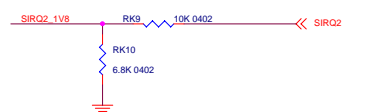
CPU IO Interface



LED



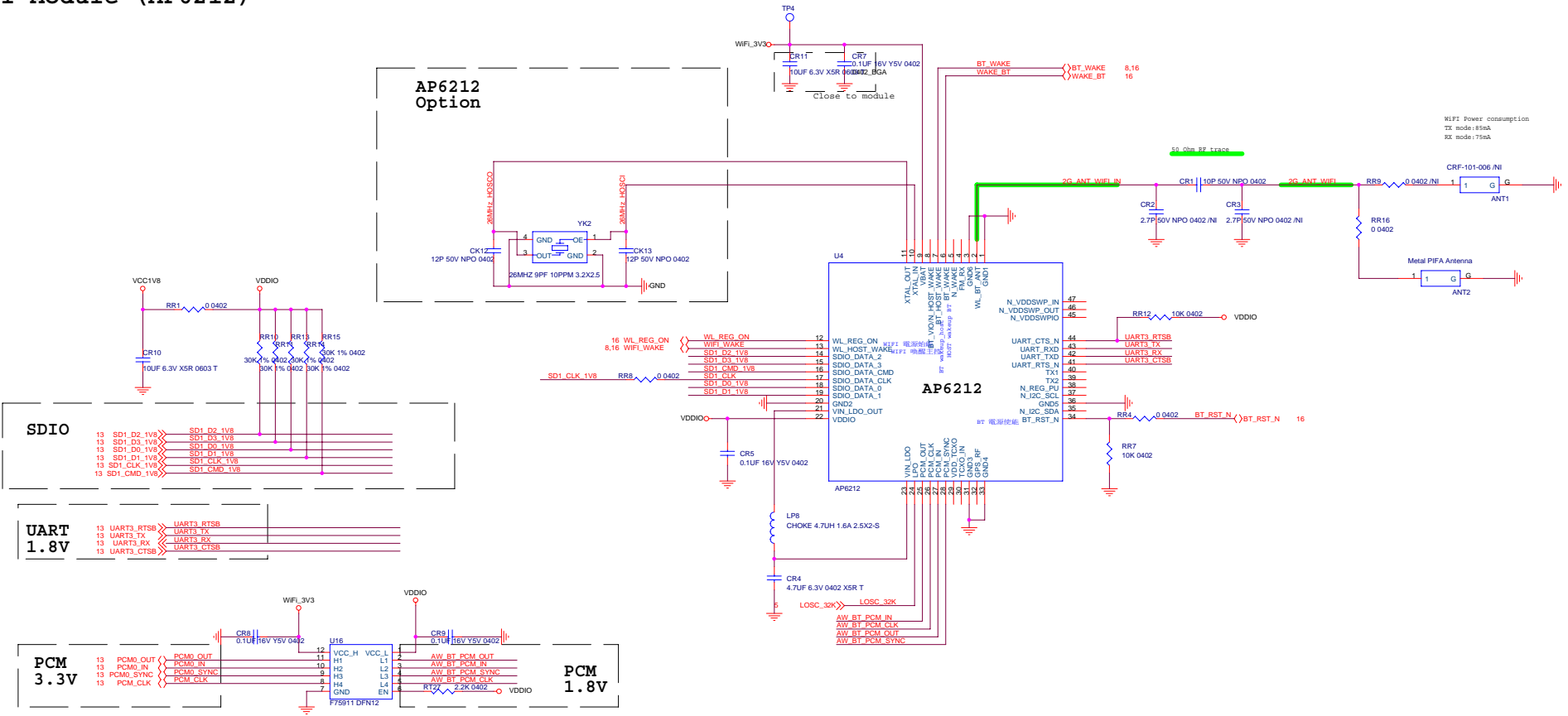
3.1V 轉 1.8V



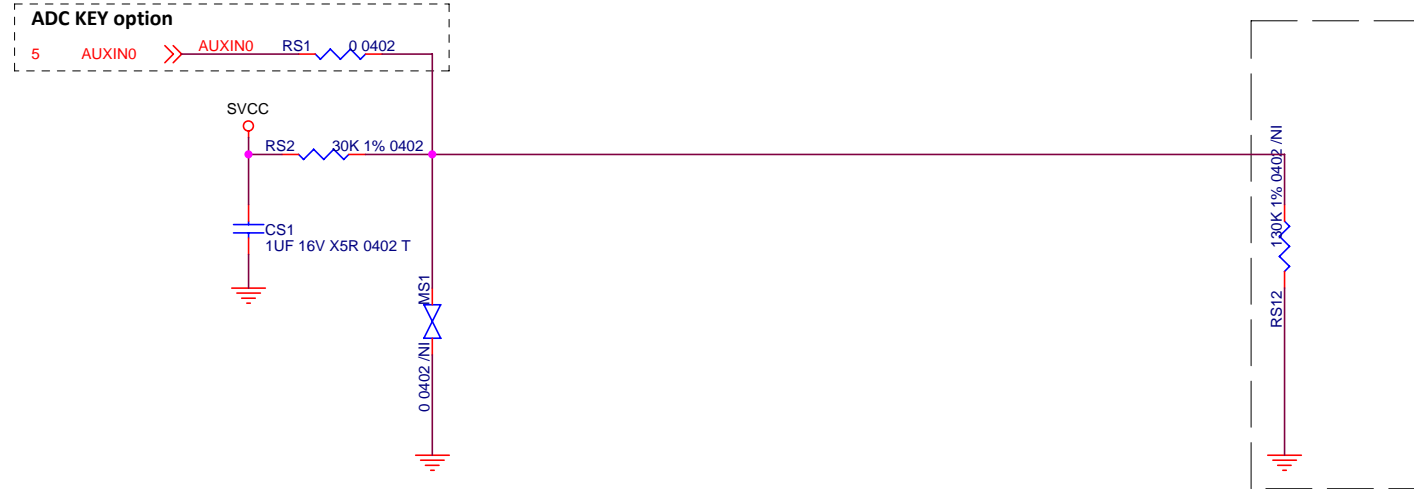
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WiFi Module (AP6212)



ADC KEY

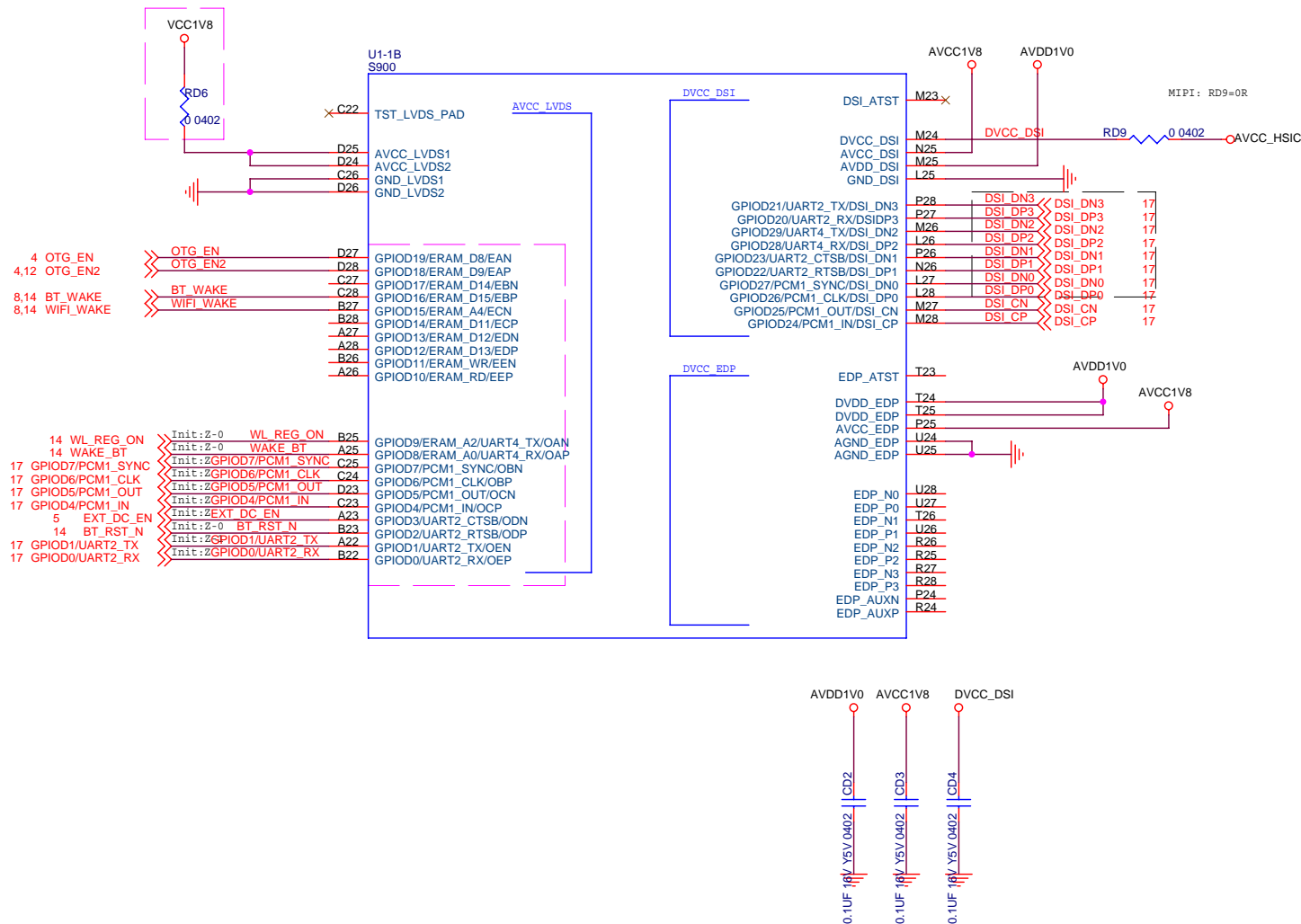


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CPU MIPI DSI&EDP Interface

Note:if don't need use LVDS Panel,and use the gpio functions that The AVCC_LVDS need use VCC1V8 power Source.



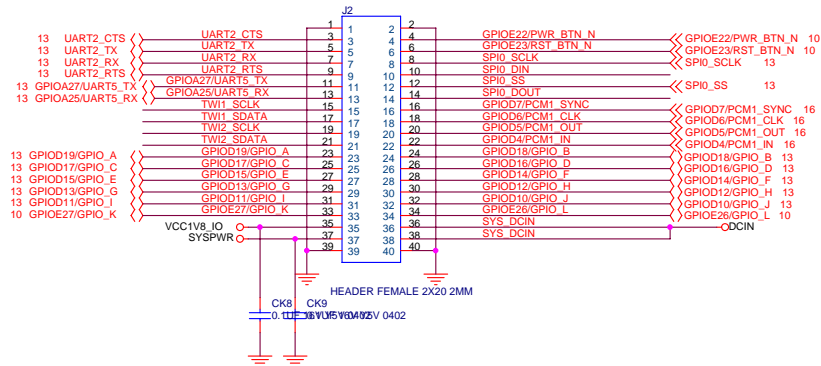
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Bubblegum-96

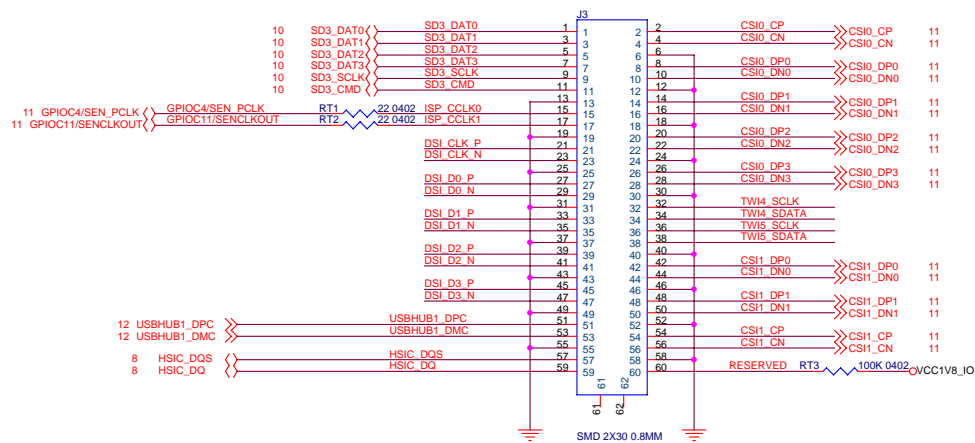
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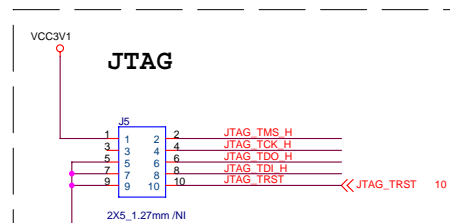
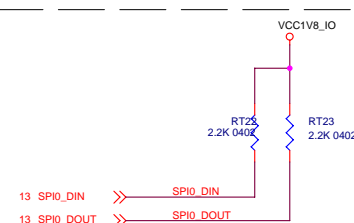
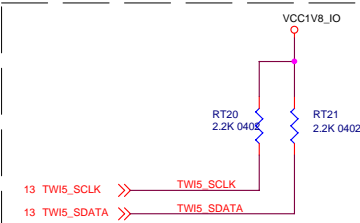
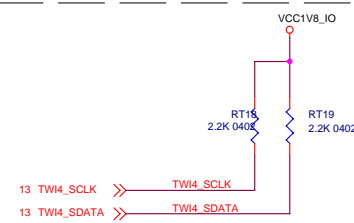
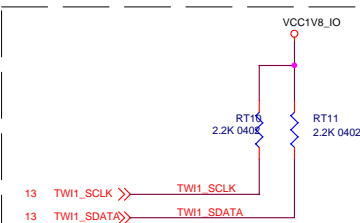
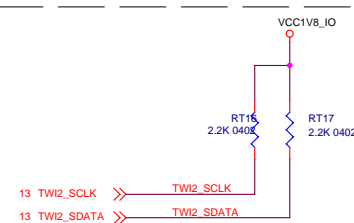
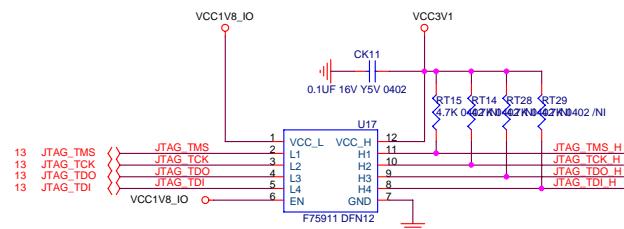
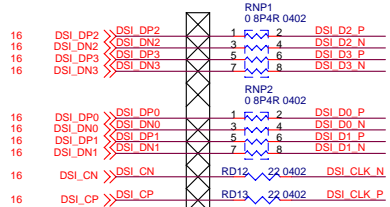
UART0/UART1/I2C0/I2C1/GPIO/SPI/PCM/PWR BTN/RST BTN/1V8/5V/SYS DCIN/GND



MIPI DSI/MIPI CSI/USB2.0/I2C



differential-100R impedance



GPIUART2 for Kernel Log (Debug use)

