S900 Multi-Mode Application Processor

Function Description

Version *1.0*

Date *2015-10-28*

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About This Document

Purpose

This document describes the function and the basic module of the S900 SoC.

Revision History

Date	Revision	Description
2015-10-28	1.0	First Release

Intended Audience

This document is intended for:

- Field application engineers
- Hardware engineers

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1 Introduction

1.1 Overview

The contents of this document are organized as:

- Chapter 1 Introduction. This chapter describes the S900 architecture.
- Chapter 2 System Control
- Chapter 3 Media System
- Chapter 4 Memory Control
- Chapter 5 Peripheral Interfaces
- Appendix Acronyms and Terms

1.2 Architecture

S900 integrates Quad-Core 64-bit Cortex-A53 CPU with advanced SIMD co-processor and VFPv4 instruction set. It is Actions' latest 28nm super high performance Application Processor with low power consumption. The compact integrated PowerVR G6230 GPU and Video Processing Unit provides up to 4K video effects and gaming experience. The advanced ISP supports camera sensors up to 13M pixel resolutions.

S900 provides rich interfaces such as HDMI, eDP, MIPI CSI, DSI, LVDS and USB3, etc. Bluetooth, WiFi and display peripherals can be easily integrated to construct flexible solutions. Efficient memory systems are built on high performance DDR3/DDR3L/LPDDR2/LPDDR3 and large capacity dual channel NAND Flash controller.

Together with Actions' in-house designed companion chip ATC260x which integrated PMU and Audio Codec together, S900 really makes it the best choice for high performance open platform.

1.2.1 Key Features

Overall Features

- High performance application processor with low power consumption, support high definition video decoding and recording, rich high speed peripherals for multimedia applications
- Integrated Quad-core 64-bit ARM Cortex-A53 processor, up to 1.6GHz
- Integrated PowerVR G6230 GPU and Video Processing unit for 4K video effects and 3D gaming
- ARM TrustZone security engine
- Secure accelerator for AES-128 Encrypt & Decrypt in ECB/CBC/CBC-CTS/CTR mode
- Built-in HDPC 2.2 hardware
- Advanced ISP supports sensors up to 13M pixel resolution
- DDR3/DDR3L/LPDDR2/LPDDR3 and large capacity dual channel NAND Flash

controller

- 28nm semiconductor process
- FCCSP package, 642 balls, 19mm*19mm body size, 0.65mm Pitch
- Work together with Actions' in-house designed companion chip ATC260x which integrated PMU and Audio Codec

Multimedia Features

- Support up to 4K Real-time video decoding of most popular video formats (some are supported by the 3rd party applications), such as H.265, MPEG-4 and H.264, etc.
- HEVC/H.265 up to 4096*2304@30fps
- Embedded video encoder support H.264 baseline profile, up to 1080p @60fps
- Integrated 3D/2D PowerVR G6230 GPU support OpenGL-ES1.1/2.0/3.0/3.1, OpenGL 3.2, DirectX 10 and OpenCL 1.2EP
- Support Dual cameras recording simultaneously, support PIP (Picture In Picture) and support RAW data capture
- Support automatic white balance (AWB), automatic exposure (AE) and automatic focus (AF)
- Support contrast, saturation, hue, brightness adjustment
- Up to 2560*1440 LCD display
- Support dual channel LVDS interface LCD display
- Support HDMI up to 1080p@60fps and 4k*2k@30fps display, support MHL2.1 up to 1080p@60fps

Interface Features

- Display interface: HDMI 1.4b & MHL 2.1, dual channel LVDS, 4-lane MIPI DSI V1.1 and eDP V1.3
- DDR3/DDR3L/LPDDR2/LPDDR3 SDRAM frequency up to 720MHz
- Dual channel NAND support SLC, MLC & TLC, and managed NAND Flash
- Four SD/MMC/EMMC controller, support SD3.0, MMC4.5, eMMC4.5, clock up to 200MHz
- One USB3.0, two USB2.0 OTG
- Support 10/100M Ethernet MAC with RMII/SMII interface
- Six TWI (Two Wire Interface) controller integrated, max speed up to 3.4Mbps
- Seven UART (Universal Asynchronous Receiver Transmitter) interfaces
- Four SPI (Synchronous Physical Interface) interfaces
- Six programmable PWM (Pulse Width Modulation) interfaces
- I2S, PCM and SPDIF audio interfaces are supported
- IRC (Infrared Controller) support RC5/RC6/NEC/9012 protocol

1.2.2 Logic Block Diagram

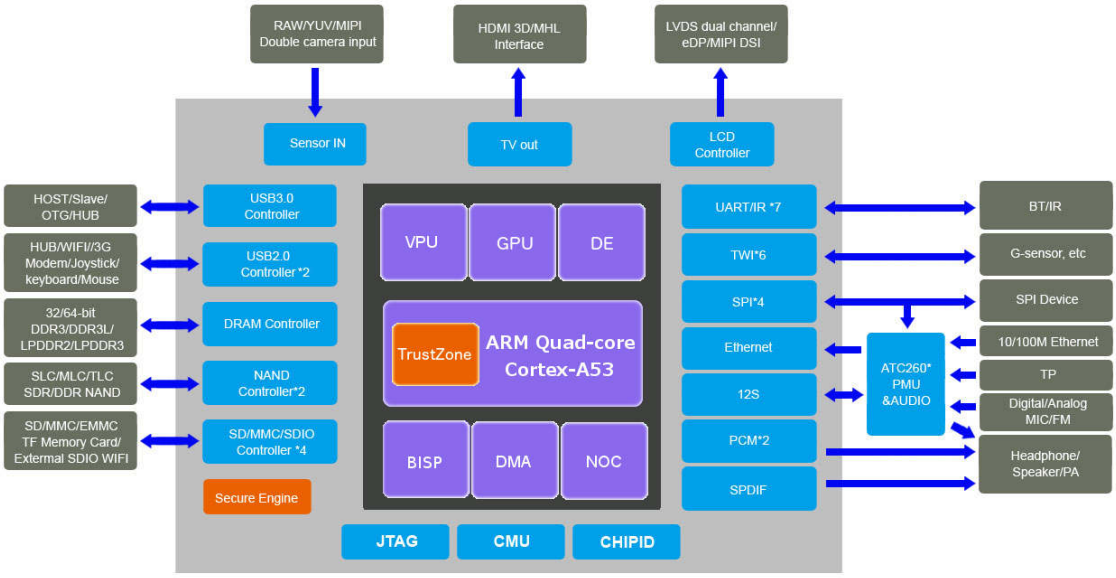


Figure 1 - 1 **Logic Block Diagram**

1.2.3 Application Scope

Applications of S900 include but not limited to the followings:

- Ultra book
- Virtual Reality glasses
- Smart Video Monitors
- Action Cameras
- Tablets
- MID (Multimedia Internet Device)
- POS machines
- Advertising Machines
- Other Cloud-connected applications

1.3 MPCore CPU

1.3.1 Function

The Cortex-A53 delivers 64-bit capability and significantly increases performance in a footprint suited for cost-sensitive applications.

- ARMv8-A architecture
- 32KB Instruction cache, 32KB data cache
- 1MB L2 Cache

- Four 64-bit idle counter and one 64-bit system counter
- 31*64-bit general purpose registers
- AArch32 for full backward compatibility with ARMv7
- AArch64 for 64-bit support and new architectural features
- NEON advanced SIMD
- In-Order Pipeline of lower power consumption
- Double Precession Floating Point SIMD extensions
- VFPv4 Floating point
- TrustZone security technology supported
- Support Hardware virtualization

1.3.2 Generic Interrupt Controller

SCU is responsible for managing the interconnect, arbitration, communication, cache to cache and system memory transfers, cache coherency and other capabilities for the processor. The Cortex-A53 MPCore processor also exposes these capabilities to other system accelerators and non-cached DMA driven peripherals to increase performance and reduce system wide power consumption. This system coherence also reduces software complexity involved in maintaining software coherence within each OS driver.

Implementing the standardized and architected interrupt controller, the GIC provides a rich and flexible approach to inter-processor communication and the routing and prioritization of system interrupts. Under software control, each interrupt can be distributed across CPU, hardware prioritized, and routed between the operating system and TrustZone software management layer. This routing flexibility and the support for virtualization of interrupts into the operating system, provides one of the key features required to enhance the capabilities of a solution utilizing a hypervisor.

See <ARM Generic Interrupt Controller Architecture> for more information.

1.4 Reset Management

1.4.1 Function

RMU is in control of the reset of CPU_VDD and CORE_VDD power domain, and support reset triggers from watchdog, core, CMU and etc. Each block can be reset by different reset source at same time.

1.4.2 Reset Source

Table 1 - 1 Reset Source of Each Block

Block	POR	Warm Reset[Note2]	WDx Reset	WD0_RST_Whole Reset	Trst Reset	CMU Reset	Power Domain
L2 & SCU	**Yes**	No	No	**Yes**	No	No	CPU (M) _VDD
CoreSight	**Yes**	No	No	**Yes**	**Yes**[Note3]	No	CPU_VDD
GIC_400	**Yes**	No	No	**Yes**	No	**Yes**	CPU_VDD
CPU[x]	**Yes**	**Yes**	**Yes**	**Yes**	No	**Yes**[Note1]	CPU (M) _VDD
Idle_CNT[x]	**Yes**	No	No	**Yes**	No	No	CPU_VDD
WatchDog[x]	**Yes**	No	No	**Yes**	No	**Yes**[Note1]	CPU_VDD
System_CNT	**Yes**	No	No	**Yes**	No	**Yes**	CPU_VDD
SPS_CPU	**Yes**	No	No	**Yes**	No	**Yes**	CORE_VDD
Register Configure	**Yes**	No	No	**Yes**	No	No	CORE_VDD & CPU_VDD
GPU_PA	-	No	No	**Yes**	**Yes**	**Yes**	GPU_VDD
GPU_PB	-	No	No	-	**Yes**	**Yes**	GPU_VDD
CMU	**Yes**	No	No	**Yes**	No	No	CORE_VDD
SPS	**Yes**	No	No	**Yes**	No	No	CORE_VDD
NOC	**Yes**	No	No	**Yes**	No	No	CORE_VDD
Other always on modules	**Yes**	No	No	**Yes**	No	**Yes**	CORE_VDD
Other switchable modules	-	No	No	-	No	**Yes**	CORE_VDD

Notes:

1. *CPU[x] can only be reset together with WatchDog[x].*
2. *CPU[x] WarmReset reset has three reset sources: software configuration, CoreSight and CPU[x]*
3. *Trst can only reset JTAG part in CoreSignt.*

1.5 Clock Management

1.5.1 Function

CMU manages the clock system of S900, of which clock source are from HOSC (Host Oscillator), 10 PLLs and LOSC (internal low frequency oscillator). Analog part are these three clock sources, and digital part are consists of frequency dividing circuit, clock control circuit and MUX circuit. Features of CMU are listed below:

- CMU clock source: HOSC, PLL, LOSC
- 10 PLLs are embedded:
  - CORE_PLL for CPU
  - DEV_PLL for AHB and APB
  - NAND_PLL for NAND and SD
  - DDR_PLL for DDR
  - DISPLAY_PLL for display and high clock frequency modules
  - AUDIO_PLL for audio application
  - TVOUT_PLL for for TV/HDMI
  - DSI_PLL for MIPI DSI
  - DP_PLL for eDP
  - ASSIST_PLL for Ethernet and etc.
- HOSC is the clock source of all the PLLs

1.6 System Boot

System boot involves the process of hardware peripherals initiation, Power on sequence, loading and driving from storage medium, and firmware update. S900 supports booting from external storage drivers, including NAND Flash, SPI NOR and SD/MMC/eMMC. The BRECLauncher block will conduct loading boot code from external storage drivers, it will check the storage drivers' ID and find the right driver. The right boot code will be loaded into internal SRAM and run. If no storage diver is found right, S900 will load boot code from ADFULauncher. After boot code is executed, the operating system will be boot up or uploaded.

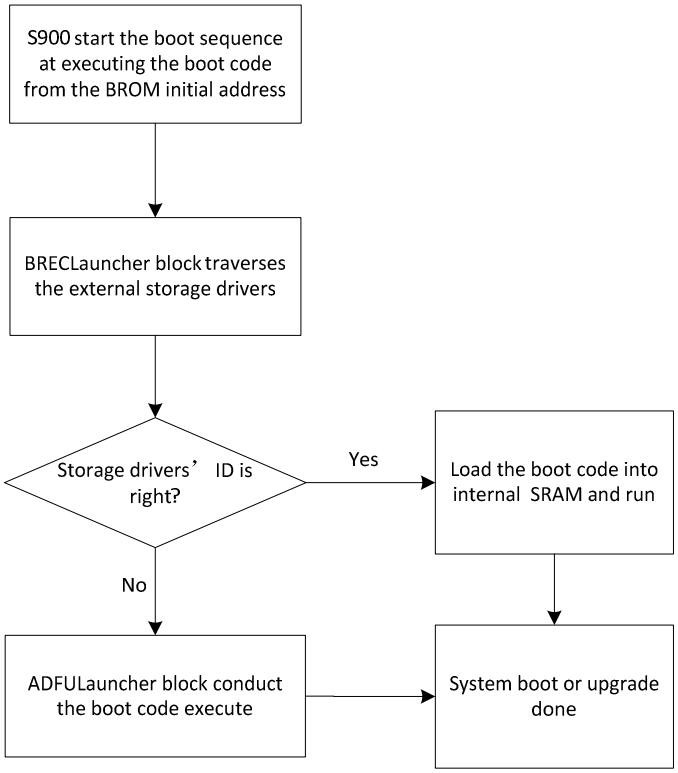


Figure 1 - 2 Boot Sequence Diagram

1.7 Address Mapping

Table 1 - 2 Address Mapping

Physical Address		Size (Byte)	Function
Start	**End**		
0x00000000	0xDFFFFFFF	3.5G	DDR Memory (Bottom)
0xE0000000	0xE7FFFFFF	128M	IO device
0xE8000000	0xEFFFFFFF	128M	Reserved
0xF0000000	0xFCFFFFFF	208M	Reserved
0xFD000000	0xFFFFFFFF	48M	ERAM / BROM *Note:* *[0xFD000000, 0xFEFFFFFF] is ERAM address space* *[0xFFFF0000, 0xFFFFFFFF] is BROM address space* *ERAM and BROM use the same HSEL.*
0x1_00000000	0x1_DFFFFFFF	3.5G	Reserved
0x1_E0000000	0x1_FFFFFFFF	512M	DDR Memory (Top) *Note: accessed by CPU only.*
IO device			
0xE0000000	0xE00FFFFF	1M	Reserved
0xE0100000	0xE010FFFF	64K	AUDIO (I2S/SPDIF)
0xE0110000	0xE0117FFF	32K	PCM0 Controller

0xE0118000	0xE011FFFF	32K	PCM1 Controller
0xE0120000	0xE0121FFF	8K	UART0/IRC Controller
0xE0122000	0xE0123FFF	8K	UART1 Controller
0xE0124000	0xE0125FFF	8K	UART2 Controller
0xE0126000	0xE0127FFF	8K	UART3 Controller
0xE0128000	0xE0129FFF	8K	UART4 Controller
0xE012A000	0xE012BFFF	8K	UART5 Controller
0xE012C000	0xE012DFFF	8K	UART6 Controller
0xE012E000	0xE012FFFF	8K	SPS&RMU
0xE0130000	0xE0131FFF	8K	AVS
0xE0132000	0xE013FFFF	56K	Reserved
0xE0140000	0xE015FFFF	128K	Reserved
0xE0160000	0xE0167FFF	32K	CMU
0xE0168000	0xE016FFFF	32K	Reserved
0xE0170000	0xE0171FFF	8K	TWI0 Controller
0xE0172000	0xE0173FFF	8K	TWI1 Controller
0xE0174000	0xE0175FFF	8K	TWI2 Controller
0xE0176000	0xE0177FFF	8K	TWI3 Controller
0xE0178000	0xE0179FFF	8K	TWI4 Controller
0xE017A000	0xE017BFFF	8K	TWI5 Controller
0xE017C000	0xE017FFFF	16K	Reserved
0xE0180000	0xE018FFFF	64K	Reserved
0xE0190000	0xE019FFFF	64K	eDP Controller
0xE01A0000	0xE01AFFFF	64K	Reserved
0xE01B0000	0xE01BFFFF	64K	GPIO/MFP Controller (include PWM)
0xE01C0000	0xE01CFFFF	64K	Reserved
0xE01D0000	0xE01D3FFF	16K	SPI0 Controller
0xE01D4000	0xE01D7FFF	16K	SPI1 Controller
0xE01D8000	0xE01DBFFF	16K	SPI2 Controller
0xE01DC000	0xE01DFFFF	16K	SPI3 Controller
0xE01E0000	0xE01E7FFF	32K	MIPI DSI
0xE01E8000	0xE01EFFFF	32K	Reserved
0xE01F0000	0xE01FFFFF	64K	Reserved
0xE0200000	0xE021FFFF	128K	Reserved
0xE0220000	0xE0227FFF	32K	Reserved
0xE0228000	0xE022FFFF	32K	Timer
0xE0230000	0xE0237FFF	32K	HDE
0xE0238000	0xE023FFFF	32K	HDCP2Tx
0xE0240000	0xE0247FFF	32K	SRAMI (Nor/SRAM/BROM Controller/ShareSRAMCTL)
0xE0248000	0xE024FFFF	32K	SecureEngine Controller
0xE0250000	0xE025FFFF	64K	HDMI&MHL Controller
0xE0260000	0xE026FFFF	64K	DMA Controller

0xE0270000	0xE0277FFF	32K	BISP Controller
0xE0278000	0xE027FFFF	32K	IMX
0xE0280000	0xE0287FFF	32K	VDE
0xE0288000	0xE028FFFF	32K	VCE
0xE0290000	0xE029FFFF	64K	DDR Controller (including 2-ch controller+phy)
0xE02A0000	0xE02AFFFF	64K	LCD Controller
0xE02B0000	0xE02BFFFF	64K	USBH0
0xE02C0000	0xE02CFFFF	64K	USBH1
0xE02D0000	0xE02D7FFF	32K	MIPI CSI_0
0xE02D8000	0xE02DFFFF	32K	MIPI CSI_1
0xE02E0000	0xE02EFFFF	64K	DE (Display Engine)
0xE02F0000	0xE02FFFFF	64K	Reserved
0xE0300000	0xE0307FFF	32K	NAND Flash Controller_0
0xE0308000	0xE030FFFF	32K	NAND Flash Controller_1
0xE0310000	0xE031FFFF	64K	Ethernet Controller
0xE0320000	0xE032FFFF	64K	Reserved
0xE0330000	0xE0333FFF	16K	SD0 Controller
0xE0334000	0xE0337FFF	16K	SD1 Controller
0xE0338000	0xE033BFFF	16K	SD2 Controller
0xE033C000	0xE033FFFF	16K	SD3 Controller
0xE0340000	0xE03FFFFF	768K	Reserved
0xE0400000	0xE04FFFFF	1M	USB3.0 Controller
0xE0500000	0xE05FFFFF	1M	NOC
0xE0600000	0xE06FFFFF	1M	GPU
0xE0700000	0xE07FFFFF	1M	Reserved
SRAMOC:			
0xE4000000	0xE405FFFF	384K	Reserved
0xE4060000	0xE40BFFFF	384K	ShareSRAM 1. 0xE4060000~0xE4067FFF (Independent 32KB SRAM for secure world) 2. 0xE4068000~0xE407FFFF (96KB SRAM shared from DE)
0xE40E0000	0xE40FFFFF	128K	Reserved
0xE4100000	0xE7FFFFFF	63M	Reserved
SRAMI Memory:			
0xFD000000	0xFD00FFFF	64K	ERAM (in normal mode)
0xFFFF0000	0xFFFFFFFF	64K	BROM (in normal mode)

2 System Control

2.1 Timer

2.1.1 Function

There are 4 32-bit timers with IRQ, and all timers are same logic. Timer 2/3 only used in Secure mode.

32-bit register T0_VAL and T0_CMP are writable and readable, T0_CMP can be written at any time.

When EN=0, T0_VAL can be written, but timer0 does not count up.

When EN=1, T0_VAL will carry on counting from whatever value is loaded into it. However, OS timers are usually implemented by leaving T0_VAL free-running and writing T0_CMP as necessary.

T0_VAL counts up at the clock from 24MHz, if IRQEN=1, An IRQ will generate when T0_VAL equals T0_CMP. The IRQ can be cleared by writing 1 to PD.

2.1.2 Register List

Table 2 - 1 Timer Base Address

Name	Physical Base Address
Timer	0xE0228000

Table 2 - 2 Timer Register List

Offset	Register Name	Description
0x0008	T0_CTL	Timer0 Control register
0x000C	T0_CMP	Timer0 Compare Register
0x0010	T0_VAL	Timer0 Value Register
0x0014	T1_CTL	Timer1 Control register
0x0018	T1_CMP	Timer1 Compare Register
0x001C	T1_VAL	Timer1 Value Register
0x0030	T2_CTL	Timer2 Control register
0x0034	T2_CMP	Timer2 Compare Register
0x0038	T2_VAL	Timer2 Value Register
0x003c	T3_CTL	Timer3 Control register
0x0040	T3_CMP	Timer3 Compare Register
0x0044	T3_VAL	Timer3 Value Register

Note: When Setting the TIMERs, program must disable the corresponding enable bit at first and then enable it after setting the value.

2.1.3 Register Description

2.1.3.1 T0_CTL

Timer0 Control Register (VDD)

Offset = 0x0008

Bits	Name	Description	Access	Reset
31	ERR_FLAG	Error flag bit 0:T0 running normally 1:T0 has synchronous reading error This bit can be cleared only by disable T0	R	0
30:3	-	Reserved	-	-
2	EN	Timer0 Enable 0:Disable 1:Enable	RW	0
1	IRQEN	T0 send IRQ Enable When this bit is enabled, if T0_VAL equals T0_CMP, IRQ signal will be sent out until the IRQ pending bit was cleared.	RW	0
0	PD	Timer0 IRQ Pending, Writing 1 to clear this bit.	RW	0

2.1.3.2 T0_CMP

Timer0 compare Register (VDD)

Offset = 0x000C

Bits	Name	Description	Access	Reset
31:0	CMP	compare value	RW	0

2.1.3.3 T0_VAL

Timer0 Value Register (VDD)

Offset = 0x0010

Bits	Name	Description	Access	Reset
31:0	VAL	Read or write current Timer0 value	RW	0

2.1.3.4 T1_CTL

Timer1 Control Register (VDD)

Offset = 0x0014

Bits	Name	Description	Access	Reset
31	ERR_FLAG	Error flag bit	R	0

		0:T1 running normally 1:T1 has synchronous reading error This bit can be cleared only by disable T1		
30:3	-	Reserved	-	-
2	EN	Timer1 Enable 0:Disable 1:Enable	RW	0
1	IRQEN	T1 send IRQ Enable When this bit is enabled, If T1_VAL equals T1_CMP, IRQ signal will be sent out until the IRQ pending bit was cleared.	RW	0
0	PD	Timer1 IRQ Pending, Writing 1 to clear this bit.	RW	0

2.1.3.5 T1_CMP

Timer1 compare Register (VDD)

Offset = 0x0018

Bits	Name	Description	Access	Reset
31:0	CMP	compare value	RW	0

2.1.3.6 T1_VAL

Timer1 Value Register (VDD)

Offset = 0x001C

Bits	Name	Description	Access	Reset
31:0	VAL	Read or write current Timer1 value	RW	0

2.2 DMA

2.2.1 Function

DMA is the data transmission engine for CPU system memory and peripheral slaves including AXI, AHB and APB. The AXI slave devices include DDR, ShareRAM, NAND Flash, SD/MMC. AHB slave consists of SRAMI, SPI and MIPI DSI. APB slave devices include UART, I2S, PCM, SPDIF, HDMIAudio, etc.

The system transmission engine DMA support 12 logic channels, 32 bytes burst transfer, 4 read outstanding requests, link list mode and unaligned word transfer.

2.2.2 DRQ Source

DMA supports 4 software configurable interrupt lines. Interrupt events include: super block transmission over interrupt (for linklist), block transmission over interrupt, frame transmission over interrupt, half of frame transmission over interrupt, start of last frame transmission over interrupt, and address unaligned error interrupt.

Table 2 - 3 DRQ Trig Source Table

DRQ Source	DRQ_Trig Field (5bit)	DRQ Connect	Simultaneous Task Num	FIFO Depth	FIFO Wide	DRQ Threshold	Operation Wide
DCU (ShareSRAM/srmi)	0	DRQ0	>2 (SRC|DST)	RAM	32	Always	128
SD0	2	DRQ2	1 (SRC|DST)	512B	32	8	32
SD1	3	DRQ3	1 (SRC|DST)	512B	32	8	32
SD2	4	DRQ4	1 (SRC|DST)	512 B	32	8	32
NANDDATA0	6	DRQ6	1 (SRC|DST)	1KB	0	0	32
I2S_t	7	DRQ7	1 (DST)	32	24	16	32
I2S_r	8	DRQ8	1 (SRC)	16	24	8	32
PCM0_t	9	DRQ9	1 (DST)	16	16	16	32
PCM0_r	10	DRQ10	1 (SRC)	16	16	8	32
PCM1_t	11	DRQ11	1 (DST)	16	16	16	32
PCM1_r	12	DRQ12	1 (SRC)	16	16	8	32
SPDIF	13	DRQ13	1 (DST)	32	24	16	32
HDMIaudio	14	DRQ14	1 (DST)	32	24	16	32
I2STX_SPDIF_HDMI	15	DRQ15	1 (DST)	32	24	16	32
UART0_t	16	DRQ16	1 (DST)	16	8	1	32
UART0_r	17	DRQ17	1 (SRC)	32	8	1	32
UART1_t	18	DRQ18	1 (DST)	16	8	1	32
UART1_r	19	DRQ19	1 (SRC)	32	8	1	32
UART2_t	20	DRQ20	1 (DST)	16	8	1	32
UART2_r	21	DRQ21	1 (SRC)	32	8	1	32
UART3_t	22	DRQ22	1 (DST)	16	8	1	32
UART3_r	23	DRQ23	1 (SRC)	32	8	1	32
UART4_t	24	DRQ24	1 (DST)	16	8	1	32
UART4_r	25	DRQ25	1 (SRC)	32	8	1	32
UART5_t	26	DRQ26	1 (DST)	16	8	1	32
UART5_r	27	DRQ27	1 (SRC)	32	8	1	32
SPI0_t	28	DRQ28	1 (DST)	32	32	16	32
SPI0_r	29	DRQ29	1 (SRC)	32	32	16	32
SPI1_t	30	DRQ30	1 (DST)	32	32	16	32
SPI1_r	31	DRQ31	1 (SRC)	32	32	16	32
SPI2_t	32	DRQ32	1 (DST)	32	32	16	32

SPI2_r	33	DRQ33	1 (SRC)	32	32	16	32
SPI3_t	34	DRQ34	1 (DST)	32	32	16	32
SPI3_r	35	DRQ35	1 (SRC)	32	32	16	32
DSI_t	36	DRQ36	1 (SRC)	32	32	11/16	32
DSI_r	37	DRQ37	1 (DST)	32	32	11/16	32
HDCP2.0_t	41	DRQ41	1 (SRC)	12	32	8	32
HDCP2.0_r	40	DRQ40	1 (DST)	12	32	8	32
UART6_t	42	DRQ42	1 (DST)	16	8	1	32
UART6_r	43	DRQ43	1 (SRC)	32	8	1	32
NANDDATA1	45	DRQ45	1 (SRC|DST)	1KB	0	0	32
SD3	46	DRQ46	1 (SRC|DST)	512 B	32	8	32

2.2.3 Register List

Table 2 - 4 DMA Controller Registers Address

Name	Physical Base Address
DMA_GLOBAL	0xE0260000
DMA0	0xE0260100
DMA1	0xE0260200
DMA2	0xE0260300
DMA3	0xE0260400
DMA4	0xE0260500
DMA5	0xE0260600
DMA6	0xE0260700
DMA7	0xE0260800
DMA8	0xE0260900
DMA9	0xE0260A00
DMA10	0xE0260B00
DMA11	0xE0260C00

Table 2 - 5 DMA Global Controller Registers

Offset	Register Name	Description
0x0000~0x000C	DMA_IRQ_PD0~3	DMA IRQ Pending Register0~3
0x0010~0x001C	DMA_IRQ_EN0~3	DMA IRQ enable Register0~3
0x0020	DMA_SECURE_ACCESS_CTL	CTRL of DMA secure access
0x0024	DMA_NIC_QOS	QOS of DMA to NIC
0x002C	DMA_IDLE_STAT	DMA status register

Table 2 - 6 DMA Logical Channel Controller Registers

Offset	Register Name	Description
0000	DMAx_MODE	Mode Register
0x0004	DMAx_SOURCE	Source address Register

0x0008	DMAx_DESTINATION	Destination Address Register
0x000C	DMAx_FRAME_LEN	Frame Length Register
0x0010	DMAx_FRAME_CNT	Frame Count Register
0x0014	DMAx_REMAIN_FRAME_CNT	Remain Frames in the Current Block
0x0018	DMAx_REMAIN_CNT	Remain Count in the Current Frame
0x001C	DMAx_SOURCE_STRIDE	Source Stride Register
0x0020	DMAx_DESTINATION_STRIDE	Destination Stride Register
0x0024	DMAx_START	Start DMA demand
0x0028	DMAx_PAUSE	DMA PAUSE
0x002C	DMAx_CHAINED_CTL	Chained Control Register
0x0030	DMAx_CONSTANT	Constant Fill Mode Data Register
0x0034	DMAx_LINKLIST_CTL	Link list Control Register
0x0038	DMAx_NEXT_DESCRIPTOR	Link list Next DESCRIPTOR Pointer Register
0x003C	DMAx_CURRENT_DESCRIPTOR_NUM	Link list Next DESCRIPTOR Pointer Register
0x0040	DMAx_INT_CTL	Interrupt Control Register
0x0044	DMAx_INT_STATUS	Interrupt Status Register
0x0048	DMAx_CURRENT_SOURCE_POINTER	Current Source Pointer Register
0x004C	DMAx_CURRENT_DESTINATION_POINTER	Current Destination Pointer Register

2.2.4 Register Description

2.2.4.1 DMA_IRQ_PD0~3

DMA IRQx Pending Register

Offset = 0x0000+x*0x0004, 0≤x≤3

Bits	Name	Description	Access	Reset
31:12	-	Reserved	-	-
11	DMA11PD	DMA11 Interrupt Pending: (write 1 to reset, write 0 no effect) 0: DMA11 has no interrupt request on interrupt line x 1: DMA11 has interrupt request on interrupt line x	RW	0
10	DMA10PD	DMA10 Interrupt Pending: (write 1 to reset, write 0 no effect) 0: DMA10 has no interrupt request on interrupt line x 1: DMA10 has interrupt request on interrupt line x	RW	0
9	DMA9PD	DMA9 Interrupt Pending: (write 1 to reset, write 0 no effect) 0: DMA9 has no interrupt request on interrupt line x 1: DMA9 has interrupt request on interrupt line x	RW	0
8	DMA8PD	DMA8 Interrupt Pending: (write 1 to reset, write 0 no effect)	RW	0

		0: DMA8 has no interrupt request on interrupt line x 1: DMA8 has interrupt request on interrupt line x		
7	DMA7PD	DMA7 Interrupt Pending: (write 1 to reset, write 0 no effect) 0: DMA7 has no interrupt request on interrupt line x 1: DMA7 has interrupt request on interrupt line x	RW	0
6	DMA6PD	DMA6 Interrupt Pending: (write 1 to reset, write 0 no effect) 0: DMA6 has no interrupt request on interrupt line x 1: DMA6 has interrupt request on interrupt line x	RW	0
5	DMA5PD	DMA5 Interrupt Pending: (write 1 to reset, write 0 no effect) 0: DMA5 has no interrupt request on interrupt line x 1: DMA5 has interrupt request on interrupt line x	RW	0
4	DMA4PD	DMA4 Interrupt Pending: (write 1 to reset, write 0 no effect) 0: DMA4 has no interrupt request on interrupt line x 1: DMA4 has interrupt request on interrupt line x	RW	0
3	DMA3PD	DMA3 Interrupt Pending: (write 1 to reset, write 0 no effect) 0: DMA3 has no interrupt request on interrupt line x 1: DMA3 has interrupt request on interrupt line x	RW	0
2	DMA2PD	DMA2 Interrupt Pending: (write 1 to reset, write 0 no effect) 0: DMA2 has no interrupt request on interrupt line x 1: DMA2 has interrupt request on interrupt line x	RW	0
1	DMA1PD	DMA1 Interrupt Pending: (write 1 to reset, write 0 no effect) 0: DMA1 has no interrupt request on interrupt line x 1: DMA1 has interrupt request on interrupt line x	RW	0
0	DMA0PD	DMA0 Interrupt Pending: (write 1 to reset, write 0 no effect) 0: DMA0 has no interrupt request on interrupt line x 1: DMA0 has interrupt request on interrupt line x	RW	0

2.2.4.2 DMA_IRQ_EN0~3

DMA IRQx Enable Register

Offset = 0x0010+x*0x0004, 0≤x≤3

Bits	Name	Description	Access	Reset
31:12	-	Reserved	-	-
11	DMA11IRQEN	DMA11 Interrupt Enable: 0: DMA11 disabled interrupt on interrupt line x 1: DMA11 enabled interrupt on interrupt line x	RW	0

10	DMA10IRQEN	DMA10 Interrupt Enable: 0: DMA10 disabled interrupt on interrupt line x 1: DMA10 enabled interrupt on interrupt line x	RW	0
9	DMA9IRQEN	DMA9 Interrupt Enable: 0: DMA9 disabled interrupt on interrupt line x 1: DMA9 enabled interrupt on interrupt line x	RW	0
8	DMA8IRQEN	DMA8 Interrupt Enable: 0: DMA8 disabled interrupt on interrupt line x 1: DMA8 enabled interrupt on interrupt line x	RW	0
7	DMA7IRQEN	DMA7 Interrupt Enable: 0: DMA7 disabled interrupt on interrupt line x 1: DMA7 enabled interrupt on interrupt line x	RW	0
6	DMA6IRQEN	DMA6 Interrupt Enable: 0: DMA6 disabled interrupt on interrupt line x 1: DMA6 enabled interrupt on interrupt line x	RW	0
5	DMA5IRQEN	DMA5 Interrupt Enable: 0: DMA5 disabled interrupt on interrupt line x 1: DMA5 enabled interrupt on interrupt line x	RW	0
4	DMA4IRQEN	DMA4 Interrupt Enable: 0: DMA4 disabled interrupt on interrupt line x 1: DMA4 enabled interrupt on interrupt line x	RW	0
3	DMA3IRQEN	DMA3 Interrupt Enable: 0: DMA3 disabled interrupt on interrupt line x 1: DMA3 enabled interrupt on interrupt line x	RW	0
2	DMA2IRQEN	DMA2 Interrupt Enable: 0: DMA2 disabled interrupt on interrupt line x 1: DMA2 enabled interrupt on interrupt line x	RW	0
1	DMA1IRQEN	DMA1 Interrupt Enable: 0: DMA1 disabled interrupt on interrupt line x 1: DMA1 enabled interrupt on interrupt line x	RW	0
0	DMA0IRQEN	DMA0 Interrupt Enable: 0: DMA0 disabled interrupt on interrupt line x 1: DMA0 enabled interrupt on interrupt line x		

2.2.4.3 DMAx_MODE

DMAx Mode Register

Offset = 0x0100+x*0x0100, 0≤x≤11

Bits	Name	Description	Access	Reset
31	CME	Chained Mode Enable: 0: Disable 1: Enable	RW	0
30	LME	Link list Mode Enable: 0: Disable	RW	0

		1: Enable		
29	CFE	Constant Fill Mode Enable: 0: Disable 1: Enable	RW	0
28	NDDBW	NIC Device Data Bus Width: 0: 32 1: 8 (only for UART byte transfer, not applicable for other device)	RW	0
27:24	-	Reserved	-	-
23	CB	Critical Bit: (only take effect in AXI ID field) 0: Identify the request sent to DCU as non-real time request 1: Identify the request sent to DCU as real time request	RW	0
22:20	PW	Priority Weight: N 0: 1 1: 2 2: 4 3: 8 4: 16 5: 32 6: 64 7: 128	RW	0
19:18	DAM	Destination Address Mode: 0: Constant 1: Increment 2: Stride 3: Reserved	RW	0
17:16	SAM	Source Address Mode: 0: Constant 1: Increment 2: Stride 3: Reserved	RW	0
15:12	-	Reserved	-	-
11:10	DT	Destination Type: 0: Device 1: Reserved 2: DCU 3: ShareRAM	RW	0
9..8	ST	Source Type: 0: Device 1: Reserved 2: DCU 3: ShareRAM	RW	0
7:6	-	Reserved	-	-
5:0	TS	Trigger Source:	RW	0

		Refer to the 2nd column of Trig source Table, named **DRQ connect**		

2.2.4.4 DMAx_SOURCE

DMAx Source Register

Offset = 0x0104+x*0x0100, 0≤x≤11

Bits	Name	Description	Access	Reset
31:0	DSA	DMA Source Address	RW	0

2.2.4.5 DMAx_DESTINATION

DMAx Destination Register

Offset = 0x0108+x*0x0100, 0≤x≤11

Bits	Name	Description	Access	Reset
31:0	DDA	DMA Destination Address	RW	0

2.2.4.6 DMAx_FRAME_LEN

DMAx Frame Length Register

Offset = 0x010C+x*0x0100, 0≤x≤11

Bits	Name	Description	Access	Reset
31:24	-	Reserved	R	0
23:0	DFL	DMA Frame Length (by bytes)	RW	0

2.2.4.7 DMAx_FRAME_CNT

DMAx Frame Count Register

Offset = 0x0110+x*0x0100, 0≤x≤11

Bits	Name	Description	Access	Reset
31:12	-	Reserved	R	0
11:0	DFC	DMA Frame Count (by frames)	RW	1

Note: limitations about the transmission length and address aligning are listed below:

1. *If logic channel is const fill mode, frame_length must be multiples of 4-byte*
2. *All the access address of all devices must be word aligned (including srmi)*
3. *Frame and framecount should not exceed 4G*

Besides all these limitations, address is not request to be aligned; frame length and stride are not limited.

2.2.4.8 DMAx_REMAIN_FRAME_CNT

DMAx Remain Frame Count Register

Offset = 0x0114+x*0x0100, 0≤x≤11

Bits	Name	Description	Access	Reset
30:12	-	Reserved	-	-
11:0	DTRC	DMA Remain Frame Count in the Current Block (by frames)	R	0

2.2.4.9 DMAx_REMAIN_CNT

DMAx Current Frame Remain Count Register

Offset = 0x0118+x*0x0100, 0≤x≤11

Bits	Name	Description	Access	Reset
31:24	-	Reserved	-	-
23:0	DCFRC	DMA Remain Count in the Current Frame (by bytes)	R	0

2.2.4.10 DMAx_SOURCE_STRIDE

DMAx Source Stride Register

Offset = 0x011C+x*0x0100, 0≤x≤11

Bits	Name	Description	Access	Reset
31:0	DSS	DMA Source Stride (by bytes)	RW	0

2.2.4.11 DMAx_DESTINATION_STRIDE

DMAx Destination Stride Register

Offset = 0x0120+x*0x0100, 0≤x≤11

Bits	Name	Description	Access	Reset
31:0	DDS	DMA Destination Stride (by bytes)	RW	0

2.2.4.12 DMAx_START

DMAx Start Register

Offset = 0x0124+x*0x0100, 0≤x≤11

Bits	Name	Description	Access	Reset
31:1	-	Reserved	-	-
0	DSE	DMA Start Enable: 0: Disable 1: Enable *Note: After a transfer has been finished, the bit will be auto cleared. Writing 0 to START bit can terminate*	RW	0

		this DMA task whenever transfer is going on.		

2.2.4.13 DMAx_PAUSE

DMAx ACP Attribute Register

Offset = 0x0128+x*0x0100, 0≤x≤11

Bits	Name	Description	Access	Reset
31:1	-	Reserved	-	-
0	PAUSE	DMA PAUSE: 0: Disable 1: Enable	RW	0

2.2.4.14 DMAx_CHAINED_CTL

DMAx Chained Control Register

Offset = 0x012C+x*0x0100, 0≤x≤11

Bits	Name	Description	Access	Reset
31:4	-	Reserved	-	-
3:0	NLCN	Next Logical Channel Number (which will be hardware auto started after this DMA task finishes)	RW	0

2.2.4.15 DMAx_CONSTANT

DMAx Constant Data Register

Offset = 0x0130+x*0x0100, 0≤x≤11

Bits	Name	Description	Access	Reset
31:0	DCD	DMA Constant Data	RW	0

2.2.4.16 DMAx_LINKLIST_CTL

DMAx Link list Control Register

Offset = 0x0134+x*0x0100, 0≤x≤11

Bits	Name	Description	Access	Reset
31:17	-	Reserved	-	-
16	SUSPEND	Suspend the linked-list transfer at completion of the current block transfer. 0: Linked list is active. 1: Linked list is suspended at the boundary of next descriptor loading.	RW	0
15:12	-	Reserved	-	-
11:10	DAV	Destination Address Valid 0: The destination address is not present in the next	RW	0

		descriptor and continuous incrementing is enabled. 1: The destination address must be reloaded in the next descriptor transfer. 0x2: The destination start address is not present in the next descriptor. But will reload the one from configuration memory which belongs to the previous descriptor. 0x3: Reserved		
9..8	SAV	Source Address Valid 0: The source address is not present in the next descriptor and continuous incrementing is enabled. 1: The source address must be reloaded in the next descriptor transfer. 0x2: The source start address is not present in the next descriptor. But will reload the one from configuration memory which belongs to the previous descriptor. 0x3: Reserved	RW	0
7:0	-	Reserved	-	-

2.2.4.17 DMAx_NEXT_DESCRIPTOR

DMAx Next DESCRIPTOR Register

Offset = 0x0138+x*0x0100, 0≤x≤11

Bits	Name	Description	Access	Reset
31:2	NDP	Next Descriptor Pointer: This register contains the Next descriptor Address Pointer for the link list	RW	0
1:0	-	Reserved	-	-

2.2.4.18 DMAx_CURRENT_DESCRIPTOR_NUM

DMAx Current Descriptor Number Register

Offset = 0x013C+x*0x0100, 0≤x≤11

Bits	Name	Description	Access	Reset
31:16	-	Reserved	-	-
15:0	NDP	This register contains the current active descriptor number in the link list when it is read	R	0

2.2.4.19 DMAx_INT_CTL

DMAx Interrupt Control Register

Offset = 0x0140+x*0x0100, 0≤x≤11

Bits	Name	Description	Access	Reset

31:5	-	Reserved	-	-
4	ELF	Enable Last Frame Interrupt (start of last frame) : 0: Disable 1: Enable	RW	0
3	EEHF	Enable End of Half Frame Interrupt: 0: Disable 1: Enable	RW	0
2	EEF	Enable End of Frame Interrupt: 0: Disable 1: Enable	RW	0
1	EESB	Enable End of Super Block Interrupt: 0: Disable 1: Enable	RW	0
0	EEB	Enable End of Block Interrupt: 0: Disable 1: Enable	RW	0

2.2.4.20 DMAx_INT_STATUS

DMAx Interrupt Status Register

Offset = 0x0144+x*0x0100, 0≤x≤11

Bits	Name	Description	Access	Reset
31:5	-	Reserved	-	-
4	LF	Last Frame Interrupt (start of last frame) : 0: Not Take Place 1: Take Place	RW	0
3	EHF	End of Half Frame Interrupt: 0: Not Take Place 1: Take Place	RW	0
2	EF	End of Frame Interrupt: 0: Not Take Place 1: Take Place	RW	0
1	ESB	End of Super Block Interrupt: 0: Not Take Place 1: Take Place	RW	0
0	EB	End of Block Interrupt: 0: Not Take Place 1: Take Place	RW	0

2.2.4.21 DMAx_CURRENT_SOURCE_POINTER

DMAx Current Source Pointer Register

Offset = 0x0148+x*0x0100, 0≤x≤11

Bits	Name	Description	Access	Reset
31:0	DCSP	DMA Current Source Pointer	R	0

2.2.4.22 DMAx_CURRENT_DESTINATION_POINTER

DMAx Current Destination Pointer Register

Offset = 0x014C+x*0x0100, 0≤x≤11

Bits	Name	Description	Access	Reset
31:0	DCDP	DMA Current Destination Pointer	R	0

2.3 SPS (Smart Power System)

2.3.1 Function

It's very important to provide stable and adequate power for high-speed digital and sensitive analog circuit. Power and ground are separated into several groups to achieve good and stable power quality. This part will introduce the power system of S900, which are divided into several VDD voltage domains.

2.3.2 Power on Sequence

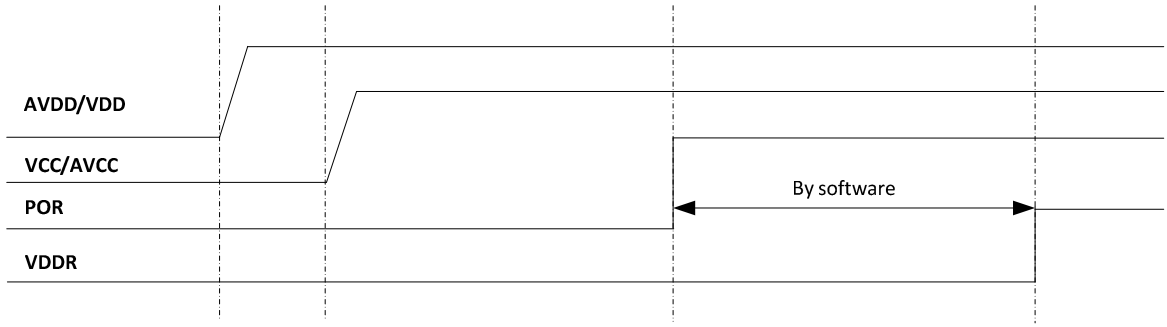


Figure 2 - 1 S900 Power on Sequence (co-work with ATC260x)

S900 get power source from our co-chip ATC260x PMIC, first stage is the power on process of ATC260x, at S900 AVDD/VDD is firstly given and VCC/AVCC will be powered closely after that. Once the power of PMIC is steady, it will send POR (Power on Reset) signal to S900. Then the S900 enters power on stage, after a while the system is powered on, then VDDR's power can be configured by software.

2.4 Secure Engine

2.4.1 Function

The security of the TrustZone subsystem is achieved by partitioning SoC's hardware and software resources into two worlds: Secure world for security subsystem and Normal/non-security world for everything else. The physical processor core provide two virtual cores, one called normal world and other secure. The non-secure virtual processor can only access non-secure system resources, but the secure virtual processor can see all resources. The monitor mode is introduced to switch context between these two worlds. The entry to monitor can be triggered by software executing dedicated instruction or by hardware exception.

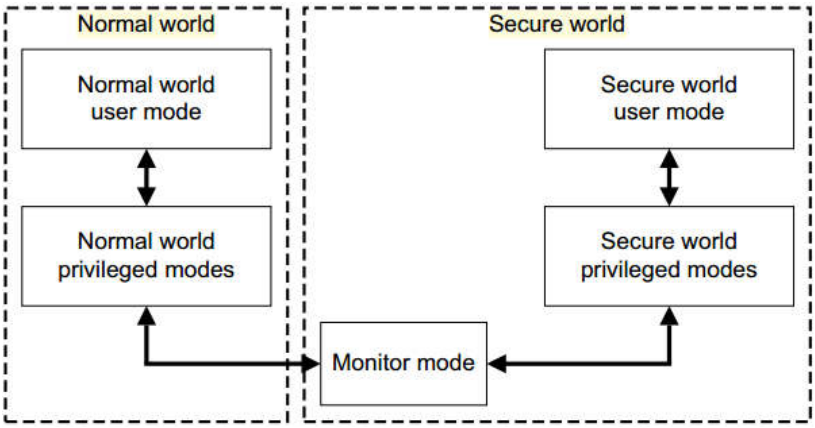


Figure 2 - 2 Modes in ARM Core Implementing Secure Extensions

The primary component in implementing the system wide isolation is the AMBA3 AXI bus matrix, which is extended for extra control signal (NS bits) to distinguish secure resources from non-secure resources.

The AMBA3 APB does not carry NS bits, so that it is compatible with the AMBA2 APB bus. In security system, it is attached to the system bus through an AXI-to-APB and APB-to-AXI bridges, which is responsible for managing the security of the APB peripherals.

More details on the TrustZone, please refer to ARM technical book.

2.5 HDCP2Tx

2.5.1 Function

A HDCP Transmitter (Tx) and Receiver (Rx) pair performs authentication before it performs AV data transfer. Authentication involves a series of control messages to be exchanged among transmitter and receiver. After receiver is authentic and a secret key that will be used for encrypting AV data, encrypted datum begin to transfer between a HDCP pair.

Hardware and Software together play a role in authentication process. Software detects receiver when it is connected and directs the Hardware to start authentication. Hardware generates control message and associated data for authentication, writes the data to registers and inform Software to let it transfer

messages to receiver. Control messages received from the other end are written to register set by Software thereby Hardware reads and performs authentication checks.

When successfully finishing authentication, Software started PES payload Encryption after setting raw and encryption datum information, then Hardware would auto got plaintext datum from Input RFIFO, encrypted 128-bit block of payload, put encrypted 128-bit block into Output EFIFO. Hardware could output Encrypted datum with format of no TS Packet, Blu-ray TS Packet or MPEG2 TS Packet.

3 Multimedia System

3.1 MIPI CSI2

3.1.1 Function

The Mobile Industry Processor Interface (MIPI) Alliance defines Camera Serial Interface-2 (CSI2) between a peripheral device (camera) and a host processor (AP) . It receives data transmitted from camera sensor and sends it to the image processor for further processing and finally transferred to host processor. S900 has two channel of CSI interface, CSI0 and CSI1. Features of MIPI CSI2 are listed below:

- Compliant with MIPI CSI-2 Specification version 1.0 and D-PHY specification version 0.9
- High-Speed Mode: 80 Mbps to 1 Gbps synchronous
- Low-Power Mode: spaced one-hot encoding for data
- Ultra low power support
- Support Data Type: YUV422-8bit, RGB565, RGB888, RAW8, RAW10
- Dual channel CSI of CSI0 (4 lane) and CSI1 (2 lane)
- 1-4 Data Lanes Configurable

3.1.2 Register List

Table 3 - 1 CSI-2 Receiver Registers Address

Name	Physical Base Address
CSI0	0xE02D0000
CSI1	0xE02D8000

Table 3 - 2 CSI-2 Receiver Registers

Offset	Register Name	Description
0x00	CSIx_CTRL	CSI-2 Receiver Control Register
0x04	CSIx_SHORT_PACKET	Short Packet Register
0x08	CSIx_ERROR_PENDING	Error Pending Register
0x0C	CSIx_STATUS_PENDING	Status Pending Register
0x10	CSIx_LANE_STATUS	Lane Status Register
0x14	CSIx_PHY_T0	CSI PHY Timing0 Register
0x18	CSIx_PHY_T1	CSI PHY Timing1 Register
0x1C	CSIx_PHY_T2	CSI PHY Timing2 Register
0x20	CSIx_ANALOG_PHY	CSI analog PHY config Register
0x28	CSIx_PIN_MAP	CSI data lane pin mapping control
0x100	CSIx_CONTEXT_CFG	Context Configuration Register

0x104	CSIx_CONTEXT_STATUS	Context Status Register

Note: 'x' in CSIx_CTRL represents that Each Context is configured independently with a register block, As follows:

Table 3 - 3 Data Lane configuration register block base address

Data Lane	Registers Block Base Address Offset
Context0	0x100
Context1	0x120

Table 3 - 4 Context configuration register

Offset	Register Name	Description
0x00	CONTEXTX_CFG	Context Configuration Register
0x04	CONTEXTX_STATUS	Context Status Register

3.1.3 Register Description

3.1.3.1 CSIx_CTRL

This register is mainly used to configure the CSI-2 Receiver to fit the application.

CSI_CTRL Offset=0x00

Bits	Name	Description	Access	Reset
31:11	-	Reserved	-	-
10	HSCLK_EDGE	HSCLK Sample Edge 0:Rising Edge 1:Falling Edge	RW	0
09	PHY_INIT_SEL	0: check the init LP11 sequence 1: don't check init LP11 sequence	RW	0
08	CLK_LANE_HS	Force receiving hs clock omitting hs entry sequence: 0: Disable 1: Enable	RW	0
07	CCE	CRC Check Enable 0: Disable 1: Enable	RW	0
06	ECE	ECC Check Enable 0: Disable 1: Enable	RW	0
05:04	LANE_NUM	Data Lane Number 00: Data Lane 0 (1 Data Lane) 01: Data Lane 0 ~ 1 (2 Data Lanes) 10: Data Lane 0 ~ 2 (3 Data Lanes) 11: Data Lane 0 ~ 3 (4 Data Lanes)	RW	0
03	PHY_CALEN	Init the D-PHY calibration	RW	0

		0: do not operate 1: Init the D-PHY calibration Note: After D-PHY is calibration done, this bit will be changed to '0' .		
02	D_PHY_EN	D-PHY Block Enable 0: Disable (D-PHY is powered off) 1: Enable (D-PHY is powered on)	RW	0
01	-	Reserved	-	-
00	EN	CSI-2 Receiver ENABLE Enable logical operation of CSI-2 Receiver 1: Enable 0: Disable *Note: When CSI-2 Receiver is enabled, Data Lane and Clock Lane are both enable, and Data Lane is forced into Receive mode and wait for Stop State. When CSI-2 Receiver is disabled, the state of digital logic goes to initial state.*	RW	0

3.1.3.2 CSIx_SHORT_PACKET

This register is mainly used to store the short packet information from Image Sensor.

SHORT_PACKET Offset=0x04

Bits	Name	Description	Access	Reset
31:24	-	Reserved	-	-
23:00	SHORT_PACKET	Short Packet Information (Not include ECC)	R	0

3.1.3.3 CSIx_ERROR_PENDING

This register reflects the error pending bit of CSI-2 Receiver .

ERROR_PENDING Offset=0x08

Bits	Name	Description	Access	Reset
31:30	-	Reserved	-	-
29	OVF	FIFO Overflow 0: no FIFO Overflow Error 1: FIFO Overflow Error Write 1 to clear the bit	RW	0
28	ERR_CONTROL_CLK	False Control Error of Clock Lane 0: no error occurred 1: an incorrect line state sequence is detected. Write 1 to clear the bit	RW	0
27:24	ERR_SOTSYNCHS_D	Start-of-Transmission (SoT) Error 0: no error occurred	RW	0

		1: An incorrect synchronization sequence is detected (more than 1 bit error) .. Write 1 to clear the bit		
23:20	ERR_CONTROL_D	False Control Error 0: no error occurred 1: an incorrect line state sequence is detected. For example, if a BTA request or escape mode request is immediately followed by a Stop state instead of the required Bridge state. Write 1 to clear the bit	RW	0
19:16	ERR_ESC_D	Escape Entry Error Pending Bit 0: no error occurred 1: an unrecognized escape entry command is received. Write 1 to clear the bit	RW	0
15:14	-	Reserved	-	-
13	ERR_CRC	Receive CRC Error Bit 0: no error occured 1: a CRC Error occured when receiving long packet Write 1 to clear the bit	RW	0
12	ERR_ECC	Receive ECC Error Bit 0: no error occurred or a single-bit error occurs and corrected 1: multi-bit errors occur Write 1 to clear the bit	RW	0
11:08	ERR_ID_VC	An error Identification on Virtual Channel 0~3 is received 0: no error occurred 1: an unrecognized or unimplemented data ID is received. Write 1 to clear the bit	RW	0
07:04	EFS_VC	Error of Frame Sync Packet on Virtual Channel 0~3 0: No error occurred 1: Error occurred Write 1 to clear the bit	RW	0
03:00	ELS_VC	Error of Line Sync Packet on Virtual Channel 0~3 0: No error occurred 1: Error occurred Write 1 to clear the bit	RW	0

3.1.3.4 CSIx_STATUS_PENDING

This register reflects the status pending bit of CSI-2 Receiver .

STATUS_PENDING Offset=0x0C

Bits	Name	Description	Access	Reset
31:23	-	Reserved	-	-
22	SOFT_ERROR	Soft Error Pending Bit 0: No error occurred 1: Error occurred Write 1 to clear the bit	RW	0
21	HARD_ERROR	Hard Error Pending Bit 0: No error occurred 1: Error occurred Write 1 to clear the bit	RW	0
20	SP_RX_DONE	Short Packet received done 0: no short packet is received 1: a short packet is received Write 1 to clear the bit	RW	0
19:17	-	Reserved	-	-
16	CONTEXT0	Context 0 Event Complete bit 0: Context 0 Event doesn’t complete 1: Context 0 Event completes Note: The corresponding FE of the context is received indicates that event completes. Write 1 to clear the bit	RW	0
15:06	-	Reserved	-	-
05	HARD_ERROR_EN	Hard Error Interrupt Enable 0: Disable 1: Enable	RW	0
04	SP_RX_DONE_EN	Short Packet received done Interrupt Enable 0: Disable 1: Enable	RW	0
03:01	-	Reserved	-	-
0	CONTEXT0_EN	Context 0 Event Complete Interrupt Enable 0: Disable 1: Enable	RW	0

3.1.3.5 CSIx_LANE_STATUS

This register specifies the Lane Status of the CSI-2 Receiver

LANE_STATUS Offset=0x10

Bits	Name	Description	Access	Reset
31:10	-	Reserved	-	-
09:06	DULP	Data Lane is in Ultra-Low Power State 0: Data Lane is not in Ultra-Low Power State 1: Data Lane is in Ultra-Low Power State Note: Bit 9 for Data Lane 3, Bit 8 for Data Lane 2, Bit 7 for Data Lane 1, Bit 6 for Data Lane 0	R	0
05:02	DST	Data Lane is in RX Stop-State 0: Data Lane is not in RX Stop State 1: Data Lane is in RX Stop State Note: Bit 5 for Data Lane 3, Bit 4 for Data Lane 2, Bit 3 for Data Lane 1, Bit 2 for Data Lane 0	R	0
01	CULP	Clock Lane is in Ultra-Low Power State 0: Lane is not in Ultra-Low Power State 1: Lane is in Ultra-Low Power State	R	0
00	CST	Clock Lane is in RX Stop State 0: Lane is not in RX Stop State 1: Lane is in RX Stop State	R	0

3.1.3.6 CSIx_PHY_T0

CSI D-PHY Operation Timing0 Register – For Clock Lane/Data Lane initial time.

CSI_PHY_T0 Offset=0x14

Bit (s)	Name	Description	Access	Reset
31:12	-	Reserved	-	-
11:00	$T_{INITIAL}$	Initial Time for Clock Lane/Data Lane. $T = 16 * (T_{INITIAL} + 1) * T_{CSI2\_Clk}$ Note: The timing parameter in multiples of CSI2_Clk period.	RW	0x1FF

3.1.3.7 CSIx_PHY_T1

CSI D-PHY Operation Timing1 Register – For Clock Lane

CSI_PHY_T1 Offset=0x18

Bit (s)	Name	Description	Access	Reset
31:12	-	Reserved	-	-
11:04	T_{CLK_SETTLE}	Settle Time for Clock Lane. $T = (T_{CLK\_SETTLE} + 1) * T_{CSI2\_Clk}$ Note: The timing parameter in multiples of CSI2_Clk period.	RW	0xF
03:00	$T_{CLK\_TERM\_EN}$	Time to enable Clk Lane receiver line termination measured from when DN crossed	RW	0x3

		Vilmax. $T = (T_{Clk\text{-}TERM\text{-}EN} + 1) * T_{CSI2\_Clk}$ Note: The timing parameter in multiples of CSI2_Clk period.		

3.1.3.8 CSIx_PHY_T2

CSI D-PHY Operation Timing2 Register – For Data Lane

CSI_PHY_T2 Offset=0x1c

Bit (s)	Name	Description	Access	Reset
31:12	-	Reserved	-	-
11:04	T_{HS_SETTLE}	Settle Time for Data Lane. $T = (T_{HS\text{-}SETTLE} + 1) * T_{CSI2\_Clk}$ Note: The timing parameter in multiples of CSI2_Clk period.	RW	0xF
03:00	$T_{D\_TERM\text{-}EN}$	Time to enable Data Lane receiver line termination measured from when DN crossed Vilmax. $T = (T_{D\text{-}TERM\text{-}EN} + 1) * T_{CSI2\_Clk}$ Note: The timing parameter in multiples of CSI2_Clk period.	RW	0x3

3.1.3.9 CSIx_ANALOG_PHY

CSI analog-PHY Operation config

CSI_Analog_PHY Offset=0x20

Bit (s)	Name	Description	Access	Reset
31:30	-	Reserved	-	-
29:26	DATA3_PH	Adjust data3 phase	RW	0x8
25:22	DATA2_PH	Adjust data2 phase	RW	0x8
21:18	DATA1_PH	Adjust data1 phase	RW	0x8
17:14	DATA0_PH	Adjust data0 phase	RW	0x8
13:10	CLK_PH	Adjust CLOCK lane phase	RW	0x8
9:6	DRT_DATA	Direction of CSI datalane3,2,1,0 0: obverse 1:inverse	RW	0
5	DRT_CLK	Direction of CSI Clk lane 0: obverse 1:inverse	RW	0
4:0	CLK_DATA_EN	Clk lane and four data lane enable signal Order is D4 D3 D2 D1 CK	RW	0

3.1.3.10 CSIx_PIN_MAP

CSI data lane pin mapping control

CSI_PIN_MAP Offset=0x28

Bits	Name	Description	Access	Reset
31:12	-	Reserved	-	-
11:9	DLANE3_MAP	MIPI CSI Lane 3 Mapping: 0: Data 0 1: Data 1 0x2: Data 2 0x3: Data 3 Others: Reserved	RW	0x3
8:6	DLANE2_MAP	MIPI CSI Lane 2 Mapping: 0: Data 0 1: Data 1 0x2: Data 2 0x3: Data 3 Others: Reserved	RW	0x2
5:3	DLANE1_MAP	MIPI CSI Lane 1 Mapping: 0: Data 0 1: Data 1 0x2: Data 2 0x3: Data 3 Others: Reserved	RW	1
2:0	DLANE0_MAP	MIPI CSI Lane 0 Mapping: 0: Data 0 1: Data 1 0x2: Data 2 0x3: Data 3 Others: Reserved	RW	0

3.1.3.11 CSIx_CONTEXT_CFG

This register is mainly used to configure the format of Context x.

Offset=0x100

Note: In the register descripiton, the prosfix "x" means each Context has the register

Bits	Name	Description	Access	Reset
31:09	-	Reserved	-	-
08:07	VCN	Virtual Channel Number	RW	0
06:01	DT	Data Type of received Long Packet	RW	0x1E

		0x12: Embedded 8-bit non Image Data 0x1E: YUV422 8-bit 0x22: RGB565 0x24: RGB888 0x2A: RAW8 0x2B: RAW10 0x2C: RAW12 0x30: User Defined 8-bit Data Type 1 0x31: User Defined 8-bit Data Type 2 0x32: User Defined 8-bit Data Type 3 0x33: User Defined 8-bit Data Type 4 Others: Reserved *Note: Hardware will use the data type to detect the desired long packet.*		
00	EN	Enable the Context 0: disable 1: enable	RW	0

3.1.3.12 CSIx_CONTEXT_STATUS

This register is mainly used to store the status of Context x.

Offset=0x104

Note: In the register descripiton, the prosfix "x" means each Context has the register

Bits	Name	Description	Access	Reset
31:16	-	Reserved	-	-
15:00	LINE_NUM	Current Line Number	R	0

3.2 LVDS

3.2.1 Function

LVDS module is to convert the pixel stream output from the display engine to the standard display panels. The features of LVDS module is listed below:

- Support dual channel LVDS interface LCD
- Support max clock frequency up to 200M
- Support LVDS RGB 24/18bit data
- Support data lanes swap for convenient PCB design

The LVDS controller supports single lane or dual lane LVDS interface LCD panel and can be configured to 18bits or 24bits interface. It consists of 8 data channels & 2 clock channels (5 even channels, 5 odd channels)

3.2.2 Register List

Table 3 - 5 TVOUT Controller Registers Address

Name	Physical Base Address
LCD	0xE02A0000
LVDS	0xE02A0200

Table 3 - 6 LCD Controller Registers

Offset	Register Name	Description
0x0000	LCD_CTL	LCD Control register
0x0004	LCD_SIZE	LCD Size register
0x0008	LCD_STATUS	LCD Status register
0x000C	LCD_TIM0	LCD RGB Timing0 register
0x0010	LCD_TIM1	LCD RGB Timing1 register
0x0014	LCD_TIM2	LCD RGB Timing2 register
0x0018	LCD_COLOR	LCD Color register
0x001C	LCD_IMG_XPOS	LCD image x position in the screen
0x0020	LCD_IMG_YPOS	LCD image y position in the screen
0x0000	LVDS_CTL	LVDS Control Register
0x0004	LVDS_ALG_CTL0	LVDS Analog Control Register 0

3.2.3 Register Description

3.2.3.1 LCD_CTL

LCD RGB Control register

Offset = 0x00

Bit (s)	Name	Description	Access	Reset
31	-	Reserved	-	-
30	SELF_RST	Self reset enable 0:disable, do not reset when DE_LCD_ST rising edge 1:enable, reset when DE_LCD_ST rising edge	RW	0
29:21	-	Reserved	-	-
20	PD_IDL_STA	LCD pad idle state configuration: 0: default level. 1: all LCD pad are drive low. *Note:* *1,If you set this bit, the output of all LCD pads will be low .* *2,If you want send normal data to LCD, this bit must be cleared.*	RW	0
19	-	Reserved	-	-
18:16	PAR_SER_SEL	Panel RGB Interface Type Select 000: 24-bit parallel 001: 18-bit parallel 010: 16-bit (5-6-5 format) parallel 011: 8-color mode parallel 100: 24-bit (8-8-8 format) serial 101: 18-bit (6-6-6 format) serial 110,111: reserved *Note: The unused pins of LD[23:0] should be in stable output state to avoid EMI.FOR RGB IF ONLY*	RW	0
15:13	CC_ODD	LCD color sequence configuration for odd line 000:RGB 001:RBG 010:GRB 011:GBR 100:BRG 101:BGR Other: reserved	RW	0
12:10	CC_EVEN	LCD color sequence configuration for even line 000: RGB	RW	0

		001:RBG 010:GRB 011:GBR 100:BRG 101:BGR Other: reserved		
9: 8	PAD	Color padding to 32 bit/pixel 00: do not pad 01: pad X after 10: pad X before 11:reserved For example: if CC_ODD=0 and PAD=01, then the serial output should be RGBX. FOR RGB IF ONLY	RW	0
7:6	VOM	Video Output Mode 00:dual mode, drive the LCD with DE0 and DE1. (used with bit28 DUAL_EN) 00: Reserved 01: Reserved. 10: Drive the LCD form DE. 11: Drive the LCD with default color.	RW	0x3
5: 2		Reserved	-	-
1	RB_SWAP	Swap R,B in input data 0:R,B NO SWAP 1:R,B SWAP	RW	0
0	EN	LCDC ENABLE 0:disable 1:enable RGB IF: when enable, LCDC get ready to start RGB IF timing *Note: LCDC go start when the LCD_ST signal comes*	RW	0

3.2.3.2 LCD_SIZE

LCD RGB Size register

Offset = 0x04

Bit (s)	Name	Description	Access	Reset
31:28	-	Reserved	-	-
27:16	Y	Screen Height (in pixels) for RGB IF IF Panel height is Y+1	RW	0
15:12	-	Reserved	-	-
11: 0	X	Screen Width (in pixels) for RGB IF	RW	0

		Panel width is X+1		

3.2.3.3 LCD_STATUS

LCD Status register

Offset = 0x08

Bit (s)	Name	Description	Access	Reset
31	VBI	Vertical Blanking pending Asserted during vertical no-display period every frame. Interrupt triggered at the beginning of blanking period Write '1' clear.	RW	0
30	VBE	VB interrupt enable	RW	0
29	HBI	Horizontal Blanking state Asserted during horizontal no-display period every scan line. Interrupt triggered at the beginning of blanking period Write '1' clear.	RW	0
28	HBE	HB interrupt enable	RW	0
27	AVSI	Active Video Display pending Asserted during active video display time for each line, Interrupt triggered at the beginning of active period for each line Write '1' clear.	RW	0
26	AVSE	AVS interrupt enable	RW	0
25	FEIP	Frame trans end interrupt pending Write '1' clear.	RW	0
24	FEIE	FEI enable	RW	0
23:12	CX	Current scan pixel's x AXIs location (in pixels)	R	1
11:0	CY	Current scan pixel's y AXIs location (in pixels)	R	0

3.2.3.4 LCD_TIM0

LCD RGB Timing0 register

Offset = 0x0C

Bit (s)	Name	Description	Access	Reset
31:14	-	Reserved	-	-
13	PREL_EN	Pre_line enable 1:enable pre_line function 0:disable pre_line function	RW	0
12:8	PREL_CNT	Pre_line counter.	RW	0

		If this counter set x, the LCDC will send a pre_line signal to DE when is has send [VSPW-x)] valid horizontal data pulse.		
7	VSYNC_INV	Vsync Output Polarity Inversion	RW	0
6	HSYNC_INV	Hsync Output Polarity Inversion	RW	0
5	DCLK_INV	DCLK Output Polarity Inversion	RW	0
4	LDE_INV	LDE Output Polarity Inversion	RW	0
3:0	-	Reserved	-	-

Notes:

*When we define the timing parameters, it often refers to TpClk (short for "pixel cycle period") . In parallel output mode, TpClk = TdClk; in serial mode, TpClk = TdClk * 3.*

3.2.3.5 LCD_TIM1

LCD RGB Timing1 register

Offset = 0x10

Bit (s)	Name	Description	Access	Reset
31:30	-	Reserved	-	-
29:20	HSPW	Horizontal Sync Pulse Width (in pixels) Thspw = (HSPW+1) * TpClk	RW	0
19:10	HFP	Horizontal Front Porch (in pixels) Thfp = (HFP +1) * TpClk	RW	0
9:0	HBP	Horizontal Back Porch (in pixels) Thbp = (HBP +1) * TpClk	RW	0

3.2.3.6 LCD_TIM2

LCD RGB Timing2 register

Offset = 0x14

Bits	Name	Description	Access	Reset
31:30	-	Reserved	-	-
28:20	VSPW	Vertical Sync Pulse Width (in lines) Tvspw = (VSPW+1) * Thsync	RW	0
19:10	VFP	Vertical Front Porch (in lines) Tvfp = (VFP +1) * Thsync	RW	0
9:0	VBP	Vertical Back Porch (in lines) Tvbp = (VBP +1) * Thsync	RW	0

3.2.3.7 LCD_COLOR

LCD RGB LCD Color register

Offset = 0x18

Bit (s)	Name	Description	Access	Reset
31:24	-	Reserved	-	-
23:16	R	panel's default color R	RW	0
15:8	G	panel's default color G	RW	0
7:0	B	panel's default color B	RW	0

3.2.3.8 LCD_IMG_XPOS

LCD image x position in the screen

Offset = 0x2C

Bit (s)	Name	Description	Access	Reset
31:28	-	Reserved	-	-
27:16	XSTART	At which line does the image begin	RW	0
15:12	-	Reserved	-	-
11:00	XEND	At which line does the image end	RW	0

3.2.3.9 LCD_IMG_YPOS

LCD image y position in the screen

Offset = 0x30

Bit (s)	Name	Description	Access	Reset
31:28	-	Reserved	-	-
27:16	YSTART	At which column does the image begin	RW	0
15:12	-	Reserved	-	-
11:00	YEND	At which column does the image end	RW	0

3.2.3.10 LVDS_CTL

LVDS Control Register

Offset = 0x0000

Bit (s)	Name	Description	Access	Reset
31:21	-	Reserved	-	-
20	E_RSV	Even Port RSV Signal Select 0: Always '0' 1: Always '1'	RW	0
19:18	E_DE	Even Port DE Signal Select 00: Always '0' 01: Always '1' 1x: DE	RW	0
17:16	E_VS	Even Port VS Signal Select 00: Always '0' 01: Always '1'	RW	0

		1x: VS		
15:14	E_HS	Even Port HS Signal Select 00: Always '0' 01: Always '1' 1x: HS	RW	0
13	O_RSV	Odd Port RSV Signal Select 0: Always '0' 1: Always '1'	RW	0
12:11	O_DE	Odd Port DE Signal Select 00: Always '0' 01: Always '1' 1x: DE	RW	0
10:9	O_VS	Odd Port VS Signal Select 00: Always '0' 01: Always '1' 1x: VS	RW	0
8:7	O_HS	Odd Port HS Signal Select 00: Always '0' 01: Always '1' 1x: HS	RW	0
6	MIRROR	LVDS Mirror Select 0: Normal (TXE3+ TXE3- … TXO0+ TIO0-) 1: Mirror (TXO0+ TXO0- … TXE3+ TIE3-)	RW	0
5	CH_SWAP	LVDS Channel Swap Select 0: No Swap 1: Odd/Even Swap	RW	0
4:3	MAPPING	Output Mapping Select 00: NS Mode 01: JEIDA Mode Others: Reserved	RW	0
2	CHANNEL	Channel Select 0: Single Channel 1: Dual Channel	RW	0
1	FORMAT	Output Format 0: 18-bit 1: 24-bit	RW	0
0	EN	LVDS Interface Enable 0: Disable 1: Enable (LVDS & RSDS can't be both enabled)	RW	0

3.2.3.11 LVDS_ALG_CTL0

LVDS Analog Control Register 0

Offset = 0x04

Bit (s)	Name	Description	Access	Reset
31	IBPOWL	Bias current on&off	RW	0
30	PLLPOWL	PLL power on	RW	0
29:26	-	Reserved	-	-
25:24	SLVDSIL	Set LVDS Tx CMFB Circuit Bias Current 'IBLV<14:0>' (IBLV<14>, IBLV<13> not used) 20u*[1]+10u*[0]+50u	RW	0x2
23	-	Reserved	-	-
22:20	SVOCML	Set LVDS Tx common mode reference voltage 'vocm' 000->1.04V 001->1.08V 010->1.13V 011->1.18V 100->1.22V 101->1.27V 110->1.32V 111->1.37V	RW	0x4
19:18	-	Reserved	-	-
17:15	SPLLIL	Set PLL charge pump current 20u*[2]+10u*[1]+5u*[0]+5u	RW	0x6
14:13	SPLLRL	Set PLL LPF resistor 00->6kOhm 01->8kOhm 10->10kOhm 11->12kOhm	RW	1
12:11	WDMODEL	PLL watch dog mode 00: WD active 01: set vc=1.5 1x: Disable WD	RW	0
10	PLLPOLARL	PLL input clock delay 180°or not 0: not delay 1: delay	RW	0
9:7	-	Reserved	-	-
6	POLARL	LVDS/RSDS output signal polarity control 0: polarity not changed 1: polarity reversed (all ! P/N swap)	RW	0
5	ELVDSPOWL	EVEN PORT Output driver power on	RW	1
4	OLVDSPOWL	ODD PORT Output driver power on	RW	1
3	ECKPOLARL	Bring forward EVEN PORT channel [D] Serializers clock 'CKOUT' 180°or not ('CKSEL' is also brought forward half period of 'CKOUT') 0:not 1:ahead 180°	RW	0

2	OCKPOLARL	Bring forward ODD PORT channel [D] Serializers clock 'CKOUT' 180°or not ('CKSEL' is also brought forward half period of 'CKOUT') 0:not 1:ahead 180°	RW	0
1	ENVBPBL	Bring forward DUAL-PORT (except channel [D]) Serializes clock 'CKOUT' 180°or not ('CKSEL' is also brought forward half period of 'CKOUT') 0:not 1:ahead 180°	RW	0
0	LVDS_LOCK	LVDS PLL status	R	0

3.3 eDP (embedded Display Port)

3.3.1 Function

The embedded interface of eDP is the electrical transport for video and auxiliary data between the graphics hardware and the display panel. It primarily connects external box-to-box interfaces. The external interfaces must interoperate with any connected compliant system over a variety of compliant calbes. Features of eDP interface are listed below.

- DisplayPort 1.2 functionality
  - compliance tested core
  - software link policy maker
  - not support HDCP function
  - SST only
  - Deep color to 24 bits per pixel
- Full link rate and lane count support
  - 1, 2, or 4 lanes
  - 1.62Gbps, 2.7Gbps, or 5.4Gbps
- Embedded DisplayPort 1.3
  - Alternate framing / scrambler reset
  - Fast link training
  - Panel self-refresh
- Main link – 1, 2, or 4 lanes
  - Component bit depth 8 bits per color plane
  - RGB, YCbCr444/422
- Aux Channel
  - Host initiated transactions
  - Hardware request and reply engines
- Hot Plug Detection
  - insertion event detection
  - interrupt detection
  - Audio not support
- eDP PHY supported

3.3.2 Register List

Table 3 - 7 eDP Base Address

Name	Physical Base Address
eDP_Register	0xE0190000

Table 3 - 8 eDP Offset Address

Offset	Register Name	Description
Link configuration Register		
0x0004	EDP_LNK_LANE_COUNT	LINK LANE Count set register
0x0008	EDP_LNK_ENHANCED	LINK Enhanced Frame enable Register
0x0014	EDP_LNK_SCR_CTRL	LINK Scrambling disable register
0x0018	EDP_LNK_DSPR_CTRL	V LINK Downspread control register
0x0020	EDP_LNK_PANEL_SRF	LINK Panel Self Refresh Register
Core Enable Register		
0x0080	EDP_CORE_TX_EN	CORE Transmitter Output enable Register
0x0084	EDP_CORE_MSTREAM_EN	CORE Main Stream enable Register
0x0088	EDP_CORE_SSTREAM_EN	CORE Secondary Stream Enable Register
0x00C4	EDP_CORE_USER_CFG	CORE User control Status Register
0x00F8	EDP_CORE_CAPS	CORE Capabilities Register
0x00FC	EDP_CORE_ID	CORE ID register
AUX Channel Interface Register		
0x0100	EDP_AUX_COMD	AUX Channel COMMAND Register
0x0104	EDP_AUX_WR_FIFO	AUX_WRITE_FIFO register
0x0108	EDP_AUX_ADDR	AUX_ADDRESS register
0x010C	EDP_AUX_CLK_DIV	Generating the internal 1MHz clock from the 24M clock.
0x0130	EDP_AUX_STATE	AUX status register
0x0134	EDP_AUX_RPLY_DAT	AUX Channel reply data register
0x0138	EDP_AUX_RPLY_CODE	Contains the reply code received from the most recent AUX Channel request.
0x013C	EDP_AUX_RPLY_COUNT	Provides an internal count of the number of reply transactions received on the AUX Channel.
0x0140	EDP_AUX_INT_STAT	AUX_INTERRUPT_STATUS Register
0x0144	EDP_AUX_INT_MASK	AUX_INTERRUPT_MASK Register
0x0148	EDP_AUX_RPLY_DAT_CNT	Returns the total number of data bytes received during a reply transaction from the sink device.
0x014C	EDP_AUX_STATUS	AUX_STATUS register
0x0150	EDP_AUX_RCLK_WIDTH	Reports the width of the AUX channel reply clock in APB_CLK cycles.
Main Stream Attributes Register		
0x0180	EDP_MSTREAM_HTOTAL	Specifies the total number of clocks in the horizontal framing period for the main stream video signal.
0x0184	EDP_MSTREAM_VTOTAL	Provides the total number of lines between vertical sync pulses in the main stream video frame.
0x0188	EDP_MSTREAM_POLARITY	Provides the polarity values for the video horizontal and vertical sync signals.
0x018C	EDP_MSTREAM_HSWIDTH	Sets the width of the horizontal sync pulse

		measured in pixel clock periods.
0x0190	EDP_MSTREAM_VSWIDTH	Sets the width of the vertical sync pulse in lines.
0x0194	EDP_MSTREAM_HRES	Number of active pixels per line of the main stream video.
0x0198	EDP_MSTREAM_VRES	Number of active lines of video in the main stream video source.
0x019C	EDP_MSTREAM_HSTART	Specifies the number of clocks between the leading edge of the horizontal sync and the start of active data.
0x01A0	EDP_MSTREAM_VSTART	Number of lines between the leading edge of the vertical sync and the first line of active data.
0x01A4	EDP_MSTREAM_MISC0	contains information about the main link video stream clocking and color representation. These bits are mapped from the DisplayPort specification MISC0 register definitions.
0x01A8	EDP_MSTREAM_MISC1	provide interlaced and stereo video information
0x01AC	EDP_M_VID	M_VID value
0x01B0	EDP_MTRANSFER_UNIT	TRANSFER_UNIT_SIZE register
0x01B4	EDP_N_VID	N_VID value
0x01B8	EDP_USER_PIXEL_WIDTH	Select single or dual pixel wide interface
0x01BC	EDP_USER_DATA_COUNT	this value is the total number of 16-bit words in a line of active data.
0x01C0	EDP_MSTREAM_INTERLACED	Informs the DisplayPort transmitter main link that the source video is interlaced.
0x01C4	EDP_USER_SYNC_POLARITY	Indicates the polarity of the video source sync signals.
PHY configuration and Status Register		
0x0200	EDP_PHY_RESET	Primary reset for the transmitter PHY.
0x0204	EDP_PHY_PREEM_L0	Controls the pre-emphasis level for lane 0 of the transmitter.
0x0208	EDP_PHY_PREEM_L1	Controls the pre-emphasis level for lane 1 of the transmitter.
0x020C	EDP_PHY_PREEM_L2	Controls the pre-emphasis level for lane 2 of the transmitter.
0x0210	EDP_PHY_PREEM_L3	Controls the pre-emphasis level for lane 3 of the transmitter.
0x0214	EDP_PHY_VSW_L0	Controls the voltage swing for lane 0 of the transmitter.
0x0218	EDP_PHY_VSW_L1	Controls the voltage swing for lane 1 of the transmitter.
0x021C	EDP_PHY_VSW_L2	Controls the voltage swing for lane 2 of the transmitter.
0x0220	EDP_PHY_VSW_L3	Controls the voltage swing for lane 3 of the transmitter.

0x0224	EDP_PHY_VSW_AUX	Controls the voltage swing for aux channel.
0x0228	EDP_PHY_PWR_DOWN	power down the lanes
0x022C	EDP_PHY_CAL_CONFIG	Controls the calibrate function register
0x0230	EDP_PHY_CAL_CTRL	
0x0234	EDP_PHY_CTRL	Controls the PHY channel register.
EDP RGB control Register		
0x0500	EDP_RGB_CTL	RGB control register
0x0504	EDP_RGB_STATUS	RGB status register
0x0508	EDP_RGB_COLOR	Set RGB default color

3.3.3 Register Description

3.3.3.1 EDP_LNK_LANE_COUNT

LINK LANE Count set register

Offset = 0x0004

Bit (s)	Name	Description	Access	Reset
31:5	-	Reserved	-	-
4:0	LCS	LANE_COUNT_SET The transmitter uses this register to set the number of lanes that will be used to configure and operate the link. Unused lanes will not be active during training or video transmission. In some implementations, the external PHY will set the unused lanes to the electrically state. 4:0 – This field is equivalent to the DPCD register of the same name. Supported values are 1, 2, or 4 lanes.	RW	0x0

3.3.3.2 EDP_LNK_ENHANCED

LINK Enhanced Frame enable Register

Offset=0x0008

Bit (s)	Name	Description	Access	Reset
31:1	-	Reserved	-	-
0	EFE	ENHANCED_FRAME_EN Enables the enhanced framing mode as supported by the DisplayPort specification. This mode must be used when supporting HDCP functions. Set to a '1' by the source to enable the enhanced framing symbols.	RW	0x0

3.3.3.3 EDP_LNK_SCR_CTRL

LINK Scrambling disable register

Offset=0x0014

Bit (s)	Name	Description	Access	Reset
31:1	-	Reserved	-	-
0	SD	SCRAMBLING_DISABLE Used to disable the internal scrambling function of the DisplayPort transmitter. This bit must be set during the link training process. Set to a '1' to disable the hardware scrambling function. Set to a '0' for normal operation.	RW	0x0

3.3.3.4 EDP_LNK_DSPR_CTRL

LINK Downspread control register

Offset=0x0018

Bit (s)	Name	Description	Access	Reset
31:1	-	Reserved	-	-
0	DSC	DOWNSPREAD_CTRL In order to reduce the electrical noise generated by the DisplayPort link, the transmitter may implement clock downspreading. This function must also be supported by the target sink device as reported in the DPCD information. Set to a '1' to enable a 0.5% spreading of the clock or '0' for none. Note: The clock downspreading function is implemented in the PHY and is dependent on the platform specific implementation.	RW	0x0

3.3.3.5 EDP_LNK_PANEL_SRF

LINK Panel Self Refresh Register

Offset=0x0020

Bit (s)	Name	Description	Access	Reset
31:1	-	Reserved	-	-
0	PSR	PANEL_SELF_REFRESH Writing to this register causes the DisplayPort controller to issue a properly formatted secondary packet to receiver at the end of the current video frame. This secondary packet instructs the receiver to	RW	0x0

		enter the panel self-refresh mode. Set to a '1' to command the connected receiver into panel self-refresh mode. This bit will remain high until cleared. When in panel self-refresh mode, the core will ignore all video data on the user input port. User data transmission will be resumed at the next input vertical sync after this bit is cleared.		

3.3.3.6 EDP_CORE_TX_EN

CORE Transmitter Output enable Register

Offset=0x0080

Bit (s)	Name	Description	Access	Reset
31:1	-	Reserved	-	-
0	TOE	TRANSMITTER_OUTPUT_ENABLE This bit is used to disable all output of the main link framing logic. When set to '0', the transmitter core will output only stuffing symbols onto the link. No control symbols or valid link data are transmitted when disabled. This bit prevents the link controller core from interfering with the PHY power up sequence. Set to a '1' after the link output has been configured and the external PHY is ready to begin operations.	RW	0x0

3.3.3.7 EDP_CORE_MSTREAM_EN

CORE Main Stream enable Register

Offset=0x0084

Bit (s)	Name	Description	Access	Reset
31:1	-	Reserved	-	-
0	MSE	MAIN_STREAM_ENABLE Once the link is configured and is ready to begin transmitting user video and audio data, this bit is written to a '1'. When set to '0', the active lanes of the DisplayPort transmitter will output the "No Video" pattern. Secondary stream data will continue to transmit. Setting this bit to a '0' and the SECONDARY_STREAM_ENABLE bit to a '1' will result in an audio only configuration.	RW	0

		When set to '0', the active lanes of the DisplayPort transmitter will output only VB-ID information with the NoVideoStream flag set to a '1'.		

3.3.3.8 EDP_CORE_SSTREAM_EN

CORE Secondary Stream Enable Register

Offset=0x0088

Bit (s)	Name	Description	Access	Reset
31:1	-	Reserved	-	-
0	SSE	SECONDARY_STREAM_ENABLE When the host system is ready to begin the transmission of secondary packets including audio information, this bit is written to a '1'. When set to '0', the active lanes of the DisplayPort transmitter will not send secondary data as a part of the stream. A value of '0' in this register will disable secondary data and will set the AudioMute flag in the VB-ID to a '1'.	RW	0

3.3.3.9 EDP_CORE_USER_CFG

CORE User control Status Register

Offset=0x00C4

Bit (s)	Name	Description	Access	Reset
31:4	-	Reserved	-	-
3	UCOE	USER_CONTROL_ODDEVEN: state of the polarity corrected vid_oddeven control input.	R	0
2	UCD	USER_CONTROL_DEN: state of the polarity corrected vid_enable control input.	R	0
1	UCH	USER_CONTROL_HSYNC: state of the polarity corrected vid_hsync control input.	R	0
0	UCV	Provides a direct copy of the polarity corrected control signals from the user data interface. This register may be used to trigger specific events in the host system. 0 – USER_CONTROL_VSYNC: state of the polarity corrected vid_vsync control input.	R	0

3.3.3.10 EDP_CORE_CAPS

CORE Capabilities Register

Offset=0x00F8

Bit (s)	Name	Description	Access	Reset
31:11	-	Reserved	-	-
10	EP	EMBEDDED_PRESENT: set to '1' when support for embedded DisplayPort is present	R	0x1
9	SP	SECONDARY_PRESENT: set to '1' when the secondary channel is present.	R	0x1
8	HP	HDCP_PRESENT: set to '1' when the HDCP cipher logic is present.	R	0x0
7:3	-	Reserved	-	-
2:0	LC	Determines what functionality is available in a specific implementation of the core. This register may be used by software to determine the configuration of the core. 2:0 – LANE_COUNT: number of lanes implemented.	R	0x4

3.3.3.11 EDP_CORE_ID

CORE ID register

Offset=0x00FC

Bit (s)	Name	Description	Access	Reset
31:16	CID	Returns the unique identification code of the core. Core ID is fixed at 0x000A	R	0xA
15:0	RID	Returns the unique identification code of the current revision level. These codes may be used by the software to determine the revision level of the core. Core revision level is fixed at 0x0200	R	0x0305

3.3.3.12 EDP_AUX_COMD

AUX Channel COMMAND Register

Offset =0x0100

Bit (s)	Name	Description	Access	Reset
31:13	-	Reserved	-	-
12	AO	ADDRESS_ONLY: Set to a '1' to initiate an address only request.	RW	0x0

11:8	AC	COMMAND: AUX Channel Command. 0x8: AUX Write 0x9: AUX Read 0x0: I2C over AUX Write 0x4: I2C over AUX Write, Middle of Transaction bit set 0x1: I2C over AUX Read 0x5: I2C over AUX Read, Middle of Transaction bit set 0x2: I2C over AUX Write Status	RW	0x0
7:4	-	Reserved	-	-
3:0	Num	Specifies the number of bytes to transfer with the current command. The range of the register is 0 to 15 indicating between 1 and 16 bytes of data.	RW	0x0

Note: Initiates an AUX channel command of the specified length when written. This register is written last as part of the AUX channel request set up process. When written, the internal state machines will begin transmitting the request to the sink device. The AUX_ADDRESS and, when applicable, the AUX_WRITE_FIFO must be set up before writing this register.

3.3.3.13 EDP_AUX_WR_FIFO

AUX WRITE FIFO register
Offset=0x0104

Bit (s)	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7:0	AWF	Before initiating a native or I2C write request on the AUX channel, the host system must provide the write data to the FIFO mapped to this address. Only the number of bytes required to support the current transaction must be written to the FIFO. Subsequent writes to the FIFO must not be performed until the REQUEST_IN_PROGRESS bit is clear. 7:0 – Write only AUX Channel byte data. A read from this register is not supported, but will return the last data byte written.	W	0x0

3.3.3.14 EDP_AUX_ADDR

AUX ADDRESS register
Offset=0x0048

Bit (s)	Name	Description	Access	Reset

31:20	-	Reserved	-	-
19:0	AADDR	Each AUX request requires a 20-bit address for native AUX requests or an 8-bit address for I2C over AUX requests. This register specifies the address for the current AUX channel command. These bits are used without modification for the address field of the request. 19:0 – Twenty bit address for the start of the AUX Channel burst.	RW	0x0

3.3.3.15 EDP_AUX_CLK_DIV

AUX CLOCK DIVIDER register

Offset=0x010C

Bit (s)	Name	Description	Access	Reset
31:9	-	Reserved	-	-
8:0	ADIV	Contains the clock divider value for generating the internal 1MHz clock from the APB host interface clock. The clock divider register provides integer division only and does not support fractional APB clock rates. (e.g. set to 75 for a 75MHz APB clock) 8:0 – APB clock divider value. The valid range is 10 to 400.	RW	0x0

3.3.3.16 EDP_AUX_STATE

AUX STATE Register

Offset=0x0130

Bit (s)	Name	Description	Access	Reset
31:4	-	Reserved	-	-
3	RT	Holds status bits which report the internal state of the AUX channel management logic. Some of these signals are used to generate interrupts and can be used as polled status for systems that do not implement interrupts.. REPLY_TIMEOUT: a '1' indicates that a reply timeout has occurred	R	0x0
2	RR	REPLY_RECEIVED: a '1' indicates that a reply has been received	R	0x0
1	RIP	REQUEST_IN_PROGRESS: a '1' indicates that a	R	0x0

		request is currently being sent		
0	HPDS	HPD_STATE: contains the raw state of the HPD pin on the DisplayPort connector	R	0x1

3.3.3.17 EDP_AUX_RPLY_DAT

AUX Channel REPLY DATA Register

Offset=0x0134

Bit (s)	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7:0	ARDAT	This read only address maps to the internal FIFO which contains up to 16 bytes of information received during the AUX channel reply. Reply data is read from the FIFO starting with byte 0. The number of valid bytes in the FIFO corresponds to the number of bytes received as indicated by the REPLY_DATA_COUNT register. 7:0 – AUX reply data from the sink device. Each read advances the internal read pointer.	R	0x0

3.3.3.18 EDP_AUX_RPLY_CODE

AUX REPLY CODE Register

Offset=0x0138

Bit (s)	Name	Description	Access	Reset
31:4	-	Reserved	-	-
3:0	ARCOD	Contains the reply code received from the most recent AUX Channel request. This code is the four bit field received by the reply controller from the sink device. The value of the code maps to the DisplayPort specification section 2.4.1.2 which is repeated below for clarity. 3:0 – AUX channel reply code received from the sink device. 0x0 = Native AUX ACK 0x1 = Native AUX NACK 0x2 = Native AUX Defer 0x0 = I2C over AUX ACK 0x4 = I2C over AUX NACK 0x8 = I2C over AUX Defer	R	0x0

3.3.3.19 EDP_AUX_RPLY_COUNT

AUX_REPLY_COUNT Register
Offset=0x013C

Bit (s)	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7:0	ARC	Provides an internal count of the number of reply transactions received on the AUX Channel. Each reply received from the sink device increments the count by 1. The reply code is not considered when incrementing this counter. Writing a '1' to this register clears the count. 7:0 – Current reply count. The value of this register will automatically roll over after reaching 255 replies received. 0 – write a '1' to this bit to clear the value	RW	0x0

3.3.3.20 EDP_AUX_INT_STAT

AUX_INTERRUPT_STATUS Register
Offset=0x0140

Bit (s)	Name	Description	Access	Reset
31:4	-	Reserved	-	-
3	RT	The transmitter core interrupt status register contains the cause of an interrupt asserted by the core. The specific events that can cause an interrupt and the associated status bits are shown below. A read from this register clears all values. REPLY_TIMEOUT: a reply timeout has occurred when the sink has not sent a response 400us after the transmitter has sent a request.	RW	0x0
2	RR	REPLY_RECIEVED: an AUX reply transaction has been detected. This value may be used to allow a system to process other events while waiting for a response from the sink device.	RW	0x0
1	HPE	HPD_EVENT: the core has detected the	RW	0x0

		presence of the HPD signal. This interrupt asserts immediately after the detection of HPD and after the loss of HPD for 2 msec.		
0	HPI	HPD_IRQ: an IRQ framed with the proper timing on the HPD signal has been detected.	RW	0x0

3.3.3.21 EDP_AUX_INT_MASK

AUX_INTERRUPT_MASK Register

Offset=0x0144

Bit (s)	Name	Description	Access	Reset
31:4	-	Reserved	-	-
3	RT	REPLY_TIMEOUT_MASK: write a '0' to this bit to allow reply timeout events to cause an interrupt to be asserted	RW	0x1
2	RR	REPLY_RECEIVED_MASK: write a '0' to this bit to allow reply received events to cause an interrupt	RW	0x1
1	HPE	HPD_EVENT_MASK: write a '0' to this bit to allow HPD present events to cause an interrupt	RW	0x1
0	HPI	HPD_IRQ_EVENT: write a '0' to this bit to allow HPD_IRQ events to cause an interrupt	RW	0x1

3.3.3.22 EDP_AUX_RPLY_DAT_CNT

AUX_REPLY_DATA_COUNT Register

Offset=0x0148

Bit (s)	Name	Description	Access	Reset
31:5	-	Reserved	-	-
4:0	RDC	Returns the total number of data bytes received during a reply transaction from the sink device. This register does not use the length byte of the transaction header. The number of bytes is independently counted by the reply controller. The value of this register is cleared when a request transaction is initiated by the transmitter. 4:0 – Total number of data bytes received during the reply phase of the AUX transaction.	R	0x0

3.3.3.23 EDP_AUX_STATUS

AUX_STATUS register

Offset =0x014C

Bit (s)	Name	Description	Access	Reset
31:4	-	Reserved	-	-
3	RE	REPLY_ERROR: When set to a '1', the AUX reply logic has detected an error in the reply to the most recent AUX transaction. Errors are detected when the precharge and sync phases of the reply last more than 38 cycles instead of the maximum 32. This condition typically indicates noise on the AUX channel data signals.	R	0x0
2	RQIP	REQUEST_IN_PROGRESS: The AUX transaction request controller sets this bit to a '1' while actively transmitting a request on the AUX channel. The bit is set to '0' when the AUX transaction request controller is idle.	R	0x0
1	RIP	REPLY_IN_PROGRESS: The AUX reply detection logic sets this bit to a '1' while receiving a reply on the AUX channel. The bit is '0' otherwise.	R	0x0
0	RR	REPLY_RECEIVED: This bit is set to '0' when the AUX request controller begins sending bits on the AUX serial bus. The AUX reply controller sets this bit to '1' when a complete and valid reply transaction has been received. This bit is cleared when a request transaction has been initiated by the request controller.	RW	0x0

Note: This register contains the status of the internal AUX channel controllers. The progress of request and reply transactions are monitored an reply transactions are checked for errors. These bits are valid at all times.

3.3.3.24 EDP_AUX_RCLK_WIDTH

AUX_REPLY_CLOCK_WIDTH Register

Offset =0x0150

Bit (s)	Name	Description	Access	Reset
31:10	-	Reserved	-	-
9:0	ARCW	Reports the width of the AUX channel reply	R	0x0

		clock in APB_CLK cycles. This register is only valid after a properly formatted reply transaction has been received. The clock width is measured during the sync stage of the AUX channel transaction. 9:0 – Width of the AUX channel receive clock in APB_CLK cycles.		

3.3.3.25 EDP_MSTREAM_HTOTAL

MAIN_STREAM_HTOTAL register
Offset =0x0180

Bit (s)	Name	Description	Access	Reset
31:16	-	Reserved	-	-
15:0	Htotal	Specifies the total number of clocks in the horizontal framing period for the main stream video signal. This value is sent as the Main Stream Attribute Htotal. 15:0 – Horizontal line length total in clocks	RW	0x0

3.3.3.26 EDP_MSTREAM_VTOTAL

MAIN_STREAM_VTOTAL register
Offset =0x0184

Bit (s)	Name	Description	Access	Reset
31:16	-	Reserved	-	-
15:0	Vtotal	Provides the total number of lines between vertical sync pulses in the main stream video frame. This value is provided as the Main Stream Attribute Vtotal. 15:0 – Total number of lines per video frame.	RW	0x0

3.3.3.27 EDP_MSTREAM_POLARITY

MAIN_STREAM_POLARITY Register
Offset =0x0188

Bit (s)	Name	Description	Access	Reset
31:2	-	Reserved	-	-
1	VP	Provides the polarity values for the video horizontal and vertical sync signals. These bits are sent as a part of the Main Stream	RW	0x0

		Attributes as VSP and HSP. VSYNC_POLARITY: polarity of the vertical sync pulse		
0	HP	HSYNC_POLARITY: polarity of the horizontal sync pulse	RW	0x0

3.3.3.28 EDP_MSTREAM_HSWIDTH

MAIN_STREAM_HSWIDTH Register
Offset=0x018C

Bit (s)	Name	Description	Access	Reset
31:15	-	Reserved	-	-
14:0	HSwidth	Sets the width of the horizontal sync pulse measured in pixel clock periods. This value is provided on the link as the Main Stream Attribute field HSW. 14:0 – Horizontal sync width in clock cycles.	RW	0x0

3.3.3.29 EDP_MSTREAM_VSWIDTH

MAIN_STREAM_VSWIDTH Register
Offset=0x0190

Bit (s)	Name	Description	Access	Reset
31:15	-	Reserved	-	-
14:0	VSwidth	Sets the width of the vertical sync pulse in lines. The Main Stream Attribute VSW is used to carry this information on the link. 14:0 – Width of the vertical sync in lines.	RW	0x0

3.3.3.30 EDP_MSTREAM_HRES

MAIN_STREAM_HRES Register
Offset =0x0194

Bit (s)	Name	Description	Access	Reset
31:16	-	Reserved	-	-
15:0	HRES	Horizontal resolution of the main stream video source. This value is the number of active pixels per line and is represented in the Main Stream Attributes as the Hwidth field.	RW	0x0

		15:0 – Number of active pixels per line of the main stream video.		

3.3.3.31 EDP_MSTREAM_VRES

MAIN_STREAM_VRES Register
Offset=0x0198

Bit (s)	Name	Description	Access	Reset
31:16	-	Reserved	-	-
15:0	VRES	Vertical resolution of the main stream video source. The resolution is the number of active lines per frame. The Main Stream Attribute field Vheight carries this information to the sink. 15:0 – Number of active lines of video in the main stream video source.	RW	0x0

3.3.3.32 EDP_MSTREAM_HSTART

MAIN_STREAM_HSTART Register
Offset=0x019C

Bit (s)	Name	Description	Access	Reset
31:16	-	Reserved	-	-
15:0	HSTART	Specifies the number of clocks between the leading edge of the horizontal sync and the start of active data. This value is used for the Main Stream Attribute Hstart and is measured in pixel clocks. 15:0 – Horizontal start clock count	RW	0x0

3.3.3.33 EDP_MSTREAM_VSTART

MAIN_STREAM_VSTART Register
Offset=0x01A0

Bit (s)	Name	Description	Access	Reset
31:16	-	Reserved	-	-
15:0	VSTART	Number of lines between the leading edge of the vertical sync and the first line of active data. This value is carried in the Main Stream Attributes as the Vstart field.	RW	0x0

		15:0 – Vertical start line count.		

3.3.3.34 EDP_MSTREAM_MISC0

MAIN_STREAM_MISC0 Register
Offset=0x01A4

Bit (s)	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7:5	BD	This 8-bit value contains information about the main link video stream clocking and color representation. These bits are mapped from the DisplayPort specification MISC0 register definitions. BIT_DEPTH: number of bits per color 000 = 6 bits 001 = 8 bits 010 = 10 bits 011 = 12 bits 100 = 16 bits 101, 110, 111 = Reserved	RW	0x0
4	YC	YCBCR_COLORIMETRY: colorimetry of the main link video 0 = ITU-R BT601-5 1 = ITU-R BT709-5	RW	0x0
3	DR	DYNAMIC_RANGE: color range for each plane 0 = VESA range 1 = CEA range	RW	0x0
2:1	CF	COMPONENT_FORMAT: color representation format 00 = RGB 01 = YCbCr 4:2:2 10 = YCbCr 4:4:4 11 = Reserved	RW	0x0
0	SC	SYNCHRONOUS_CLOCK: clocking mode for the user data 0 = asynchronous clock 1 = synchronous clock	RW	0x0

3.3.3.35 EDP_MSTREAM_MISC1

MAIN_STREAM_ MISC1 Register
Offset=0x01A8

Bit (s)	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7:3	ZERO	These bits represent the Main Stream Attribute field MISC1 as defined in the DisplayPort specification. These bits provide interlaced and stereo video information. ZERO This field must be set to a 0 for proper operation. Any other value in this field may cause unpredictable operation.	RW	0x0
2:1	SVA	STEREO_VIDEO_ATTRIBUTE: 00 = No stereo video transported 01 = Top field or frame is for the RIGHT eye 10 = Reserved 11 = Top field or frame is for the LEFT eye	RW	0x0
0	ITE	INTERLACED_TOTAL_EVEN: 0 = number of lines per interlaced frame is odd 1 = number of lines per interlaced frame is even	RW	0x0

3.3.3.36 EDP_M_VID

MAIN_M_VID Register
Offset=0x01AC

Bit (s)	Name	Description	Access	Reset
31:24	-	Reserved	-	-
23:0	M_VID	The clocking values for the main stream video must be calculated by the host processor and provided in this register for transmission to the sink device. For most applications, this value can be set to the user data pixel clock value in KHz. 23:0 – unsigned value computed in the asynchronous clock mode	RW	0x0

3.3.3.37 EDP_MTRANSFER_UNIT

MAIN_TRANSFER_UNIT_SIZE Register
Offset=0x01B0

Bit (s)	Name	Description	Access	Reset

31:7	-	Reserved	-	-
6:0	TUS	A transfer unit is a DisplayPort micro-packet and represents valid data symbols and stuffing symbols. This register value sets the size of a transfer unit in the transmitter framing logic. Due to the design of the core, only even values are supported by this register. 6:0 – this number must be in the range of 32 to 64 for DisplayPort compliance and is typically set to a fixed value which depends on the inbound video mode. Larger values should be used for video modes with slower pixel clock rates. Smaller values should be used for video modes with higher pixel clock rates.	RW	0x20

3.3.3.38 EDP_N_VID

MAIN_N_VID Register
Offset =0x01B4

Bit (s)	Name	Description	Access	Reset
31:24	-	Reserved	-	-
23:0	N_VID	The second clocking value for the Main Stream Attributes is set based upon the link rate. This value, when used in conjunction with the M-VID value allows the sink device to recover the frequency of the user data pixel clock. 23:0 – unsigned value computed in the asynchronous clock mode. This value should be set to 162000 when operating the link in 1.62Gbps mode, 270000 when operating the link in 2.7Gbps mode, or 540000 when operating the link is 5.4Gbps mode.	RW	0x0

3.3.3.39 EDP_USER_PIXEL_WIDTH

MAIN_USER_PIXEL_WIDTH
Offset=0x01B8

Bit (s)	Name	Description	Access	Reset
31:2	-	Reserved	-	-
1:0	UPW	The user data interface to the transmitter core accepts either one or two pixels per clock cycle. This register selects the width of the user data input port and should be set before main link video is enabled. At reset, this register defaults to 1. 1:0 – Set to a value of 1 for a single pixel wide interface or 2 for a dual pixel wide interface.	RW	0x1

3.3.3.40 EDO_USER_DATA_COUNT

MAIN_USER_DATA_COUNT PER LANE
Offset=0x01BC

Bit (s)	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	UDCPL	USER_DATA_COUNT_PER_LANE Determines the total data count for the transmitter framing logic to read from the user FIFO before sending a blanking start symbol. In other words, this value is the total number of 16-bit words in a line of active data. The calculated value should be rounded up. 17:0 – set to HRES * bits per pixel / 16 - 1	RW	0x0

3.3.3.41 EDP_MSTREAM_INTERLACED

MAIN_STREAM_INTERLACED
Offset=0x01C0

Bit (s)	Name	Description	Access	Reset
31:1	-	Reserved	-	-
0	INLA	Informs the DisplayPort transmitter main link that the source video is interlaced. By setting this bit to a '1', the transmitter will set the appropriate fields in the VBID value and Main Stream Attributes. This bit must be set to a '1' for the proper transmission of interlaced sources. 0 – Set to a '1' when transmitting interlaced	RW	0x0

		images or ‘0’ for progressive sources.		

3.3.3.42 EDP_USER_SYNC_POLARITY

MAIN_USER_SYNC_POLARITY
Offset=0x01C4

Bit (s)	Name	Description	Access	Reset
31:4	-	Reserved	-	-
3	UOEP	Indicates the polarity of the video source sync signals. Set each bit to a ‘1’ for active high or a ‘0’ for active low. USER_ODDEVEN_POLARITY: polarity of the input odd/even field flag.	RW	0x1
2	UDEP	USER_DATA_ENABLE_POLARITY: polarity of the input user data enable signal.	RW	0x1
1	UVP	USER_VSYNC_POLARITY: polarity of the input user vertical sync pulse.	RW	0x1
0	UHP	USER_HSYNC_POLARITY: polarity of the input user horizontal sync	RW	0x1

3.3.3.43 EDP_PHY_RESET

EDP_PHY_RESET
Offset =0x0200

Bit (s)	Name	Description	Access	Reset
31:1	-	Reserved	-	-
0	PRST	This reset applies to the entire PHY implementation and holds all analog and digital portions of the implementation in reset. 0: normal operation 1: hold the PHY in reset.	RW	0x1

3.3.3.44 EDP_PHY_PREEM_L0

EDP_PHY_PRE_EMPHASIS_LANE0
Offset=0x0204

Bit (s)	Name	Description	Access	Reset
31:4	-	Reserved	-	-
3:0	PREML0	Controls the pre-emphasis level for lane 0 of the transmitter. 0000: 0dB	RW	0x0

		0001:3.5dB 0010:6dB other reserved		

3.3.3.45 EDP_PHY_ PREEM_L1

EDP_PHY_PRE_EMPHASIS_LANE1

Offset=0x0208

Bit (s)	Name	Description	Access	Reset
31:4	-	Reserved	-	-
3:0	PREML1	Controls the pre-emphasis level for lane 1 of the transmitter. 0000: 0dB 0001:3.5dB 0010:6dB other reserved	RW	0x0

3.3.3.46 EDP_PHY_ PREEM_L2

EDP_PHY_PRE_EMPHASIS_LANE2

Offset=0x020C

Bit (s)	Name	Description	Access	Reset
31:4	-	Reserved	-	-
3:0	PREML2	Controls the pre-emphasis level for lane 2 of the transmitter. 0000: 0dB 0001:3.5dB 0010:6dB other reserved	RW	0x0

3.3.3.47 EDP_PHY_ PREEM_L3

EDP_PHY_PRE_EMPHASIS_LANE3

Offset=0x0210

Bit (s)	Name	Description	Access	Reset
31:4	-	Reserved	-	-
3:0	PREML0	Controls the pre-emphasis level for lane 3 of the transmitter. 0000: 0dB 0001:3.5dB 0010:6dB other reserved	RW	0x0

3.3.3.48 EDP_PHY_VSW_L0

EDP_PHY_VOLTAGE_DIFF_LANE0

Offset=0x0214

Bit (s)	Name	Description	Access	Reset
31:4	-	Reserved	-	-
3:0	VDL0	Controls the voltage swing for lane 0 of the transmitter. 0000: 400mV 0001: 600mV 0010: 800mV Other reserved	RW	0x0

3.3.3.49 EDP_PHY_VSW_L1

EDP_PHY_VOLTAGE_DIFF_LANE1

Offset=0x0218

Bit (s)	Name	Description	Access	Reset
31:4	-	Reserved	-	-
3:0	VDL1	Controls the voltage swing for lane 1 of the transmitter. 0000: 400mV 0001: 600mV 0010: 800mV Other reserved	RW	0x0

3.3.3.50 EDP_PHY_VSW_L2

EDP_PHY_VOLTAGE_DIFF_LANE2

Offset=0x021C

Bit (s)	Name	Description	Access	Reset
31:4	-	Reserved	-	-
3:0	VDL2	Controls the voltage swing for lane 2 of the transmitter. 0000: 400mV 0001: 600mV 0010: 800mV Other reserved	RW	0x0

3.3.3.51 EDP_PHY_VSW_L3

EDP_PHY_VOLTAGE_DIFF_LANE3

Offset=0x0220

Bit (s)	Name	Description	Access	Reset
31:4	-	Reserved	-	-
3:0	VDL3	Controls the voltage swing for lane 3 of the transmitter. 0000: 400mV 0001: 600mV 0010: 800mV Other reserved	RW	0x0

3.3.3.52 EDP_PHY_VSW_AUX

EDP_PHY_VOLTAGE_DIFF_AUX

Offset=0x0224

Bit (s)	Name	Description	Access	Reset
31:4	-	Reserved	-	-
3:0	VDA	Controls the voltage swing for aux channel of the transmitter. 0000: 400mV 0001: 600mV 0010: 800mV Other reserved	RW	0x0

3.3.3.53 EDP_PHY_PWR_DOWN

EDP_PHY_POWER_DOWN Register

Offset=0x0228

Bit (s)	Name	Description	Access	Reset
31: 4	-	Reserved	-	-
3	PDL3	All PHY implementations support a power down function to place unused transmitter lanes into a low power state. These register bits control this function within the PHY. These register bits should be set to '0' for normal operation. 0: lane3 enable 1: lane3 power down	RW	0x1
2	PDL2	0: lane2 enable 1: lane2 power down	RW	0x1
1	PDL1	0: lane1 enable 1: lane1 power down	RW	0x1
0	PDL0	0: lane0 enable 1: lane0 power down	RW	0x1

3.3.3.54 EDP_PHY_CAL_CONFIG

PHY calibrate configure Register

Offset=0x022C

Bit (s)	Name	Description	Access	Reset
31	-	EDP PHY driver bypass res calibrate set 0 :default 1: bypass	RW	0x0
30:26	-	Reserved	-	-
25:24	CAL_RES	res calibrate setting 00: 50.67 01: 50 10: 49.34 11: 48.7	RW	0x1
23	-	Reserved	-	-
22:16	TRA_OV	EDP PHY preemable strength overide value when bit31 is high.	RW	0x0
15	-	Reserved	-	-
14:8	SEL_OV	EDP PHY sel pmos dirver number overide value when bit31 is high.	RW	0x5
7	-	Reserved	-	-
6:0	PSW_OV	EDP PHY driver resister control number overide value when bit31 is high.	RW	0x31

3.3.3.55 EDP_PHY_CAL_CTRL

PHY calibrate control Register

Offset=0x0230

Bit (s)	Name	Description	Access	Reset
31:9	-	Reserved	-	-
8	CAL_EN	EDP res calibrate enable signal, 0: disable 1: active Write 1 enable the RES calibrate, when calibrate finish, auto clear to 0.	RW	0x0
7	-	Reserved	-	-
6:0	CAL_CODE	Indicate the res calibrate output control code when calibrate finish done	R	0x30

3.3.3.56 EDP_PHY_CTRL

EDP_PHY control Register

Offset=0x0234

Bit (s)	Name	Description	Access	Reset
31: 16	-	Reserved	-	-
15	mirror	Main lane output channel Mirror Select 0: Normal 1: Mirror	RW	0x0
14: 13	-	Reserved	-	-
12	SEREN3	EDP PHY data lane3 parallel to serial function enable bit 0: disable 1: enable	RW	0x0
11	SEREN2	EDP PHY data lane2 parallel to serial function enable bit 0: disable 1: enable	RW	0x0
10	SEREN1	EDP PHY data lane1 parallel to serial function enable bit 0: disable 1: enable	RW	0x0
9	SEREN0	EDP PHY data lane0 parallel to serial function enable bit 0: disable 1: enable	RW	0x0
8	PAS	EDP PHY aux channel output signal Polarity select 0: polarity not changed 1: polarity reversed	RW	0x0
7	PLPS3	EDP PHY data lane3 output signal Polarity select 0: polarity not changed 1: polarity reversed	RW	0x0
6	PLPS2	EDP PHY data lane2 output signal Polarity select 0: polarity not changed 1: polarity reversed	RW	0x0
5	PLPS1	EDP PHY data lane1 output signal Polarity select 0: polarity not changed 1: polarity reversed	RW	0x0
4	PLPS0	EDP PHY data lane0 output signal Polarity select 0: polarity not changed 1: polarity reversed	RW	0x0
3	PLES3	EDP PHY data lane3 edge select signal when receive digital data bus. 0: Posedge, 1: Negedge	RW	0x0
2	PLES2	EDP PHY data lane2 edge select signal when receive digital data bus. 0: Posedge,	RW	0x0

		1: Negadge		
1	PLES1	EDP PHY data lane1 edge select signal when receive digital data bus. 0: Posedge, 1: Negedge	RW	0x0
0	PLES0	EDP PHY data lane0 edge select signal when receive digital data bus. 0: Posedge, 1: Negedge	RW	0x0

3.3.3.57 EDP_RGB_CTL

EDP RGB Control register

This register is mainly used to configure the controller to fit the specified RGB IF panel

Offset = 0x0500

Bits	Name	Description	Access	Reset
31:9	-	Reserved	-	-
8:4	PREL_CNT	Pre_line counter. if this counter set x, the RGB will send a pre_line signal to DE when is has send [VSPW-x)] valid horizontal data pluse.	RW	0x0
3:2	-	Reserved	-	-
1	VOM	Video Output Mode 0: Drive the LCD form DE. 1: Drive the LCD with default color.	RW	0x0
0	EN	RGB ENABLE 0： disable 1： enable when enable, RGB controller get ready to start RGB IF timing	RW	0

3.3.3.58 EDP_RGB_STATUS

EDP Status register

Offset = 0x0504

Bits	Name	Description	Access	Reset
31:1	-	Reserved	-	-
0	FEIE	Frame trans complete bit 0: not complete 1: complete Write ‘1’ clear.	RW	0x0

3.3.3.59 EDP_RGB_COLOR

EDP Color register

Offset = 0x0508

Bits	Name	Description	Access	Reset
31:24	-	Reserved	-	-
23:16	R	panel's default color R	RW	0x0
15:8	G	panel's default color G	RW	0x0
7:0	B	panel's default color B	RW	0x0

3.4 MIPI DSI

3.4.1 Function

MIPI DSI (Display Serial Interface) is the standard display interface that complies with MIPI Alliance. The DSI Host Controller deals with data transmit and receive. When transmitting data, DSI Host Controller may work in High-Speed mode or Low-power mode; when receiving data, DSI Host Controller works in Low-Power mode only. Features of MIPI DSI are listed below:

- Compliant with MIPI DSI Specification version 1.1 and the D-PHY specification version 1.1
- Support Command and Video mode Transmissions
- Support three Transmission Timings in Video mode:
  - Non-Burst Mode with Sync Pulses
  - Non-Burst Mode with Sync Events
  - Burst Mode
- Pixel Format:
  - Command Mode: 8bits, 12bits, 16bits, 18bits, and 24bits per pixel
  - Video Mode: RGB565, RGB666 (Packed), RGB666, and RGB888
- Support Power Save Mode during HS Transmission
- Support LP and ULP transmission
- Support Bus Turn-Around for receiving peripheral-to-processor transmissions
- Support 1-4 data lanes, from 75 Mbps to 1Gbps per lane
- Support four data lanes random mapping

3.4.2 Register List

Table 3 - 9 MIPI DSI Controller Registers Address

Name	Physical Base Address
DSI	0xE01E0000

Table 3 - 10 MIPI DSI Controller Registers

Offset	Register Name	Description
0x0000	DSI_CTRL	DSI Control Register
0x0004	DSI_SIZE	DSI Screen Size Register
0x0008	DSI_COLOR	DSI Default Color Register
0x000C	DSI_VIDEO_CFG	DSI Video Configure Register
0x0010	DSI_RGBHT0	DSI RGB Hsync Timing0 Register
0x0014	DSI_RGBHT1	DSI RGB Hsync Timing1 Register
0x0018	DSI_RGBVT0	DSI RGB Vsync Timing0 Register
0x001c	DSI_RGBVT1	DSI RGB Vsync Timing1 Register
0x0020	DSI_TIMEOUT	DSI Time Out Register

0x0024	DSI_TR_STA	DSI Transfer State Register
0x0028	DSI_INT_EN	DSI Interrupt Enable Register
0x002c	DSI_ERROR_REPORT	DSI Error Report Register
0x0030	DSI_FIFO_ODAT	DSI FIFO Output Data Register
0x0034	DSI_FIFO_IDAT	DSI FIFO Input Data Register
0x0038	DSI_IPACK	DSI Input Packet Information Register
0x0040	DSI_PACK_CFG	DSI Packet Configure Register
0x0044	DSI_PACK_HEADER	DSI Packet Header Register
0x0048	DSI_TX_TRIGGER	DSI TX Trigger Register
0x004c	DSI_RX_TRIGGER	DSI RX Trigger Register
0x0050	DSI_LANE_CTRL	DSI Lane Control Register
0x0054	DSI_LANE_STA	DSI Lane State Register
0x0060	DSI_PHY_T0	DSI PHY Timing0 Register
0x0064	DSI_PHY_T1	DSI PHY Timing1 Register
0x0068	DSI_PHY_T2	DSI PHY Timing2 Register
0x007c	DSI_LANE_SWAP	DSI LANE SWAP Control Register
0x0080	DSI_PHY_CTRL	DSI D-PHY Control Register

3.4.3 Register Description

3.4.3.1 DSI_CTRL

DSI Control Register

Offset=0x00

Bits	Name	Description	Access	Reset
31	DSI_PHY_EN	D-PHY Block Enable 0: Disable (D-PHY is powered off) 1: Enable (D-PHY is powered on)	RW	0x0
30	DSI_CALEN	Init and CAL the D-PHY Block 0: do not operate 1: CAL the D-PHY Note: After D-PHY is powered on, software must initial the D-PHY. When D-PHY_INIT goes to low, Analog Phy completes the initialization process. And Digital Phy starts to work after that	RW	0x0
29:13	-	Reserved	-	-
12	TR_MODE	0: Command Mode 1: Video Mode	RW	0x0
11:10	VC	Virtual channel number (also for Odd Field in Interlaced Video)	RW	0x0

09:08	DL_NUM	Data Lane Number 00: Data Lane 0 (1 Data Lane) 01: Data Lane 0 ~ 1 (2 Data Lanes) 10: Data Lane 0 ~ 2 (3 Data Lanes) 11: Data Lane 0 ~ 3 (4 Data Lanes)	RW	0x0
07	VOM	Video Output Mode 0: Drive the panel with video from DE 1: Drive the panel with default color	RW	0x0
06	CON_CLK	Continue Clock Lane 1: Continue Clock Lane 0: non-Continue Clock Lane	RW	0x0
05	RB_SWAP	Swap R,B in input data 0: R,B NO SWAP 1: R,B SWAP	RW	0x0
04	EOTP_EN	EOTP Enable 0: Disable 1: Enable Note: Devices compliant to DSI spec v1.0 and earlier do not support EOTP	RW	0x0
03	SOFT_RST	Soft Reset for RX FIFO 、RX Logic and TX FIFO、TX Logic when received error occurs. 0: no Reset 1: Reset	RW	0x0
02:00	-	Reserved	-	-

Note: This register is mainly used to configure the controller to fit the application.

3.4.3.2 DSI_SIZE

DSI Screen Size Register

Offset=0x04

Bits	Name	Description	Access	Reset
31:28	-	Reserved	-	-
27:16	Y	Active lines per frame (Active lines per field for interlaced video)	RW	0x0
15:00	-	Reserved	-	-

*Note: This register is used to configure the size of the active pixel per line and active lines per frame. Support up to 2048*2048.*

3.4.3.3 DSI_COLOR

DSI Default Color Register

Offset=0x08

Bits	Name	Description	Access	Reset

31:24	-	Reserved	-	-
23:16	R	panel's default color R	RW	0x0
15:08	G	panel's default color G	RW	0x0
7:0	B	panel's default color B	RW	0x0

Note: This register specifies panel's default color.

3.4.3.4 DSI_VIDEO_CFG

DSI Video Configure Register

Offset=0x0C

Bits	Name	Description	Access	Reset
30:15	-	Reserved	-	-
14	HSA_PS_EN	HSA period in Video mode Power-Saving Mode Enable (only active in Non-Burst Mode with Sync Pulses mode) 1 : Enable 0 : Disable	RW	0x0
13	HBP_PS_EN	HBP period in Video mode Power-Saving Mode Enable 1 : Enable 0 : Disable	RW	0x0
12	HFP_PS_EN	HFP period in Video mode Power-Saving Mode Enable 1 : Enable 0 : Disable	RW	0x0
11	-	Reserved	-	-
10:08	RGB_FM	RGB Color Format 000: 16-bit Format (RGB565) 001: 18-bit Packed Format (RGB666) 010: 18-bit Loosely Packed Format (RGB666) 011: 24-bit Format (RGB888) Others: reserved	RW	0x0
07	-	Reserved	-	-
06:05	EVEN_VC	Virtual channel number For Even Filed (Only Active for Interlaced Video)	RW	0x0
04	SCAN_MODE	Video Scan Format Select 0 : Progressive 1 : Interlaced	RW	0x0
03	BLLP_PS_EN	BLLP period Power-Saving Mode Enable 1 : Enable 0 : Disable	RW	0x0
02:01	VMS	Video Mode Select 00: Non-Burst Mode with Sync Pulses (Sync mode) 01: Non-Burst Mode with Sync Events (DE mode) 10: Burst Mode (time-compressed mode) 11: reserved	RW	0x0

00	EN	Video Mode Start to process 1 : Enable 0 : Disable	RW	0x0

Note: This register is mainly used to configure the video mode. (Only for video mode)

3.4.3.5 DSI_RGBHT0

DSI RGB Hsync Timing0 Register

Offset=0x10

Bits	Name	Description	Access	Reset
31:30	-	Reserved	-	-
29:20	HAS	Horizontal Sync Active Width T_{hsa} = HAS * T_{phy_clk} / lane_num	RW	0x0
19:10	HFP	Horizontal Front Porch T_{hfp} = HFP * T_{phy_clk} / lane_num	RW	0x0
9:0	HBP	Horizontal Back Porch T_{hbp} = HBP * T_{phy_clk} / lane_num	RW	0x0

Note: This register specifies timing parameters of the horizontal sync signal.
The timing settings do not include Packet Header and Packet Foot. Software must consider PH and PF in order to satisfy the accurate Peripheral timing requirement.

3.4.3.6 DSI_RGBHT1

DSI RGB Hsync Timing1 Register

Offset=0x14

Bits	Name	Description	Access	Reset
31:12	-	Reserved	-	-
11:00	BLLP	Blanking or Low-Power Interval T_{BLLP} = BLLP * T_{phy_clk} / lane_num	RW	0x0

Note: This register specifies timing parameters of the BLLP for burst mode.
The timing settings do not include Packet Header and Packet Foot. Software must consider PH and PF in order to satisfy the accurate Peripheral timing requirement.

3.4.3.7 DSI_RGBVT0

DSI RGB Vsync Timing0 Register

Offset=0x18

Bits	Name	Description	Access	Reset
31:28	-	Reserved	-	-
27:24	VFL	DSI_Vsync (to DE) Falling-edge to Active Line Distance 0x0: Reserved; 0x1: 1 lines; 0x2: 2lines; 0x3: 3 lines; …… 0xc: 12 lines; 0xd: 13 lines; 0xe: 14 lines; 0xf: 15 lines	RW	0x0

23:20	PLS	DSI Preline Number Set (to DE) 0x0: 1 line; 0x1: 2 lines; … 0xE: 15 lines; 0xF: 16 lines	RW	0x0
19:13	VSA	Vertical Sync Active Width (in lines) T_{vsa} = VSA * T_{line}	RW	0x0
12:00	LTOTAL	Total Line in one frame (in lines) T_{ltotal} = LTOTAL * T_{line} Note: 1 field /1frame of Progressive; 2 fields/1 frame of Interlaced.	RW	0x0

Note: This register specifies timing parameters of the vertical sync signal.

3.4.3.8 DSI_RGBVT1

DSI RGB Vsync Timing1 Register

Offset=0x1C

Bits	Name	Description	Access	Reset
31:29	-	Reserved	-	-
28:16	LSEF	Active Line Start Position in Even field of Interlaced scan	RW	0x0
15:12	-	Reserved	-	-
11:00	LSOF	Active Line Start Position in Progressive scan or Odd field of Interlaced scan	RW	0x0

Note: This register specifies timing parameters of the vertical sync signal.

3.4.3.9 DSI_TIMEOUT

DSI Time Out Register

Offset=0x20

Bits	Name	Description	Access	Reset
31:24	-	Reserved	-	-
23:00	BTA_TO	Time for BTA timeout Specify time out from Host initiate BTA request to bus grant turns over form DSI peripheral to DSI Host with respect to TX escape clock.	RW	0x0

Note: This register specifies the time of BTA time-out.

3.4.3.10 DSI_TR_STA

DSI Transfer State Register

Offset=0x24

Bits	Name	Description	Access	Reset
31	VBI	Vertical Blanking Interrupt Pending (Video Mode)	RW	0x0

		Asserted during vertical no-display period every frame. Interrupt triggered at the beginning of blanking period. Write 1 to clear.		
30:20	-	Reserved	-	-
19	TCIP	Transfer Complete Interrupt Pending Bit (CMD Mode) 0: Transfer is not Complete 1: Transfer is Complete Write 1 to clear the bit Note : After a command mode transfer or a trigger transfer finish, the bit is set to 1	RW	0x0
18	BUS_TURN OVER	Indicates when Bus grant turns over from DSI Peripheral to DSI Host 0: Bus Turn over not finish 1: Bus grant turns over from DSI Peripheral to DSI Host Write 1 to clear the bit	RW	0x0
17	RX_DAT_DO NE	Indicates when a LPDT packet (except for Ack and Error report packet) is received 0: no LPDT packet is received 1: a LPDT packet is received Write 1 to clear the bit	RW	0x0
16	RX_ACK_PA CK	Indicates when an Ack and Error report packet is received. 0: no Ack and Error report packet is received 1: an Ack and Error report packet is received Write 1 to clear the bit	RW	0x0
15	RX_TRIGGE R	Indicates when a RX Trigger is received. 0: no RX Trigger is received 1: a RX Trigger is received Write 1 to clear the bit	RW	0x0
14:11	-	Reserved	-	-
10	UDF	Output FIFO underflow pending bit Set when output fifo is empty, hardware still detects the write pointer of FIFO move. 0: no error occurred 1: error occurred Write 1 to clear the bit	RW	0x0
09	OVF	Input FIFO overflow pending bit Set when input fifo is full, hardware still detects the write pointer of FIFO move. 0: no error occurred 1: error occurred Write 1 to clear the bit	RW	0x0
08	IFIFO_EMP	Input FIFO Empty Flag 0: Not Empty	R	x

		1: Empty		
07	ERR_BTA_TO	BTA Time Out Error occur 0: no error occurred 1: a BTA Time Out Error occurred when initiate a BTA request Write 1 to clear the bit	RW	0x0
06	ERR_RX_CRC	Receive CRC Error Bit in LPDR 0: no error occurred 1: a CRC Error occurred when receiving long packet Write 1 to clear the bit	RW	0x0
05	ERR_RX_ECC	Receive ECC Error Bit in LPDR 0: no error occurred or a single-bit error occurs and corrected 1: multi-bit errors occur Write 1 to clear the bit	RW	0x0
04	ERR_ESC	Escape Mode Entry Error Pending Bit 0: no error occurred 1: an unrecognized escape entry command is received. Write 1 to clear the bit Note: an unknown Entry Command is received, the bit is also set to '1'.	RW	0x0
03	ERR_SYNC_ESC	Low-Power Data Transmission Synchronization Error 0: no error occurred 1: the number of bits received during a LPDT is not a multiple of eight when the transmission ends. Write 1 to clear the bit	RW	0x0
02	ERR_CONTROL	False Control Error 0: no error occurred 1: an incorrect line state sequence is detected. For example, if a BTA request or escape mode request is immediately followed by a Stop state instead of the required Bridge state. Write 1 to clear the bit	RW	0x0
01	ERR_CON_LP1	LP1 Contention Error 0: no error occurred 1.DP Line Contention Write 1 to clear the bit	RW	0x0
00	ERR_CON_LP0	LP0 Contention Error 0: no error occurred 1.DN Line Contention Write 1 to clear the bit	RW	0x0

Note: This register reflects the transfer status of the controller.

3.4.3.11 DSI_INT_EN

DSI Interrupt Enable Register

Offset=0x28

Bits	Name	Description	Access	Reset
31	VBI_EN	VBI interrupt pending enable 0: Disable; 1: Enable	RW	0x0
30:20	-	Reserved	-	-
19	TCIP_EN	TCIP interrupt pending enable 0: Disable; 1: Enable	RW	0x0
18	BUS_TURNOVER_EN	BUS_TURNOVER interrupt pending enable 0: Disable; 1: Enable	RW	0x0
17	RX_DAT_DONE_EN	RX_DAT_DONE interrupt pending enable 0: Disable; 1: Enable	RW	0x0
16	RX_ACK_PACK_EN	RX_ACK_PACK interrupt pending enable 0: Disable; 1: Enable	RW	0x0
15	RX_TRIGGER_EN	RX_TRIGGER interrupt pending enable 0: Disable; 1: Enable	RW	0x0
14:11	-	Reserved	-	-
10	UDF_EN	UDF interrupt pending enable 0: Disable; 1: Enable	RW	0x0
09	OVF_EN	OVF interrupt pending enable 0: Disable; 1: Enable	RW	0x0
08	-	Reserved	-	-
07	ERR_BTA_TO_EN	ERR_BTA_TO interrupt pending enable 0: Disable; 1: Enable	RW	0x0
06	ERR_RX_CRC_EN	ERR_RX_CRC interrupt pending enable 0: Disable; 1: Enable	RW	0x0
05	ERR_RX_ECC_EN	ERR_RX_ECC interrupt pending enable 0: Disable; 1: Enable	RW	0x0
04	ERR_ESC_EN	ERR_ESC interrupt pending enable 0: Disable; 1: Enable	RW	0x0
03	ERR_SYNC_ESC_EN	ERR_SYNC_ESC interrupt pending enable 0: Disable; 1: Enable	RW	0x0
02	ERR_CONTROL_EN	ERR_CONTROL interrupt pending enable 0: Disable; 1: Enable	RW	0x0
01	ERR_CON_LP1_EN	ERR_CON_LP1 interrupt pending enable 0: Disable; 1: Enable	RW	0x0
00	ERR_CON_LP0_EN	ERR_CON_LP0 interrupt pending enable 0: Disable; 1: Enable	RW	0x0

Note: This register enable or mask the interrupt sources.

3.4.3.12 DSI_ERROR_REPORT

DSI Error Report Register

Offset=0x2C

Bits	Name	Description	Access	Reset
31:16	-	Reserved	-	-
15:00	REPORT	Error Reporting Bit (Detailed description see MIPI DSI Spec 1.0) Before a new transfer is started, software must clear the bits to 0x0000	RW	0x0

Note: This register stores the Error Reporting Packet received from the peripherals.

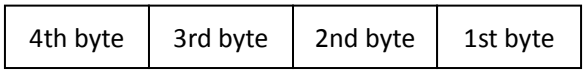
3.4.3.13 DSI_FIFO_ODAT

DSI FIFO Output Data Register

Offset=0x30

Bits	Name	Description	Access	Reset
31:00	DATA	FIFO DATA for Output	RW	0x0

Note: The byte sequence is arranged in little-endian format. The right side (LSB) of the word is sent first. The data stored in LCD is word-aligned, so DSI Host Controller must discard several bytes if the word counter of sending data is not word-aligned.



MSB LSB

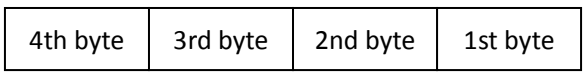
3.4.3.14 DSI_FIFO_IDAT

DSI FIFO Input Data Register

Offset=0x34

Bits	Name	Description	Access	Reset
31:00	DATA	FIFO DATA for Input	RW	0x0

Note: The byte sequence is arranged in little-endian format. That is the first byte received is on the right side (LSB) of the word. When the last bytes received cannot compose a word, the bytes should be placed on the right side (LSB) of the word. And FIFO's other bytes must be filled with 0xFF in order to satisfy the word- aligned rule.



MSB LSB

3.4.3.15 DSI_IPACK

DSI Input Packet Information Register

Offset=0x38

Bits	Name	Description	Access	Reset
31:25	-	Reserved	-	-
24	IPACK_TYPE	Input Packet Type: 0x0: Short Packet; 0x1: Long Packet	R	0x0
23:16	IPACK_DI	Input Packet Data Identifier	R	0x0
15:0	IPACK_WC	Input Packet Word Count	R	0x0

3.4.3.16 DSI_PACK_CFG

DSI Packet Configure Register (used in command mode)

Offset=0x40

Bits	Name	Description	Access	Reset
31:20	-	Reserved	-	-
19:18	PT	Packet Type 00: Short Packet without reading back data 01: Long Packet (Normal Data From FIFO) 10: Long Packet (Pixel Data From DE) Others: Reserved Note: When PT set to 10, Pixel Data must be sent in a packet per line.	RW	0x0
17	-	Reserved	-	-
16	CRC_CK_EN	CRC Check Enable 0: Disable 1: Enable when receiving data	RW	0x0
15	-	Reserved	-	-
14	TR_MODE	Transmission Mode Select 0: High-Speed 1: Low-Power Note: High-Speed is preferred. If fetch data from DE, High-Speed mode is only allowed.	RW	0x0
13:08	DT	Data Type	RW	0x0
07	-	Reserved	-	-
06:04	PTBM	Pixel To Byte Mapping 001: Eight bits per pixel format 010: Twelve bits per pixel format 011: Sixteen bits per pixel format 100: Eighteen bits per pixel format 101: Twenty-four bits per pixel format Others : Reserved	RW	0x3

03:02	-	Reserved	-	-
01	CCM	Command Continuous Mode (only in Pixel data from DE)	RW	0x0
00	ST	Write “1” to start Packet transmission, auto return to “0” by hardware.	RW	0x0

Note: When starting a short packet transmission, the data to be transmitted is from DSI_Pack_Header register. When starting a long packet transmission, the data to be transmitted is from DMA or from DE.

When in CMD Mode, only one packet per transmission is support.

When reading back data (Use LPDT), the host controller shall judge what type of packet the current transferring packet is. If the read-back packet is Acknowledge and Error Report, store the read-back data in ERR_REP (error report) register. If the read-back packet is other type, store the data in DSI_FIFO_DAT.

3.4.3.17 DSI_PACK_HEADER

DSI Packet Header Register

Offset=0x44

Bits	Name	Description	Access	Reset
31:16	Null_Packet_PH	The Null Packet Header of Transmit packet. Note: active when Null_Packet_PH>0 and transmit after RGB Packet. [7:0] = Data0 (Word Count lower byte for long packet) [15:8] = Data1 (Word Count upper byte for long packet)	RW	0x0
15:00	PH	The Packet Header of Transmit packet. [7:0] = Data0 (Word Count lower byte for long packet) [15:8] = Data1 (Word Count upper byte for long packet)	RW	0x0

Note: This register defines the packet header to DSI packets.

When transmission long packet, this register should be set earlier than starting DMA transmission.

3.4.3.18 DSI_TX_TRIGGER

DSI TX Trigger Register

Offset=0x48

Bits	Name	Description	Access	Reset
31:16	-	Reserved	-	-
15:08	TRIGGER	Entry Command Pattern	RW	0x0
07:01	-	Reserved	-	-

00	ST	Start a trigger transmit 0: do not operate 1: Start a trigger	RW	0x0

Note: This register is used to send trigger.

3.4.3.19 DSI_RX_TRIGGER

DSI RX Trigger Register

Offset=0x4C

Bits	Name	Description	Access	Reset
31:08	-	Reserved	-	-
07:00	TRIGGER	Entry Command Pattern	RW	0x0

Note: This register stored the received trigger.

Only when a new trigger is received, the register is update. CPU can also write value to the register.

3.4.3.20 DSI_LANE_CTRL

DSI Lane Control Register

Offset=0x50

Bits	Name	Description	Access	Reset
31:07	-	Reserved	-	-
06	CLK_ULPS	Force Clock Lane Module to enter the Ultra-Low Power State. 0: No force; 1: Force Note : the bit is auto-cleared after 1 byte_clk.	RW	0x0
05	CLK_ULPS_EXIT	Force Clock Lane Module to exit the Ultra-Low Power State. 0: No force; 1: Force Note : the bit is auto-cleared after 1 byte_clk.	RW	0x0
04	CLK_TXSTOP	Force Clock Lane Module into Transmit mode / (Generate Stop State) 0: No force; 1: Force Note : the bit is auto-cleared after 1 byte_clk.	RW	0x0
03	DL_ULPS	Force DATA Lane Module to enter the Ultra-Low Power State. 0: No force; 1: Force Note : the bit is auto-cleared after 1 byte_clk.	RW	0x0
02	DL_ULPS_EXIT	Force DATA Lane Module to exit the Ultra-Low Power State. 0: No force; 1: Force Note : the bit is auto-cleared after 1 byte_clk.	RW	0x0
01	DL_TXSTOP	Force DATA Lane Module into Transmit mode / (Generate Stop State)	RW	0x0

		0: No force; 1: Force Note: the bit is auto-cleared after 1 byte_clk. Whether D-PHY is in TX state or RX state, force TX state to STOP-State and direction go to 0.		
00	DL0_BTA	Force Data Lane 0 Module Bus Turn Around (Only for Data Lane 0) 0: No force; 1: Force Note : the bit is auto-cleared after 1 byte_clk.	RW	0x0

Note: This register is mainly used to control the lane state.

The setting for Data Lane Control is useful for both Data Lane 0 and Data Lane 1, except for DL_RXMODE and DL_BTA. The setting of DL_RXMODE and DL_BTA is useful only for Data Lane 0.

3.4.3.21 DSI_LANE_STA

DSI Lane State Register

Offset=0x54

Bits	Name	Description	Access	Reset
31:16	-	Reserved	-	-
15:12	DL_ST	Data Lane is in Stop State 0: Data Lane is not in Stop State 1: Data Lane is in Stop State Note : Bit 15 for Data Lane 3, Bit 14 for Data Lane 2, Bit 13 for Data Lane 1, Bit 12 for Data Lane 0	R	x
11:08	DL_ULPS	Data Lane is in Ultra-Low Power State 0: Data Lane is not in Ultra-Low Power State 1: Data Lane is in Ultra-Low Power State Note : Bit 11 for Data Lane 3, Bit 10 for Data Lane 2, Bit 9 for Data Lane 1, Bit 8 for Data Lane 0	R	x
07:06	-	Reserved	-	-
05	CLK_ST	Clk Lane is in Stop State 0: Clock Lane is not in Stop State 1: Clock Lane is in Stop State	R	x
04	CLK_ULPS	Clk Lane is in Ultra-Low Power State 0: Clock Lane is not in Ultra-Low Power State 1: Clock Lane is in Ultra-Low Power State	R	x
03:01	-	Reserved	-	-
00	DIR	Transmit/Receive Direction (Data Lane 0 Only) 0: The Lane is in transmitting mode. 1: The Lane is in receiving mode.	R	x

Note: This register reflects the status of the lane module.

3.4.3.22 DSI_PHY_T0

DSI PHY Operation Timing0 – For Clock Lane

Offset=0x60

Bit (s)	Name	Description	Access	Reset
31:14	-	Reserved	-	-
13:11	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst. 000: 2 * Phy_Clk 001: 4 * Phy_Clk 010: 6 * Phy_Clk 011: 8 * Phy_Clk 100: 12 * Phy_Clk 101: 16 * Phy_Clk 110-111: Reserve	RW	0x3
10:08	$T_{CLK-POST}$	Timing that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode. 000: 8 * Phy_Clk 001: 12 * Phy_Clk 010: 16 * Phy_Clk 011: 20 * Phy_Clk 100: 24 * Phy_Clk 101: 28 * Phy_Clk 110: 32 * Phy_Clk 111: 36 * Phy_Clk	RW	0x3
07:06	$T_{CLK-PRE}$	Timing that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode. 00: 1 * Phy_Clk 01: 2 * Phy_Clk 10: 3 * Phy_Clk 11: 4 * Phy_Clk	RW	0x2
05:03	$T_{CLK-ZERO}$	Time for lead HS-0 drive period before starting Clock. 000: 2 * Phy_Clk 001: 4 * Phy_Clk 010: 8 * Phy_Clk 011: 16 * Phy_Clk 100: 32 * Phy_Clk 101: 64 * Phy_Clk 110: 96 * Phy_Clk 111: 128 * Phy_Clk	RW	0x3
02:00	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission 000: 1 * Phy_Clk	RW	0x3

		001: 2 * Phy_Clk 010: 4 * Phy_Clk 011: 8 * Phy_Clk 100: 12 * Phy_Clk 101: 16 * Phy_Clk 110-111: Reserve		

3.4.3.23 DSI_PHY_T1

D-PHY TX Operation Timing1 – For Data Lane

Offset=0x64

Bit (s)	Name	Description	Access	Reset
31:14	-	Reserved	-	-
13:11	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst. 000: 2 * Phy_Clk 001: 4 * Phy_Clk 010: 8 * Phy_Clk 011: 16 * Phy_Clk 100: 24 * Phy_Clk 101: 32 * Phy_Clk 110: 48 * Phy_Clk 111: 64 * Phy_Clk	RW	0x3
10:08	$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst. 000: 2 * Phy_Clk 001: 4 * Phy_Clk 010: 6 * Phy_Clk 011: 8 * Phy_Clk 100: 12 * Phy_Clk 101: 16 * Phy_Clk 110-111: Reserve	RW	0x3
07:06	-	Reserved	-	-
05:03	$T_{HS-ZERO}$	Time to drive HS-0 before the Sync sequence 000: 2 * Phy_Clk 001: 4 * Phy_Clk 010: 8 * Phy_Clk 011: 16 * Phy_Clk 100: 24 * Phy_Clk 101: 32 * Phy_Clk 110: 48 * Phy_Clk 111: 64 * Phy_Clk	RW	0x3
02:00	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission 000: 1 * Phy_Clk 001: 2 * Phy_Clk	RW	0x3

		010: 4 * Phy_Clk 011: 8 * Phy_Clk 100: 12 * Phy_Clk 101: 16 * Phy_Clk 110-111: Reserve		

3.4.3.24 DSI_PHY_T2

D-PHY TX Operation Timing2 – For LPClk

Offset=0x68

Bit (s)	Name	Description	Access	Reset
31:24	-	Reserved	-	-
23:16	INIT	Time for initial from PHY CAL Done T_{INIT} = (INIT * 256+1) * T_{LPX} Note: The minimum requirement of T_{INT} is 100us, normally sets to 400us – 500us.	RW	0x10
15:08	WAKEUP	Time for wake up from ULPS. (Data Lane & Clock Lane) T_{WAKEUP} = (WAKEUP * 256 +1) * T_{LPX}	RW	0x3
07	TA_SURE	Time-out before new TX side starts driving $T_{TA-SURE}$ = (TA_SURE + 1) * T_{LPX}	RW	0x0
06:00	PRE_SCALAR	Low-Power Clock pre-scalar value T_{LPX} = (PRE_SCALAR + 1) * T_{Phy_Clk} $T_{LP\ CLK}$ = 2 * T_{LPX}	RW	0xf

3.4.3.25 DSI_LANE_SWAP

DSI LANE SWAP Control Register

Offset=0x7C

Bit (s)	Name	Description	Access	Reset
31:12	-	Reserved	-	-
11:9	DLane3_MAP	MIPI DSI Lane 3 Mapping: 0x0: Data 0 (both direction) ; 0x1: Data 1 (normally using tx direction) ; 0x2: Data 2 (normally using tx direction) ; 0x3: Data 3 (normally using tx direction) ; Others: Reserved	RW	0x3
8:6	DLane2_MAP	MIPI DSI Lane 2 Mapping: 0x0: Data 0 (both direction) ; 0x1: Data 1 (normally using tx direction) ; 0x2: Data 2 (normally using tx direction) ; 0x3: Data 3 (normally using tx direction) ; Others: Reserved	RW	0x2

5:3	DLane1_MAP	MIPI DSI Lane 1 Mapping: 0x0: Data 0 (both direction) ; 0x1: Data 1 (normally using tx direction) ; 0x2: Data 2 (normally using tx direction) ; 0x3: Data 3 (normally using tx direction) ; Others: Reserved	RW	0x1
2:0	DLane0_MAP	MIPI DSI Lane 0 Mapping: 0x0: Data 0 (both direction) ; 0x1: Data 1 (normally using tx direction) ; 0x2: Data 2 (normally using tx direction) ; 0x3: Data 3 (normally using tx direction) ; Others: Reserved	RW	0x0

3.4.3.26 DSI_PHY_CTRL

DSI D-PHY Control Register

Offset=0x80

Bit (s)	Name	Description	Access	Reset
31	-	Reserved	-	-
30	CLK_LANE_EN	CLK LANE ENABLE signal 0: disable 1 enable	RW	0x0
29:26	DATA_LANE_EN	DATA LANE3,2,1,0 enable signal 0: disable 1:enable	RW	0x0
25:24	Output_swing	CLK LANE & ALL DATA LANE output differential swing in HS mode	RW	0x0
23:22	Output_slew	LANE & ALL DATA LANE output differential signal slew rate control in HS mode 00: slowest 11:fastest	RW	0x1
21:18	CLK_delay	CLK LANE match delay setting,the bigger ,the delay further	RW	0x3
17	CLK_LANE_SWAP	CLK LANE port SWAP control signal 0: normal 1:swap positive port with negedge port	RW	0x0
16:13	DATA_LANE_SWAP	DATA LANE3,2,1,0 port SWAP control signal 0: normal 1:swap positive port with negedge port	RW	0x0
12:9	LANE_ phase	DATA LANE3,2,1,0 edge select signal 0: positive edge 1: negedge edge	RW	0x0
8:7	LP_CD_time	DATA LANE LP cd debunce timing length select signal	RW	0x1

		00: the shortest 11:the longest		
6:3	LP_RX_EN	DATA LANE3,2,1,0 LPRX enable signal 0: disable 1: enable	RW	0x0
2:0	LP_Driver	DATA LANE LP TX driver setting.	RW	0x2

3.5 HDMI/MHL

3.5.1 Function

The High Definition Multimedia Interface (HDMI) Module consists of HDMI Video Interface, HDMI Audio Interface, and HDMI Transmitter Core. The HDMI Transmitter Core is a full-function, single-link transmitter with high-bandwidth digital content protection (HDCP), which transmits studio-quality video and/or audio to any HDMI/DVI/HDCP-enabled digital receivers. This module is fully compliant with the HDMI 1.4b (3D Feature), MHL 2.1 (3D Feature), DVI 1.0, and HDCP 1.4 specifications. Following is the main features:

- Compatible with HDMI 1.4b, MHL 2.1, HDCP1.4 and DVI 1.0
- Supports most video formats from 480p to 4kx2k, such as:
  - 640*480p@59.94/60Hz
  - 720*480p@59.94/60Hz
  - 720*576p@50Hz
  - 1280*720p@59.94/60Hz
  - 1280*720p@50Hz
  - 720 (1440) *480i@59.94/60Hz
  - 720 (1440) *576i@50Hz
  - 1440*480p@59.94/60Hz
  - 1440*576p@50Hz
  - 1920*1080i@59.94/60Hz
  - 1920*1080i@50Hz
  - 1920*1080p@24Hz
  - 1920*1080p@59.94/60Hz
  - 1920*1080p@50Hz
  - 4k*2k@30Hz
- Supports 24bit, 30bit, 36bit, 48bit RGB/YCbCr 4:4:4 format (Deep Color)
- Supports 24bit RGB and YCbCr4:4:4 format in MHL Mode
- Supports PackedPixel YCbCr4:2:2 format in MHL Mode
- Supports xvYCC601, xvYCC709 Enhanced Colorimetry format
- Supports IEC60958 audio format up to 24bits
- Supports High-bitrate compressed audio formats
- Supports up to 8-channel Audio sample, supports 48/96/192/384/44.2/88.4/176.8/353.6kHz audio sample rate
- Supports Auto-Lipsync Correction feature
- Supports 3D Frame Packing Structure with 1080p@24Hz, 720p@50Hz, 720p@59.94/60Hz, etc.
- Supports 3D Side-by-Side (Half) Structure with 1080i@59.94/60Hz, 1080i@50Hz, etc.
- Supports 3D Top-and-Bottom Structure with 1080p@24Hz, 720p@50Hz, 720p@59.94/60Hz, etc.

3.6 Audio IN/Out

3.6.1 Function

I2S and SPDIF interface are supported by S900 for audio IN/OUT. I2S is also known as Inter-IC Sound, it is and electrical serial bus interface for digital audio signals, used to communicate PCM audio data between IC and devices. SPDIF is a transmitter interface for digital audio devices, data transmitted is also PCM encoded audio signals. Features of Audio interface are listed below:

- Support I2S, SPDIF, HDMI transmit audio simultaneously.
- Support mix voice from I2S receiver with HDMI audio, SPDIF, I2S transmitter directly in digital domain for karaoke.

I2S:

- Supports 2.0-channel I2S transmitter and receiver
- Supports 7.1-channel and 5.1-channel through I2S transmitter with ext.8-channel and 6-channel DAC or with ATC260x, by TDM (time-division multiplexed) Mode.
- Supports 4-channel through I2S receiver with ATC260x, by TDM Mode for 4-channel record.
- Support stereo DMIC in ATC260x, and data received by I2S receiver of S900.
- I2S can only work as Master Mode.
- I2S supports sample rate 192k/96k/48k/32k/24k/16k/12k/8k/88.2k/44.1k/22.5k/11.025k
- I2S transmitter has 24bit*32level FIFO, and I2S receiver has 24bit*16level FIFO.

SPDIF:

- SPDIF supports transmitter mode only.
- SPDIF supports sample rate 96k/48k/44.1k/32k.

3.6.1.1 I2S Interface

I2S mode supports sample rate 192K/96K/88.2K/48K/44.1K/32K/24K/22.05K/16K/12K/11.025K/8KHz. I2S Module can work as I2S Receiver (I2S RX) and I2S Transmitter (I2S TX), only work as Master Mode. I2S TX Supports 5.1-channel and 7.1-channel with ext.6-channel/8-channel DAC by TDM Mode. It also supports 2.0-Channel Mode. Clock and Data are sent through 4 pins: BCLK, LRCLK, DOUT, and MCLK.

3.6.1.2 SPDIF Interface

S/PDIF is used to transmit digital signals of a number of formats, the most common being the 48 kHz sample rate format used in DAT and the 44.1 kHz format used in CD audio. Instead the data is sent using Biphase mark code, which has either one or two transitions for every bit, allowing the original sample clock to be extracted from the signal itself.

S/PDIF is used for transmitting 20 bit audio data streams plus other related information. To transmit sources with less than 20 bits of sample accuracy, the superfluous bits will be set to zero. S/PDIF can also transport 24 bit samples by way of four extra bits, but not all equipment supports this, and might ignore these extra bits.

3.6.2 Register List

Table 3 - 11 I2S_SPDIF Controller Registers Address

Name	Physical Base Address
I2S_SPDIF	0xE0100000

Table 3 - 12 I2S/SPDIF Controller Registers

Offset	Register Name	Description
0x0000	I2S_CTL	I2S Control Register
0x0004	I2S_FIFOCTL	I2S FIFO Control Register
0x0008	I2STX_DAT	I2S TX FIFO Data Register
0x000c	I2SRX_DAT	I2S RX FIFO Data Register
0x0010	SPDIF_HDMI_CTL	SPDIF and HDMI FIFO Control Register
0x0014	SPDIF_DAT	SPDIF FIFO Data Register
0x0018	SPDIF_CLSTAT	SPDIF TX Channel Low Statue Register
0x001c	SPDIF_CHSTAT	SPDIF TX Channel High Statue Register
0x0020	HDMI_DAT	HDMI FIFO Data Register
0x002c	I2STX_SPDIF_HDMI_CTL	I2S TX, SPDIF, HDMI FIFO Virtual Address Control Register
0x0030	I2STX_SPDIF_HDMI_DAT	I2S TX, SPDIF, HDMI FIFO Data Register

3.6.3 Register Description

3.6.3.1 I2S_CTL

I2S Control Register

Offset = 0x00

Bit (s)	Name	Description	Access	Reset
31:13	-	Reserved	-	-
12:11	I2SPM	I2S PINS MODE: 00: 3-wire 01: 4-wire 10: 6-wire 11: reserved	RW	0x0
10	I2SRCS	I2S RX Clock Select: 0: from I2S_CLK2 1: from I2S_CLK1 (used by I2S TX)	RW	0x0
9:8	I2SRXM	I2S RX MODE: 00: 2.0-Channel Mode 01: 4-Channel TDM Mode A 1x: 4-Channel TDM Mode B	RW	0x0

7	-	Reserved	-	-
6:4	I2STXM	I2S TX MODE: 000: 2.0-Channel Mode 001: 5.1-Channel TDM Mode A 010: 5.1-Channel TDM Mode B 011: 7.1-Channel TDM Mode A 1xx: 7.1-Channel TDM Mode B	RW	0x0
3	I2STTDMRF	I2S TX TDM Mode data sample edge: 0: BCLK rising edge sample 1: BCLK falling edge sample	RW	0x0
2	-	Reserved	-	-
1	I2SREN	I2S RX Enable. 0: Disable 1: Enable	RW	0x0
0	I2STEN	I2S TX Enable. 0: Disable 1: Enable	RW	0x0

3.6.3.2 I2S_FIFOCTL

I2S FIFO Control Register

Offset = 0x04

Bit	Name	Description	Access	Reset
31:21	-	Reserved	-	-
20:19	KMCMMI2ST	Karaoke Multi-Channel Mix Mode.（not valid in Stereo Mix Mode） I2S RX Data Mix to I2S TX Data : 00: mix to all channels 01: mix to FL,FR 10: mix to FL,FR,C 11: mix to C	RW	0x0
18	I2STFSS	I2S TX Fifo Source Select: 0: APB 1: I2STX_SPDIF_HDMI_DAT	RW	0x0
17	I2SRFEF	I2S RX FIFO Empty Flag. 0: Not Empty 1: Empty	R	0x1
16	-	Reserved	-	-
15	I2STXKA	I2S TX Data Mix With I2S RX Data for Karaoke: 0: Disable 1: Enable	RW	0x0
14:13	-	Reserved	-	-
12	I2SRFIP	I2S RX FIFO Full IRQ Pending Bit.	RW	0x0

		0: No IRQ 1: IRQ Writing 1 to the bit is clear it.		
11	I2SRFIEN	I2S RX FIFO Full IRQ Enable. 0: Disable 1: Enable	RW	0x0
10	I2SRFDEN	I2S RX FIFO Full DRQ Enable. 0: Disable 1: Enable	RW	0x0
9	I2SRFR	I2S RX FIFO Reset. 0: Reset FIFO 1: Enable FIFO	RW	0x0
8	I2STFFF	I2S TX FIFO Full Flag. 0: Not Full 1: Full	R	0x0
7:4	-	Reserved	-	-
3	I2STFIP	I2S TX FIFO Empty IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit is clear it.	RW	0x0
2	I2STFIEN	I2S TX FIFO Empty IRQ Enable. 0: Disable 1: Enable	RW	0x0
1	I2STFDEN	I2S TX FIFO Empty DRQ Enable. 0: Disable 1: Enable	RW	0x0
0	I2STFR	I2S TX FIFO Reset. It Controls Virtual Address Fifo and Actual Address Fifo. 0: Reset FIFO 1: Enable FIFO	RW	0x0

3.6.3.3 I2STX_DAT

I2S TX FIFO Data Register

Offset = 0x08

Bit	Name	Description	Access	Reset
31:8	I2STFDA	I2STX FIFO Data.	W	x
7:0	-	Reserved	-	-

3.6.3.4 I2SRX_DAT

I2S RX FIFO Data Register

Offset = 0x0c

Bit	Name	Description	Access	Reset
31:8	I2SRFDA	I2S RX FIFO Data.	R	x
7:0	-	Reserved	-	-

3.6.3.5 SPDIF_HDMI_CTL

SPDIF and HDMI Control Register

Offset = 0x010

Bit	Name	Description	Access	Reset
31:17	-	Reserved	-	-
16:15	KMCMMHDM	Karaoke Multi-Channel Mix Mode.（not valid in Stereo Mix Mode） I2S RX Data Mix to HDMI Data : 00: mix to all channels 01: mix to FL,FR 10: mix to FL,FR,C 11: mix to C	RW	0x0
14	HDMFSS	HDMI Fifo Source Select: 0: APB 1: I2STX_SPDIF_HDMI_DAT	RW	0x0
13	SPDFSS	SPDIF Fifo Source Select: 0: APB 1: I2STX_SPDIF_HDMI_DAT	RW	0x0
12	HDMKA	HDMI Data Mix With I2S RX Data for Karaoke: 0: Disable 1: Enable	RW	0x0
11	SPDKA	SPDIF Data Mix With I2S RX Data for Karaoke: 0: Disable 1: Enable	RW	0x0
10	SPDEN	SPDIF Enable. 0: Disable (will reset TX state machine) 1: Enable	RW	0x0
9	HDMFIEN	HDMI FIFO Empty IRQ Enable. 0: Disable 1: Enable	RW	0x0
8	HDMFDEN	HDMI FIFO Empty (16 level left) DRQ Enable. 0: Disable 1: Enable	RW	0x0
7	HDMFFF	HDMI FIFO FULL Flag. 0: Not Full 1: Full	R	0x0
6	HDMFIP	HDMI FIFO Empty IRQ Pending Bit. 0: No IRQ	RW	0x0

		1: IRQ Writing 1 to the bit is clear it.		
5	SPDFIEN	SPDIF FIFO Empty IRQ Enable. 0: Disable 1: Enable	RW	0x0
4	SPDFDEN	SPDIF FIFO Empty (16 level) DRQ Enable. 0: Disable 1: Enable	RW	0x0
3	SPDFFF	SPDIF FIFO FULL Flag. 0: Not Full 1: Full	R	0x0
2	SPDFIP	SPDIF FIFO Empty IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit is clear it.	RW	0x0
1	HDMFR	HDMI FIFO Reset. It Controls Virtual Address Fifo and Actual Address Fifo. 0: Reset FIFO 1: Enable FIFO	RW	0x0
0	SPDFR	SPDIF FIFO Reset. It Controls Virtual Address Fifo and Actual Address Fifo. 0: Reset FIFO 1: Enable FIFO	RW	0x0

3.6.3.6 SPDIF_DAT

SPDIF FIFO Data Register

Offset = 0x14

Bit	Name	Description	Access	Reset
31:8	SPDFDA	SPDIF FIFO Data.	W	x
7:0	-	Reserved	-	-

3.6.3.7 SPDIF_CLSTAT

SPDIF TX Channel Low Statue Register

Offset = 0x18

Bit	Name	Description	Access	Reset
31:0	SPDCLSTAT	SPDIF TX Channel Low Status. (Channel status bit31 to bit0.)	RW	x

3.6.3.8 SPDIF_CHSTAT

SPDIF TX Channel High Statue Register

Offset = 0x1c

Bit	Name	Description	Access	Reset
31:16	-	Reserved	-	-
15:0	SPDCHSTAT	SPDIF TX Channel High Status. (Channel status bit47 to bit32.)	RW	x

3.6.3.9 HDMI_DAT

HDMI FIFO Data Register

Offset = 0x20

Bit	Name	Description	Access	Reset
31:8	HDMFDA	HDMI FIFO Data.	W	x
7:0	-	Reserved	-	-

3.6.3.10 I2STX_SPDIF_HDMI_CTL

I2S TX, SPDIF, HDMI FIFO Virtual Address Control Register

Offset = 0x2c

Bit	Name	Description	Access	Reset
7:0	-	Reserved	-	-
1	VADEN	Virtual Address DRQ Enable: 0: disable 1: enable	RW	0x0
0	VASS	Virtual Address Source Select: 0: Reserved 1: from APB	RW	0x0

3.6.3.11 I2STX_SPDIF_HDMI_DAT

I2S TX, SPDIF, HDMI FIFO Data Register

Offset = 0x30

Bit	Name	Description	Access	Reset
31:8	ISHFDA	I2S TX, SPDIF, HDMI FIFO Data. When writing to this address, data will be sent to I2STFDA, SPDFDA and HDMFDA correspondingly if I2STF2ISHFDA, SPDF2ISHFDA ,HDMF2ISHFDA are enable.	W	x
7:0	-	Reserved	-	-

3.7 PCM

3.7.1 Features

Pulse Code Modulation (PCM) is the method of encoding an audio signal in digital format. Features of PCM are listed below.

- Include 2 PCM Modules, PCM0 and PCM1
- Include PCM TX and PCM RX, both can work as Master Mode or Slave Mode
- Linear PCM (13-16bit), u-Law (8bit), A-Law (8bit)
- PCM clock in Master Mode 2.048MHz, in Slave Mode up to 2.048MHz
- Long Frame Sync and Short Frame Sync

3.7.2 Register List

Table 3 - 13 PCMx Controller Registers Address

Name	Physical Base Address
PCM0	0xE0110000
PCM1	0xE0118000

Table 3 - 14 PCMx Controller Registers

Offset	Register Name	Description
0x0000	PCMx_CTL	PCM Control Register
0x0004	PCMx_STAT	PCM Status Register
0x0008	PCMx_RXDAT	PCM Receive FIFO Data Register
0x000C	PCMx_TXDAT	PCM Transmit FIFO Data Register

Note: x=0,1

3.7.3 Register Description

3.7.3.1 PCMx_CTL

PCMx Control Register

Offset = 0x00+x*0x8000, x=0,1

Bit (s)	Name	Description	Access	Reset
31:20	-	Reserved	-	-
19	EN	PCM Enable. 0: Disable 1: Enable	RW	0

18	SEN	Sign Extension Enable (only when 16bit slots are used) . 0: Select zeros padding or audio gain. 1: Select sign extension. When writing the bit is 0, the unused bits are audio gain for 13-bit linear sample and zeros padding for 8-bit compounded sample. When writing the bit is 1, the unused bits are both sign extension.	RW	0
17	SAMF	Sample Format 0: 8bit sample with 8 cycle slot duration 1: 8bit sample with 16 cycle slot duration	RW	0
16	IVEN	Inversion Enable. 0: Disable 1: Enable. When inversion enables, inversion is performed for A-Law even bit and for u-Law all bit.	RW	0
15	MS	PCM Master/Slave Select. 0: Master 1: Slave	RW	0
14	FRMS	PCM Frame Mode Select 0: Short Frame Sync Mode 1: Long Frame Sync Mode	RW	0
13	FINS	PCM FIFO Input Source Select. 0: Data from APB 1: Data from ADC The data will be send out through PCM_OUT pin	RW	0
12	LBEN	Loop Back Enable. Set this bit to enable a loop back mode that data coming on the input will be presented on the output. 0: Disable 1: Enable	RW	0
11:10	-	Reserved	-	-
9	LMFR	LSB or MSB First. 0: MSB first 1: LSB first when transmitting and receiving voice samples.	RW	0
8	SSOE	SYNC Suppress Output Enable. 0: Enable SYNC output 1: Disable SYNC output	RW	0

		when keeping PCM_CLK running when in master mode. Some CODEC utilize the mode to enter a low power mode.		
7	TXIE	PCM TX IRQ Enable. 0: Disable 1: Enable	RW	0
6	RXIE	PCM RX IRQ Enable. 0: Disable 1: Enable	RW	0
5	TXDE	PCM TX DRQ Enable 0: Disable 1: Enable	RW	0
4	RXDE	PCM RX DRQ Enable 0: Disable 1: Enable	RW	0
3	DATO	PCM Data Output Mode. 0: Normal Output 1: Forces PCM_OUT to output 0	RW	0
2:0	DATM	PCM Data Mode Select 000: u-Law (8bit) 001: A-Law (8bit) 010: linear PCM (13bit) 011: linear PCM (14bit) 100: linear PCM (15bit) 101: linear PCM (16bit)	RW	0

3.7.3.2 PCMx_STAT

PCMx Status Register

Offset = 0x04+x*0x8000, x=0,1

Bit (s)	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7	TFES	TX FIFO empty Status 1: empty 0: no empty	R	1
6	RFFS	RX FIFO full Status 0: no full 1: full	R	0
5	TFFU	TX FIFO Full. 1: Full 0: No Full	R	0
4	RFEM	RX FIFO Empty. 1: Empty 0: No Empty	R	1

3	TFEP	TX FIFO Error Pending Bit. 0: No Error 1: Error Writing 1 to the bit will clear it or reset FIFO clear it.	RW	0
2	RFEP	RX FIFO Error Pending Bit. 0: No Error 1: Error Writing 1 to the bit will clear it or reset FIFO clear it.	RW	0
1	TIP	TX IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit will clear the bit.	RW	1
0	RIP	RX IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit will clear it.	RW	0

3.7.3.3 PCMx_RXDAT

PCMx RX FIFO Data Register

Offset = 0x08+x*0x8000, x=0,1

Bit (s)	Name	Description	Access	Reset
31:16	-	Reserved	-	-
15:0	RXDAT	PCM RX FIFO Data. The depth of FIFO is 16bit x 16 levels.	R	x

3.7.3.4 PCMx_TXDAT

PCMx TX FIFO Data Register

Offset = 0x0c+x*0x8000, x=0,1

Bit (s)	Name	Description	Access	Reset
31:16	-	Reserved	-	-
15:0	TXDAT	PCM TX FIFO Data. The depth of FIFO is 16bit x 16 levels.	W	x

4 Memory Control

4.1 SDC (SD/MMC Controller)

4.1.1 Function

The general purpose of the SDC is to translate the host bus protocol to the SD bus protocol. The SDC is based on a state machine which has 11 transfer modes to select. Every mode has a certain consequence to follow and a certain state to be updated to the registers. This module is managing the data transfers between RAM and SD devices. The RAM may be the SRAM or the DDR. The SD devices maybe a SD card, MMC card, eMMC flash, or a SDIO device.

The SDIO interface is connecting the host bus protocol to the SD bus protocol and provide the following features :

- Support SD/HCSD/SDXC (SRD50 mode), miniSD, microSD, memory card, MMC/RSMMC/ MMCPLUS card, INAND, MOVINAND, eMMC 4.51 SPEC, SDIO card etc.
- Support 1 bit, 4bit, 8bit, bus mode.
- Clock max rate up to 200MHz. Support HS200 Single Data Rate eMMC @ 200 MHz - 1.8V I/O.
- Contain 512 Byte SRAM*2
- Read /Write CRC Status Hardware auto checked.
- Support Auto multi Block read/write mode.
- Support SDIO function.
- Support boot mode based on eMMC4.5 SPEC.
- Hardware timeout/delay function.
- Integrated Clock Delay Chain Technique to Regulate Card Interface Timing.
- Built-in pull up resistance for CMD/DAT lines.

4.1.2 Register List

Table 4 - 1 SDC Base Address

Name	Physical Base Address
SD0	0xE0330000
SD1	0xE0334000
SD2	0xE0338000
SD3	0xE033C000

Table 4 - 2 SDx Register List

Offset	Register Name	Description
0x0000	SDx_EN	SDC card enable register
0x0004	SDx_CTL	SDC control register

0x0008	SDx_STATE	SDC STATU register
0x000C	SDx_CMD	SDC command register
0x0010	SDx_ARG	SDC argument register
0x0014	SDx_RSPBUF0	SDC RSP Buffer0 (Bit31~0) register
0x0018	SDx_RSPBUF1	SDC RSP Buffer1 (Bit63~32) register
0x001C	SDx_RSPBUF2	SDC RSP Buffer2 (Bit95~64) register
0x0020	SDx_RSPBUF3	SDC RSP Buffer3 (Bit127~96) register
0x0024	SDx_RSPBUF4	SDC RSP Buffer4 (Bit135~128) register
0x0028	SDx_DAT	SDC DATA register
0x002C	SDx_BLK_SIZE	SDC block size register
0x0030	SDx_BLK_NUM	SDC block number register
0x0034	SDx_BUF_SIZE	SDC buffer size per ping-pong

4.1.3 Register Description

4.1.4 SDx_EN

SDCx Enable Register

Offset = 0x0000

Bits	Name	Description	Access	Reset
31	RANE	Randomize enable 1: enable rand0mize 0: disable randomize	RW	0x0
30	-	Reserved	-	-
29:24	RAN_SEED	Randomize seed The randomize function will has a initial seed as this five bits.	RW	0x00
23:13	-	Reserved	-	-
12	S18EN	Pad power and pull on level SEL bit 0:Enable default 3.3V signaling; 1:Enable1.8V signaling	RW	0x0
11	-	Reserved	-	-
10	RESE	Build-in Pull up resistance enable. When set ,CMD,DATAS will be pull up to VCC. The number of data lines will be pulled up is equal to SD DATA BUS WIDTH. 1: Eenable 0: Disable	RW	0x0
9	DAT1_S	SD MMC DAT1 pad select 0: DAT1 to pad SD0_D1A 1: DAT1 to pad SD0_D1B	RW	0x0

8	CLK_S	SD MMC CLK pad select 0: CLK to pad SD0_CLKA 1: CLK to pad SD0_CLKB	RW	0x0
7	EN	SD module Enable 1: Enable 0: Disable	RW	0x0
6:4	-	Reserved	-	-
3	SDIOEN	1: SDIO function enable; 0: SDIO function disabled;	RW	0x0
2	DDREN	When enabled, the SDC will send and receive data use the DDR mode. the CMD line has no effect whether this bit is set or not. 1:DDR mode enabled 0:DDR mode disabled	RW	0x0
1:0	DATAWID	SD Interface Data Width select 00b : 1 bit 01b: 4 bit 10b: 8 bit 11b: Reserved	RW	0x0

4.1.5 SDx_CTL

SDC control register

Offset = 0x0004

Bits	Name	Description	Access	Reset
31	TOUTEN	Enable hardware r/w time out function. 0: Disable Hardware Timeout. 1: Enable Hardware Timeout. The timeout period is configured by Data Timeout Counter	RW	0x0
30-24	TOUTCNT	Hardware Time out counter value: This counter determine the timeout time of SD card data output. (used in TM_mode3~7 and boot mode)	RW	0x00
23-20	RDELAY	Latch Input DATA delay Time select (when host controller latching data, delay the inside latching data clock to compensate signal transmission delay) : **value** / **delay (ns)** 0x00 / 0 0x01 / 0.4 0x02 / 0.8	RW	0x4

<table>
<tr><td></td><td></td><td><table>
<tr><td>0x03</td><td>1.2</td></tr>
<tr><td>0x04</td><td>1.6</td></tr>
<tr><td>0x05</td><td>2</td></tr>
<tr><td>0x06</td><td>2.4</td></tr>
<tr><td>0x07</td><td>2.8</td></tr>
<tr><td>0x08</td><td>3.2</td></tr>
<tr><td>0x09</td><td>3.6</td></tr>
<tr><td>0x0A</td><td>4.6</td></tr>
<tr><td>0x0B</td><td>5.6</td></tr>
<tr><td>0x0C</td><td>6.6</td></tr>
<tr><td>0x0D</td><td>7.6</td></tr>
<tr><td>0x0E</td><td>8.6</td></tr>
<tr><td>0x0F</td><td>13.6</td></tr>
</table></td><td></td><td></td></tr>
<tr><td>19-16</td><td>WDELAY</td><td>OUT DATA delay Time select (when host controller OUT put data, delay the inside output data clock to compensate signal transmission delay) :<table>
<tr><th>value</th><th>delay (ns)</th></tr>
<tr><td>0x00</td><td>0</td></tr>
<tr><td>0x01</td><td>0.4</td></tr>
<tr><td>0x02</td><td>0.8</td></tr>
<tr><td>0x03</td><td>1.2</td></tr>
<tr><td>0x04</td><td>1.6</td></tr>
<tr><td>0x05</td><td>2</td></tr>
<tr><td>0x06</td><td>2.4</td></tr>
<tr><td>0x07</td><td>2.8</td></tr>
<tr><td>0x08</td><td>3.2</td></tr>
<tr><td>0x09</td><td>3.6</td></tr>
<tr><td>0x0A</td><td>4.6</td></tr>
<tr><td>0x0B</td><td>5.6</td></tr>
<tr><td>0x0C</td><td>6.6</td></tr>
<tr><td>0x0D</td><td>7.6</td></tr>
<tr><td>0x0E</td><td>8.6</td></tr>
<tr><td>0x0F</td><td>13.6</td></tr>
</table></td><td>RW</td><td>0x4</td></tr>
<tr><td>15:14</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>13</td><td>CMDLEN</td><td>CMD LOW Enable
Enable CMD line drive low level by Software
1: Drive CMD line to low level
0: not drives CMD line to low.

NOTE:
The software can set this bit to 1 to drive CMD line to low level. After power up, the card can be maintained in boot mode if the CMD line is</td><td>RW</td><td>0x0</td></tr>
</table>

		always low level. So you can read boot data using mode 9 or mode 10.		
12	SCC	Sending continuous clock. 1: Enable 0: Disable, write 0 to this bit, stop continuance sending clock (should clear it after transfer start bit is set)	RW	0x0
11:8	TCN	Transfer clock number. The clock number is 16 times of this field value. ”0” means 256 clks. (used with TM_MODE8)	RW	0x0
7	TS	Transfer Start: 1: When write 1 by software to set this bit, SDC transfer starts according to The Transfer Mode, access mode, and other control field. It will automatically clear to 0 after transfer complete or any Err oroccurred. 0 : When write 0 by software to clear this bit. The controller needs a few CLKs to stop transfer and reset the state machine fully so the software must check the result after writing “0” to it. Note: Software can not start a new transfer until it comes to “0” actually..	RW	0x0
6	LBE	Data in mode the last block enable bit 0: Disable 1: Enable When set, at the end of the read last block, SDC will send more 8 clocks for the card to complete the operation.	RW	0x0
5	C7EN	Command CRC Check 1: Disable CRC7 checked 0: Enable CRC7 checked When set, this indicates don’t check CRC7	RW	0x0
4	-	Reserved	-	-
3:0	TM	Transfer Mode[3:0] Specifies the transfer mode when transfer start bit is set 0000: Transfer command without response 0001: Transfer command with 6 bytes response (not including Data transfer) 0010: Transfer command with 17 bytes response (not including Data transfer)	RW	0xF

		0011: Transfer command with 6 bytes response, and with busy (not including Data transfer) 0100: Transfer data in mode with command and response (include crc16 checked) 0101: Transfer data out mode with command and response (include CRC and busy checked) 0110: Transfer data in mode without command and response 0111: Transfer data out mode without command and respon (include CRC and busy checked) 1000: Transfer only clock (without any command, response, and data) 1001: BOOT mode ,Transfer data in mode with Command (hardware check data CRC16, do not check boot mode acknowledge.) 1010: BOOT mode ,Transfer data in mode with Command (hardware check data CRC16, check boot mode acknowledge) . 1011~1111: Reserved		

4.1.6 SDx_STATE

SDC STATU register

Offset = 0x0008

Bits	Name	Description	Access	Reset
31:19	-	Reserved	-	-
18	D1B_S	SD0_D1B Status: This bit reflects the level of the DAT1 Signal of SD/MMC cardB	R	0x1
17	SDIOB_P	SDIOB IRQ pending bit 1: One SDIOB interrupt has happened 0: No SDIOB interrupt happened. Write1 to this bit will clear it.	RW	0x0
16	SDIOB_EN	SDIOB IRQ enable 1: SDIOB IRQ enable (the interrupt trigger form SD0_D1B PIN) 0: SDIOA interrupt disable	RW	0x0
15	TOUTE	Time out error	R	0x0

		If set means a timeout error has happened. Next transfer started will clear it.		
14	BAEP	Boot mode acknowledge error When in TM_MODE9, (boot mode with hardware check acknowledge), if set means a acknowledge error or timeout has happened. Next transfer started will clear it.	R	0x0
13	-	Reserved	-	-
12	MEMRDY	Memory ready 1: memory ready for read or write 0: memory is not ready for read and write	R	0x0
11	CMDS	CMD Status: This bit reflects the level of the CMD Signal of SD/MMC card	R	0x1
10	D1A_S	SD0_D1A Status: This bit reflects the level of the DAT1 Signal of SD/MMC cardA	R	0x1
9	SDIOA_P	SDIOA IRQ pending bit 1: One SDIOA interrupt has happened 0: No SDIOA interrupt happened. Write1 to this bit will clear it.	RW	0x0
8	SDIOA_EN	SDIOA IRQ enable 1: SDIOA IRQ enable (the interrupt trigger form SD0_D1A PIN) 0: SDIOA interrupt disable	RW	0x0
7	DAT0S	DAT0 Status: This bit reflects the level of the DAT0 Signal of SD/MMC card	R	0x1
6	TEIE	Transfer end IRQ enable: When set, enable interrupt request.	RW	0x0
5	TEI	Transfer end IRQ pending. Write1 to this bit will clear it.	R	0x0
4	CLNR	Command Line No response (only for command with response)	R	0x0

		This bit is auto cleared when Transfer Start is set.		
3	CLC	Command Line transfer Complete: This bit is auto cleared when Transfer Start is set, and is set when command line transfer is complete.	R	0x0
2	WC16ER	CRC Write data Error: When set, this indicated a CRC write error detected over the data line. This bit is auto cleared when Transfer Start is set.	R	0x0
1	RC16ER	CRC Read data Error: When set, this indicated a CRC16 error detected over the received data. This bit is auto cleared when Transfer Start is set.	R	0x0
0	CRC7ER	CRC command response Error: When set, this indicated CRC7 error detected over the response. This bit is auto cleared when Transfer Start is set.	R	0x0

4.1.7 SDx_CMD

SDC send command register

Offset = 0x000C

Bits	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7:0	CMD	Command register. Fixed the bit7 is '0' The bit6 is '1'	RW	0x40

4.1.8 SDx_ARG

SD MMC 0 argument register

Offset = 0x0010

Bits	Name	Description	Access	Reset
31:0	ARG	Be written before SD_CMD	RW	0x00000000

4.1.9 SDx_RSPBUF0

SDC RSP Buffer0 (Bit31~0) register

Offset = 0x0014

Bits	Name	Description	Access	Reset
31:0	RSP0	Bit31~0	R	0x00000000

4.1.10SDx_RSPBUF1

SDC RSP Buffer1 (Bit63~32) register

Offset = 0x0018

Bits	Name	Description	Access	Reset
31:0	RSP1	Bit63~32	R	0x00000000

4.1.11SDx_RSPBUF2

SDC RSP Buffer2 (Bit95~64) register

Offset = 0x001C

Bits	Name	Description	Access	Reset
31:0	RSP2	Bit95~64	R	0x00000000

4.1.12SDx_RSPBUF3

SDC RSP Buffer3 (Bit127~96) register

Offset = 0x0020

Bits	Name	Description	Access	Reset
31:0	RSP3	Bit127~96	R	0x00000000

4.1.13SDx_RSPBUF4

SDC RSP Buffer4 (Bit135~128) register

Offset = 0x0024

Bits	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7:0	RSP4	Bit135~128	R	0x00

4.1.14SDx_DAT

SDC DATA register

Offset = 0x0028

Bits	Name	Description	Access	Reset
31:0	DATA	Data register	R	0xxxxxxxxx

4.1.15SDx_BLK_SIZE

SDC Block size

Offset = 0x002C

Bits	Name	Description	Access	Reset
31:11	-	Reserved	-	-
9:0	BS	Block Size[9:0]. This field determines a block size, that is how many bytes found a block. In SDR50 mode, only 512bytes/block can be set.	RW	0x000

4.1.16SDx_BLK_NUM

SDC Block number

Offset = 0x0030

Bits	Name	Description	Access	Reset
31:14	-	Reserved	-	-
13:0	BN	This field determines block number in one read or write operations. Default value is 1. “0” means no block will be transferred.	RW	0x001

4.1.17SDx_BUF_SIZE

SDC BUFFER SIZER PER PING-PONG

Offset = 0x0034

Bits	Name	Description	Access	Reset
31:10	-	Reserved	-	-
9:0	BUFS	This field determines BUFFER SIZE in one PING-PONG read or write operations. Default value is 0X200. “0” means no block will be transferred.	RW	0X200

5 Peripheral Interfaces

5.1 USB3

5.1.1 Function

- A DRD module, no support to OTG.
- Fully compliant with USB Specification 3.0 and 2.0
- USB Supper Speed (5Gb/s), High Speed (480Mb/s) and Full Speed (12Mb/s) supported in Device Mode
- USB Supper Speed, High Speed, Full Speed and Low Speed (1.5Mb/s) supported in Host Mode
- Support Control, Bulk, Isochronous and Interrupt Transfers
- Embedded USB high-speed Transceiver which complies with Interface UTMI+ (level3)
- Embedded USB Supper Speed Transceiver which complies with Interface PIPE3 (32 bits)
- Support DMA master interface
- Support 4 out endpoints and 4 In endpoints excluded control endpoints
- Support 3 USB ports (1 supper speed port and 3 high speed ports) for Host Use, and up to 31 devices supported
- External SRAM, ROM, MCU is supported
- External PHY is supported (optional)
- Support USB remote wake-up feature

5.2 USBH_HSIC

5.2.1 Function

- Complies with On-The-Go Supplement to the USB2.0 Specification Revision 1.0a.
- UTMI+ level2 Transceiver Macrocell Interface.
- HSIC Interface for an option.
- Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP) with USB20.
- Supports point-to-point communication with one low-speed, full-speed or high-speed device in Host mode (one series downstream HUB supported) .
- Supports full-speed or high-speed in peripheral mode.
- Supports 15 IN endpoints and 15 OUT endpoints besides Control endpoint0.
- Supports high-speed high-bandwidth Isochronous transfer and Interrupt transfer.
- Integrated 15KB single port RAM as IN, OUT endpoint buffer. Partially configurable endpoint buffer size, endpoint type with single, double, triple or quad buffering.
- Supports suspend, resume and power managements function.
- Support remote wakeup.

- An optional HSIC interface for USBH1 controller.
- One OTG function and the other working as either Device or Host
- 32 bit AHB bus interface to uP for debug use
- Master access to DDR with 32-bit UDMA bus

5.3 Ethernet MAC Controller

5.3.1 Function

The MAC Ethernet controller implements Carrier Sense Multiple Access with Collision Detection (CSMA/CD) algorithms defined by IEEE 802.3 for media access control over the 10Mbps and 100Mbps Ethernet

Communication with an external host is implemented via a set of Control and Status Registers and the DMA controller for external shared RAM memory. For data transfers the MAC AHB operates as a DMA master. It automatically fetches from transmit data buffers and stores received data buffers into external RAM with minimum CPU intervention.

- Supports 10/100Mbps data transfer rate
- Supports RMII/SMII interface
- Meets the IEEE 802.3 CSMA/CD standard
- Full or half duplex operation
- Flexible address filtering
- External RAM for storing MAC addresses
- Up to 16 physical addresses
- 512 bit hash table for multicast addresses
- 32 bit slave AHB interface
- Single interrupt line
- Interrupt mitigation control mechanism
- 32 bit data AHB bus interface
- Scatter/gather capabilities
- Configurable burst length
- Intelligent bus arbitration schemes
- Descriptor "ring" or "chain" structures
- Single descriptor points to up to two data buffers
- Automatic descriptor list polling
- Independent clocks for data and control paths
- Running/Suspended/Stopped modes
- Clock switching support
- Operates as internal configurable FIFOs
- Programmable transmit threshold levels
- Transmit FIFO "store and forward" functionality

5.4 SPI (Serial Peripheral Interface)

5.4.1 Function

SPI (Serial Peripheral Interface) is a four wire, master-slave, full-duplex serial communication protocol. S900 integrated 4 SPI modules, the 4 channels can be configured as either a master or slave device. Features of SPI interface are listed below.

- Support master mode and slave mode. The speed of master mode up to 60Mbps, and slaver up to 20Mbps.
- Support dual I/O write and read mode while use as master
- Support single data rate mode and double data rate (DDR mode) while use as master
- Support two wire mode, only use SCLK and MOSI signal
- Support IRQ and DMA mode to transmit data
- Support system program boot from SPI Nor-flash
- 4 SPI modules

5.4.2 Register List

Table 5 - 1 SPI Registers Block Base Address

Name	Physical Base Address
SPI0	0xE01D0000
SPI1	0xE01D4000
SPI2	0xE01D8000
SPI3	0xE01DC000

Table 5 - 2 SPI Registers Offset Address

Offset	Register Name	Description
0x0000	SPIx_CTL	SPI Control Register
0x0004	SPIx_CLKDIV	SPI Clock Divide Register
0x0008	SPIx_STAT	SPI Status Register
0x000C	SPIx_RXDAT	SPI Receive FIFO Data Register
0x0010	SPIx_TXDAT	SPI Transmit FIFO Data Register
0x0014	SPIx_TCNT	SPI Transmit counter for read only
0x0018	SPIx_SEED	SPI Randomizer seed
0x001C	SPIx_TXCR	SPI TX DMA counter Register
0x0020	SPIx_RXCR	SPI RX DMA counter Register

5.4.3 Register Description

5.4.3.1 SPIx_CTL

SPIx Control Register

Offset = 0x0000

Bits	Name	Description	Access	Reset
31:29	SDT	Sample delay time 000: No delay 001: Delay 1 HCLK cycle time 010: 2 HCLK cycle time 011: 3 HCLK cycle time 100: 4 HCLK cycle time 101: 5 HCLK cycle time 110~111: Reserved	RW	0
28	BM	Boot mode, read only. The function is set in SRAMi module. The default value is defined by the status of CE0S pin. 0: normal mode 1: boot mode, the SPI mode is set to MODE3 and the SPI_CLKDIV is set to 0x02 by hardware automatically. Only SPI0 support this function.	R	x
27	GM	GPS mode 0: normal mode 1:GPS mode When select GPS mode, 3 wires and don't care the SPI SS pin.	RW	0
26	CEB	Convert Endian bit 0: not convert Endian 0x76543210 ->0x76543210 1: convert Endian 16bit mode: 0x3210->0x1032 32-bit mode: 0x76543210 ->0x10325476 MSB or LSB first shift in or out	RW	0
25	-	Reserved	-	-
24	RANEN	Randomizer enable bit 0: normal (randomizer bypass) 1: randomizer enable Only SPI0 and SPI1 support this function.	RW	0
23:22	RDIC	RX DRQ/IRQ Control. 00: Set when at least one byte received in IRQ mode.	RW	0

		01: Set when 8 level received in IRQ/DRQ mode 10: Set when 16 level received in IRQ/DRQ mode 11: Set when 24 level received in IRQ/DRQ mode In DMA mode, DO not set 00, 01, because at least 8 level necessary.		
21:20	TDIC	TX DRQ/IRQ Control. 00: Set when TX FIFO is 1 level empty in IRQ mode. 01: Set when TX FIFO is 8 level empty in IRQ/DRQ mode. 10: Set when TX FIFO is 16 level empty in IRQ/DRQ mode. 11: Set when TX FIFO is 24 level empty in IRQ/DRQ mode. In DMA mode, DO not set 00, 01, because at least 8 level necessary.	RW	0
19	TWME	Two wire mode enable bit 0: Normal 4 wire mode 1: Two wire mode, use two pin, SPI_CLK and SPI_MOSI	RW	0
18	EN	Enable. 0: Disable 1: Enable	RW	0
17:16	RWC	RW control 00: Write and read 01: Write only 10: Read only 11: Reserved	RW	0
15	DTS	Read Start Control Write 1 to start Read clock while use DMA to read data, available only in master read only mode. When transfer is finished, this bit will be auto cleared	RW	0
14	SSATEN	SPI_SS active automatically enable when in mode 0 and mode 2 (CPHA=0), only use in standard mode, except dual and DDR mode. 0: Disable 1: Enable	RW	0
13:12	DM	Dual mode and Double data rate Dual mode: Two data wire to read or write Double data rate: DDR 00: Single data wire and single data rate read or write 01: Dual and single data rate mode 10: Single data wire and DDR mode 11: Dual and DDR mode	RW	0
11	-	Reserved	-	-
10	MS	Master/Slave Select. 0: Master 1: Slave	RW	0
9:8	DAWS	Data/Address Width. Select	RW	0

		00: 8 bit data and address, low 8 bit 01: 16 bit data and address, low 16bit 10: 32 bit data and address 11: Reserved		
7:6	CPOS	Clock Polarity Select. CPOL CPHA 00: Mode 0 01: Mode 1 10: Mode 2 11: Mode 3	RW	0x3
5	LMFS	LSB/MSB First Select. 0: Transmit and receive MSB first 1: Transmit and receive LSB first	RW	0
4	SSCO	SPI_SS Control Output (only for master mode) . 1: Output high 0: Output low.	RW	1
3	TIEN	TX IRQ Enable. 0: Disable 1: Enable	RW	0
2	RIEN	RX IRQ Enable. 0: Disable 1: Enable	RW	0
1	TDEN	TX DRQ Enable. 0: Disable 1: Enable	RW	0
0	RDEN	RX DRQ Enable. 0: Disable 1: Enable	RW	0

5.4.3.2 SPIx_CLKDIV

SPIx Clock Divide Control Register

Offset = 0x0004

Bits	Name	Description	Access	Reset
31:10	-	Reserved	-	-
9:0	CLKDIV	In master mode: SPICLK=HCLK/ (CLKDIV*2) While CLKDIV is set to 1, the divide is 2. The SPI clock rate up to 60MHz. In slave mode: Need not to set this register. Supporting SPI clock rate up to 20MHz. When use, this register cannot be set to 0	RW	0

5.4.3.3 SPIx_STAT

SPIx Status Register

Offset = 0x0008

Bits	Name	Description	Access	Reset
31:10	-	Reserved	-	-
9	TFEM	TX FIFO Empty. 1: Empty 0: Not Empty	R	1
8	RFFU	RX FIFO Full. 1: Full 0: Not Full	R	0
7	TFFU	TX FIFO Full. 1: Full 0: Not Full	R	0
6	RFEM	RX FIFO Empty. 1: Empty 0: Not Empty	R	1
5	TFER	TX FIFO Error. When overflow, the bit is set to 1. Write 1 to the bit will clear the bit and reset the FIFO.	RW	0
4	RFER	RX FIFO Error. When overflow, the bit is set to 1. Write 1 to the bit will clear the bit and reset the FIFO.	RW	0
3	BEB	Bus error bit. Write 1 to the bit will clear the bit 0: No error 1: Bus error	RW	0
2	TCOM	Transfer Complete Bit. DMA mode: This bit will be set to 1 when all the data sent out or receive over, that the SCK has not clock. CPU mode: This bit will be set to 1 when every byte data sent out or receive over, that the SCK has not clock. Write 1 will clear to zero	RW	0
1	TIP	TX IRQ Pending Bit. 0: No IRQ 1: IRQ Write 1 to the bit will clear it.	RW	0
0	PIP	RX IRQ Pending Bit. 0: No IRQ 1: IRQ Write 1 to this bit will clear it.	RW	0

5.4.3.4 SPIx_RXDAT

SPIx RXData Register

Offset = 0x000C

Bits	Name	Description	Access	Reset
31:0	RXDAT	Receive Data. The depth of RXFIFO is 32-bit×32 levels.	R	x

5.4.3.5 SPIx_TXDAT

SPIx TXData Register

Offset = 0x0010

Bits	Name	Description	Access	Reset
31:0	TXDAT	Transmit Data. The depth of RXFIFO is 32-bit×32 levels.	W	x

5.4.3.6 SPIx_TCNT

SPI transmit counter Register

Offset = 0x0014

Bits	Name	Description	Access	Reset
31:12	-	Reserved	-	-
11:0	TCNT	Transmit counter, use to count the clock that sent out to read data in master mode. In read only mode, must first set this counter to determine how much clocks need to send out. The units of the count depend on the data width set by SPI_CTL. For example, if SPI is set 8bit mode, then each byte count 1. If SPI is set 32-bit mode, then each word count 1. This counter only use in read only mode, include CPU and DMA receive	RW	0

5.4.3.7 SPIx_SEED

SPI Randomizer seed Register

Offset = 0x0018

Bits	Name	Description	Access	Reset
31:13	-	Reserved	-	-
12:0	RS	Randomizer seed	RW	0

5.4.3.8 SPIx_TXCR

SPI TX DMA counter Register

Offset = 0x001C

Bits	Name	Description	Access	Reset
31:16	-	Reserved	-	-
15:0	TDWC	TX DMA word counter, use to count data Sent by DMA	RW	0

5.4.3.9 SPIx_RXCR

SPI RX DMA counter Register

Offset = 0x0020

Bits	Name	Description	Access	Reset
31:16	-	Reserved	-	-
15:0	RDWC	RX DMA word counter, use to count data Received by DMA	RW	0

5.5 UART/IR

5.5.1 Function

UART (Universal Asynchronous Receiver/Transmitter) is usually an individual (or part of an) integrated circuit used for serial communications over a computer or peripheral device serial port. This module integrates 7 UART interface, the UART and IR module features are listed below:

UART:

- 5-8 Data Bits and LSB first in Transmit and Received
- 1-2 Stop Bits
- Even, Odd, or No Parity
- 32 levels Transmit FIFO and 32 levels Receive FIFO
- Capable of speeds up to 3Mbps to enable connections with Bluetooth and other peripherals
- Support IRQ and DMA mode to transmit data.
- Only UART2/3/4 support RTS/CTS Automatic Hardware Flow Control to reduce interrupts to host system
- Only UART0 support IRC (infrared remote control) Inputs

IRC:

- Support RC6/RC5/9012/NEC (8-bit) protocol.
- Need to connect an IR receiver when use.
- Support IR Paddle

5.5.2 Register List

Each UART is controlled by a register block.

Table 5 - 3 UART Registers Block Base Address

Name	Physical Base Address
UART0	0xE0120000
UART1	0xE0122000
UART2	0xE0124000
UART3	0xE0126000
UART4	0xE0128000
UART5	0xE012A000
UART6	0xE012C000
IRC	0xE0120050

Each register block contains the registers.

Table 5 - 4 UART Registers Offset Address

Offset	Register Name	Description
0x0000	UARTx_CTL	UART Control Register
0x0004	UARTx_RXDAT	UART Receive FIFO Data Register
0x0008	UARTx_TXDAT	UART Transmit FIFO Data Register
0x000C	UARTx_STAT	UART Status Register

Table 5 - 5 IRC Registers Offset Address

Offset	Register Name	Description
0x00	IR_CTL	Infrared remote control (IRC) interface control register
0x04	IR_STAT	IRC status register
0x08	IR_CC	IRC customer code register
0x0C	IR_KDC	IRC key data code register
0x10	IR_TCOUNTER	IR handle bit width counter
0x14	IR_RCC	The received customer code register, read only
0x18	IR_FILTER	Infrared remote control filter register

5.5.3 Register Description

5.5.3.1 UARTx_CTL

UART Control Register

Offset = 0x0000

Bits	Name	Description	Access	Reset
31:23	-	Reserved	-	-

22	DTCR	DMA TX counter reset Write 1 to this bit will reset UART TX internal DMA transmit counter. Auto clear to 0 while reset over.	RW	0
21	DRCR	DMA RX counter reset Write 1 to this bit will reset UART RX internal DMA transmit counter. Auto clear to 0 while reset over.	RW	0
20	LBEN	Loop Back Enable. Set this bit to enable a loop back mode that data coming on the input will be presented on the output. 0: Disable 1: Enable	RW	0
19	TXIE	UART TX IRQ Enable. 0: Disable 1: Enable	RW	0
18	RXIE	UART RX IRQ Enable. 0: Disable 1: Enable	RW	0
17	TXDE	UART TX DRQ Enable. 0: Disable 1: Enable	RW	0
16	RXDE	UART RX DRQ Enable. 0: Disable 1: Enable	RW	0
15	EN	UART Enable. When this bit is clear, the UART clock source is inhibited. This can be used to place the module in a low power standby state.	RW	0
14	TRFS	UART TX/RX FIFO Select TX/RX FIFO Level is reflected in bit[15] to bit[12] of UART_STAT Register. 0: RX FIFO 1: TX FIFO	RW	0
13	-	Reserved	-	-
12	AFE	Autoflow Enable Setting this bit enables automatic hardware flow control. Enabling this mode overrides software control of the signals. *Note:* *This function only used in UART2\UART3\UART4. UART0 and UART1\5\6 not support 4-wire function*	RW	0
11:7	-	Reserved	-	-

6:4	PRS	Parity Select. Bit 6: PEN, Parity enable Bit 5: STKP, Stick parity Bit 4: EPS, Even parity PEN STKP EPS Selected Parity 0 x x None 1 0 0 Odd 1 0 1 logic 1 1 1 0 Even 1 1 1 logic 0	RW	0
3	-	Reserved	-	-
2	STPS	STOP Select. If this bit is 0, 1 stop bit is generated in transmission. If this bit is 1, 2 stop bits are generated.	RW	0
1:0	DWLS	Data Width Length Select. 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits	RW	0

Note: FIFO threshold setting requirement:

2. *TXFIFO (32 layers in total) threshold:*
   a) *IRQ: 16 layers empty*
   b) *DRQ: Burst mode*
3. *RX FIFO (32 layers in total) threshold:*
   a) *IRQ: 16 layers received*
   b) *DRQ: single mode*

5.5.3.2 UARTx_RXDAT

UART Receive FIFO Data Register

Offset = 0x0004

Bits	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7:0	RXDAT	Received Data. The depth of FIFO is 8bit×32levels.	R	x

5.5.3.3 UARTx_TXDAT

UART Transmit FIFO Data Register

Offset = 0x0008

Bits	Name	Description	Access	Reset
31:8	-	Reserved	-	-

7:0	TXDAT	Received Data. The depth of FIFO is 8bit×32 levels	R	x

5.5.3.4 UARTx_STAT

UART Status Register

Offset = 0x000C

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17	UTBB	UART TX busy bit 0:not busy, TX FIFO is empty and all data be shift out 1:busy	R	0
16:11	TRFL	TX/RX FIFO Level. The field indicates the current RX and TX FIFO level.	R	0
10	TFES	TX FIFO empty Status 1: empty 0: no empty	R	1
9	RFFS	RX FIFO full Status 0: no full 1: full	R	0
8	RTSS	RTS Status. The bit reflects the status of the external RTS- pin.	R	x
7	CTSS	CTS Status. The bit reflects the status of the external CTS- pin.	R	x
6	TFFU	TX FIFO Full. 1: Full 0: No Full	R	0
5	RFEM	RX FIFO Empty. 1: Empty 0: No Empty	R	1
4	RXST	Receive Status. 0: receive OK 1: receive error. Writing 1 to the bit will clear the bit.	RW	0
3	TFER	TX FIFO Error. 0: No Error 1: Error Writing 1 to the bit will clear the bit and reset the TX FIFO.	RW	0
2	RXER	RX FIFO Error. 0: No Error 1: Error Writing 1 to the bit will clear the bit and reset the RX FIFO.	RW	0

1	TIP	TX IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit to clear the bit.	RW	0
0	RIP	RX IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit to clear it.	RW	0

5.5.3.5 IR_CTL

infrared remote control register

Offset = 0x00

Bits	Name	Description	Access	Reset
31:5	-	Reserved	-	-
4	IPE	IR Paddle enable 0:disable 1:enable When use IR Paddle, must set IRC enable bit; when this bit is set, other IRC mode is not valid.	RW	0
3	IRCE	IRC enable 0:disable 1:enable	RW	0
2	IIE	IRC IRQ enable 0:disable 1:enable	RW	0
1:0	ICMS	IRC coding mode select 00:9012 code 01:8bits NEC code 10:RC5 code 11:RC6 code	RW	0

5.5.3.6 IR_STAT

Infrared remote control register

Offset = 0x04

Bit (s)	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7	IRFE	IR Receive FIFO empty bit (only use in IR Paddle mode) 0: empty 1: not empty, generate IRQ	R	0
6	UCMP	User code don’t match pending bit. Write 1 to this bit will	RW	0

		clear it, or auto clear if receive the correct user code the next time. 0: user code match 1: user code don't match		
5	KDCM	Key data code don't match pending bit. Write 1 to this bit will clear it, or auto clear if receive the correct key data code the next time 0: key data code match 1: key data code don't match	RW	0
4	RCD	Repeated code detected, write 1 to this bit will clear it, otherwise don't change 0: no repeat code 1: detect repeat code	RW	0
3	-	Reserved	-	-
2	IIP	IRC IRQ pending bit, write 1 to this bit will clear it 0: no IRQ pending 1: IRQ pending The precondition of generating interrupt is all the received code is correct, including user code and key value, moreover, if the user code and key value is not correct, the repeat code reveived following this frame can't generate interrupt. In IR Paddle mode When FIFO is not empty, generate IRQ	RW	0
1	-	Reserved	-	-
0	IREP	IRC receive error pending 0: receive OK 1: receive error occurs if not match the protocol. Writing 1 to this bit will clear this bit, or auto clear if receive the correct user code and key data code the next time.	RW	0

5.5.3.7 IR_CC

Infrared remote control customer code register

Offset = 0x08

Bit (s)	Name	Description	Access	Reset
31:16	-	Reserved	-	-
15:0	ICCC	Infrared remote control customer code **In RC5 mode:** Bit[4:0] is the customer code **In 9012 and NEC mode:** Bit[15:0] is the customer code, **In RC6 mode:** Bit[7:0] is the customer code.	RW	0

		In Paddle mode: Reserved		

5.5.3.8 IR_KDC

Infrared remote control KEY data code register

Offset = 0x0C

Bit (s)	Name	Description	Access	Reset
31:20	-	Reserved	-	-
19:0	IKDC	IRC key data code **In RC5 mode:** Bit 5:0 is the Key data **In 9012 and NEC mode:** Bit 7:0 is the Key data; Bit 15:8 is the Key anti-data **In RC6 mode:** Bit 7:0 is the Key data; If key value is received, register will be updated, if repeat code is received, register won't be updated. **In IR Paddle mode:** key data code is 20bit x 8 level RX FIFO	R	0

5.5.3.9 IR_TCOUNTER

Infrared remote control KEY data code register

Offset = 0x10

Bit (s)	Name	Description	Access	Reset
15:14	-	Reserved	-	-
13:8	ILWC	IR Paddle Leader code width TL counter Determine the length of lead code width TL of infrared game paddle; Determine the number of 200kHz clock source cycles, each cycle is 5μs, 2 cycles (10μs) is a unit here, for example, to set T = 150μs, then 150/10 = 15 should be write here. Default value is 150μs.	RW	0x0F
7:6	-	Reserved	-	-
5:0	IBWC	IR Paddle bit width T counter Determine the length of key width T of infrared game paddle; Determine the number of 200kHz clock source	RW	0x15

		cycles, each cycle is 5μs, 2 cycles (10μs) is a unit here, for example, to set T = 210μs, then 210/10 = 21 should be write here.		

5.5.3.10 IR_RCC

Receive customer code register

Offset = 0x14

Bit (s)	Name	Description	Access	Reset
31:16	-	Reserved	-	-
15:0	ICCC	Received customer code **In RC5 mode:** Bit 4:0 is the customer code **In 9012 and NEC mode:** Bit 15:0 is the customer code, **In RC6 mode:** Bit 7:0 is the customer code, **In Paddle mode:** Reserved The received user code is used to display the received user code for customers' reference	R	0

5.5.3.11 IR_FILTER

Infrared remote control filter register

Offset = 0x18

Bit (s)	Name	Description	Access	Reset
31:9	-	Reserved	-	-
8	FC	IR Filter control bit 0: disable 1: enable	RW	0
7:6	-	Reserved	-	-
5:0	IFC	IR filter counter Determine the filtered pulse width; Determine the number of 200kHz clock source cycles, each cycle is 5μs, one cycle is a unit here, for example, to set T = 200μs, then 200/5 = 40 should be write here.	RW	0

5.6 TWI

5.6.1 Function

TWI (Two Wire Interface) is used to communicate across circuit-board distances. At the low end of the spectrum of communication options for "inside the box" communication is TWI. TWI provides support for communication with various slow, on-board peripheral devices that are accessed intermittently, while being extremely modest in its hardware resource needs. It is a simple, low-bandwidth, short-distance protocol. Most available TWI devices operate at speeds up to 400Kbit/s, with some venturing up into the low megahertz range. TWI is easy to use to link multiple devices together since it has a built-in addressing scheme.

- Both master and slave functions support
- Support standard mode (100kbps), fast-speed mode (400kpbs), High-Speed mode (3.4Mbps)
- Multi-master capability
- 10-bit address mode not support
- Internal Pull-Up Resistor (1.5kOhm) optional
- 6 TWI modules
- 8Bit * 128 TX FIFO and 8Bit * 128 RX FIFO

Pull-up resistors are required on both of the TWI signal lines as the TWI drivers are open drain Typically external 2.2kOhm resisters are used to pull the signals up to VCC if not select internal Pull-Up resistor in standard and fast mode.

5.6.2 Register List

Table 5 - 6 TWI Block Base Address

Name	Physical Base Address
TWI0	0xE0170000
TWI1	0xE0172000
TWI2	0xE0174000
TWI3	0xE0176000
TWI4	0xE0178000
TWI5	0xE017a000

Each register block contains the registers.

Table 5 - 7 TWI Block Configuration Registers List

Offset	Register Name	Description
0x0000	TWIx_CTL	TWI Control Register
0x0004	TWIx_CLKDIV	TWI Clock Divide Register
0x0008	TWIx_STAT	TWI Status Register
0x000C	TWIx_ADDR	TWI Address Register
0x0010	TWIx_TXDAT	TWI TX Data Register
0x0014	TWIx_RXDAT	TWI RX Data Register

0x0018	TWIx_CMD	TWI Command Register
0x001C	TWIx_FIFOCTL	TWI FIFO control Register
0x0020	TWIx_FIFOSTAT	TWI FIFO status Register
0x0024	TWIx_DATCNT	TWI Data transmit counter
0x0028	TWIx_RCNT	TWI Data transmit remain counter

5.6.3 Register Description

5.6.3.1 TWIx_CTL

TWI Control Register

Offset = 0x0000

Bits	Name	Description	Access	Reset
31:12	-	Reserved	-	-
11	CSE	current-source enable bit 0: normal operation 1: Reserved	RW	0
10	SHSM	Standard high speed mode 0: disable standard high speed mode 1: enable standard high speed mode	RW	0
9	FHSM	Force in High speed mode 0: not in High speed mode 1: Force to High speed mode (3.4MHz)	RW	0
8	AE	Arbitrate enable 0: disable 1: enable	RW	0
7	EN	Enable. When enable, reset the status machine to IDLE 0: Disable 1: Enable	RW	0
6	-	Reserved	-	-
5	IRQE	IRQ Enable. 0: Disable 1: Enable FIFO mode added: When the following conditions is satisfied, IRQ will generate: 1. When writing TX FIFO empty, counter doesn't count to 0, then IRQ generates; if the counter counts to 0, then IRQ generates after it is stopped. 2. When reading RX FIFO full. 3. Stop generated or received	RW	0

		4. Received local slave address as slave device 6. Received NACK (not neglected NACK)		
4	-	Reserved	-	-
3:2	GBCC	Generating Bus Control Condition (only for master mode) . 00: No effect 01: Generating START condition 10: Generating STOP condition 11: Generating Repeated START condition Write the slave address to the TWI_DAT register, select start or restart, and then the start or restart command follow by the slave address will occur on the bus.	RW	0
1	RB	Release Bus. Write 1 to this bit will release the bus.	RW	0
0	GRAS	Generate ACK or NACK Signal. When receive data 0: generate the ACK signal at 9th clock of SCL 1: generate the NACK signal at 9th clock of SCL	RW	0

5.6.3.2 TWIx_CLKDIV

TWI Clock Divide Control Register

Offset = 0x0004

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:16	CLKCOMP	Clk counter compensation 00: no compensation 01: 10ns 10: 20ns 11: 30ns *Note: if the clock rising time too slow results in that the pin speed slower than configuration, this bit can be used to compensate.*	RW	0
15:8	HDIV	High speed mode Clock Divider Factor (only for the master mode) . Calculating SCL is as following: SCL=100M/ (CLKDIV*6)	RW	0
7:0	CLKDIV	Clock Divider Factor (only for master mode) . TWI clock (SCL) can select standard (100kbps) mode and fast (400kbps) mode. Calculating SCL is as following: SCL=100M/ (CLKDIV*16)	RW	0

5.6.3.3 TWIx_STAT

TWI Status Register

Offset = 0x0008

Bits	Name	Description	Access	Reset
31:11	-	Reserved	R	0
10	SRGC	Slave receive general call 0: not receive a general call 1: receive a general call	R	0
9	SAMB	Slave address match bit 0: slave address not match 1: slave address match	R	0
8	LBST	Last Byte Status Bit. 0: Indicate the last byte received or transmitted is address 1: Indicate the last byte received or transmitted is data	R	0
7	TCB	Transfer complete bit 0: not finish transfer 1: In normal mode: A byte transfer finish, include transfer the ACK or NACK bit Writing 1 to this bit will clear it.	RW	0
6	BBB	Bus busy bit 0: Not busy 1: Busy This bit will set to 1 while the start command detected, and set to 0 after the stop command	R	0
5	STAD	Start detect bit, include restart. The bit is clear when the TWI module is disable or when the STOP condition is detected. Writing 1 to the bit will clear it. 0: Start bit is not detected 1: Start bit is detected	RW	0
4	STPD	Stop detect bit The bit is clear when the TWI module is disable or when the START condition is detected. Writing 1 to the bit will clear it. 0: Stop bit is not detected 1: Stop bit is detected	RW	0
3	LAB	Lose arbitration bit 0: not lose 1: lose arbitration	RW	0

		Write 1 clear it The bit is clear when the TWI module is disable will clear it.		
2	IRQP	IRQ Pending Bit. 1: IRQ 0: No IRQ Set condition: 1. transfer complete 2. detect normal stop bit (no bus error) 3. arbit fail Clear condition: Writing 1 to this bit will clear it.	RW	0
1	BEB	Bus error bit 0: No error occur 1: Bus error occur Write “1” to clear this bit The below conditions occur generate error bit: Detect stop bit right after detect start/restart bit. Detect stop, start bit when sending or receiving data.	RW	0
0	RACK	Receive ACK or NACK when transmit data or address 0: NACK 1: ACK The bit will be updated when the 9th of next byte clock arrived	R	0

5.6.3.4 TWIx_ADDR

TWI Address Register

Offset = 0x000C

Bits	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7:1	SDAD	Own Slave Device Address. Only use in slave mode. TWI_ADDR contains the own address of the module when the device is use in slave mode. Content of the register is irrelevant when the TWI module is functioning as a master.	RW	0
0	-	Reserved	-	-

5.6.3.5 TWIx_TXDAT

TWI Data Register

Offset = 0x0010

Bits	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7:0	DA	The register of Data or address to be transferred or received to. TWIDAT contains the byte to be transmitted on the TWI-bus or a byte that has been received from the TWI-bus. In master mode, along with the data byte to be transmitted, it also includes the slave address. The seven MSB's are the slave TWI device address while the LSB is the Read/Write bit. 128 layer FIFO, 8*128.	RW	0

5.6.3.6 TWIx_RXDAT

TWI Data Register

Offset = 0x0014

Bits	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7:0	DA	The Receive data Register 128 layer FIFO, 8*128.	RW	0

5.6.3.7 TWIx_CMD

TWI Data Register

Offset = 0x0018

Bits	Name	Description	Access	Reset
31:16	-	Reserved	-	-
15	SECL	Start to execute the command list 0: not execute 1: execute command If this bit is not enabled, then FIFO cannot be used, but the original non-FIFO in TWI module can be used.	RW	0
14:13	-	Reserved	-	-
12	WRS	Write or Read select 0: write 1: read This bit only used in Slave mode.	RW	0

		When used as master device, write or read flag can be identified by the bit[0] following the start bit.		
11	MSS	Master or slave mode select 0: slave mode 1: Master mode	RW	0
10	SE	Stop enable 0: disable 1: enable	RW	0
9	NS	NACK select 0: not select 1: select generate the NACK signal at 9th clock of SCL of the last byte when read data	RW	0
8	DE	Data enable 0: disable 1: enable The counts of data transmitted depend on the TWIx_CNT register.	RW	0
7:5	SAS	Second address select 000: no address 001: 1 byte address 010: 2 byte address 011: 3 byte address 100: 4 byte address 101: 5 byte address 110: 6 byte address 111: 7 byte address The address domain following the Restart command.	RW	0
4	RBE	Restart bit enable 0: not send restart bit 1: send restart bit	RW	0
3:1	AS	Address select 000: no address 001: 1 byte address 010: 2 byte address 011: 3 byte address 100: 4 byte address 101: 5 byte address 110: 6 byte address 111: 7 byte address The address includes slave address and slave internal memory address.	RW	0

		The address domain following the Start command.		
0	SBE	Start bit enable 0: not send start bit 1: send start bit	RW	0

5.6.3.8 TWIx_FIFOCTL

TWI Counter Register

Offset = 0x001C

Bits	Name	Description	Access	Reset
31:3	-	Reserved	-	-
2	TFR	TX FIFO reset bit Write 1 to reset TX FIFO, auto clear to 0 when Tx FIFO reset complete.	RW	0
1	RFR	RX FIFO reset bit Write 1 to reset RX FIFO, auto clear to 0 when Rx FIFO reset complete.	RW	0
0	NIB	NACK Ignore Bit 0: not ignore, when receive NACK when write, generate Error, do not continue the command list execute, generate IRQ 1: ignore NACK, when receive NACK, don't generate error, and will continue the command list execute	RW	0

Note: the threshold of Tx FIFO and Rx FIFO generating IRQ is all-empty or all-full.

5.6.3.9 TWIx_FIFOSTAT

TWI Counter Register

Offset = 0x0020

Bits	Name	Description	Access	Reset
31:24	-	Reserved	-	-
23:16	TFD	Tx FIFO level display This field indicate the current Tx FIFO level	R	0
15:8	RFD	Rx FIFO level display This field indicate the current Rx FIFO level	R	0
7	-	Reserved	-	-
6	WRS	Write or read status bit when acts as slave, used only in FIFO mode 0: master write to slave 1: master read from slave	R	0
5	TFF	TX FIFO full bit	R	0

		0: not full 1: full		
4	TFE	TX FIFO empty bit 0: empty 1: not empty	R	0
3	RFF	RX FIFO full bit 0: not full 1: full	R	0
2	RFE	RX FIFO empty bit 0: empty 1: not empty	R	0
1	RNB	Receive NACK Error bit 0: not receive NACK 1: receive NACK when write data Write 1 to clear this bit When writing data outside, if besides the last byte, other byte receives NACK in the transmission, and if FIFOCTL[0] is 0, then this bit should write 1, stop executing CMD and generate interrupt; If FIFOCTL[0] is 1, then this bit should not be set, and continue executing CMD.	RW	0
0	CECB	Command Execute Complete bit 0: not complete 1: complete Writing this bit to 1 meaning that all the instruction and data has been written or read.	R	1

5.6.3.10 TWIx_DATCNT

TWI Counter Register

Offset = 0x0024

Bits	Name	Description	Access	Reset
31:10	-	Reserved	-	-
9:0	TC	Data Transmit counter, is related to CMD register bit[8], if TWI_CMD[8] is not enabled, then this counter is invalid.	RW	0

5.6.3.11 TWIx_RCNT

TWI remain Counter Register

Offset = 0x0028

Bits	Name	Description	Access	Reset

31:10	-	Reserved	-	-
9:0	TC	Remain counter Displaying the number of data that has not been transmitted.	R	0

5.7 GPIO and I/O Multiplexer

5.7.1 Function

This chapter will describe the multiplexing of the whole system and the GPIO/PWM function. There are 146 bits General purpose I/O port and 6 PWM output port in S900 to bring more flexible application possibility. The multiplexing is software controlled and can be configured for different application. Some special pads with build-in pull up or pull down resistance are described here in this module also.

PWM output module is embedded in S900, in the purpose of controlling the external backlight IC, micro-step motor or the buzzer conveniently. It supplies widely variable output frequency from Hz to MHz and 1024-level duty occupancy for precise adjustment.

Features of GPIO and PWM are listed below:

- Built-in pull-up or pull-down resistance in some functional pads

GPIO:

- 146 GPIOs with independent output and input function
- Several different driving capacity of 146 GPIOs
- Software control for Multiplexing

PWM:

- 6 independent PWM signal from Hz to MHz
- PWM with 1024-level duty adjustment
- PWM with high level or low level active

5.7.2 Register List

Table 5 - 8 GPIO/MFP/PWM Base Address

Name	Physical Base Address
GPIO_MFP_PWM	0xE01B0000

Table 5 - 9 GPIO/MFP/PWM Register List

Offset	Register Name	Description
0x0000	GPIO_AOUTEN	GPIOA Output Enable Register
0x0004	GPIO_AINEN	GPIOA Input Enable Register
0x0008	GPIO_ADAT	GPIOA Data Register
0x000C	GPIO_BOUTEN	GPIOB Output Enable Register
0x0010	GPIO_BINEN	GPIOB Input Enable Register

0x0014	GPIO_BDAT	GPIOB Data Register
0x0018	GPIO_COUTEN	GPIOC Output Enable Register
0x001C	GPIO_CINEN	GPIOC Input Enable Register
0x0020	GPIO_CDAT	GPIOC Data Register
0x0024	GPIO_DOUTEN	GPIOD Output Enable Register
0x0028	GPIO_DINEN	GPIOD Input Enable Register
0x002C	GPIO_DDAT	GPIOD Data Register
0x0030	GPIO_EOUTEN	GPIOE Output Enable Register
0x0034	GPIO_EINEN	GPIOE Input Enable Register
0x0038	GPIO_EDAT	GPIOE Data Register
0x00F0	GPIO_FOUTEN	GPIOF Output Enable Register
0x00F4	GPIO_FINEN	GPIOF Input Enable Register
0x00F8	GPIO_FDAT	GPIOF Data Register
0x0040	MFP_CTL0	Multiplexing Control 0 Register
0x0044	MFP_CTL1	Multiplexing Control 1 Register
0x0048	MFP_CTL2	Multiplexing Control 2 Register
0x004C	MFP_CTL3	Multiplexing Control 3 Register
0x0050~0x005C	PWM_CTL0~3	PWM0~3 Output Control Register
0x0060	PAD_PULLCTL0	PAD Pull Control Register 0
0x0064	PAD_PULLCTL1	PAD Pull Control Register 1
0x0068	PAD_PULLCTL2	PAD Pull Control Register 2
0x006C	PAD_ST0	PAD Schmitt Trigger enable Register0
0x0070	PAD_ST1	PAD Schmitt Trigger enable Register1
0x0074	PAD_CTL	PAD Control Register
0x0080	PAD_DRV0	PAD Drive Capacity0 Select Register
0x0084	PAD_DRV1	PAD Drive Capacity1 Select Register
0x0088	PAD_DRV2	PAD Drive Capacity2 Select Register
0x0270	PAD_SR0	PAD slew rate control Register0
0x0274	PAD_SR1	PAD slew rate control Register1
0x0278	PAD_SR2	PAD slew rate control Register2
0x0200	INTC_EXTCTL0	Interrupt0 control and status register
0x0204	INTC_GPIOACTL	GPIOA Interrupt Type control register
0x0208	INTC_GPIOA_PD	GPIOA Interrupt Pending Register
0x020C	INTC_GPIOA_MSK	GPIOA Interrupt Mask Register
0x0210	INTC_GPIOB_PD	GPIOB Interrupt Pending Register
0x0214	INTC_GPIOB_MSK	GPIOB Interrupt Mask Register
0x0218	INTC_GPIOC_PD	GPIOC Interrupt Pending Register
0x021C	INTC_GPIOC_MSK	GPIOC Interrupt Mask Register
0x0220	INTC_GPIOD_PD	GPIOD Interrupt Pending Register
0x0224	INTC_GPIOD_MSK	GPIOD Interrupt Mask Register
0x0228	INTC_GPIOE_PD	GPIOE Interrupt Pending Register
0x022C	INTC_GPIOE_MSK	GPIOE Interrupt Mask Register
0x0230	INTC_GPIOF_PD	GPIOF Interrupt Pending Register

0x0234	INTC_GPIOF_MSK	GPIOF Interrupt Mask Register
0x0240	INTC_GPIOA_TYPE0	GPIOA Interrupt TYPE0 Register
0x0244	INTC_GPIOA_TYPE1	GPIOA Interrupt TYPE1 Register
0x0248	INTC_GPIOB_TYPE0	GPIOB Interrupt TYPE0 Register
0x024C	INTC_GPIOB_TYPE1	GPIOB Interrupt TYPE1 Register
0x0254	INTC_GPIOC_TYPE	GPIOC Interrupt TYPE Register
0x0258	INTC_GPIOD_TYPE0	GPIOD Interrupt TYPE0 Register
0x025C	INTC_GPIOD_TYPE1	GPIOD Interrupt TYPE1 Register
0x0260	INTC_GPIOE_TYPE0	GPIOE Interrupt TYPE0 Register
0x0264	INTC_GPIOE_TYPE1	GPIOE Interrupt TYPE1 Register
0x0268	INTC_GPIOF_TYPE	GPIOF Interrupt TYPE Register
0x500	SGPIO_OUTEN	SGPIO Output Enable Register
0x504	SGPIO_INEN	SGPIO Input Enable Register
0x508	SGPIO_DAT	SGPIO Data Register
0x50C	SGPIO_PD	SGPIO input pending Register
0x510	SGPIO_PD_MSK	SGPIO input Pending mask Register
0x514	SGPIO_CTL	SGPIO control Register
0x518	SGPIO_MFP	SGPIO MFP control Register
0x0520~0x0524	PWM_CTL4~5	PWM4~5 Output Control Register
0x0528	INTC_EXTCTL1	Interrupt1 control and status register
0x052C	INTC_EXTCTL2	Interrupt2 control and status register
0x0540	INTC_GPIOBCTL	GPIOB Interrupt Type control register
0x0544	INTC_GPIOCCTL	GPIOC Interrupt Type control register
0x0548	INTC_GPIODCTL	GPIOD Interrupt Type control register
0x054C	INTC_GPIOECTL	GPIOE Interrupt Type control register
0x0550	INTC_GPIOFCTL	GPIOF Interrupt Type control register

5.7.3 Register Description

5.7.3.1 GPIO_AOUTEN

GPIOA Output Enable Register

Offset = 0x0000

Bits	Name	Description	Access	Reset
31:0	GPIOA_OUTEN	GPIOA[31:0] Output Enable. 0: Disable 1: Enable	RW	0

5.7.3.2 GPIO_AINEN

GPIOA Input Enable Register

Offset = 0x0004

Bits	Name	Description	Access	Reset
31:0	GPIOA_INEN	GPIOA[31:0] Input Enable. 0: Disable 1: Enable	RW	0

5.7.3.3 GPIO_ADAT

GPIOA Data Register

Offset = 0x0008

Bits	Name	Description	Access	Reset
31:0	GPIOA_DAT	GPIOA[31:0] Input/Output Data.	RW	0

5.7.3.4 GPIO_BOUTEN

GPIOB Output Enable Register

Offset = 0x000C

Bits	Name	Description	Access	Reset
31:0	GPIOB_OUTEN	GPIOB[31:0] Output Enable. 0: Disable 1: Enable	RW	0

5.7.3.5 GPIO_BINEN

GPIOB Input Enable Register

Offset = 0x0010

Bits	Name	Description	Access	Reset
31:0	GPIOB_INEN	GPIOB[31:0] Input Enable. 0: Disable 1: Enable	RW	0

5.7.3.6 GPIO_BDAT

GPIOB Data Register

Offset = 0x0014

Bits	Name	Description	Access	Reset
31:0	GPIOB_DAT	GPIOB[31:0] Input/Output Data.	RW	0

5.7.3.7 GPIO_COUTEN

GPIOC Output Enable Register

Offset = 0x0018

Bits	Name	Description	Access	Reset

31:12	-	Reserved	-	-
11:0	GPIOC_OUTEN	GPIOC[11:0] Output Enable. 0: Disable 1: Enable	RW	0

5.7.3.8 GPIO_CINEN

GPIOC Input Enable Register

Offset = 0x001C

Bits	Name	Description	Access	Reset
31:12	-	Reserved	-	-
11:0	GPIOC_INEN	GPIOC[11:0] Input Enable. 0: Disable 1: Enable	RW	0

5.7.3.9 GPIO_CDAT

GPIOC Data Register

Offset = 0x0020

Bits	Name	Description	Access	Reset
31:12	-	Reserved	-	-
11:0	GPIOC_DAT	GPIOC[11:0] Input/Output Data.	RW	0

5.7.3.10 GPIO_DOUTEN

GPIOD Output Enable Register

Offset = 0x0024

Bits	Name	Description	Access	Reset
31:30	-	Reserved	-	-
29:0	GPIOD_OUTEN	GPIOD[29:0] Output Enable. 0: Disable 1: Enable	RW	0

5.7.3.11 GPIO_DINEN

GPIOD Input Enable Register

Offset = 0x0028

Bits	Name	Description	Access	Reset
31:30	-	Reserved	-	-
29:0	GPIOD_INEN	GPIOD[29:0] Input Enable. 0: Disable 1: Enable	RW	0

5.7.3.12 GPIO_DDAT

GPIOD Data Register

Offset = 0x002C

Bits	Name	Description	Access	Reset
31:30	-	Reserved	-	-
29:0	GPIOD_DAT	GPIOD[29:0] Input/Output Data.	RW	0

Note: GPIOD[29:0] voltage is fixed 1.8V.

5.7.3.13 GPIO_EOUTEN

GPIOE Output Enable Register

Offset = 0x0030

Bits	Name	Description	Access	Reset
31:0	GPIOE_OUTEN	GPIOE[31:0] Output Enable. 0: Disable 1: Enable	RW	0

5.7.3.14 GPIO_EINEN

GPIOE Input Enable Register

Offset = 0x0034

Bits	Name	Description	Access	Reset
31:0	GPIOE_INEN	GPIOE[31:0] Input Enable. 0: Disable 1: Enable	RW	0

5.7.3.15 GPIO_EDAT

GPIOE Data Register

Offset = 0x0038

Bits	Name	Description	Access	Reset
31:0	GPIOE_DAT	GPIOE[31:0] Input/Output Data.	RW	0

Note: GPIOE[31:0] voltage is decided by NAND module.

5.7.3.16 GPIO_FOUTEN

GPIOF Output Enable Register

Offset = 0x00F0

Bits	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7:0	GPIOF_OUTEN	GPIOF[7:0] Output Enable.	RW	0

		0: Disable 1: Enable		

5.7.3.17 GPIO_FINEN

GPIOF Input Enable Register

Offset = 0x00F4

Bits	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7:0	GPIOF_INEN	GPIOF[7:0] Input Enable. 0: Disable 1: Enable	RW	0

5.7.3.18 GPIO_FDAT

GPIOF Data Register

Offset = 0x00F8

Bits	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7:0	GPIOF_DAT	GPIOF[7:0] Input/Output Data.	RW	0

Note: GPIOF[7:0] voltage is 1.8V or 3.3V optional.

5.7.3.19 MFP_CTL0

Multiplexing Control 0 Register

Offset = 0x0040

Bits	Name	Description	Access	Reset
31:23	-	Reserved	-	-
22	LVDS_OXX_UART4	LVDS PAD multiplex select. (*Note: the precondition before setting MFP is this pad has set MFP_CTL1[22] to digital function*) **PAD** / **0** / **1** OAP / ERAM_A0 / UART4_RX OAN / ERAM_A2 / UART4_TX	RW	0
21:20	RMII_MDC_MDIO	P_ETH_MDC, P_ETH_MDIO PAD multiplex select. 00: RMII_MDC, RMII_MDIO 01: PWM2,PWM3 10: UART2_RX, UART2_TX 11: Reserved	RW	0
19	P_SIRQ01	P_SIRQ0, P_SIRQ1 PAD multiplex select.	RW	0

		0: SIRQ0, SIRQ1 1: PWM0,PWM1		
18:16	RMII_TXD01	P_ETH_TXD0, P_ETH_TXD1 PAD multiplex select. 000: RMII_TXD0, RMII_TXD1 001: SMII_TX, SMII_SYNC 010: SPI2_SCLK, SPI2_SS 011: UART6_RX, UART6_TX 100: SENS0_D6,SENS0_D7 101: PWM0,PWM1 1xx: Reserved	RW	0
15:13	RMII_TXEN_RXER	P_ETH_TX_EN, P_ETH_RX_ER PAD multiplex select. 000:RMII_TX_EN, RMII_RX_ER 001: UART2_RX, UART2_TX 010: SPI3_SCLK, SPI3_MOSI 011: Reserved 100: Reserved 101: PWM2,PWM3 110: SENS0_VSYNC, SENS0_HSYNC 111: Reserved	RW	0
12:11	RMII_CRS_DV	P_ETH_CRS_DV PAD multiplex select. 00: RMII_CRS_DV 01: SMII_RX 10: SPI2_MISO 11: UART4_RX	RW	0
10:8	RMII_RXD10	P_ETH_RXD1, P_ETH_RXD0 PAD multiplex select. 000:RMII_RXD[1:0] 001: UART2_RTSB, UART2_CTSB 010: SPI3_SS, SPI3_MISO 011: Reserved 100: UART5_TX, UART5_RX 101: PWM0,PWM1 110: SENS0_D8,SENS0_D9 111: Reserved	RW	0
7:6	RMII_REF_CLK	P_ETH_REF_CLK PAD multiplex select. 00: RMII_REF_CLK/SMII_CLK 01: UART4_TX 10: SPI2_MOSI 11: Reserved *Note: IE/OE of this pad is influenced by MAC_CTRL[8], if it is 0, representing that the reference clock is from CMU internally,*	RW	0

		and will be sent to the external PHY, so this pad is OUTPUT; if it is 1, the reference is from external, this pad is INPUT.		
5	P_I2S_D0_D1	P_I2S_D0, P_I2S_D1 PAD multiplex select. 0: I2S_D0, I2S_D1 1: PCM0_OUT, PCM0_IN	RW	0
4:3	I2S_PCM1	P_I2S_LRCLK0, P_I2S_MCLK0 PAD multiplex select. 00: I2S_LRCLK0, I2S_MCLK0 01: PCM0_SYNC, PCM0_CLK 10: PCM1_SYNC, PCM1_CLK 11: Reserved	RW	0
2	I2S_PCM0	P_I2S_BCLK0,P_I2S_BCLK1, P_I2S_LRCLK1, P_I2S_MCLK1 PAD multiplex select. 0: I2S_BCLK0, I2S_BCLK1, I2S_LRCLK1, P_I2S_MCLK1 1:PCM0_SYNC, PCM0_CLK, PCM0_CLK, PCM0_SYNC	RW	0
1:0	PCM1_SPI1_TWI3	P_PCM1_IN,P_PCM1_CLK, P_PCM1_SYNC, P_PCM1_OUT PAD multiplex select. 00: PCM1_IN, PCM1_CLK, PCM1_SYNC, PCM1_OUT 01: SPI1_SCLK, SPI1_SS, SPI1_MISO, SPI1_MOSI 10: TWI3_SCLK, PWM4, PWM5, TWI3_SDATA 11: -,UART4_RTSB, UART4_CTSB,-	RW	0

5.7.3.20 MFP_CTL1

Multiplexing Control 1 Register

Offset = 0x0044

Bits	Name	Description	Access	Reset
31:29	ERAM_A[5:7]	ERAM_A[5:7] PAD multiplex select. 000: UART4_RTSB, UART4_CTSB 001:TCK, TMS, TDI 010:ERAM_A[5:7] 011:PWM0, PWM1 100: reserved 101: SENS0_D[6:8] 110 : Reserved 111 : Reserved	RW	1
28:26	ERAM_A[8:10]	ERAM_A[8:10] PAD multiplex select. 000: -,DRV_VBUS_U20,DRV_VBUS_U3	RW	1

<table>
<tr><td></td><td></td><td>001:TDO, UART5_RX, TRST
010:ERAM_A[8:10]
011: PWM1, PWM2, PWM3
100: Reserved
101:SENS0_D9, SENS0_VSYNC
110 : Reserved
111 : Reserved</td><td></td><td></td></tr>
<tr><td>25:23</td><td>ERAM_A11</td><td>ERAM_A11 PAD multiplex select.
000: Reserved
001 : Reserved
010: ERAM_A11
011: PWM2
100: UART5_TX
101: Reserved
110: SENS0_HSYNC
111 : Reserved</td><td>RW</td><td>0x4</td></tr>
<tr><td>22</td><td>LVDS_OXX</td><td>LVDS PAD multiplex select.
(Note: used as 1.8V GPIO should be switched to digital first)
<table>
<tr><th>PAD</th><th>0: (analog)</th><th>1: (digital)</th></tr>
<tr><td>OEP</td><td>OEP</td><td>UART2_RX</td></tr>
<tr><td>OEN</td><td>OEN</td><td>UART2_TX</td></tr>
<tr><td>ODP</td><td>ODP</td><td>UART2_RTSB</td></tr>
<tr><td>ODN</td><td>ODN</td><td>UART2_CTSB</td></tr>
<tr><td>OCP</td><td>OCP</td><td>PCM1_IN</td></tr>
<tr><td>OCN</td><td>OCN</td><td>PCM1_OUT</td></tr>
<tr><td>OBP</td><td>OBP</td><td>PCM1_CLK</td></tr>
<tr><td>OBN</td><td>OBN</td><td>PCM1_SYNC</td></tr>
<tr><td>OAP</td><td>OAP</td><td>ERAM_A0</td></tr>
<tr><td>OAN</td><td>OAN</td><td>ERAM_A2</td></tr>
</table></td><td>RW</td><td>0</td></tr>
<tr><td>21</td><td>LVDS_EXX</td><td>LVDS PAD multiplex select.
(Note: used as 1.8V GPIO should be switched to digital first)
<table>
<tr><th>PAD</th><th>0: (analog)</th><th>1: (digital)</th></tr>
<tr><td>EEP</td><td>EEP</td><td>ERAM_RD</td></tr>
<tr><td>EEN</td><td>EEN</td><td>ERAM_WR</td></tr>
<tr><td>EDP</td><td>EDP</td><td>ERAM_D13</td></tr>
<tr><td>EDN</td><td>EDN</td><td>ERAM_D12</td></tr>
<tr><td>ECP</td><td>ECP</td><td>ERAM_D11</td></tr>
<tr><td>ECN</td><td>ECN</td><td>ERAM_A4</td></tr>
<tr><td>EBP</td><td>EBP</td><td>ERAM_D15</td></tr>
<tr><td>EBN</td><td>EBN</td><td>ERAM_D14</td></tr>
<tr><td>EAP</td><td>EAP</td><td>ERAM_D9</td></tr>
</table></td><td>RW</td><td>0</td></tr>
</table>

		EAN EAN ERAM_D8		
20:6	-	Reserved	-	-
5:4	SPI0_TWI3_PCM	P_SPI0_SCLK, P_SPI0_MOSI PAD multiplex select. 00: SPI0_SCLK, SPI0_MOSI 01: ERAM_A12, ERAM_A15 10: TWI3_SCLK, TWI3_SDATA 11: PCM0_CLK, PCM0_SYNC	RW	0
3:1	SPI0_I2S_PCM	P_SPI0_SS, P_SPI0_MISO PAD multiplex select. 000: SPI0_SS, SPI0_MISO 001: ERAM_A[13:14] 010: I2S_LRCLK1, I2S_MCLK1 011: PCM1_OUT, PCM1_IN 100: PCM0_OUT, PCM0_IN 101: PWM4, PWM5 1xx: Reserved	RW	0
0	-	Reserved	-	-

5.7.3.21 MFP_CTL2

Multiplexing Control 2 Register

Offset = 0x0048

Bits	Name	Description	Access	Reset
31:24	-	Reserved	-	-
23	UART2_RTSB	P_UART2_RTSB PAD multiplex select. 0: UART2_RTSB 1: UART0_RX	RW	0
22	UART2_CTSB	P_UART2_CTSB PAD multiplex select. 0: UART2_CTSB 1: UART0_TX	RW	0
21	UART3_RTSB	P_UART3_RTSB PAD multiplex select. 0: UART3_RTSB 1: UART5_RX	RW	0
20	UART3_CTSB	P_UART3_CTSB PAD multiplex select. 0: UART3_CTSB 1: UART5_TX	RW	0
19:17	SD0_D0	P_SD0_D0 PAD multiplex select. 000: SD0_D0 001: ERAM_D0 010: Reserved 011: TRST 100: UART2_RX 101: UART5_RX	RW	0

		101: UART5_RX 110: GPU_TRST 111: Reserved		
16:14	SD0_D1	P_SD0_D1 PAD multiplex select. 000: SD0_D1 001: ERAM_D1 010: GPU_PAD_RESET 011: Reserved 100: UART2_TX 101: UART5_TX 11x: Reserved	RW	0
13:11	SD0_D2_D3	P_SD0_D[2:3] PAD multiplex select. 000: SD0_D[2:3] 001: ERAM_D[2:3] 010: Reserved 011: TDO, TDI 100: UART2_RTSB, UART2_CTSB 101: UART1_TX, UART1_RX 110: GPU_TDO, GPU_TDI 111: Reserved	RW	0
10:9	SD1_D0_D3	P_SD1_D[0:3] PAD multiplex select. 00: SD1_D[0:3] 01: ERAM_D[4:7] 10: Reserved 11: Reserved	RW	0
8:7	SD0_CMD	P_SD0_CMD PAD multiplex select. 00: SD0_CMD 01: ERAM_A1 10: GPU_TMS 11: TMS	RW	0
6:5	SD0_CLK	P_SD0_CLK PAD multiplex select. 00: SD0_CLK 01: ERAM_A3 10: TCK 11: GPU_TCK	RW	0
4:3	SD1_CMD_CLK	P_SD1_CMD, P_SD1_CLK PAD multiplex select. 00: SD1_CMD, SD1_CLK 01: ERAM_CEB0_7, ERAM_D10 10: Reserved11: Reserved	RW	0
2:0	UART0_RX	P_UART0_RX PAD multiplex select. 000: UART0_RX 001: UART2_RX 010: SPI1_MISO	RW	0

		011: TWI5_SDATA 100: PCM1_IN 101: I2S_MCLK1 11x: Reserved		

5.7.3.22 MFP_CTL3

Multiplexing Control 3 Register

Offset = 0x004C

<table>
<tr><th>Bits</th><th>Name</th><th>Description</th><th>Access</th><th>Reset</th></tr>
<tr><td>31:28</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>27</td><td>DNAND0_SD2</td><td>P_DNAND0 and SD2 PAD multiplex select.
<table>
<tr><th>PAD</th><th>0:</th><th>1:</th></tr>
<tr><td>P_NAND0_D0_D</td><td>NAND0_D0</td><td>SD2_D0</td></tr>
<tr><td>P_NAND0_D1_D</td><td>NAND0_D1</td><td>SD2_D1</td></tr>
<tr><td>P_NAND0_D2_D</td><td>NAND0_D2</td><td>SD2_D2</td></tr>
<tr><td>P_NAND0_D3_D</td><td>NAND0_D3</td><td>SD2_D3</td></tr>
<tr><td>P_NAND0_D4_D</td><td>NAND0_D4</td><td>SD2_D4</td></tr>
<tr><td>P_NAND0_D5_D</td><td>NAND0_D5</td><td>SD2_D5</td></tr>
<tr><td>P_NAND0_D6_D</td><td>NAND0_D6</td><td>SD2_D6</td></tr>
<tr><td>P_NAND0_D7_D</td><td>NAND0_D7</td><td>SD2_D7</td></tr>
<tr><td>P_NAND0_DQSN_D</td><td>NAND0_DQSN</td><td>SD2_CMD</td></tr>
<tr><td>P_NAND0_CEB3_D</td><td>NAND0_CEB3</td><td>SD2_CLK</td></tr>
</table></td><td>RW</td><td>0</td></tr>
<tr><td>26:22</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>21:19</td><td>UART0_TX</td><td>P_UART0_TX PAD multiplex select.
000: UART0_TX
001: UART2_TX
010: SPI1_SS
011: TWI5_SCLK
100: SPDIF
101: PCM1_OUT
110: I2S_LRCLK1
1xx: Reserved</td><td>RW</td><td>0</td></tr>
<tr><td>18:16</td><td>TWI0_MFP</td><td>P_TWI0_SCLK, P_TWI0_SDATA PAD multiplex select.
000: TWI0_SCLK, TWI0_SDATA
001: UART2_RTSB, UART2_CTSB
010: TWI1_SCLK, TWI1_SDATA
011: UART1_TX, UART1_RX
100: SPI1_SCLK, SPI1_MOSI
101: Reserved11x: Reserved</td><td>RW</td><td>0</td></tr>
<tr><td>15</td><td>CSI0_CN_CP</td><td>CSI0_CN, CSI0_CP multiplex select.
Note: the precondition of setting this MFP is that this pad has set MFP_CTL3[14] to digital function.</td><td>RW</td><td>0</td></tr>
</table>

<table>
<tr><td></td><td></td><td><table>
<tr><th>PAD</th><th>0</th><th>1</th></tr>
<tr><td>CSI0_CN</td><td>SENS0_D0</td><td>SENS0_VSYNC</td></tr>
<tr><td>CSI0_CP</td><td>SENS0_D1</td><td>SENS0_HSYNC</td></tr>
</table></td><td></td><td></td></tr>
<tr><td>14</td><td>CSI0_SENS0</td><td>CSI0 PAD multiplex select.<table>
<tr><th>PAD</th><th>0: (analog)</th><th>1: (digital)</th></tr>
<tr><td>CSI0_DN0</td><td>CSI0_DN0</td><td>SENS0_D2</td></tr>
<tr><td>CSI0_DP0</td><td>CSI0_DP0</td><td>SENS0_D3</td></tr>
<tr><td>CSI0_DN1</td><td>CSI0_DN1</td><td>SENS0_D4</td></tr>
<tr><td>CSI0_DP1</td><td>CSI0_DP1</td><td>SENS0_D5</td></tr>
<tr><td>CSI0_CN</td><td>CSI0_CN</td><td>SENS0_D0</td></tr>
<tr><td>CSI0_CP</td><td>CSI0_CP</td><td>SENS0_D1</td></tr>
<tr><td>CSI0_DN2</td><td>CSI0_DN2</td><td>SENS0_D6</td></tr>
<tr><td>CSI0_DP2</td><td>CSI0_DP2</td><td>SENS0_D7</td></tr>
<tr><td>CSI0_DN3</td><td>CSI0_DN3</td><td>SENS0_D8</td></tr>
<tr><td>CSI0_DP3</td><td>CSI0_DP3</td><td>SENS0_D9</td></tr>
</table></td><td>RW</td><td>0</td></tr>
<tr><td>13</td><td>CSI1_SENS0</td><td>CSI1 PAD multiplex select.<table>
<tr><th>PAD</th><th>0: (analog)</th><th>1: (digital)</th></tr>
<tr><td>CSI1_DN0</td><td>CSI1_DN0</td><td>SENS0_D0</td></tr>
<tr><td>CSI1_DP0</td><td>CSI1_DP0</td><td>SENS0_D1</td></tr>
<tr><td>CSI1_DN1</td><td>CSI1_DN1</td><td>SENS0_D2</td></tr>
<tr><td>CSI1_DP1</td><td>CSI1_DP1</td><td>SENS0_D3</td></tr>
<tr><td>CSI1_CN</td><td>CSI1_CN</td><td>SENS0_D4</td></tr>
<tr><td>CSI1_CP</td><td>CSI1_CP</td><td>SENS0_D5</td></tr>
</table></td><td>RW</td><td>0</td></tr>
<tr><td>12</td><td>DSI</td><td>DSI PAD multiplex select.
(Note: used as 1.8V GPIO should be switched to digital first)<table>
<tr><th>PAD</th><th>0: (analog)</th><th>1: (digital)</th></tr>
<tr><td>DSI_DP3</td><td>DSI_DP3</td><td>UART2_RX</td></tr>
<tr><td>DSI_DN3</td><td>DSI_DN3</td><td>UART2_TX</td></tr>
<tr><td>DSI_DP1</td><td>DSI_DP1</td><td>UART2_RTSB</td></tr>
<tr><td>DSI_DN1</td><td>DSI_DN1</td><td>UART2_CTSB</td></tr>
<tr><td>DSI_CP</td><td>DSI_CP</td><td>PCM1_IN</td></tr>
<tr><td>DSI_CN</td><td>DSI_CN</td><td>PCM1_OUT</td></tr>
<tr><td>DSI_DP0</td><td>DSI_DP0</td><td>PCM1_CLK</td></tr>
<tr><td>DSI_DN0</td><td>DSI_DN0</td><td>PCM1_SYNC</td></tr>
<tr><td>DSI_DP2</td><td>DSI_DP2</td><td>UART4_RX</td></tr>
<tr><td>DSI_DN2</td><td>DSI_DN2</td><td>UART4_TX</td></tr>
</table></td><td>RW</td><td>0</td></tr>
<tr><td>11</td><td>DNAND1_SD3</td><td>P_DNAND1 and SD3 PAD multiplex select.<table>
<tr><th>PAD</th><th>0:</th><th>1:</th></tr>
<tr><td>P_NAND1_D0_D</td><td>NAND1_D0</td><td>SD3_D0</td></tr>
<tr><td>P_NAND1_D1_D</td><td>NAND1_D1</td><td>SD3_D1</td></tr>
<tr><td>P_NAND1_D2_D</td><td>NAND1_D2</td><td>SD3_D2</td></tr>
</table></td><td>RW</td><td>0</td></tr>
</table>

<table>
<tr><td></td><td></td><td>
<table>
<tr><td>P_NAND1_D3_D</td><td>NAND1_D3</td><td>SD3_D3</td></tr>
<tr><td>P_NAND1_D4_D</td><td>NAND1_D4</td><td>SD3_D4</td></tr>
<tr><td>P_NAND1_D5_D</td><td>NAND1_D5</td><td>SD3_D5</td></tr>
<tr><td>P_NAND1_D6_D</td><td>NAND1_D6</td><td>SD3_D6</td></tr>
<tr><td>P_NAND1_D7_D</td><td>NAND1_D7</td><td>SD3_D7</td></tr>
<tr><td>P_NAND1_DQSN_D</td><td>NAND1_DQSN</td><td>SD3_CMD</td></tr>
<tr><td>P_NAND1_CEB1_D</td><td>NAND1_CEB1</td><td>SD3_CLK</td></tr>
</table>
</td><td></td><td></td></tr>
<tr><td>10</td><td>DNAND1_PCM01</td><td>P_DNAND1 and PCM01 multiplex select.
<table>
<tr><th>PAD</th><th>0:</th><th>1:</th></tr>
<tr><td>P_NAND1_CEB3_D</td><td>NAND1_CEB3</td><td>PWM0</td></tr>
<tr><td>P_NAND1_CEB0_D</td><td>NAND1_CEB0</td><td>PWM1</td></tr>
</table></td><td>RW</td><td>0</td></tr>
<tr><td>9</td><td>CSI1_DN0_DP0</td><td>CSI1_DN0, CSI1_DP0 multiplex select.
Note: the precondition of setting this MFP is that this pad has set MFP_CTL3[13] to digital function.
<table>
<tr><th>PAD</th><th>0</th><th>1</th></tr>
<tr><td>CSI1_DN0</td><td>SENS0_D0</td><td>SENSOR0_PCLK</td></tr>
<tr><td>CSI1_DP0</td><td>SENS0_D1</td><td>SENSOR0_CKOUT</td></tr>
</table></td><td>RW</td><td>0</td></tr>
<tr><td>8</td><td>UART4_TWI4</td><td>P_UART4_RX, P_UART4_TX PAD multiplex select.
0: UART4_RX, UART4_TX
1: TWI4_SCLK, TWI4_SDATA</td><td>RW</td><td>0</td></tr>
<tr><td>7:0</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
</table>

5.7.3.23 PWM_CTL0~3

PWMx Output Control Register (x = 0~3)

Offset = 0x0050 + 4 * x

Bits	Name	Description	Access	Reset
31:29	-	Reserved	-	-
28:19	DUTY	Duty select: 0: Duty =0 1: Duty =1 2: Duty =2 … 63: Duty =63 … 1023: Duty =1023 T active = (DUTY+1) /DIV	RW	0
18:9	DIV	DIV select: 0: reserved 1: DIV=2 2: DIV=3	RW	0x3F

		… 63: DIV=64 (default value) … 1023: DIV=1024		
8	POL_SEL	Polarity select 0:PWM low voltage level active 1:PWM high voltage level active	RW	0
7:0	-	Reserved	-	-

5.7.3.24 PAD_PULLCTL0

PAD Pull Control Register 0

Offset = 0x0060

Bits	Name	Description	Access	Reset
31:17	-	Reserved	-	-
19:18	P_ETH_RX_ER_P	P_ETH_RX_ER PAD pull control. 00: hi-Z 01: pull-up 10: pull-down 11: repeater (hold)		0
17:16	P_SIRQ0_P	P_SIRQ0 PAD pull control. 00: hi-Z 01: pull-up 10: pull-down 11: repeater (hold)	RW	0
15:14	P_SIRQ1_P	P_SIRQ1 PAD pull control. 00: hi-Z 01: pull-up 10: pull-down 11: repeater (hold)	RW	0
13:12	P_SIRQ2_P	P_SIRQ2 PAD pull control. 00: hi-Z 01: pull-up 10: pull-down 11: repeater (hold)	RW	0
11:10	P_TWI0_SDATA_P	P_TWI0_SDATA PAD pull control. 00: hi-Z 01: pull-up 10: pull-down 11: repeater (hold)	RW	0
9:8	P_TWI0_SCLK_P	P_TWI0_SCLK PAD pull control. 00: hi-Z 01: pull-up 10: pull-down	RW	0

		11: repeater (hold)		
7:6	P_ERAM_A5_P	P_ERAM_A5 PAD pull control. 00: hi-Z 01: pull-up 10: pull-down 11: repeater (hold)	RW	1
5:4	P_ERAM_A6_P	P_ERAM_A6 PAD pull control. 00: hi-Z 01: pull-up 10: pull-down 11: repeater (hold)	RW	1
3:2	P_ERAM_A7_P	P_ERAM_A7 PAD pull control. 00: hi-Z 01: pull-up 10: pull-down 11: repeater (hold)	RW	1
1:0	P_ERAM_A10_P	P_ERAM_A10 PAD pull control. 00: hi-Z 01: pull-up 10: pull-down 11: repeater (hold)	RW	1

5.7.3.25 PAD_PULLCTL1

PAD Pull Control Register 1

Offset = 0x0064

Bits	Name	Description	Access	Reset
31:30	P_PCM1_IN	P_PCM1_IN PAD pull control. 00: hi-Z 01: pull-up 10: pull-down 11: repeater (hold)	RW	0
29:28	P_PCM1_OUT	P_PCM1_OUT PAD pull control. 00: hi-Z 01: pull-up 10: pull-down 11: repeater (hold)	RW	0
27:26	P_SD0_D0_P	P_SD0_D0 PAD pull control. 00: hi-Z 01: pull-up 10: pull-down 11: repeater (hold)	RW	1
25:24	P_SD0_D1_P	P_SD0_D1 PAD pull control. 00: hi-Z	RW	0

		01: pull-up 10: pull-down 11: repeater (hold)		
23:22	P_SD0_D2_P	P_SD0_D2 PAD pull control. 00: hi-Z 01: pull-up 10: pull-down 11: repeater (hold)	RW	0
21:20	P_SD0_D3_P	P_SD0_D3 PAD pull control. 00: hi-Z 01: pull-up 10: pull-down 11: repeater (hold)	RW	1
19:18	P_SD0_CMD_P	P_SD0_CMD PAD pull control. 00: hi-Z 01: pull-up 10: pull-down 11: repeater (hold)	RW	1
17:16	P_SD0_CLK_P	P_SD0_CLK PAD pull control. 00: hi-Z 01: pull-up 10: pull-down 11: repeater (hold)	RW	1
15:14	P_SD1_CMD_P	P_SD1_CMD PAD pull control. 00: hi-Z 01: pull-up 10: pull-down 11: repeater (hold)	RW	0
13:12	P_SD1_D0_P	P_SD1_D0 PAD pull control. 00: hi-Z 01: pull-up 10: pull-down 11: repeater (hold)	RW	0
11:10	P_SD1_D1_P	P_SD1_D1 PAD pull control. 00: hi-Z 01: pull-up 10: pull-down 11: repeater (hold)	RW	0
9:8	P_SD1_D2_P	P_SD1_D2 PAD pull control. 00: hi-Z 01: pull-up 10: pull-down 11: repeater (hold)	RW	0
7:6	P_SD1_D3_P	P_SD1_D3 PAD pull control.	RW	0

		00: hi-Z 01: pull-up 10: pull-down 11: repeater (hold)		
5:4	P_UART0_RX_P	P_UART0_RX PAD pull control. 00: hi-Z 01: pull-up 10: pull-down 11: repeater (hold)	RW	0
3:2	P_UART0_TX_P	P_UART0_TX PAD pull control. 00: hi-Z 01: pull-up 10: pull-down 11: repeater (hold)	RW	0
1:0	-	Reserved	-	-

5.7.3.26 PAD_PULLCTL2

PAD Pull Control Register 2

Offset = 0x0068

Bits	Name	Description	Access	Reset
31:28	-	Reserved	-	-
27:26	P_TWI2_SDATA_P	P_TWI2_SDATA PAD pull control. 00: hi-Z 01: pull-up 10: pull-down 11: repeater (hold)	RW	0
25:24	P_TWI2_SCLK_P	P_TWI2_SCLK PAD pull control. 00: hi-Z 01: pull-up 10: pull-down 11: repeater (hold)	RW	0
23:22	P_SPI0_SCLK_P	P_SPI0_SCLK PAD pull control. 00: hi-Z 01: pull-up 10: pull-down 11: repeater (hold)	RW	0
21:20	P_SPI0_MOSI_P	P_SPI0_MOSI PAD pull control. 00: hi-Z 01: pull-up 10: pull-down 11: repeater (hold)	RW	0
19:18	P_TWI1_SDATA_P	P_TWI1_SDATA PAD pull control. 00: hi-Z	RW	0

		01: pull-up 10: pull-down 11: repeater (hold)		
17:16	P_TWI1_SCLK_P	P_TWI1_SCLK PAD pull control. 00: hi-Z 01: pull-up 10: pull-down 11: repeater (hold)	RW	0
15	P_NAND0_D[0:7]_D	P_NAND0_D[0:7]_D PAD pull control. 0:30K pull-up disable 1:30K pull-up enable	RW	0
14	P_NAND0_DQSN_D	P_NAND0_DQSN_D PAD pull control. 0:30K pull-up disable 1:30K pull-up enable	RW	1
13	P_NAND0_DQS_D	P_NAND0_DQS_D PAD pull control. 0:30K pull-down disable 1:30K pull-down enable	RW	1
12	P_NAND1_D[0:7]_D	P_NAND1_D[0:7]_D PAD pull control. 0:30K pull-up disable 1:30K pull-up enable	RW	0
11	P_NAND1_DQSN_D	P_NAND1_DQSN_D PAD pull control. 0:30K pull-up disable 1:30K pull-up enable	RW	1
10	P_NAND1_DQS_D	P_NAND1_DQS_D PAD pull control. 0:30K pull-down disable 1:30K pull-down enable	RW	1
9:8	SGPIO2_P	SGPIO2 PAD pull control. 00: hi-Z 01: pull-up 10: pull-down 11: repeater (hold)	RW	0
7:6	SGPIO3_P	SGPIO3 PAD pull control. 00: hi-Z 01: pull-up 10: pull-down 11: repeater (hold)	RW	0
5:4	P_UART4_RX_P	P_UART4_RX PAD pull control. 00: hi-Z 01: pull-up 10: pull-down 11: repeater (hold)	RW	0
3:2	P_UART4_TX_P	P_UART4_TX PAD pull control. 00: hi-Z 01: pull-up	RW	0

		10: pull-down 11: repeater (hold)		
1:0	-	Reserved	-	-

5.7.3.27 PAD_ST0

PAD Schmitt Trigger enable Register0

Offset = 0x006C

Bits	Name	Description	Access	Reset
31	-	Reserved	-	-
30	P_TWI0_SDATA_ST	P_TWI0_SDATA pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	1
29	P_UART0_RX_ST	P_UART0_RX pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	0
28	P_ETH_MDC	P_ETH_MDC pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	0
27:24	-	Reserved	-	-
23	P_I2S_MCLK1_ST	P_I2S_MCLK1 pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	0
22	P_ETH_REF_CLK_ST	P_ETH_REF_CLK pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	1
21	P_ETH_TX_EN_ST	P_ETH_TX_EN pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	0
20	P_ETH_TXD0_ST	P_ETH_TXD0 pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	0
19	P_I2S_LRCLK1_ST	P_I2S_LRCLK1 pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	0
18	SGPIO2_ST	SGPIO2 pad Schmitt trigger	RW	0

		enable 1: enable Schmitt trigger 0: disable Schmitt trigger		
17	SGPIO3_ST	SGPIO3 pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	0
16	P_UART4_TX_ST	UART4_TX pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	0
15	P_I2S_D1_ST	P_I2S_D1 pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	0
14	P_UART0_TX_ST	P_UART0_TX pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	0
13	P_SPI0_SCLK_ST	P_SPI0_SCLK pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	1
12	P_SD0_CLK_ST	P_SD0_CLK pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	1
11	P_ERAM_A5_ST	P_ERAM_A5 pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	1
10:8	-	Reserved	-	-
7	P_TWI0_SCLK_ST	P_TWI0_SCLK pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	1
6	P_ERAM_A9_ST	P_ERAM_A9 pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	0
5	P_OEP_ST	P_OEP pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	0

4	P_ODN_ST	P_ODN pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	0
3	P_OAP_ST	P_OAP pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	0
2	P_I2S_BCLK1_ST	P_I2S_BCLK1 pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	0
1:0	-	Reserved	-	-

5.7.3.28 PAD_ST1

PAD Schmitt Trigger enable Register1

Offset = 0x0070

Bits	Name	Description	Access	Reset
31:30	-	Reserved	-	-
29	P_I2S_LRCLK0_ST	P_I2S_LRCLK0 pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	0
28	P_UART4_RX_ST	P_UART4_RX pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	0
27	P_UART3_CTSB_ST	P_UART3_CTSB pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	0
26	P_UART3_RTSB_ST	P_UART3_RTSB pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	0
25	P_UART3_RX_ST	P_UART3_RX pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	0
24	P_UART2_RTSB_ST	P_UART2_RTSB pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	0

23	P_UART2_CTSB_ST	P_UART2_CTSB pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	0
22	P_UART2_RX_ST	P_UART2_RX pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	0
21	P_ETH_RXD0_ST	P_ETH_RXD0 pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	0
20	P_ETH_RXD1_ST	P_ETH_RXD1 pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	0
19	P_ETH_CRS_DV_ST	P_ETH_CRS_DV pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	0
18	P_ETH_RX_ER_ST	P_ETH_RX_ER pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	0
17	P_ETH_TXD1_ST	P_ETH_TXD1 pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	0
16	OCP_ST	OCP pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	0
15	OBP_ST	OBP pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	0
14	OBN_ST	OBN pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	0
13	-	Reserved	-	-
12	P_PCM1_OUT_ST	P_PCM1_OUT pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	0
11	P_PCM1_CLK_ST	P_PCM1_CLK pad Schmitt trigger enable	RW	0

		1: enable Schmitt trigger 0: disable Schmitt trigger		
10	P_PCM1_IN_ST	P_PCM1_IN pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	0
9	P_PCM1_SYNC_ST	P_PCM1_SYNC pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	0
8	P_TWI1_SCLK_ST	P_TWI1_SCLK pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	1
7	P_TWI1_SDATA_ST	P_TWI1_SDATA pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	1
6	P_TWI2_SCLK_ST	P_TWI2_SCLK pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	1
5	P_TWI2_SDATA_ST	P_TWI2_SDATA pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	1
4	P_SPI0_MOSI_ST	P_SPI0_MOSI pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	0
3	P_SPI0_MISO_ST	P_SPI0_MISO pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	0
2	P_SPI0_SS_ST	P_SPI0_SS pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	0
1	P_I2S_BCLK0_ST	P_I2S_BCLK0 pad Schmitt trigger enable 1: enable Schmitt trigger 0: disable Schmitt trigger	RW	0
0	P_I2S_MCLK0_ST	P_I2S_MCLK0 pad Schmitt trigger enable	RW	0

		1: enable Schmitt trigger 0: disable Schmitt trigger		

5.7.3.29 PAD_CTL

PAD Control Register

Offset = 0x0074

Bits	Name	Description	Access	Reset
31:11	-	Reserved	-	-
10:9	PCM0_MODULE_SEL	00: PCM0 MODULE is master mode 01: PCM0 MODULE is slaver mode1 10: PCM0 MODULE is slaver mode2 11: PCM0 MODULE is slaver mode3	RW	0
8	SD0_PAD_POWER	P_SD0_D0 P_SD0_D1 P_SD0_D2 P_SD0_D3 P_SD0_CMD P_SD0_CLK Power (VCC4) select: 0:3.3V 1:1.8V	RW	0
7	SD1_PAD_POWER	P_SD1_D0 P_SD1_D1 P_SD1_D2 P_SD1_D3 P_SD1_CMD P_SD1_CLK Power (VCC3) select: 0:3.3V 1:1.8V	RW	0
6	OTHER_PAD_POWER	The other pad (except LVDS, DSI, NAND, SD01, UART3_TWI2_SGPIO123 and PCM1_I2S) Power (VCC0) select: 0:3.3V 1:1.8V	RW	0
5	UART3_TWI2_SGPIO123_PAD_POWER	P_UART3_RX P_UART3_TX P_UART3_RTSB P_UART3_CTSB P_TWI2_SCLK	RW	0

		P_TWI2_SDATA SGPIO1 SGPIO2 SGPIO3 power (VCC2) select: 0:3.3V 1:1.8V		
4	PCM1_I2S_PAD_POWER	P_I2S_D0 P_I2S_BCLK0 P_I2S_LRCLK0 P_I2S_MCLK0 P_I2S_D1 P_I2S_BCLK1 P_I2S_LRCLK1 P_I2S_MCLK1 P_PCM1_IN P_PCM1_CLK P_PCM1_SYNC P_PCM1_OUT Power (VCC1) select: 0:3.3V 1:1.8V	RW	0
3:2	-	Reserved	-	-
1	PADEN	PAD Enable. All of the PAD are enabled (Not high-z) with their functions determined by the multi-function register's values. 0: Disable 1: Enable *Note: If some input PADs are enabled, they shall be configured as GPIO outputs to avoid current leakage.*	RW	0
0	-	Reserved	-	-

5.7.3.30 PAD_DRV0

PAD Drive Capacity0 Select Register

Offset = 0x0080

Bits	Name	Description	Access	Reset
31:30	SGPIO3	SGPIO3 PAD drive level select 00: 2mA 01: 4mA	RW	0

		10: 8mA 11: 12mA		
29:28	SGPIO2	SGPIO2 PAD drive level select 00: 2mA 01: 4mA 10: 8mA 11: 12mA	RW	0
27:26	SGPIO1	SGPIO1 PAD drive level select 00: 2mA 01: 4mA 10: 8mA 11: 12mA	RW	0
25:24	SGPIO0	SGPIO0 PAD drive level select 00: 2mA 01: 4mA 10: 8mA 11: 12mA	RW	0
23:22	RMII_TXD01	P_ETH_TXD0, P_ETH_TXD1 PAD drive level select 00: 2mA 01: 4mA 10: 8mA 11: 12mA	RW	0
21:20	RMII_TXEN_RXER	P_ETH_TX_EN, P_ETH_RX_ER PAD drive level select 00: 2mA 01: 4mA 10: 8mA 11: 12mA	RW	0
19:18	RMII_CRS_DV	P_ETH_CRS_DV PAD drive level select 00: 2mA 01: 4mA 10: 8mA 11: 12mA	RW	0
17:16	RMII_RXD10	P_ETH_RXD1, P_ETH_RXD0 PAD drive level select 00: 2mA 01: 4mA 10: 8mA 11: 12mA	RW	0
15:14	RMII_REF_CLK	P_ETH_REF_CLK PAD drive level select 00: 2mA 01: 4mA 10: 8mA	RW	0

		11: 12mA		
13:12	RMII_MDC_MDIO	P_ETH_MDC, P_ETH_MDIO PAD drive level select 00: 2mA 01: 4mA 10: 8mA 11: 12mA	RW	0
11:10	SIRQ01	P_SIRQ0, P_SIRQ1 PAD drive level select 00: 2mA 01: 4mA 10: 8mA 11: 12mA	RW	0
9:8	SIRQ2	P_SIRQ2 PAD drive level select 00: 2mA 01: 4mA 10: 8mA 11: 12mA	RW	0
7:6	I2S_D01	P_I2S_D0, P_I2S_D1 PAD drive level select 00: 2mA 01: 4mA 10: 8mA 11: 12mA	RW	0
5:4	I2S_PCM1	P_I2S_LRCLK0, P_I2S_MCLK0 PAD drive level select 00: 2mA 01: 4mA 10: 8mA 11: 12mA	RW	0
3:2	I2S_PCM0	P_I2S_BCLK0,P_I2S_BCLK1, P_I2S_LRCLK1, P_I2S_MCLK1 PAD drive level select 00: 2mA 01: 4mA 10: 8mA 11: 12mA	RW	0
1:0	PCM1_SPI1_TWI3	P_PCM1_IN,P_PCM1_CLK, P_PCM1_SYNC, P_PCM1_OUT PAD drive level select 00: 2mA 01: 4mA 10: 8mA 11: 12mA	RW	0

5.7.3.31 PAD_DRV1

PAD Drive Capacity1 Select Register

Offset = 0x0084

Bits	Name	Description	Access	Reset
31:30	-	Reserved	-	-
29:28	LVDS_ERAM_UART4	LVDS OAP, OAN PAD drive level select. 00: level1 01: level2 10: level3 11: reserved	RW	0
27:26	LVDS_UART2	LVDS OEP, OEN, ODP, ODN PAD drive level select. 00: level1 01: level2 10: level3 11: reserved	RW	0
25:24	LVDS_PCM1	LVDS OCP, OCN, OBP, OBN PAD drive level select. 00: level1 01: level2 10: level3 11: reserved	RW	0
23:22	LVDS_ERAM	LVDS EEP, EEN, EDP, EDN, ECP, ECN, EBP, EBN, EAP, EAN PAD drive level select. 00: level1 01: level2 10: level3 11: reserved	RW	0
21:20	-	Reserved	-	-
19:18	SD1_ERAM	P_SD1_D[3:0] PAD drive level select 00: 2mA 01: 4mA 10: 8mA 11: 12mA	RW	0
17:16	SD01_CLK_CMD	P_SD0_CLK, P_SD0_CMD, P_SD1_CLK, P_SD1_CMD PAD drive level select 00: 2mA 01: 4mA 10: 8mA 11: 12mA	RW	0
15:14	SPI0_ERAM_TWI3_PCM0	P_SPI0_SCLK, P_SPI0_MOSI PAD drive level select 00: 2mA	RW	0

		01: 4mA 10: 8mA 11: 12mA		
13:12	SPI0_ERAM_I2S_PCM01	P_SPI0_SS, P_SPI0_MISO PAD drive level select 00: 2mA 01: 4mA 10: 8mA 11: 12mA	RW	0
11:10	UART0	P_UART0_RX, P_UART0_TX PAD drive level select 00: 2mA 01: 4mA 10: 8mA 11: 12mA	RW	0
9:8	UART4	P_UART4_RX, P_UART4_TX PAD drive level select 00: 2mA 01: 4mA 10: 8mA 11: 12mA	RW	0
7:6	UART2	P_UART2_RX,P_UART2_TX,P_UART2_RTSB,P_UART2_CTSB PAD drive level select 00: 2mA 01: 4mA 10: 8mA 11: 12mA	RW	0
5:4	UART3	P_UART3_RX,P_UART3_TX,P_UART3_RTSB,P_UART3_CTSB PAD drive level select 00: 2mA 01: 4mA 10: 8mA 11: 12mA	RW	0
3:0	-	Reserved	-	-

5.7.3.32 PAD_DRV2

PAD Drive Capacity2 Select Register

Offset = 0x0088

Bits	Name	Description	Access	Reset
31:30	TWI01_UART12_SPI1	P_TWI0_SCLK,P_TWI0_SDATA PAD drive level select 00: 2mA 01: 4mA	RW	0

		10: 8mA 11: 12mA		
29:28	TWI1	P_TWI1_SCLK,P_TWI1_SDATA PAD drive level select 00: 2mA 01: 4mA 10: 8mA 11: 12mA	RW	0
27:26	TWI2	P_TWI2_SCLK,P_TWI2_SDATA PAD drive level select 00: 2mA 01: 4mA 10: 8mA 11: 12mA	RW	0
25:22	-	Reserved	-	-
21:20	PCLK_CKOUT	P_SENSOR0_PCLK, P_SENSOR0_CKOUT PAD drive level select 00: 2mA 01: 4mA 10: 8mA 11: 12mA	RW	0
19:0	-	Reserved	-	-

5.7.3.33 PAD_SR0

PAD slew rate control Register0

Offset = 0x270

Bits	Name	Description	Access	Reset
31:16	-	Reserved	-	-
15	SGPIO3	SGPIO3 PAD slew rate select 0: slow (half frequency) 1: fast	RW	1
14	SGPIO2	SGPIO2 PAD slew rate select 0: slow (half frequency) 1: fast	RW	1
13	SGPIO1	SGPIO1 PAD slew rate select 0: slow (half frequency) 1: fast	RW	1
12	SGPIO0	SGPIO0 PAD slew rate select 0: slow (half frequency) 1: fast	RW	1
11	RMII_TXD01	P_ETH_TXD0, P_ETH_TXD1 PAD slew rate select 0: slow (half frequency)	RW	1

		1: fast		
10	RMII_TXEN_RXER	P_ETH_TX_EN, P_ETH_RX_ER PAD slew rate select 0: slow (half frequency) 1: fast	RW	1
9	RMII_CRS_DV	P_ETH_CRS_DV PAD slew rate select 0: slow (half frequency) 1: fast	RW	1
8	RMII_RXD10	P_ETH_RXD1, P_ETH_RXD0 PAD slew rate select 0: slow (half frequency) 1: fast	RW	1
7	RMII_REF_CLK	P_ETH_REF_CLK PAD slew rate select 0: slow (half frequency) 1: fast	RW	1
6	RMII_MDC_MDIO	P_ETH_MDC, P_ETH_MDIO PAD slew rate select 0: slow (half frequency) 1: fast	RW	1
5	SIRQ01	P_SIRQ0, P_SIRQ1 PAD slew rate select 0: slow (half frequency) 1: fast	RW	1
4	SIRQ2	P_SIRQ2 PAD slew rate select 0: slow (half frequency) 1: fast	RW	1
3	I2S_D01	P_I2S_D0, P_I2S_D1 PAD slew rate select 0: slow (half frequency) 1: fast	RW	1
2	I2S_PCM1	P_I2S_LRCLK0, P_I2S_MCLK0 PAD slew rate select 0: slow (half frequency) 1: fast	RW	1
1	I2S_PCM0	P_I2S_BCLK0,P_I2S_BCLK1, P_I2S_LRCLK1, P_I2S_MCLK1 PAD slew rate select 0: slow (half frequency) 1: fast	RW	1
0	PCM1_SPI1_TWI3	P_PCM1_IN,P_PCM1_CLK, P_PCM1_SYNC, P_PCM1_OUT PAD slew rate select 0: slow (half frequency) 1: fast	RW	1

5.7.3.34 PAD_SR1

PAD slew rate control Register1

Offset = 0x274

Bits	Name	Description	Access	Reset
31:26	-	Reserved	-	-
25	SD1_ERAM	P_SD1_D[3:0] PAD slew rate select 0: slow (half frequency) 1: fast	RW	1
24	SD01_CLK_CMD	P_SD0_CLK, P_SD0_CMD, P_SD1_CLK, P_SD1_CMD PAD slew rate select 0: slow (half frequency) 1: fast	RW	1
23	SPI0_ERAM_TWI3_PCM0	P_SPI0_SCLK, P_SPI0_MOSI PAD slew rate select 0: slow (half frequency) 1: fast	RW	1
22	SPI0_ERAM_I2S_PCM01	P_SPI0_SS, P_SPI0_MISO PAD slew rate select 0: slow (half frequency) 1: fast	RW	1
21	UART0	P_UART0_RX, P_UART0_TX PAD slew rate select 0: slow (half frequency) 1: fast	RW	1
20	UART4	P_UART4_RX, P_UART4_TX PAD slew rate select 0: slow (half frequency) 1: fast	RW	1
19	UART2	P_UART2_RX,P_UART2_TX,P_UART2_RTSB,P_UART2_CTSB PAD slew rate select 0: slow (half frequency) 1: fast	RW	1
18	UART3	P_UART3_RX,P_UART3_TX,P_UART3_RTSB,P_UART3_CTSB PAD slew rate select 0: slow (half frequency) 1: fast	RW	1
17:0	-	Reserved	-	-

5.7.3.35 PAD_SR2

PAD slew rate control Register2

Offset = 0x278

Bits	Name	Description	Access	Reset

31	TWI01_UART12_SPI1	P_TWI0_SCLK,P_TWI0_SDATA PAD slew rate select 0: slow (half frequency) 1: fast	RW	1
30	TWI1	P_TWI1_SCLK,P_TWI1_SDATA PAD slew rate select 0: slow (half frequency) 1: fast	RW	1
29	TWI2	P_TWI2_SCLK,P_TWI2_SDATA PAD slew rate select 0: slow (half frequency) 1: fast	RW	1
28:26	-	Reserved	-	-
25	PCLK_CKOUT	P_SENSOR0_PCLK, P_SENSOR0_CKOUT PAD slew rate select 0: slow (half frequency) 1: fast	RW	1
24:0	-	Reserved	-	-

5.7.3.36 INTC_EXTCTL0

External Interrupt0 Control and Status Register (VDD)

Offset = 0x0200

Bits	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7:6	E0TYPE	External Interrupt 0 Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
5	E0EN	Enable external interrupt 0 (IRQ) 0 Disable 1 Enable	RW	0
4	SIRQ0_CLK_SEL	External Interrupt SIRQ0 sample Clk select 0: 32KHz 1: 24MHz	RW	0
3:1	-	Reserved	-	-
0	E0PD	External Interrupt 0 Pending 0 External interrupt source 0 is not active. 1 External interrupt source 0 is active. Write 1 to the bit will clear it. If external interrupt source 0 is edge-triggered, this bit must be cleared by software after detected.	RW	0

Note: External interrupt 0 is used in different trigger method settings, the P_SIRQ0 pull up and pull

down state should be set relatively, details refer to register PAD_PULLCTL0[17:16].

5.7.3.37 INTC_GPIOACTL

GPIOA Interrupt Type Control Register

Offset = 0x0204

Bits	Name	Description	Access	Reset
31:3	-	Reserved	-	-
2	GPIOA_CLK_SEL	GPIOA Interrupt sample Clk select 0: 32K 1: 24M	RW	0
1	GAEN	Enable GPIOA interrupt 0 Disable 1 Enable	RW	0
0	GAPD	GPIOA Interrupt Pending 0 GPIOA interrupt source is not active. 1 GPIOA interrupt source is active. Write 1 to the bit will clear it. If GPIOA is edge-triggered, this bit must be cleared by software after detected.	RW	0

5.7.3.38 INTC_GPIOA_PD

GPIOA Interrupt Pending Register (VDD)

Offset = 0x0208

Bits	Name	Description	Access	Reset
31:0	GPIOA_PD	Interrupt Pending bit. Interrupt num “n” accords to GPIOA number. 0: Interrupt source n request is not active 1: Interrupt source n request is active. Write 1 to the bit will clear it. If GPIOA is edge-triggered, this bit must be cleared by software after detected.	R	x

5.7.3.39 INTC_GPIOA_MSK

GPIOA Interrupt Mask Register (VDD)

Offset = 0x020C

Bits	Name	Description	Access	Reset
31:0	GPIOA_MSK	GPIOA Interrupt Mask bit. 0: Interrupt source n request is not active 1: Interrupt source n request is active.	RW	0

5.7.3.40 INTC_GPIOB_PD

GPIOB Interrupt Pending Register (VDD)

Offset = 0x0210

Bits	Name	Description	Access	Reset
31:0	GPIOB_PD	Interrupt Pending bit. Interrupt num “n” accords to GPIOB number. 0: Interrupt source n request is not active 1: Interrupt source n request is active. Write 1 to the bit will clear it. If GPIOB is edge-triggered, this bit must be cleared by software after detected.	R	x

5.7.3.41 INTC_GPIOB_MSK

GPIOB Interrupt Mask Register (VDD)

Offset = 0x0214

Bits	Name	Description	Access	Reset
31:0	GPIOB_MSK	GPIOB Interrupt Mask bit. 0: Interrupt source n request is not active 1: Interrupt source n request is active.	RW	0

5.7.3.42 INTC_GPIOC_PD

GPIOC Interrupt Pending Register (VDD)

Offset = 0x0218

Bits	Name	Description	Access	Reset
31:12	-	Reserved	-	-
11:0	GPIOC_PD	Interrupt Pending bit. Interrupt num “n” accords to GPIOC number. 0: Interrupt source n request is not active 1: Interrupt source n request is active. Write 1 to the bit will clear it. If GPIOC is edge-triggered, this bit must be cleared by software after detected.	R	x

5.7.3.43 INTC_GPIOC_MSK

GPIOC Interrupt Mask Register (VDD)

Offset = 0x021C

Bits	Name	Description	Access	Reset
31:12	-	Reserved	-	-

11:0	GPIOC_MSK	GPIOC Interrupt Mask bit. 0: Interrupt source n request is not active 1: Interrupt source n request is active.	RW	0

5.7.3.44 INTC_GPIOD_PD

GPIOD Interrupt Pending Register (VDD)

Offset = 0x0220

Bits	Name	Description	Access	Reset
31:30	-	Reserved	-	-
29:0	GPIOD_PD	Interrupt Pending bit. Interrupt num “n” accords to GPIOD number. 0: Interrupt source n request is not active 1: Interrupt source n request is active. Write 1 to the bit will clear it. If GPIOD is edge-triggered, this bit must be cleared by software after detected.	R	x

5.7.3.45 INTC_GPIOD_MSK

GPIOD Interrupt Mask Register (VDD)

Offset = 0x0224

Bits	Name	Description	Access	Reset
31:30	-	Reserved	-	-
29:0	GPIOD_MSK	GPIOD Interrupt Mask bit. 0: Interrupt source n request is not active 1: Interrupt source n request is active.	RW	0

5.7.3.46 INTC_GPIOE_PD

GPIOE Interrupt Pending Register (VDD)

Offset = 0x0228

Bits	Name	Description	Access	Reset
31:0	GPIOE_PD	Interrupt Pending bit. Interrupt num “n” accords to GPIOE number. 0: Interrupt source n request is not active 1: Interrupt source n request is active. Write 1 to the bit will clear it. If GPIOE is edge-triggered, this bit must be cleared by software after detected.	R	x

5.7.3.47 INTC_GPIOE_MSK

GPIOE Interrupt Mask Register (VDD)

Offset = 0x22c

Bits	Name	Description	Access	Reset
31:0	GPIOE_MSK	GPIOE Interrupt Mask bit. 0: Interrupt source n request is not active 1: Interrupt source n request is active.	RW	0

5.7.3.48 INTC_GPIOF_PD

GPIOF Interrupt Pending Register (VDD)

Offset = 0x230

Bits	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7:0	GPIOF_PD	Interrupt Pending bit. Interrupt num “n” accords to GPIOF number. 0: Interrupt source n request is not active 1: Interrupt source n request is active. Write 1 to the bit will clear it. If GPIOF is edge-triggered, this bit must be cleared by software after detected.	R	x

5.7.3.49 INTC_GPIOF_MSK

GPIOFInterrupt Mask Register (VDD)

Offset = 0x234

Bits	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7:0	GPIOF_MSK	GPIOF Interrupt Mask bit. 0: Interrupt source n request is not active 1: Interrupt source n request is active.	RW	0

5.7.3.50 INTC_GPIOA_TYPE0

GPIOA Interrupt Pending Register0 (VDD)

Offset = 0x0240

Bits	Name	Description	Access	Reset
31:30	GA31_TYPE	GPIOA31 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered.	RW	0

		11: Falling edge-triggered.		
29:28	GA30_TYPE	GPIOA30 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
27:26	GA29_TYPE	GPIOA29 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
25:24	GA28_TYPE	GPIOA28 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
23:22	GA27_TYPE	GPIOA27 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
21:20	GA26_TYPE	GPIOA26 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
19:18	GA25_TYPE	GPIOA25 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
17:16	GA24_TYPE	GPIOA24 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
15:14	GA23_TYPE	GPIOA23 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
13:12	GA22_TYPE	GPIOA22 Interrupt Type 00: High level active. 01: Low level active.	RW	0

		10: Rising edge-triggered. 11: Falling edge-triggered.		
11:10	GA21_TYPE	GPIOA21 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
9:8	GA20_TYPE	GPIOA20 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
7:6	GA19_TYPE	GPIOA19 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
5:4	GA18_TYPE	GPIOA18 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
3:2	GA17_TYPE	GPIOA17 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
1:0	GA16_TYPE	GPIOA16 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0

5.7.3.51 INTC_GPIOA_TYPE1

GPIOA Interrupt Pending Register1 (VDD)

Offset = 0x0244

Bits	Name	Description	Access	Reset
31:30	GA15_TYPE	GPIOA15 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
29:28	GA14_TYPE	GPIOA14 Interrupt Type	RW	0

		00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.		
27:26	GA13_TYPE	GPIOA13 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
25:24	GA12_TYPE	GPIOA12 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
23:22	GA11_TYPE	GPIOA11 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
21:20	GA10_TYPE	GPIOA10 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
19:18	GA9_TYPE	GPIOA9 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
17:16	GA8_TYPE	GPIOA8 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
15:14	GA7_TYPE	GPIOA7 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
13:12	GA6_TYPE	GPIOA6 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0

11:10	GA5_TYPE	GPIOA5 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
9:8	GA4_TYPE	GPIOA4 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
7:6	GA3_TYPE	GPIOA3 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
5:4	GA2_TYPE	GPIOA2 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
3:2	GA1_TYPE	GPIOA1 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
1:0	GA0_TYPE	GPIOA0 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0

5.7.3.52 INTC_GPIOB_TYPE0

GPIOB Interrupt Pending Register0 (VDD)

Offset = 0x0248

Bits	Name	Description	Access	Reset
31:30	GB31_TYPE	GPIOB31 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
29:28	GB30_TYPE	GPIOB30 Interrupt Type 00: High level active. 01: Low level active.	RW	0

		10: Rising edge-triggered. 11: Falling edge-triggered.		
27:26	GB29_TYPE	GPIOB29 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
25:24	GB28_TYPE	GPIOB28 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
23:22	GB27_TYPE	GPIOB27 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
21:20	GB26_TYPE	GPIOB26 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
19:18	GB25_TYPE	GPIOB25 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
17:16	GB24_TYPE	GPIOB24 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
15:14	GB23_TYPE	GPIOB23 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
13:12	GB22_TYPE	GPIOB22 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
11:10	GB21_TYPE	GPIOB21 Interrupt Type 00: High level active.	RW	0

		01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.		
9:8	GB20_TYPE	GPIOB20 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
7:6	GB19_TYPE	GPIOB19 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
5:4	GB18_TYPE	GPIOB18 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
3:2	GB17_TYPE	GPIOB17 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
1:0	GB16_TYPE	GPIOB16 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0

5.7.3.53 INTC_GPIOB_TYPE1

GPIOB Interrupt Pending Register1 (VDD)

Offset = 0x024C

Bits	Name	Description	Access	Reset
31:30	GB15_TYPE	GPIOB15 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
29:28	GB14_TYPE	GPIOB14 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0

27:26	GB13_TYPE	GPIOB13 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
25:24	GB12_TYPE	GPIOB12 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
23:22	GB11_TYPE	GPIOB11 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
21:20	GB10_TYPE	GPIOB10 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
19:18	GB9_TYPE	GPIOB9 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
17:16	GB8_TYPE	GPIOB8 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
15:14	GB7_TYPE	GPIOB7 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
13:12	GB6_TYPE	GPIOB6 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
11:10	GB5_TYPE	GPIOB5 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered.	RW	0

		11: Falling edge-triggered.		
9:8	GB4_TYPE	GPIOB4 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
7:6	GB3_TYPE	GPIOB3 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
5:4	GB2_TYPE	GPIOB2 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
3:2	GB1_TYPE	GPIOB1 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
1:0	GB0_TYPE	GPIOB0 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0

5.7.3.54 INTC_GPIOC_TYPE

GPIOC Interrupt Pending Register (VDD)

Offset = 0x0254

Bits	Name	Description	Access	Reset
31:24	-	Reserved	-	-
23:22	GC11_TYPE	GPIOC11 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
21:20	GC10_TYPE	GPIOC10 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
19:18	GC9_TYPE	GPIOC9 Interrupt Type	RW	0

		00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.		
17:16	GC8_TYPE	GPIOC8 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
15:14	GC7_TYPE	GPIOC7 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
13:12	GC6_TYPE	GPIOC6 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
11:10	GC5_TYPE	GPIOC5 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
9:8	GC4_TYPE	GPIOC4 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
7:6	GC3_TYPE	GPIOC3 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
5:4	GC2_TYPE	GPIOC2 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
3:2	GC1_TYPE	GPIOC1 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0

1:0	GC0_TYPE	GPIOC0 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0

5.7.3.55 INTC_GPIOD_TYPE0

GPIOD Interrupt Pending Register0 (VDD)

Offset = 0x0258

Bits	Name	Description	Access	Reset
31:28	-	Reserved	-	-
27:26	GD29_TYPE	GPIOD29 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
25:24	GD28_TYPE	GPIOD28 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
23:22	GD27_TYPE	GPIOD27 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
21:20	GD26_TYPE	GPIOD26 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
19:18	GD25_TYPE	GPIOD25 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
17:16	GD24_TYPE	GPIOD24 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
15:14	GD23_TYPE	GPIOD23 Interrupt Type 00: High level active.	RW	0

		01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.		
13:12	GD22_TYPE	GPIOD22 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
11:10	GD21_TYPE	GPIOD21 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
9:8	GD20_TYPE	GPIOD20 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
7:6	GD19_TYPE	GPIOD19 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
5:4	GD18_TYPE	GPIOD18 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
3:2	GD17_TYPE	GPIOD17 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
1:0	GD16_TYPE	GPIOD16 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0

5.7.3.56 INTC_GPIOD_TYPE1

GPIOD Interrupt Pending Register1 (VDD)

Offset = 0x025C

Bits	Name	Description	Access	Reset

31:30	GD15_TYPE	GPIOD15 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
29:28	GD14_TYPE	GPIOD14 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
27:26	GD13_TYPE	GPIOD13 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
25:24	GD12_TYPE	GPIOD12 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
23:22	GD11_TYPE	GPIOD11 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
21:20	GD10_TYPE	GPIOD10 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
19:18	GD9_TYPE	GPIOD9 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
17:16	GD8_TYPE	GPIOD8 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
15:14	GD7_TYPE	GPIOD7 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered.	RW	0

		11: Falling edge-triggered.		
13:12	GD6_TYPE	GPIOD6 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
11:10	GD5_TYPE	GPIOD5 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
9:8	GD4_TYPE	GPIOD4 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
7:6	GD3_TYPE	GPIOD3 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
5:4	GD2_TYPE	GPIOD2 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
3:2	GD1_TYPE	GPIOD1 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
1:0	GD0_TYPE	GPIOD0 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0

5.7.3.57 INTC_GPIOE_TYPE0

GPIOE Interrupt Pending Register0 (VDD)

Offset = 0x0260

Bits	Name	Description	Access	Reset
31:30	GE15_TYPE	GPIOE15 Interrupt Type 00: High level active.	RW	0

		01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.		
29:28	GE14_TYPE	GPIOE14 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
27:26	GE13_TYPE	GPIOE13 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
25:24	GE12_TYPE	GPIOE12 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
23:22	GE11_TYPE	GPIOE11 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
21:20	GE10_TYPE	GPIOE10 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
19:18	GE9_TYPE	GPIOE9 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
17:16	GE8_TYPE	GPIOE8 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
15:14	GE7_TYPE	GPIOE7 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
13:12	GE6_TYPE	GPIOE6 Interrupt Type	RW	0

		00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.		
11:10	GE5_TYPE	GPIOE5 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
9:8	GE4_TYPE	GPIOE4 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
7:6	GE3_TYPE	GPIOE3 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
5:4	GE2_TYPE	GPIOE2 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
3:2	GE1_TYPE	GPIOE1 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
1:0	GE0_TYPE	GPIOE0 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0

5.7.3.58 INTC_GPIOE_TYPE1

GPIOE Interrupt Pending Register1 (VDD)

Offset = 0x0264

Bits	Name	Description	Access	Reset
31:30	GE31_TYPE	GPIOE31 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered.	RW	0

		11: Falling edge-triggered.		
29:28	GE30_TYPE	GPIOE30 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
27:26	GE29_TYPE	GPIOE29 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
25:24	GE28_TYPE	GPIOE28 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
23:22	GE27_TYPE	GPIOE27 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
21:20	GE26_TYPE	GPIOE26 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
19:18	GE25_TYPE	GPIOE25 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
17:16	GE24_TYPE	GPIOE24 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
15:14	GE23_TYPE	GPIOE23 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
13:12	GE22_TYPE	GPIOE22 Interrupt Type 00: High level active. 01: Low level active.	RW	0

		10: Rising edge-triggered. 11: Falling edge-triggered.		
11:10	GE21_TYPE	GPIOE21 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
9:8	GE20_TYPE	GPIOE20 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
7:6	GE19_TYPE	GPIOE19 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
5:4	GE18_TYPE	GPIOE18 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
3:2	GE17_TYPE	GPIOE17 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
1:0	GE16_TYPE	GPIOE16 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0

5.7.3.59 INTC_GPIOF_TYPE

GPIOF Interrupt Pending Register (VDD)

Offset = 0x0268

Bits	Name	Description	Access	Reset
15:14	GF7_TYPE	GPIOF7 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
13:12	GF6_TYPE	GPIOF6 Interrupt Type	RW	0

		00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.		
11:10	GF5_TYPE	GPIOF5 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
9:8	GF4_TYPE	GPIOF4 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
7:6	GF3_TYPE	GPIOF3 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
5:4	GF2_TYPE	GPIOF2 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
3:2	GF1_TYPE	GPIOF1 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
1:0	GF0_TYPE	GPIOF0 Interrupt Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0

5.7.3.60 SGPIO_OUTEN

SGPIO Output Enable Register

Offset = 0x500

Bits	Name	Description	Access	Reset
31	ISO_EN	Cpu_2_Core power domain isolation enable 0: isolation disable 1: isolation enable *Note:*	RW	0

		1.in isolation disable mode in default *2.only need to set the value, when external DC-DC controls the CPU_VDD* *3.only effect the CPU_VDD power down process, not the isolation of power on process.*		
30:4	-	Reserved	-	-
3:0	SGPIO_OUTEN	SGPIO[3:0] Output Enable 0: Disable 1: Enable	RW	0

5.7.3.61 SGPIO_INEN

SGPIO Input Enable Register

Offset = 0x504

Bits	Name	Description	Access	Reset
31:4	-	Reserved	-	-
3:0	SGPIO_INEN	SGPIO[3:0] Input Enable. 0: Disable 1: Enable	RW	0

5.7.3.62 SGPIO_DAT

SGPIO Data Register

Offset = 0x508

Bits	Name	Description	Access	Reset
31:4	-	Reserved	-	-
3:0	SGPIO_DAT	SGPIO[3:0] Input/Output Data.	RW	0

5.7.3.63 SGPIO_PD

SGPIO wake-up input Pending Register

Offset = 0x50C

Bits	Name	Description	Access	Reset
31:4	-	Reserved	-	-
3:0	SGPIO[3:0]_PD	SGPIO[3:0] wake-up input Pending bit. 0: wake-up input is not active 1: wake-up input is active. *Note: This register is Only for wake-up mode, Write 1 to clear it.*	RW	0

5.7.3.64 SGPIO_PD_MSK

SGPIO wake-up input Pending mask Register

Offset = 0x510

Bits	Name	Description	Access	Reset
31:4	-	Reserved	-	-
3:0	SGPIO[3:0]_MSK	SGPIO[3:0] wake-up input Pending mask control bit. 0:wake-up input Pending is not active 1:wake-up input Pending is active *Note: This register is Only for wake-up mode*	RW	0

5.7.3.65 SGPIO_CTL

SGPIO Control Register

Offset = 0x514

Bits	Name	Description	Access	Reset
31:24	-	Reserved	-	-
23	SGPIO3_CLK_SEL	SGPIO3 sample Clk select, only for WAKE-UP mode 0: 32KHz 1: 24MHz	RW	0
22	SGPIO2_CLK_SEL	SGPIO2 sample Clk select, only for WAKE-UP mode 0: 32KHz 1: 24MHz	RW	0
21	SGPIO1_CLK_SEL	SGPIO1 sample Clk select, only for WAKE-UP mode 0: 32KHz 1: 24MHz	RW	0
20	SGPIO0_CLK_SEL	SGPIO0 sample Clk select, only for WAKE-UP mode 0: 32KHz 1: 24MHz	RW	0
19	SGPIO3_OUTPUT_LEVEL	SGPIO3 output level select 0:LOW level 1:HIGH level	RW	0
18	SGPIO2_OUTPUT_LEVEL	SGPIO2 output level select 0:LOW level 1:HIGH level	RW	0
17	SGPIO1_OUTPUT_LEVEL	SGPIO1 output level select 0:LOW level	RW	0

		1:HIGH level		
16	SGPIO0_OUTPUT_LEVEL	SGPIO0 output level select 0:LOW level 1:HIGH level *Note: this bit should be set, only when SGPIO0 is set to WAKEUP mode and SGPIO0 output is enabled, same with SGPIO1/2/3.*	RW	0
15	SGPIO3_MODE_SEL	0:WAKE-UP mode 1:NORMAL mode In normal mode, SGPIO3 act as normal GPIO	RW	0
14	SGPIO2_MODE_SEL	0:WAKE-UP mode 1:NORMAL mode In normal mode, SGPIO2 act as normal GPIO	RW	0
13	SGPIO1_MODE_SEL	0:WAKE-UP mode 1:NORMAL mode In normal mode, SGPIO1 act as normal GPIO	RW	0
12	SGPIO0_MODE_SEL	0:WAKE-UP mode 1:NORMAL mode In normal mode, SGPIO0 act as normal GPIO	RW	0
11:10	SGPIO3_INPUT_TYPE	SGPIO3 wake-up type select 00: High level 01: Low level 10: Rising edge 11: Falling edge	RW	0
9:8	SGPIO2_INPUT_TYPE	SGPIO2 wake-up type select 00: High level 01: Low level 10: Rising edge 11: Falling edge	RW	0
7:6	SGPIO1_INPUT_TYPE	SGPIO1 wake-up type select 00: High level 01: Low level 10: Rising edge 11: Falling edge	RW	0
5:4	SGPIO0_INPUT_TYPE	SGPIO0 wake-up type select 00: High level 01: Low level 10: Rising edge 11: Falling edge	RW	0

		Note: this bit should be set, only when SGPIO0 is set to WAKEUP mode and SGPIO0 output is enabled, same with SGPIO1/2/3.		
3	USB3	USB3 IRQ input control 0:Input disable 1:Input enable	RW	0
2	USB2H0	USB2H0 IRQ input control 0:Input disable 1:Input enable	RW	0
1	USB2H1	USB2H1IRQ input control 0:Input disable 1:Input enable	RW	0
0	-	Reserved	-	-

5.7.3.66 SGPIO_MFP

SGPIO Multiplexing Control Register

Offset = 0x518

Bits	Name	Description	Access	Reset
31:1	-	Reserved	-	-
0	SGPIO23_TWI5	SGPIO2, SGPIO3 PAD multiplex select. 0:SGPIO2, SGPIO3 1:TWI5_SCLK, TWI5_SDATA	RW	0

5.7.3.67 PWM_CTL4

PWM4 Output Control Register

Offset = 0x0520

Bits	Name	Description	Access	Reset
31:29	-	Reserved	-	-
28:19	DUTY	Duty select: 0: Duty =0 1: Duty =1 2: Duty =2 … 63: Duty =63 … 1023: Duty =1023 T active = (DUTY+1) /DIV	RW	0
18:9	DIV	DIV select: 0: reserved	RW	0x3F

		1: DIV=2 2: DIV=3 … 63: DIV=64 (default value) … 1023: DIV=1024		
8	POL_SEL	Polarity select 0:PWM low voltage level active 1:PWM high voltage level active	RW	0
7:0	-	Reserved	-	-

5.7.3.68 PWM_CTL5

PWM5 Output Control Register

Offset = 0x0524

Bits	Name	Description	Access	Reset
31:29	-	Reserved	-	-
28:19	DUTY	Duty select: 0: Duty =0 1: Duty =1 2: Duty =2 … 63: Duty =63 … 1023: Duty =1023 T active = (DUTY+1) /DIV	RW	0
18:9	DIV	DIV select: 0: reserved 1: DIV=2 2: DIV=3 … 63: DIV=64 (default value) … 1023: DIV=1024	RW	0x3F
8	POL_SEL	Polarity select 0:PWM low voltage level active 1:PWM high voltage level active	RW	0
7:0	-	Reserved	-	-

5.7.3.69 INTC_EXTCTL1

External Interrupt1 Control and Status Register (VDD)

Offset = 0x0528

Bits	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7:6	E1TYPE	External Interrupt 1 Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
5	E1EN	Enable external interrupt 1 (IRQ) 0 Disable 1 Enable	RW	0
4	SIRQ1_CLK_SEL	External Interrupt SIRQ1 sample Clk select 0: 32KHz 1: 24MHz	RW	0
3:1	-	Reserved	-	-
0	E1PD	External Interrupt 1 Pending 0 External interrupt source 1 is not active. 1 External interrupt source 1 is active. Write 1 to the bit will clear it. If external interrupt source 1 is edge-triggered, this bit must be cleared by software after detected.	RW	0

Note: external interrupt 1 when used in different trigger method settings, the P_SIRQ1 pull up and pull down should be set relatively, details refer to register PAD_PULLCTL0[15:14]

5.7.3.70 INTC_EXTCTL2

External Interrupt2 Control and Status Register (VDD)

Offset = 0x052C

Bits	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7:6	E2TYPE	External Interrupt 2 Type 00: High level active. 01: Low level active. 10: Rising edge-triggered. 11: Falling edge-triggered.	RW	0
5	E2EN	Enable external interrupt 2 (IRQ) 0 Disable 1 Enable	RW	0
4	SIRQ2_CLK_SEL	External Interrupt SIRQ2 sample Clk select 0: 32K	RW	0

		1: 24M		
3:1	-	Reserved	-	-
0	E2PD	External Interrupt 2 Pending 0 External interrupt source 2 is not active. 1 External interrupt source 2 is active. Write 1 to the bit will clear it. If external interrupt source 2 is edge-triggered, this bit must be cleared by software after detected.	RW	0

Note: external interrupt 2 when used in different trigger method settings, the P_SIRQ2 pull up and pull down should be set relatively, details refer to register PAD_PULLCTL0[13:12]

5.7.3.71 INTC_GPIOBCTL

GPIOB Interrupt Type Control Register
Offset = 0x0540

Bits	Name	Description	Access	Reset
31:3	-	Reserved	-	-
2	GPIOB_CLK_SEL	GPIOB Interrupt sample Clk select 0: 32K 1: 24M	RW	0
1	GBEN	Enable GPIOB interrupt 0 Disable 1 Enable	RW	0
0	GBPD	GPIOB Interrupt Pending 0 GPIOB interrupt source is not active. 1 GPIOB interrupt source is active. Write 1 to the bit will clear it. If GPIOB is edge-triggered, this bit must be cleared by software after detected.	RW	0

5.7.3.72 INTC_GPIOCCTL

GPIOC Interrupt Type Control Register
Offset = 0x0544

Bits	Name	Description	Access	Reset
31:3	-	Reserved	-	-
2	GPIOC_CLK_SEL	GPIOC Interrupt sample Clk select 0: 32K 1: 24M	RW	0
1	GCEN	Enable GPIOC interrupt 0 Disable	RW	0

		1 Enable		
0	GCPD	GPIOC Interrupt Pending 0 GPIOC interrupt source is not active. 1 GPIOC interrupt source is active. Write 1 to the bit will clear it. If GPIOC is edge-triggered, this bit must be cleared by software after detected.	RW	0

5.7.3.73 INTC_GPIODCTL

GPIOD Interrupt Type Control Register

Offset = 0x0548

Bits	Name	Description	Access	Reset
31:3	-	Reserved	-	-
2	GPIOD_CLK_SEL	GPIOD Interrupt sample Clk select 0: 32K 1: 24M	RW	0
1	GDEN	Enable GPIOD interrupt 0 Disable 1 Enable	RW	0
0	GDPD	GPIOD Interrupt Pending 0 GPIOD interrupt source is not active. 1 GPIOD interrupt source is active. Write 1 to the bit will clear it. If GPIOD is edge-triggered, this bit must be cleared by software after detected.	RW	0

5.7.3.74 INTC_GPIOECTL

GPIOE Interrupt Type Control Register

Offset = 0x054C

Bits	Name	Description	Access	Reset
31:3	-	Reserved	-	-
2	GPIOE_CLK_SEL	GPIOE Interrupt sample Clk select 0: 32K 1: 24M	RW	0
1	GEEN	Enable GPIOE interrupt 0 Disable 1 Enable	RW	0
0	GEPD	GPIOE Interrupt Pending 0 GPIOE interrupt source is not active. 1 GPIOE interrupt source is active. Write 1 to the bit will clear it. If GPIOE	RW	0

		is edge-triggered, this bit must be cleared by software after detected.		

5.7.3.75 INTC_GPIOFCTL

GPIOF Interrupt Type Control Register

Offset = 0x0550

Bits	Name	Description	Access	Reset
31:3	-	Reserved	-	-
2	GPIOF_CLK_SEL	GPIOF Interrupt sample Clk select 0: 32K 1: 24M	RW	0
1	GFEN	Enable GPIOF interrupt 0 Disable 1 Enable	RW	0
0	GFPD	GPIOF Interrupt Pending 0 GPIOF interrupt source is not active. 1 GPIOF interrupt source is active. Write 1 to the bit will clear it. If GPIOF is edge-triggered, this bit must be cleared by software after detected.	RW	0

Appendix Acronyms and Terms

ADC	Analog-to-Digital Converter
AHB	Advanced High-Performance Bus
ALE	Address-Locked Enable
APB	Advanced Peripheral Bus
BISP	Basic Image Signal Processor
BIST	Built-in Self-Test
CLE	Command-Locked Enable
CMU	Clock Management Unit
CP0	System Control Coprocessor
CRC	Cyclic Redundancy Check
CVBS	Composite Video Broadcasting Signal
DAC	Digital-to-Analog Converter
DB	Decibel
DC	Direct Current
DMA	Direct Memory RW
DSP	Digital Signal Processing
DVB	Digital Video Broadcasting
DVFS	Dynamic Voltage Frequency Scaling
EAV	End of Active Video
ECC	Error Correct Code
FIR	Fast Infrared
GPIO	General-Purpose Input/Output
I2S	Inter-IC Sound
IF	Interface
IR	Infrared
IrDA	Infrared Data Association
IRQ	Interrupt Request
JPEG	Joint Photographic Experts Group
LCD	Liquid Crystal Display
LCDC	Liquid Crystal Display Controller
Li-Ion	Lithium Ion (battery type)
LRADC	Low Resolution ADC
MAC	Multiplier Accumulator Control
MIPS	Million Instructions per Second
MIR	Mid Infrared
MJPEG	Motion JPEG
MLC	Multi-level Cell
MMC	Multimedia Card
MMU	Memory Management Unit
MPEG	Motion Picture Expert Group

MS	Memory stick card
NTSC	National Television Standards Committee
OLED	Polymer Light-Emitting Diode
OS	Operation System
PA	Power Amplifier
PAL	Phase Alteration Line
PFM	Pulse Frequency Modulation
PLL	Phase-Locked Loop
PMU	Power Management Unit
PWM	Pulse Width Modulation
RISC	Reduced Instruction Set Computing
RTC	Real-Time Clock
SAV	Start of Active Video
SD	Secure Digital memory card
SIR	Slow Infrared
SLC	Single-Level Cell
SMC	State Machine Controller
SoC	System on Chip
SPEC	Specification
SPI	Serial Peripheral Interface
SPRAM	Scratch Pad RAM
SW	Software
TFT	Thin Film Transistor
THD	Total Harmonic Distortion
TLB	Translation Look-aside Buffer
TS	Transport Stream
TWI	Two wire interface
UART	Universal Asynchronous Receiver Transmitter
WMA	Windows Media Audio
WMV	Windows Media Video

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