2.5

## Sylhet Engineering College,Sylhet

## Department of Computer Science and Engineering

3rd year 1st Semester | Term Test-01

Course No: CSE-503 | Course Title:Computer Architecture

Time:20 min | Total marks: 10

Q1. What is Instruction Format? Let $x = \frac{A+B*C}{(D-E*F+G*H)}$ Show the equation in three address and zero address format. 7

Q2. What is Addressing modes? Write the names of Addressing modes 3

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Computer Architecture

Term Test 1

Time: 30 min

Total Marks: 10

1. What are the different classes of computers? 2

2. If computer A runs a program in 10 seconds and computer B runs the same program in 30 seconds, how much faster is A than B? 3

3. Rewrite the code written in C given below using MIPS instructions. 5

```
for(i=1; i<10; )
        i = i + 1;
```

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# Sylhet Engineering College, Sylhet

(Shahjalal University of Science & Technology)

Department of Computer Science & Engineering

Final Examination, 2019

Course No: CSE 503

Time: 03 (Three) hours

3rd year 1st Semester

Course Title: Computer Architecture

Full Marks: 70

N.B. : (i) Answer any two question from each PART (ii) Use separate answer scripts for each PART

(iii) Marks allotted are indicated in the margin(iv) Special Instruction (if any)----------N/A----------

## PART-A

(Answer any twoquestions)

1. (a) What are the basic functional units of a computer? 3.5

(b) Explain in detail the various addressing modes of Central Processing Unit. 05

(c) Define Instruction format. Classify Instruction format with example. 04

(d) List and explain the steps involved in the execution of a complete instruction? 05

2. (a) What is Control Unit? 01

(b) Describe micro programmed control and hardware control circuit design. 10

(c) What is the final content of Register R at the end of the following Assembly Language code? 03

```
MOVE  R,E7H
CSR   R
ASR   R
CSL   R
AND   R,F0H
HLT
```

0011
1010
1101

0001011

(d) Define with example: (i) Throughput (ii) CPU execution time (iii) CPI 3.5

3. (a) (-6)*(4)=(-24) for this equation show the tracing table and draw the flowchart of signed multiplication using Booth's Algorithm. 10

(b) What is data dependency? Consider the following Assembly Language 4.5

```
LOAD  R1,A
ADD   R2,R1
MOVE  R1,R3
STORE B,R1
```

1001
1
1010

Show the dependency graph for this Assembly Language.

(c) How unsigned and signed number represent in memory? 03

## PART-B

(Answer any two questions)

4. (a) What is an instruction Cycle? 2.5

(b) Explain the basic organization of a microprogrammed control unit and the generation of control signals using microprogram. 06

(c) What is the difference between serial and parallel processing? 04

(d) What is the difference between direct and indirect addressing? How many memory [illegible] are required in both the cases? 05

5. (a) Discuss about instruction execution in non-pipeline and pipeline architecture. 05

(b) Describe and find the equation of (i) Speed up ratio($S_p$), (ii) Frequency (f), (iii) Efficiency($E_f$), (iv) Throughput ($H_p$) [illegible] pipeline and nonpipeline architecture 08

(c) How does CPU [illegible] work and what [illegible] 4.5

6. (a) What is RISC and CISC architecture [illegible] difference between RISC and CISC architecture 05

(b) Write the algorithm [illegible] division algorithm using Restoring Method 7.5

(c) What is virtual memory? Write the [illegible] of virtual memory 05

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# Sylhet Engineering College, Sylhet
(Shahjalal University of Science & Technology)
Department of Computer Science & Engineering

**Final Examination, 2018** — 3rd year 1st Semester
**Course No: CSE503** — **Course Title: Computer Architecture**
**Time: 03 (Three) hours** — **Full Marks: 70**

N.B. : (i) Answer any two question from each PART (ii) Use separate answer scripts for each PART
(iii) Marks allotted are indicated in the margin (iv) Special Instruction (if any)----------N/A----------

## PART-A
(Answer any two questions)

1. (a) What are the different classes of computers? 02
(b) Define embedded computer system with example. 1.5
(c) "Performance of a computer while running an application depends on the algorithm of the software." – Justify the answer. 03
(d) Define response time and throughput. 03
(e) If computer A runs a program in 20 seconds and computer B runs the same program in 60 seconds, how much faster is A than B? 04
(f) A given application written in Java runs 15 seconds on a desktop processor. A new java compiler is released that requires only 0.6 as many instructions as the old compiler. Unfortunately it increases the CPI by 1.1. How fast can we expect the application to run using this new compiler? 04

2. (a) Give example of five operators available in MIPS assembly language. 2.5
(b) Write down the four design principles of hardware design. 04
(c) Give an example of an assembly instruction that will represent one significance of $zero register. 01
(d) Write down the steps required for procedure calling. 05
(e) Rewrite the code written in C given below using MIPS instructions. 05

```
For(i=1; i<10)
    i=i+1;
```

Assume that the variable i is available in the register $s1

3. (a) What is an Instruction Cycle? 2.5
(b) Explain the basic organization of a microprogrammed control unit and the generation of control signals using microprogram. 06
(c) What is the difference between serial and parallel processing? 04
(d) What is the difference between direct and indirect addressing? How many memory References are required in both the cases? 05

## PART-B
(Answer any two questions)

4. (a) Multiply 0011 by 0101. Show all the steps according to the normal multiplication algorithm. 06
(b) What are the purposes of mfhi and mflo instructions? 02
(c) Present -0.75 using single and double precision binary representation. 05
(d) Showing all the steps perform addition between pairs given below 4.5
(i) $9.999 \times 10^{1} + 1.610 \times 10^{-1}$
(ii) $9.999 \times 10^{3} + 1.610 \times 10^{-5}$
(iii) $1.6567 \times 10^{-5} + 2.257 \times 10^{-3}$

5. (a) What are the purpose of the register $ra, $v0 and $a0? 1.5
(b) Show the structure of MIPS I-format and R-format instructions. 04
(c) What is the purpose of sign extension? Give example. 02
(d) In which cases overflow may happen for both addition and subtraction? 05
(e) Draw a diagram of the first version of the multiplication hardware. 05

6. (a) What is Inter processor communication? 2.5
(b) What do you understand by Instruction Pipeline? Mention the stages of Pipeline. 05
(c) What are the disadvantages of increasing the number of stages in pipelined processing? 05
(d) Distinguish between isolated and memory mapped I/O. 05

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# Sylhet Engineering College, Sylhet
## (Shahjalal University of Science & Technology)
## Department of Computer Science & Engineering

**Final Examination, 2018** — **3rd year 1st Semester**
**Course No: CSE503** — **Course Title: Computer Architecture**
**Time: 03 (Three) hours** — **Full Marks: 70**

N.B. : (i) Answer any two question from each PART (ii) Use separate answer scripts for each PART
(iii) Marks allotted are indicated in the margin (iv) Special Instruction (if any)----------N/A----------

## PART-A
(Answer any two questions)

1. (a) What are the different classes of computers? 02
   (b) Define embedded computer system with example. 1.5
   (c) "Performance of a computer while running an application depends on the algorithm of the software." – Justify the answer. 03
   (d) Define response time and throughput. 03
   (e) If computer A runs a program in 20 seconds and computer B runs the same program in 60 seconds, how much faster is A than B? 04
   (f) A given application written in Java runs 15 seconds on a desktop processor. A new java compiler is released that requires only 0.6 as many instructions as the old compiler. Unfortunately it increases the CPI by 1.1. How fast can we expect the application to run using this new compiler? 04

2. (a) Give example of five operators available in MIPS assembly language. 2.5
   (b) Write down the four design principles of hardware design. 04
   (c) Give an example of an assembly instruction that will represent one significance of $zero register. 01
   (d) Write down the steps required for procedure calling. 05
   (e) Rewrite the code written in C given below using MIPS instructions. 05

```
For(i=1; i<10)
    i=i+i;
```

Assume that the variable i is available in the register $s1

3. (a) What is an Instruction Cycle? 2.5
   (b) Explain the basic organization of a microprogrammed control unit and the generation of control signals using microprogram. 06
   (c) What is the difference between serial and parallel processing? 04
   (d) What is the difference between direct and indirect addressing? How many memory References are required in both the cases? 05

## PART-B
(Answer any two questions)

paper-pencil method ?

4. (a) Multiply 0011 by 0101. Show all the steps according to the normal multiplication algorithm. 06
   (b) What are the purposes of mfhi and mflo instructions? 02
   (c) Present -0.75 using single and double precision binary representation. 05
   (d) Showing all the steps perform addition between pairs given below 4.5
   (i) $9.999 \times 10^{1} + 1.610 \times 10^{-1}$
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   (d) In which cases overflow may happen for both addition and subtraction? 05
   (e) Draw a diagram of the first version of the multiplication hardware. 05

6. (a) What is Inter processor communication? 2.5
   (b) What do you understand by Instruction Pipeline? Mention the stages of Pipeline. 05
   (c) What are the disadvantages of increasing the number of stages in pipelined processing? 05
   (d) Distinguish between isolated and memory mapped I/O. 05

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# Sylhet Engineering College, Sylhet

## 3rd year 1st Semester Final Examination – 2017

### Department of Computer Science & Engineering

**Course No: CSE 503**

**Course Title: Computer Architecture**

**Time: 3.00 Hours** **Total Marks: 70**

[Answer any **four** questions taking **two** from each part]

## PART - A

1.a) Illustrate execution cycle of CPU instructions. 3.5

b) Show the binary representation of $13.75_{10}$ in Double Precision. 4

c) Translate the following HLL code into MIPS Assembly code 10

```
void orderSequence(int v[], int n){
int i, j;
     for (i = 0; i < n; i += 1) {
     for (j = i - 1; j >= 0 && v[j] > v[j + 1]; j =1) {
     interChange(v,j);
         }
       }
     }
     void interChange(int v[], int k){
     int temp;
     temp = v[k];
     v[k] = v[k+1];
     v[k+1] = temp;
     }
```

2.a) What is SISD and MISD? 2

b) Write short notes on: activation record, hardware multithreading. 3

c) Simulate the division of $13_{10}$ by $5_{10}$ using hardware division algorithm. 6

d) Depict the flowchart of Floating-point multiplication. 5

e) State Amdahl's Law. 1.5

3.a) Sketch the simple datapath for the core MIPS architecture. 6

b) Multiply decimal numbers in scientific notation by hand: 1.11010 x1010 and 9.2010 x10-5. Assume that you can store only four digits of the significand and two digits of the exponent. 5

c) Describe the steps that transform a program written in a high-level language into a representation that is directly executed by a computer processor. 2.5

d) Consider the following MIPS code segment, assuming all variables are in memory and are addressable as offsets from $t0: 4

```
lw $t1, 0($t0)
lw $t2, 4($t0)
add $t3, $t1,$t2
sw $t3, 12($t0)
lw $t4, 8($t0)
add $t5, $t1,$t4
sw $t5, 16($t0)
```

Find the hazards in the preceding code segment and reorder the instructions to avoid any pipeline stalls.

## PART - B

4.a) Define clusters. Depict the classic organization of a multiprocessor. 5

b) Suppose we have two implementations of the same instruction set architecture. Computer A has a clock cycle time of 250ps and a CPI of 2.0 for some program, and computer B has a clock cycle time of 500ps and a CPI of 1.2 for the same program, which computer is faster and by how much? 5

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c) Describe stack allocation 2.5

d) Translate the HLL code below to MIPS assembly. Every instruction should have a comment! 5

HLL Code:

```
if (i==j) {


    a[i]=b[j];
}
else {
     a[i]     =
b[j+1];
}
```

Assume the following
The starting address of array `a[]` is in $20
The starting address of array `b[]` is in $21
Index `i` maps to $5
Index `j` maps to $6
If any temporary registers are used, please start with $10

[Complete the question with 10 instructions or less]

5.a) Suppose you want to perform two sums: one is a sum of 10 scalar variables, and one is a matrix sum of a pair of two-dimensional arrays, with dimensions 10 by 10. For now let's assume only the matrix sum is parallelizable; we'll see soon how to parallelize scalar sums. What speed-up do you get with 10 versus 40 processors? Next, calculate the speed-ups assuming the matrices grow to 20 by 20. 5

b) What is the MIPS assembly code to load this 32-bit constant into register $s0 ? 3

0000 0000 0011 1101 0000 1001 0000 0000

c) Show how the value 0xabcdef12 would be arranged in memory of a little-endian and a big-endian machine. Assume the data is stored starting at address 0. 2.5

d) Explain dynamic branch prediction 3

e) What are the assembly language statements corresponding to this machine *instructions*? 4

0000 0000 1010 1111 1000 0000 0010 0000
0000 0001 1110 1111 1000 0000 0010 0010

6.a) How many total bits are required for a direct-mapped cache with 16 KiB of data and 4-word blocks, assuming a 32-bit address? 3

b) What is structural hazard? 1.5

c) Explain load-use data hazard for following instructions: 6

```
sw $s0, 80($t1)
add $t2, $t3, $s2
```

d) If we assume we place the loop starting at location 80000 in memory, what is the MIPS assembly code and machine code for following code? 7

```
for(int i=0;array[i]!='\0'; )
{
  i+=1;
}
```

--- :: ---

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